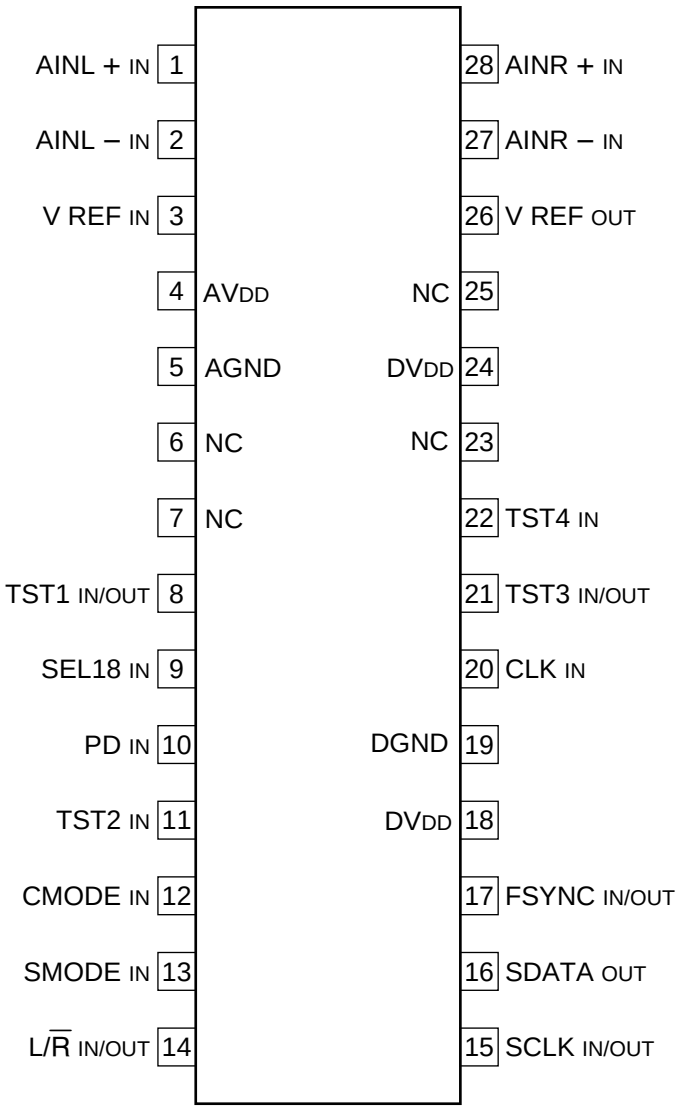
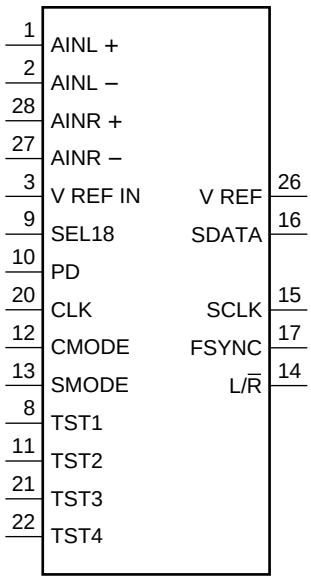
C-MOS 18-BIT 2 CHANNEL A/D CONVERTER

—TOP VIEW—





AVDD, AGND : FOR ANALOG BLOCK
DVDD, DGND : FOR DIGITAL BLOCK

INPUT

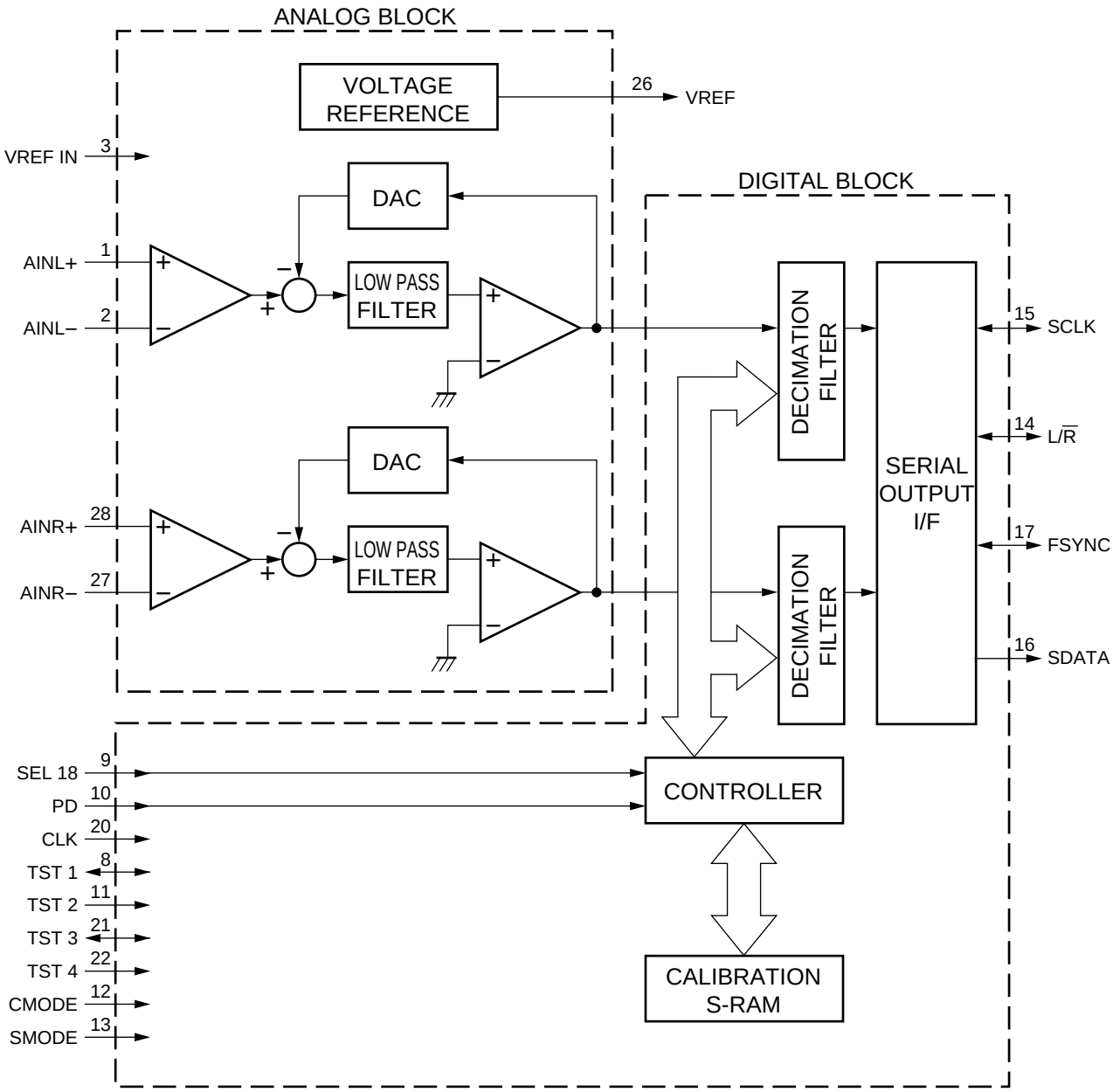
AINL +	;	L-CH ANALOG POSITIVE INPUT
AINL –	;	L-CH ANALOG NEGATIVE INPUT
AINR +	;	R-CH ANALOG POSITIVE INPUT
AINR –	;	R-CH ANALOG NEGATIVE INPUT
CLK	;	MASTER CLOCK (CMODE = H : 384 fs) (CMODE = L : 256 fs)
CMODE	;	MASTER CLOCK SELECT (L : CLK = 256 fs, 12.288 MHz @fs = 48 kHz) (H : CLK = 384 fs, 18.432 MHz @fs = 48 kHz)
PD	;	POWER DOWN FOR DIGITAL SECTION
SEL 18	;	18/16 BIT SELECT (L : 16-BIT, H : 18-BIT)
SMODE	;	INTERFACE CLOCK SELECT (L : SUB MODE) (H : MASTER MODE)
TST 2, 4	;	TEST
V REF IN	;	REFERENCE VOLTAGE

OUTPUT

SDATA	;	SERIAL DATA
V REF	;	REFERENCE VOLTAGE (–2.5V)

INPUT/OUTPUT

FSYNC	;	FRAME SYNC CLOCK (SUB MODE : FSYNC INPUT) (MASTER MODE : FSYNC OUTPUT)
L/$\overline{R}$	;	INPUT CHANNEL SELECT (SUB MODE : fs CLK INPUT) (MASTER MODE : fs CLK OUTPUT)
SCLK	;	SERIAL DATA CLOCK (SUB MODE : SCLK INPUT) (MASTER MODE : SCLK OUTPUT)
TST 1, 3	;	TEST


ANALOG BLOCK
VOLTAGE REFERENCE
26
VREF
VREF IN
3
DAC
DIGITAL BLOCK
AINL+
1
AINL–
2
LOW PASS FILTER
DECIMATION FILTER
SERIAL OUTPUT I/F
15
SCLK
14
L/R
DAC
AINR+
28
AINR–
27
LOW PASS FILTER
DECIMATION FILTER
17
FSYNC
16
SDATA
SEL 18
9
PD
10
CLK
20
TST 1
8
TST 2
11
TST 3
21
TST 4
22
CMODE
12
SMODE
13
CONTROLLER
CALIBRATION S-RAM