

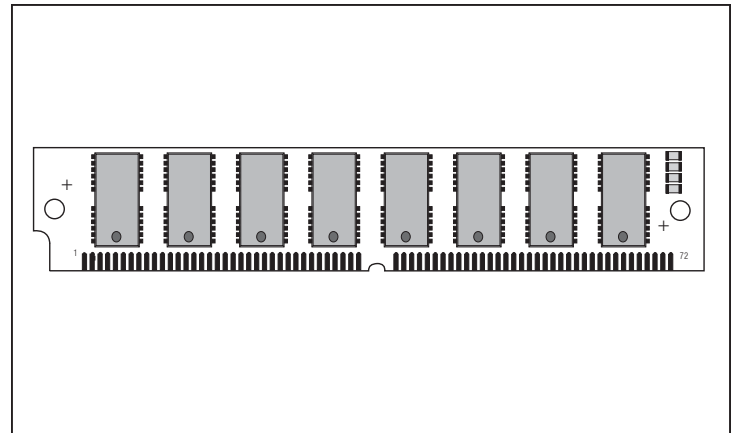
### DESCRIPTION

The Accutek AK5364096W high density memory module is a CMOS Dynamic RAM organized in 4096K x 36 bit words. The module consists of eight standard 4 Meg x 4 DRAMs and four 4 Meg x 1 DRAMs in plastic SOJ packages. The 4 Meg x 4 DRAMs are mounted on the front surface and the 4 Meg x 1 parity DRAMs are mounted on the back surface of a printed circuit board with a low profile height of only 0.875" in a 72 pin leadless SIM configuration. This configuration allows socket-mounting of large quantities of memory in applications where high density and ease of inserting additional memory are important.

The operation of the AK5364096W is identical to eight 4Meg x 4 plus four 4Meg x 1 DRAMs. There are four CAS lines and two RAS lines. Independent byte control is accomplished by four CAS lines. Each separate CAS line controls two 4Meg x 4 DRAMs, along with a 4Meg x 1 DRAM with data in tied to data out to form a 9 bit byte. The bank of 36 bits is controlled by the two  $\overline{RAS}$  lines. An eighteen bit data path can be produced by connecting DQ<sub>0</sub> to DQ<sub>18</sub>, DQ<sub>1</sub> to DQ<sub>19</sub>, etc. and alternately strobing RAS<sub>0</sub> with RAS<sub>2</sub>.

### FEATURES

- 4,194,304 x 36 bit organization
- Low profile board height of 0.875 inch
- 72 pad Single In-Line Module
- Multiple  $\overline{CAS}$  and  $\overline{RAS}$  lines allow x18 or x36 bit widths
- Power:  
7.92 Watt Max Active (60nS)  
6.60 Watt Max Active (70 nS)  
66 mW Max Standby



- CAS-before-RAS, RAS-only or hidden refresh
- Single 5 Volt Power Supply
- 2048 Refresh Cycles, 32 mSEC
- Available in Fast Page Mode, EDO and Static Column Mode
- Available in leadless SIM or leaded ZIP versions
- Downward compatible with AK5362048W, AK5361024W, AK536512W and AK536256W
- Upward compatible with AK5368192W
- Operating free air temperature 0°C to 70°C

### EXAMPLE

#### AK5364096WP-70

4Meg x 36 CMOS Dynamic RAM, SIM, Page Mode, Commercial  
70nSEC Access Time

### PIN NOMENCLATURE

A <sub>0</sub> - A <sub>10</sub>	Address Inputs
DQ <sub>0</sub> - DQ <sub>35</sub>	Data In/Data Out
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column Address Strobe
$\overline{RAS}_0$ , $\overline{RAS}_2$	Row Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD <sub>1</sub> - PD <sub>4</sub>	Presence Detect
V <sub>cc</sub>	5v Supply
V <sub>ss</sub>	Ground
NC	No Connect

### MODULE OPTIONS

Leadless SIM: AK5364096W

Leaded ZIP: AK5364096Z

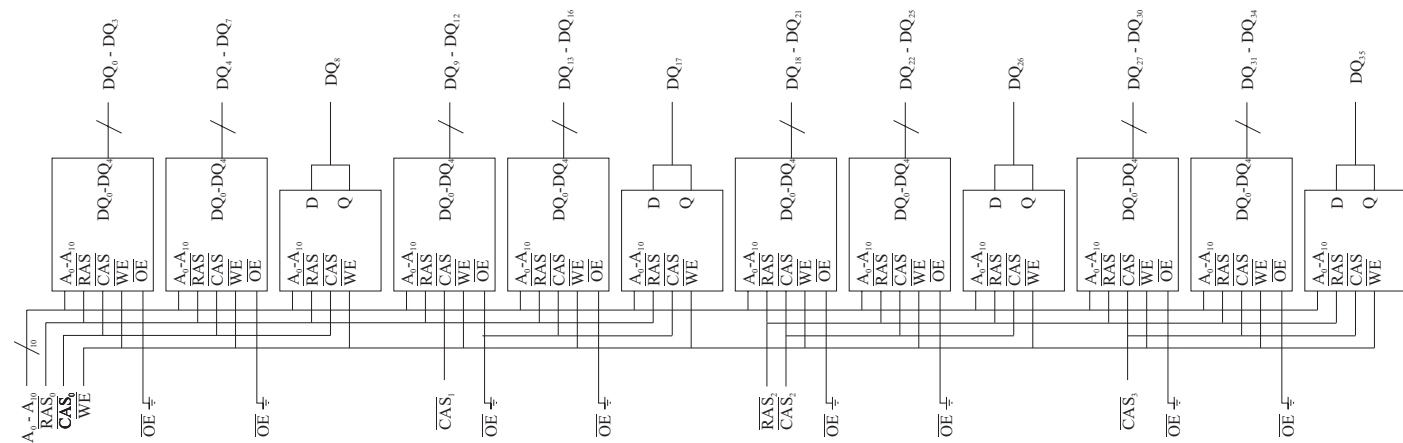
### PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V <sub>ss</sub>	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V <sub>ss</sub>	57	DQ13
4	DQ1	22	DQ5	40	CAS0	58	DQ31
5	DQ19	23	DQ23	41	CAS2	59	V <sub>cc</sub>
6	DQ2	24	DQ6	42	CAS3	60	DQ32
7	DQ20	25	DQ24	43	CAS1	61	DQ14
8	DQ3	26	DQ7	44	RAS0	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V <sub>cc</sub>	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	V <sub>cc</sub>	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	RAS2	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V <sub>ss</sub>

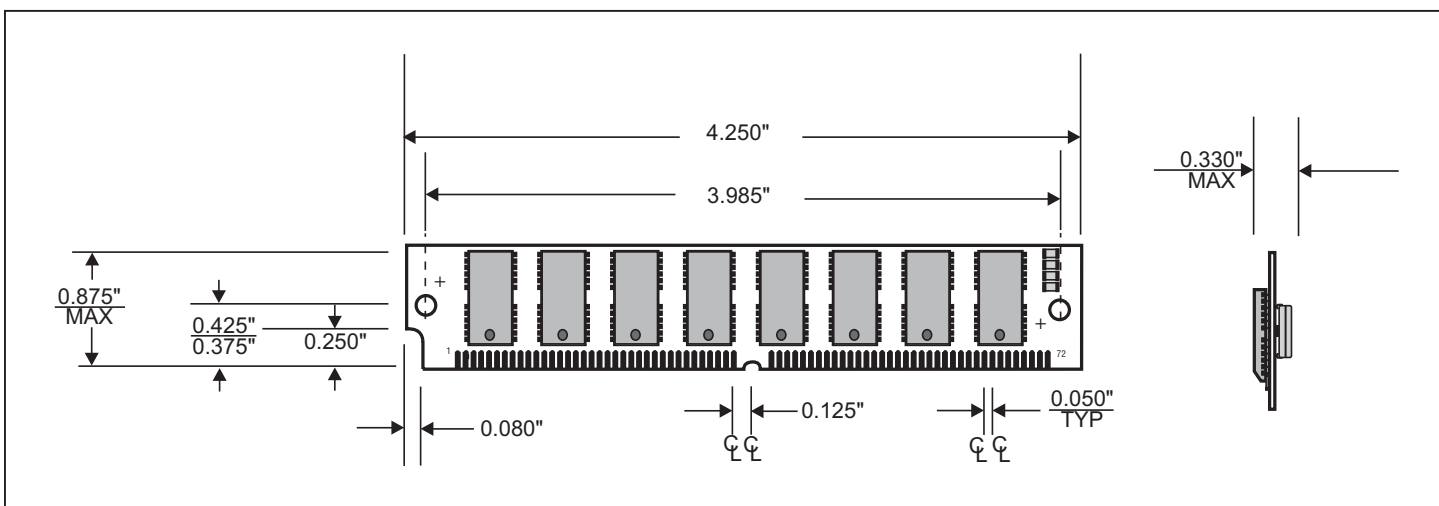
#### Presence Detect -

	-60	-70
PD1	V <sub>ss</sub>	V <sub>ss</sub>
PD2	NC	NC
PD3	NC	V <sub>ss</sub>
PD4	Nc	NC

## FUNCTIONAL DIAGRAM



## MECHANICAL DIMENSIONS



## ORDER INFORMATION

### PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8
<b>1 Product</b>	AK = Accuthek Memory							
<b>2 Type</b>	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM							
<b>3 Organization/Word Width</b>	1 = by 1 16 = by 16 4 = by 4 32 = by 32 8 = by 8 36 = by 36 9 = by 9							
<b>4 Size/Bits Depth</b>	64 = 64K      4096 = 4 MEG 256 = 256K    8192 = 8 MEG 1024 = 1 MEG   16384 = 16 MEG							

The numbers and coding on this page do not include all variations available, but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

### Position

1 2 3 4 5 6 7 8

#### 5 Package Type

- G = Single In-Line Package (SIP)
- S = Single In-Line Module (SIM)
- D = Dual In-Line Package (DIP)
- W = .050 inch Pitch Edge Connect
- Z = Zig-Zag In-Line Package (ZIP)

#### 6 Special Designation

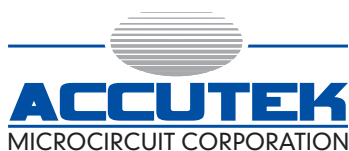
- P = Page Mode
- N = Nibble Mode
- K = Static Column Mode
- W = Write Per Bit Mode
- V = Video Ram

#### 7 Separator

- = Commercial 0°C to +70°C
- M = Military Equivalent Screened (-55°C to +125°C)
- I = Industrial Temperature Tested (-45°C to +85°C)
- X = Burned In

#### 8 Speed (first two significant digits)

DRAMS	SRAMS
50 = 50 nS	8 = 8 nS
60 = 60 nS	12 = 12 nS
70 = 70 nS	15 = 15 nS



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NEWBURYPORT, MA 01950-4040  
PHONE: 978-465-6200 FAX: 978-462-3396  
Email: sales@accuthekmicro.com  
Internet: www.accuthekmicro.com

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