AK5706

Low-Power 2-ch ADC with AAA and Audio Buffer

1. General Description

The AK5706 is a high-performance 24-bit stereo ADC (Analog-to-Digital converter) with integrated Acoustic Activity Analyzer (AAA), audio buffer, and support for digital and high-SNR microphones. The AAA listens for audio activity in a very low-power state while the rest of the device remains powered off. Once qualifying audio content is detected, the audio buffer begins recording and the rest of the AK5706 wakes up, in turn waking other devices in the system as needed. Designed for systems that must listen for specific Typ.es of audio activity while consuming very low power, the AK5706 is ideal for products such as speech recognition systems, security cameras, and smart doorbells.

2. Features

1. **Acoustic Activity Analyzer (AAA)**
   - **High Accuracy Mode (Idd = 30 µA) / External Trigger Mode (Idd = 11 µA)**
2. **Audio Buffer: 64 kB for up to 2 sec of recording**
3. **Audio Capture**
   - **2-Channel Low-Power 24-bit ADC**
     - **S/N, DR: 105 dB (High Performance Mode)**
     - **S/N, DR: 103 dB (Low Power Mode)**
     - **Single-ended Inputs or Full-differential Inputs**
     - **MIC Amplifier Gain: +30 dB to 0 dB, 3 dB steps**
   - **4-Channel Digital MIC Interface (64 fs / 32 fs / 48 fs / 24 fs)**
   - **Programmable Phase Adjustment**
   - **Selectable Digital Filter (Low-latency Sharp Roll-off or Voice)**
   - **Microphone Sensitivity Adjustment**
   - **2-output MIC Power Supplies**
     - **Low-power Mode (Idd = 1 µA): 1.1 V / 1.3 V / 1.8V / Direct Mode Selectable**
     - **Normal Mode: 2.8 V / 2.5 V / 1.8 V / Direct Mode Selectable**
4. **External Trigger Input for AAA/ADC Power-up**
5. **Multi Sync Mode for up to 8-ch recording**
6. **Digital Audio interface**
   - **Master/Slave Mode**
   - **Sampling Frequency**
     - **8 kHz to 192 kHz**
   - **Interface Formats**
     - **24 / 16-bit I^2S/MSB justified**
     - **24 / 16-bit SPI (audio buffer access)**
     - **4-ch TDM for Digital Mic**
     - **4-ch / 6-ch / 8-ch Sync Transfer for Analog Mic**
7. **Built-in PLL**
8. **Crystal Oscillator (12.288 MHz)**
9. **Control I/F: I^2C-bus (400 kHz) / SPI (13 MHz)**
10. **Operation Temperature Range: Ta = –40 to 85 °C**
11. **Power Supply:**
    - **AVDD (ADC, MIC, PLL): 1.7 to 1.9 V or 3.0 to 3.6 V**
    - **TVDD (Host & Audio I/F, LDO): 1.65 to 3.6 V**
12. **Package: 32-pin CSP (2.668 x 2.695 mm, 0.4mm pitch)**

3. Table of Contents

4. Block Diagram

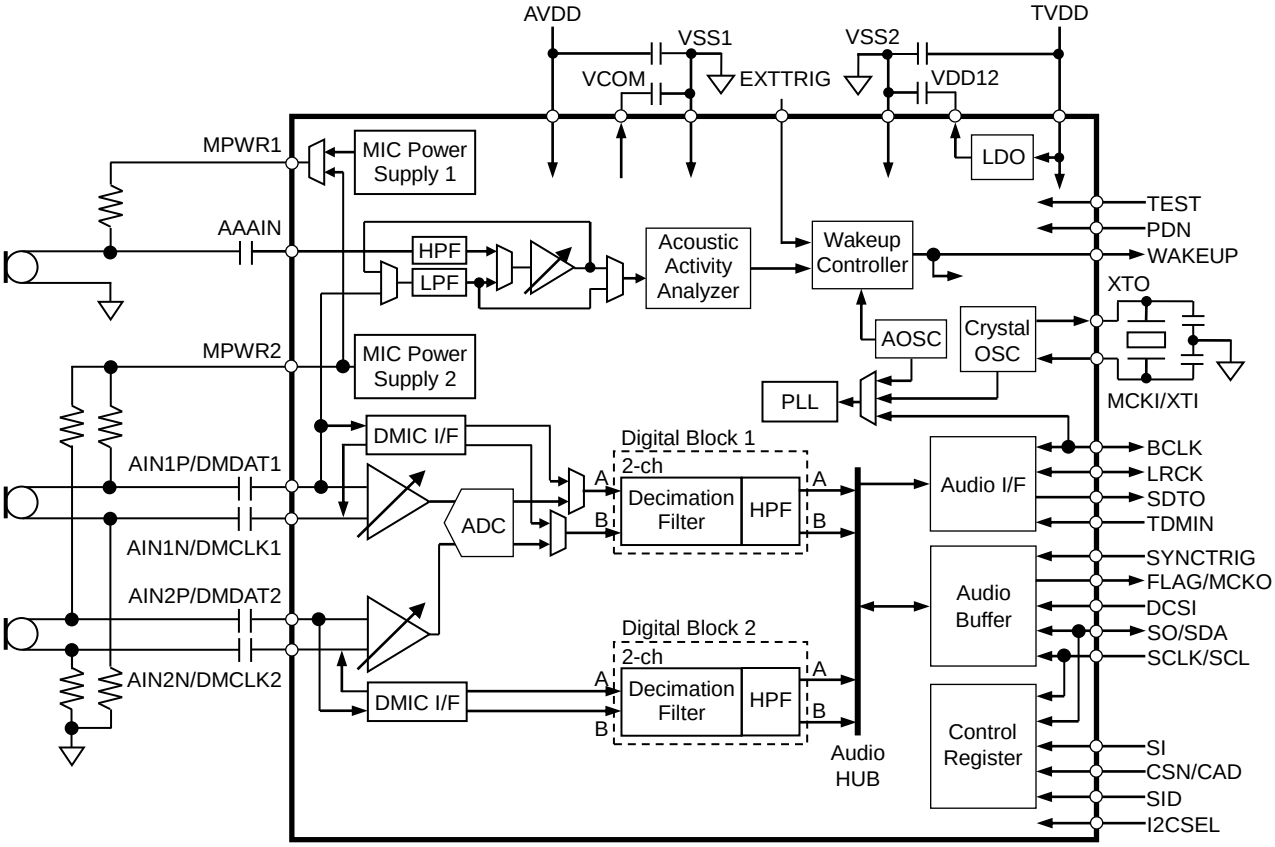
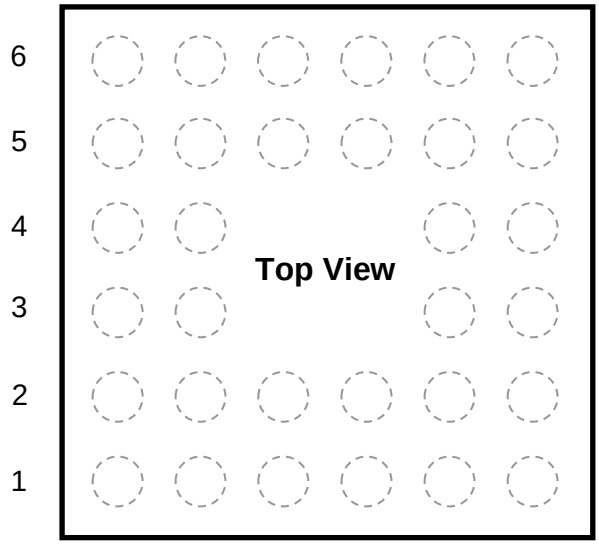


Figure 1. AK5706 Block Diagram

5. Pin Configurations and Functions

5.1. Pin Configurations

32-pin CSP



6	VSS2	VDD12	TVDD	PDN	AAAIN	VCOM
5	MCKI /XTI	BCLK	LRCK	TEST	I2CSEL	AVDD
4	XTO	SCLK /SCL	-	-	SYNCTRIG	VSS1
3	SDTO	TDMIN	-	-	AIN1N /DMCLK1	AIN2N /DMCLK2
2	SO /SDA	DCSI	SI	SID	AIN1P /DMDAT1	AIN2P /DMDAT2
1	FLAG /MCKO	WAKEUP	EXTTRIG	CSN /CAD	MPWR1	MPWR2
	A	B	C	D	E	F

Top View

5.2. Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
F5	AVDD	-	Analog Power Supply Pin, 1.7 to 1.9 V or 3.0 to 3.6 V		AVDD
F6	VCOM	O	Common Voltage Output Pin This pin must be connected to the VSS1 pin through a 2.2 µF ± 50 % ceramic capacitor. (Note 3)	AVDD/ VSS1	AVDD
F4	VSS1	-	Analog Ground Pin		
E1	MPWR1	O	MIC Power Supply 1 Pin	AVDD/ VSS1	AVDD
F1	MPWR2	O	MIC Power Supply 2 Pin	AVDD/ VSS1	AVDD
E6	AAAIN	I	AAA Input Pin	AVDD/ VSS1	AVDD
E2	AIN1P	I	Positive Analog Input 1 Pin (DMIC1 bit = “0”, Default)	AVDD/ VSS1	AVDD
	DMDAT1	I	Digital Microphone Data Input 1 Pin (DMIC1 bit = “1”)		
E3	AIN1N	I	Negative Analog Input 1 Pin (DMIC1 bit = “0”, Default)	AVDD/ VSS1	AVDD
	DMCLK1	O	Digital Microphone Clock Output 1 Pin (DMIC1 bit = “1”)		
F2	AIN2P	I	Positive Analog Input 2 Pin (DMIC2 bit = “0”, Default)	AVDD/ VSS1	AVDD
	DMDAT2	I	Digital Microphone Data Input 2 Pin (DMIC2 bit = “1”)		
F3	AIN2N	I	Negative Analog Input 2 Pin (DMIC2 bit = “0”, Default)	AVDD/ VSS1	AVDD
	DMCLK2	O	Digital Microphone Clock Output 2 Pin (DMIC2 bit = “1”)		
B1	WAKEUP	O	Wakeup Interrupt Output Pin	TVDD/ VSS2	TVDD
C1	EXTTRIG	I	External Trigger Input Pin	TVDD/ VSS2	TVDD
C6	TVDD	-	Digital I/F & LDO Power Supply Pin, 1.65 to 3.6 V		TVDD
B6	VDD12	-	LDO (1.24 V) Output Pin This pin must be connected to the VSS2 pin through a 4.7 µF ± 50 % capacitor.	TVDD/ VSS2	TVDD
A6	VSS2	-	Digital Ground Pin		
A5	MCKI	I	Master Clock Input Pin (Default)	TVDD/ VSS2	TVDD
	XTI	I	Crystal Oscillator Input Pin		
A4	XTO	O	Crystal Oscillator Output Pin	TVDD/ VSS2	TVDD
B5	BCLK	I/O	Audio Serial Data Clock Pin	TVDD/ VSS2	TVDD
C5	LRCK	I/O	Frame Sync Clock Pin	TVDD/ VSS2	TVDD
A3	SDTO	O	Audio Serial Data Output Pin	TVDD/ VSS2	TVDD
B3	TDMIN	I	TDM Data Input Pin	TVDD/ VSS2	TVDD

No.	Pin Name	I/O	Function	Protection Diode	Power Domain
A1	FLAG	O	Buffer Flag Output Pin (Default)	TVDD/ VSS2	TVDD
	MCKO	O	Master Clock Output Pin		
E4	SYNCTRIG	I	Sync Trigger Input Pin	TVDD/ VSS2	TVDD
E5	I2CSEL	I	I^2C Select Pin "L": SPI, "H": I^2C	TVDD/ VSS2	TVDD
D2	CSN	I	SPI Chip Select Pin (I2CSEL pin = "L")	TVDD/ VSS2	TVDD
	CAD	I	I^2C Chip Address Pin (I2CSEL pin = "H")		
B4	SCLK	I	SPI Serial Data Clock Pin (I2CSEL pin = "L")	TVDD/ VSS2	TVDD
	SCL	I	I^2C Serial Data Clock Pin (I2CSEL pin = "H")		
A2	SO	O	SPI Serial Data Output Pin (I2CSEL pin = "L")	TVDD/ VSS2	TVDD
	SDA	I/O	I^2C Serial Data Input/Output Pin (I2CSEL pin = "H")		
C2	SI	I	SPI Serial Data Input Pin	TVDD/ VSS2	TVDD
D2	SID	I	SPI Chip ID Pin	TVDD/ VSS2	TVDD
B2	DCSI	I	SPI Daisy Chain Data Input Pin	TVDD/ VSS2	TVDD
D6	PDN	I	Power down Pin "L": Power-down, "H": Power-Up	TVDD/ VSS2	TVDD
D5	TEST	I	TEST Input Pin This pin must be connected to VSS2.	TVDD/ VSS2	TVDD

Note 1. Do not connect a load to the VDD12 pin and/or the VCOM pin.
Note 2. Input pins (except for analog input pins AAAIN, AIN1P, AIN1N, AIN2P and AIN2N) should not be left floating.
Note 3. The recommended insulation resistance of the capacitor connected to the VCOM pin is 50 ΩF or less.

5.3. Handling of Unused Pins

Unused I/O pins must be connected as follows.

Classification	Pin Name	Setting
Analog	MPWR1, MPWR2	Open
	AAAIN	Open
	AIN1P, AIN1N	Open and PMDM1A/B[1:0] bits = "00"
	AIN2P, AIN2N	Open and PMDM2A/B[1:0] bits = "00"
Digital	WAKEUP, FLAG/MCKO, SDTO, XTO	Open
	EXTTRIG, TDMIN, SI, SID, DCSI, SYNCTRIG	Connected to VSS2
	MCKI/XTI	Connected to VSS2 and PMOSC[1:0], PMMCKIB[1:0] bits = "00"

5.4. Pin State in Power-down Mode

No.	Pin Name	I/O	Pin Power-down (PDN pin = "L")	Register Power-down (PDN pin = "H," all PMx bit = 0x0)
F5	AVDD	-	-	-
F6	VCOM	O	Pull-down to VSS1 by 290 Ω (Typ.) @ AVDD = 3.3 V Pull-down to VSS1 by 300 Ω (Typ.) @ AVDD = 1.8 V	see prev. column
F4	VSS1	-	-	-
E1	MPWR1	O	Hi-z	see prev. column
F1	MPWR2	O	Hi-z	see prev. column
E6	AAAIN	I	Hi-z	see prev. column
E2	AIN1P	I	Hi-z	see prev. column
	DMDAT1	I		
E3	AIN1N	I	Hi-z	see prev. column
	DMCLK1	O		
F2	AIN2P	I	Hi-z	see prev. column
	DMDAT2	I		
F3	AIN2N	I	Hi-z	see prev. column
	DMCLK2	O		
B1	WAKEUP	O	Hi-z	see prev. column
C1	EXTTRIG	I	Hi-z	see prev. column
C6	TVDD	-	-	-
B6	VDD12	-	Internal pull-down to VSS2: 700 Ω (Typ.)	Normal Operation
A6	VSS2	-	-	-
A5	MCKI	I	Hi-z	see prev. column
	XTI	I		
A4	XTO	O	Internal pull-down to VSS2: 2 kΩ (Typ.)	see prev. column
B5	BCLK	I/O	Internal pull-down to VSS2: 49 kΩ (Typ.)	Hi-z (MSN bit = "0")
C5	LRCK	I/O	Internal pull-down to VSS2: 49 kΩ (Typ.)	Hi-z (MSN bit = "0")
A3	SDTO	O	Internal pull-down to VSS2: 49 kΩ (Typ.)	"L" (VSS2)
B3	TDMIN	I	Hi-z	see prev. column
A1	FLAG	O	Internal pull-down to VSS2: 49 kΩ (Typ.)	"L" (VSS2)
	MCKO	O		
E4	SYNCTRIG	I	Hi-z	see prev. column
E5	I2CSEL	I	Hi-z	see prev. column
D1	CSN	I	Hi-z	see prev. column
	CAD	I		
B4	SCLK	I	Hi-z	see prev. column
	SCL	I		
A2	SO	O	Hi-z	SO or SDA
	SDA	I/O		
C2	SI	I	Hi-z	Hi-z
D2	SID	I	Hi-z	Hi-z
B2	DCSI	I	Hi-z	Hi-z
D6	PDN	I	Hi-z	Hi-z
D5	TEST	I	Hi-z	Hi-z

6. Absolute Maximum Ratings

(VSS1 = VSS2 = 0 V; Note 4, Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	–0.3	4.3	V
	Digital I/F & LDO	TVDD	–0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	± 10	mA
Analog Input Voltage (Note 6)		VINA	–0.3	4.3	V
Digital Input Voltage (Note 7)		VIND1	–0.3	TVDD + 0.3 or 4.3	V
(Note 8)		VIND2	–0.3	AVDD + 0.3 or 4.3	V
Ambient Temperature (power applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 4. All voltages are with respect to ground.
Note 5. **VSS1 and VSS2 must be connected to the same analog ground plane.**
Note 6. AAAIN, AIN1P, AIN1N, AIN2P and AIN2N pins
Note 7. EXTTRIG, MCKI, BCLK, LRCK, TDMIN, SYNCTRIG, I2CSEL, CSN/CAD, SCLK/SCL, SDA, SI, SID, DCSI, PDN and TEST pins; The maximum value is the lower of “TVDD + 0.3 V” and “4.3 V”.
Note 8. DMDAT1 and DMDAT2 pins; The maximum value is the lower of “AVDD + 0.3 V” and “4.3 V”.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 = VSS2 = 0 V; Note 9)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 10)	Analog	AVDDL	1.7	1.8	1.9	V
		AVDDH	3.0	3.3	3.6	V
	Digital I/F & LDO	TVDD	1.65	1.8	3.6	V

Note 9. All voltages are with respect to ground.
Note 10. The PDN pin must be “L” upon power-up and should be changed to “H” only after all power supplies have ramped up. TVDD should be powered up before or at the same time as AVDD.

WARNING: AKM assumes no responsibility for usage beyond the conditions in this datasheet.

8. Electrical Characteristics

8.1. Microphone & ADC Analog Characteristics (AVDD = 3.3V: AVDDMD bit = "1")

(Ta = 25 °C; AVDD = 3.3 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; Signal Frequency = 1 kHz; 24-bit Data; External Slave Mode; fs = 48 kHz, BCLK = 64 fs; Measurement Bandwidth = 20 Hz to 20 kHz unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
MIC Amplifier 1/2: AIN1P/N, AIN2P/N pins					
Input Resistance		140	200	260	kΩ
MIC-Amp 1/2 Gain	Gain Setting	0	-	+30	dB
	Step Width	2	3	4	dB
MIC Power Supply: MPWR1 pin (Low-power Mode)					
Output Voltage (Note 11)	MICL1[1:0] bits = "00"	1.0	1.1	1.2	V
	MICL1[1:0] bits = "01"	1.2	1.3	1.4	
	MICL1[1:0] bits = "10"	1.7	1.8	1.9	
	MICL1[1:0] bits = "11"	-	AVDD	-	
Load Resistance (Except for MICL1[1:0] bits = "11")		3.0	-	200	kΩ
Load Capacitance (Except for MICL1[1:0] bits = "11")		-	-	130	pF
Output Noise Level (A-weighted)	MICL1[1:0] bits = "00"	-	–72	-	dBV
	MICL1[1:0] bits = "01"	-	–71	-	
	MICL1[1:0] bits = "10"	-	–68	-	
PSRR (1 kHz) (Note 14)		-	15	-	dB
MIC Power Supply: MPWR1 pin (Bypass Mode), MPWR2 pin					
Output Voltage (Note 12, Note 13)	MICL2[1:0] bits = "00"	2.6	2.8	3.0	V
	MICL2[1:0] bits = "01"	2.3	2.5	2.7	
	MICL2[1:0] bits = "10"	1.7	1.8	1.9	
	MICL2[1:0] bits = "11"	-	AVDD	-	
Load Resistance (Except for MICL2[1:0] bits = "11")		1.0	-	-	kΩ
Load Capacitance (Except for MICL2[1:0] bits = "11")		-	-	130	pF
Output Noise Level (A-weighted)	MICL2[1:0] bits = "00"	-	–106	-	dBV
	MICL2[1:0] bits = "01"	-	–107	-	
	MICL2[1:0] bits = "10"	-	–112	-	
PSRR (1 kHz) (Note 14)		-	60	-	dB

Note 11. Output voltage for MPWR1 (Low-power Mode) is fixed regardless of the AVDD voltage. When MICL1[1:0] bits are "11", MPWR1 outputs AVDD via internal switch.

Note 12. The output voltage is proportional to AVDD. MICL2[1:0] bits = "00": Typ. 2.8 x AVDD / 3.3 V, "01": Typ. 2.5 x AVDD / 3.3 V, "10": Typ. 1.8 x AVDD / 3.3 V. When MICL2[1:0] bits are "11", MPWR1/2 output AVDD via internal switch.

Note 13. Configuring the output voltage for MPWR1 (Bypass Mode) will set the same output voltage for MPWR2. The setting of MICL2[1:0] bits = "10" is only available in Bypass Mode.

Note 14. PSRR for all power supplies is measured with respect to a 100 mVpp sine wave input.

<High Performance Mode>

Parameter			Min.	Typ.	Max.	Unit
ADC Analog Input Characteristics: AIN1P, AIN2P pins (**Single-ended Input**) or AIN1P/N, AIN2P/N pins (**Differential Input**) → ADC → SDTO; ADCLP bit = "0"						
Resolution			-	-	24	Bits
Input Full Scale Voltage (Note 15)		0 dB	1.85	2.02	2.18	Vpp
		+18 dB	-	0.255		Vpp
THD+N (–1 dBFS)	fs = 48 kHz BW = 20 kHz	0 dB	-	–90	-	dB
		+18 dB	-	–86	–71	dB
	fs = 96 kHz BW = 40 kHz	0 dB	-	–88	-	dB
		+18 dB	-	–84	-	dB
	fs = 192 kHz BW = 40 kHz	0 dB	-	–88	-	dB
		+18 dB	-	–84	-	dB
Dynamic Range (–60 dBFS, A-weighted)		0 dB	99	105	-	dB
		+18 dB	-	93	-	dB
S/N (A-weighted)		0 dB	99	105	-	dB
		+18 dB	-	93	-	dB
Interchannel Isolation		0 dB	-	100	-	dB
		+18 dB	80	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
PSRR (1 kHz) (Note 16)		0 dB	-	60	-	dB
		+18 dB	-	60	-	dB

<Low Power Mode: fs ≤ 48kHz>

Parameter			Min.	Typ.	Max.	Unit
ADC Analog Input Characteristics: AIN1P, AIN2P pins (**Single-ended Input**) or AIN1P/N, AIN2P/N pins (**Differential Input**) → ADC → SDTO; ADCLP bit = "1"						
Resolution			-	-	24	Bits
Input Full Scale Voltage (Note 15)		0 dB	1.85	2.02	2.18	Vpp
		+18 dB	-	0.255	-	Vpp
THD+N (–1 dBFS)	fs = 48 kHz BW = 20 kHz	0 dB	-	–88	-	dB
		+18 dB	-	–82	–67	dB
Dynamic Range (–60 dBFS, A-weighted)		0 dB	97	103	-	dB
		+18 dB	-	91	-	dB
S/N (A-weighted)		0 dB	97	103	-	dB
		+18 dB	-	91	-	dB
Interchannel Isolation		0 dB	-	100	-	dB
		+18 dB	80	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
PSRR (1 kHz) (Note 16)		0 dB	-	60	-	dB
		+18 dB	-	60	-	dB

Note 15. Input voltage is proportional to AVDD.
Single-ended Input: Vin = 2.02 Vpp x AVDD / 3.3 V (Typ.) @ Gain = 0 dB
Full Differential Input: Vin = (AINP) – (AINN) = 2.02 Vpp x AVDD / 3.3 V (Typ.) @ Gain = 0 dB

Note 16. PSRR for all power supplies is measured with respect to a 100 mVpp sine wave input. This ratio is based upon 100 mVpp (= –26.1 dBFS) at the ADC output.

8.2. Microphone & ADC Analog Characteristics (AVDD = 1.8V: AVDDMD bit = "0")

(Ta = 25 °C; AVDD = 1.8 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; Signal Frequency = 1 kHz; 16-bit Data; External Slave Mode; fs = 48 kHz, BCLK = 64 fs; Measurement Bandwidth = 20 Hz to 20 kHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
MIC Amplifier 1/2: AIN1P/N, AIN2P/N pins					
Input Resistance		140	200	260	kΩ
MIC-Amp 1/2 Gain	Gain Setting	0	-	+30	dB
	Step Width	2	3	4	dB
MIC Power Supply: MPWR1 pin (Low-power Mode)					
Output Voltage (Note 17)	MICL1[1:0] bits = "00"	1.0	1.1	1.2	V
	MICL1[1:0] bits = "01"	1.2	1.3	1.4	
	MICL1[1:0] bits = "11"	-	AVDD	-	
Load Resistance (Except for MICL1[1:0] bits = "11")		3.0	-	200	kΩ
Load Capacitance (Except for MICL1[1:0] bits = "11")		-	-	130	pF
Output Noise Level (A-weighted)	MICL1[1:0] bits = "00"	-	–72	-	dBV
	MICL1[1:0] bits = "01"	-	–71	-	dBV
PSRR (1 kHz) (Note 19)		-	15	-	dB
MIC Power Supply: MPWR2 pin					
Output Voltage (Note 18)	MICL2[1:0] bits = "11"	-	AVDD	-	V

Note 17. Output voltage of microphone power for MPWR1 (Low-power Mode) is fixed. When MICL1[1:0] bits are "11", MPWR1 output AVDD via internal switch. The setting of MICL1[1:0] bits = "10" is not available.

Note 18. The setting of MICL2[1:0] bits = "11" is only available.
When MICL2[1:0] bits are "11", MPWR1/2 output AVDD via internal switch.

Note 19. PSRR for all power supplies is measured with respect to a 100 mVpp sine wave input.

<High Performance Mode>

Parameter			Min.	Typ.	Max.	Unit
ADC1/2 Analog Input Characteristics: AIN1P, AIN2P pins (**Single-ended Input**) or AIN1P/N, AIN2P/N pins (**Differential Input**) → ADC → SDTO; ADCLP bit = "0"						
Resolution			-	-	24	Bits
Input Full Scale Voltage (Note 20)		0 dB	1.01	1.10	1.19	Vpp
		+18 dB	-	0.139	-	Vpp
THD+N (–1 dBFS)	fs = 48 kHz BW = 20 kHz	0 dB	-	–82	-	dB
		+18 dB	-	–78	–65	dB
	fs = 96 kHz BW = 40 kHz	0 dB	-	–82	-	dB
		+18 dB	-	–78	-	dB
	fs = 192 kHz BW = 40 kHz	0 dB	-	–82	-	dB
		+18 dB	-	–78	-	dB
Dynamic Range (–60 dBFS, A-weighted)		0 dB	93	99	-	dB
		+18 dB	-	87	-	dB
S/N (A-weighted)		0 dB	93	99	-	dB
		+18 dB	-	87	-	dB
Interchannel Isolation		0 dB	-	100	-	dB
		+18 dB	80	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
PSRR (1 kHz) (Note 21)		0 dB	-	55	-	dB
		+18 dB	-	60	-	dB

<Low Power Mode: fs ≤ 48kHz>

Parameter			Min.	Typ.	Max.	Unit
ADC1/2 Analog Input Characteristics: AIN1P, AIN2P pins (**Single-ended Input**) or AIN1P/N, AIN2P/N pins (**Differential Input**) → ADC → SDTO; ADCLP bit = "1"						
Resolution			-	-	16	Bits
Input Full Scale Voltage (Note 20)		0 dB	1.01	1.10	1.19	Vpp
		+18 dB	-	0.139	-	Vpp
THD+N (–1 dBFS)	fs = 48 kHz BW = 20 kHz	0 dB	-	–85	-	dB
		+18 dB	-	–80	–65	dB
Dynamic Range (–60 dBFS, A-weighted)		0 dB	91	97	-	dB
		+18 dB	-	85	-	dB
S/N (A-weighted)		0 dB	91	97	-	dB
		+18 dB	-	85	-	dB
Interchannel Isolation		0 dB	-	100	-	dB
		+18 dB	80	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
PSRR (1 kHz) (Note 21)		0 dB	-	60	-	dB
		+18 dB	-	60	-	dB

Note 20. Input voltage is proportional to AVDD. Typ. 1.10 Vpp x AVDD / 1.8V @ MIC-Amp Gain = 0 dB
Single-ended Input: Vin = 1.10 Vpp x AVDD / 1.8 V (Typ.) @ Gain = 0 dB
Full Differential Input: Vin = (AINP) – (AINN) = 1.10 Vpp x AVDD / 1.8 V (Typ.) @ Gain = 0 dB

Note 21. PSRR for all power supplies is measured with respect to a 100 mVpp sine wave input. This ratio is based upon 100 mVpp (= –20.8 dBFS) at the ADC output.

8.3. Acoustic Activity Analyzer Characteristics

(Ta = 25 °C; AVDD = 1.8 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V, BG[2:0] bits = "101" (26 dB); unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
AAA Analog Input Characteristics: AAAIN pin					
Input Resistance		18	25	32	kΩ
Amplifier Gain	Gain Setting	6	-	34	dB
	Step Width	3	4	5	dB
Recommended Input Level	2 kHz sine wave	–82	-	–42	dBV

8.4. PLL, AOSC Characteristics

(Ta = 25 °C; AVDD = 3.3 V or 1.8 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
PLL Characteristics					
Reference Clock		76.8	-	768	kHz
PLLCLK Frequency	44.1 kHz x 256 fs x 2	-	22.5792	-	MHz
	48 kHz x 256 fs x 2	-	24.576	-	MHz
	44.1 kHz x 288 fs x 2	-	25.4016	-	MHz
	48 kHz x 288 fs x 2	-	27.648	-	MHz
PLL Lock Time		-	-	2	msec
AOSC Characteristics					
Output Frequency		-	1.0	-	MHz
Power Up Time		-	-	50	msec

8.5. LDO Characteristics

(Ta = 25 °C; AVDD = 3.3 V or 1.8 V, TVDD = 3.3 V or 1.8 V; VSS1 = VSS2 = 0 V, C = 4.7 µF ±50 %; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
LDO Characteristics: VDD12 pin					
Power Up Time	99 %	-	-	5	msec

8.6. VCOM Characteristics

(Ta = 25 °C; AVDD = 3.3 V or 1.8 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V, C = 2.2 µF ± 50 %; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
VCOM Characteristics: VCOM pin					
Power Up Time	99 %	-	-	2	msec
Wait Time for Restart		1	-	-	msec

8.7. Power Supply Current

(Ta = 25 °C; AVDD = 3.3 V or 1.8 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
Power Supply Current					
Power Up (PDN pin = "H", All circuits power-up; Note 22)					
	AVDD (AVDD = 3.3 V)	-	2.8	4.0	mA
	AVDD (AVDD = 1.8 V)	-	2.2	3.2	mA
	TVDD	-	2.7	5.0	mA
Power Up (PDN pin = "H", All circuits power-down)					
	AVDD (AVDD = 3.3 V)	-	1.0	-	μA
	AVDD (AVDD = 1.8 V)	-	1.0	-	μA
	TVDD (Note 23)	-	15.0	-	μA
Power Down (PDN pin = "L", Note 23)					
	AVDD + TVDD	-	1	20	μA

Note 22. PLL Master Mode, BCLK = 64 fs, fs =48 kHz (PLD[15:0] bits = 000Fh, PLM[15:0] bits = 001Fh, FS[4:0] bits = "01010", PLS bit = "0", CLKOE bit = "1"); PMMCKIB[1:0] bits = "00", PMOSC[1:0] bits = "01"; MICL1[1:0] bits = "00" ; MICL2[41:0] bits = "00" @ AVDD = 3.3 V, MICL2[1:0] bits = "11"@ AVDD = 1.8 V; No signal input, No load

Note 23. All digital input pins are fixed to VSS2.

8.8. Power Consumption for Each Operation Mode (Typ.)

[AVDD = 3.3 V]

(Ta = 25 °C; AVDD = 3.3 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; External Slave Mode, MCKI = 256 fs, BCLK = 64 fs; No signal input, MPWR OFF)

Mode		AVDD [mA]	TVDD [mA]	Total Power [mW]
2-ch ADC (fs = 16 kHz)	High Performance Mode	1.27	0.51	5.88
	Low Power Mode	0.59	0.43	3.37
2-ch ADC (fs = 48 kHz)	High Performance Mode	2.35	1.31	12.08
	Low Power Mode	1.17	1.10	7.48
2-ch ADC (fs = 96 kHz)	High Performance Mode	2.36	2.03	14.52
2-ch ADC (fs = 192 kHz)	High Performance Mode	2.36	2.18	15.00
2-ch Digital MIC (fs = 16 kHz, DMCLK = 64 fs)		0.10	0.40	1.65
4-ch Digital MIC (fs = 16 kHz, DMCLK = 64 fs)		0.19	0.52	2.34
Acoustic Activity Analyzer (High Accuracy Mode)	AAAIN Input (ALPF off)	0.0162	0.0183	0.113
	AAAIN Input (ALPF on)	0.0232	0.0183	0.137
	DMIC Input (DMCLK = 1024 kHz)	0.0570	0.0230	0.264
External Trigger Mode		0.0008	0.0103	0.036

[AVDD = 1.8 V]

(Ta = 25 °C; AVDD = 1.8 V, TVDD = 1.8 V; VSS1 = VSS2 = 0 V; External Slave Mode, MCKI = 256 fs, BCLK = 64fs; No signal input, MPWR OFF)

Mode		AVDD [mA]	TVDD [mA]	Total Power [mW]
2-ch ADC (fs = 16 kHz)	High Performance Mode	1.11	0.51	2.92
	Low Power Mode	0.51	0.43	1.70
2-ch ADC (fs = 48 kHz)	High Performance Mode	1.92	1.31	5.82
	Low Power Mode	0.94	1.07	3.62
2-ch ADC (fs = 96 kHz)	High Performance Mode	1.94	2.02	7.12
2-ch ADC (fs = 192 kHz)	High Performance Mode	1.94	2.14	7.33
2-ch Digital MIC (fs = 16 kHz, DMCLK = 64 fs)		0.07	0.40	0.84
4-ch Digital MIC (fs = 16 kHz, DMCLK = 64 fs)		0.11	0.54	1.16
Acoustic Activity Analyzer (High Accuracy Mode)	AAAIN Input (ALPF off)	0.0115	0.0183	0.054
	AAAIN Input (ALPF on)	0.0185	0.0183	0.066
	DMIC Input (DMCLK = 1024 kHz)	0.0450	0.0220	0.121
External Trigger Mode		0.0006	0.0103	0.020

8.9. Filter Characteristics

8.9.1. Short Delay Sharp Roll-off Filter (ADVF bit = "0")

<fs = 48 kHz>

(Ta = −40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 48 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): ADC, DMIC (DMCLK = 64 fs: DCLKS[1:0] bits = "00")						
Passband (Note 24)	±0.16 dB	PB	0	-	18.8	kHz
	−0.28 dB		-	20.0	-	kHz
	−3.0 dB		-	22.8	-	kHz
Stopband (Note 24)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.0	-	1/fs
Group Delay Distortion (0 to 20 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 32 fs: DCLKS[1:0] bits = "01")						
Passband (Note 24)	±0.16 dB	PB	0	-	18.8	kHz
	−0.28 dB		-	20.0	-	kHz
	−3.0 dB		-	22.8	-	kHz
Stopband (Note 24)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.3	-	1/fs
Group Delay Distortion (0 to 20 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 48 fs: DCLKS[1:0] bits = "10")						
Passband (Note 24)	±0.16 dB	PB	0	-	17.7	kHz
	−0.28 dB		-	19.0	-	kHz
	−3.0 dB		-	22.7	-	kHz
Stopband (Note 24)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.3	-	1/fs
Group Delay Distortion (0 to 20 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 24 fs: DCLKS[1:0] bits = "11")						
Passband (Note 24)	±0.16 dB	PB	0	-	13.3	kHz
	−0.28 dB		-	15.1	-	kHz
	−3.0 dB		-	22.5	-	kHz
Stopband (Note 24)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.8	-	1/fs
Group Delay Distortion (0 to 20 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (HPF): HPFC[1:0] bits = "00"						
Frequency Response (Note 24)	−3.0 dB	FR	-	3.7	-	Hz

Note 24. The passband and stopband frequencies scale with fs (sampling frequency). Frequency response is measured with respect to a 1 kHz input signal.

Note 25. This time is measured from the time that an analog signal is applied to the ADC input pin until both channels' 24-bit data reach the Audio Hub's data bus. This time includes group delay induced by the HPF. The delay time due to Audio Hub is two sampling period. The group delay is increased by two sampling period.

<fs = 96 kHz>

(Ta = –40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 96 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): ADC, DMIC(DMCLK=64 fs: DCLKS[1:0] bits = "00")						
Passband (Note 24)	±0.16 dB	PB	0	-	37.6	kHz
	–0.28 dB		-	40.0	-	kHz
	–3.0 dB		-	45.6	-	kHz
Stopband (Note 24)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.0	-	1/fs
Group Delay Distortion (0 to 40 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (Decimation LPF): DMIC(DMCLK=32 fs: DCLKS[1:0] bits = "01")						
Passband (Note 24)	±0.16 dB	PB	0	-	37.6	kHz
	–0.28 dB		-	40.0	-	kHz
	–3.0 dB		-	45.6	-	kHz
Stopband (Note 24)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.3	-	1/fs
Group Delay Distortion (0 to 40 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (Decimation LPF): DMIC(DMCLK=48 fs: DCLKS[1:0] bits = "10")						
Passband (Note 24)	±0.16 dB	PB	0	-	35.4	kHz
	–0.28 dB		-	38.1	-	kHz
	–3.0 dB		-	45.5	-	kHz
Stopband (Note 24)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.3	-	1/fs
Group Delay Distortion (0 to 40 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (Decimation LPF): DMIC(DMCLK=24 fs: DCLKS[1:0] bits = "11")						
Passband (Note 24)	±0.16 dB	PB	0	-	26.6	kHz
	–0.28 dB		-	30.2	-	kHz
	–3.0 dB		-	44.9	-	kHz
Stopband (Note 24)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	5.8	-	1/fs
Group Delay Distortion (0 ~ 40 kHz)		ΔGD	-	-	2.4	1/fs
Digital Filter (HPF): HPFC[1:0] bits = "00"						
Frequency Response (Note 24)	–3.0 dB	FR	-	7.4	-	Hz

<fs = 192 kHz>

(Ta = –40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 192 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): ADC, DMIC (DMCLK = 32 fs: DCLKS[1:0] bits = "01")						
Passband (Note 24)	±0.12 dB	PB	0	-	37	kHz
	–1.0 dB		-	51	-	kHz
	–3.0 dB		-	65	-	kHz
	–6.0 dB		-	78	-	kHz
Stopband (Note 24)		SB	145.5	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	4.4	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 24 fs: DCLKS[1:0] bits = "11")						
Passband (Note 24)	±0.12 dB	PB	0	-	35	kHz
	–1.0 dB		-	49	-	kHz
	–3.0 dB		-	63	-	kHz
	–6.0 dB		-	76	-	kHz
Stopband (Note 24)		SB	145.5	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay (Note 25)		GD	-	4.4	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (HPF): HPFC[1:0] bits = "00"						
Frequency Response (Note 24)	–3.0 dB	FR	-	14.8	-	Hz

8.9.2. Voice Filter (ADVF bit = “1”)

<fs = 8 kHz>

(Ta = –40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 8 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): ADC, DMIC (DMCLK = 64 fs: DCLKS[1:0] bits = “00”)						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 3.35	3.15 -	kHz kHz
Stopband (Note 24)		SB	4.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	15.2	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 32 fs: DCLKS[1:0] bits = “01”)						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 3.35	3.15 -	kHz kHz
Stopband (Note 24)		SB	4.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	15.5	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 48 fs: DCLKS[1:0] bits = “10”)						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 3.34	3.12 -	kHz kHz
Stopband (Note 24)		SB	4.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	15.5	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 24 fs: DCLKS[1:0] bits = “11”)						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 3.32	3.07 -	kHz kHz
Stopband (Note 24)		SB	4.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	16.0	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (HPF): HPFC[1:0] bits = “00”						
Frequency Response (Note 24)	–3.0 dB	FR	-	0.6	-	Hz

<fs = 16 kHz>

(Ta = –40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; fs = 16 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): ADC, DMIC (DMCLK = 64 fs: DCLKS[1:0] bits = "00")						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 6.7	6.3 -	kHz kHz
Stopband (Note 24)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	15.2	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 32 fs: DCLKS[1:0] bits = "01")						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 6.7	6.3 -	kHz kHz
Stopband (Note 24)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	15.5	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 48 fs: DCLKS[1:0] bits = "10")						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 6.7	6.3 -	kHz kHz
Stopband (Note 24)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	15.5	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (Decimation LPF): DMIC (DMCLK = 24 fs: DCLKS[1:0] bits = "11")						
Passband (Note 24)	–0.5 dB to +0.5 dB –3.0 dB	PB	0 -	- 6.6	6.2 -	kHz kHz
Stopband (Note 24)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay (Note 25)		GD	-	16.0	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	1/fs
Digital Filter (HPF): HPFC[1:0] bits = "00"						
Frequency Response (Note 24)	–3.0 dB	FR	-	1.2	-	Hz

8.10. DC Characteristics

(Ta = –40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Normal Pin (Note 26)					
High-Level Input Voltage	VIH	70 % TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30 % TVDD	V
High-Level Output Voltage (Iout = –200 µA)	VOH	TVDD –0.2	-	-	V
Low-Level Output Voltage Except for SDA pin and WAKEUP pin (WUPOL[1:0] bits = "01"), Iout = 200 µA	VOL	-	-	0.2	V
SDA pin and WAKEUP pin (WUPOL[1:0] bits = "01"), 2 V < TVDD ≤ 3.6 V (Iout = 3 mA)	VOL	-	-	0.4	V
1.65 V ≤ TVDD ≤ 2 V (Iout = 2 mA)	VOL	-	-	20 % TVDD	V
Input Leakage Current (Note 27)	Iin	–5	-	+5	µA
Digital MIC Interface (DMDAT1/2 pin Input)					
High-Level Input Voltage	VIH2	65 % AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35 % AVDD	V
Digital MIC Interface (DMCLK1/2 pin Output)					
High-Level Output Voltage (Iout = –80 µA)	VOH2	AVDD –0.4	-	-	V
Low-Level Output Voltage (Iout = 80 µA)	VOL2	-	-	0.4	V
Input Leakage Current	Iin	–5	-	+5	µA

Note 26. XTI/MCKI, XTO, TDMIN, BCLK, LRCK, TDMIN, SDTO, FLAG/MCKO, SYNCTRIG, I2CSEL, CSN/CAD, SCLK/SCL, SO/SDA, SI, SID, DCSI, PDN, EXTTRIG, WAKEUP, TEST pins

Note 27. Except for the case where MCKI/XTI pin is connected to TVDD; in this case the value is –50 µA to +50 µA.

8.11. Switching Characteristics

(Ta = −40 to 85 °C; AVDD = 1.7 to 1.9 V or 3.0 to 3.6 V; TVDD = 1.65 to 3.6 V; C_L = 50 pF(MCKO, BCLK, LRCK pins), 20 pF(SDTO pin); unless otherwise specified)

<System Clock>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Input Timing					
Input Frequency	fMCK	0.256	-	24.576	MHz
Pulse Width Low	tMCKL	0.4 / fMCK	-	-	nsec
Pulse Width High	tMCKH	0.4 / fMCK	-	-	nsec
Crystal Oscillator (XTI pin)					
Input Frequency	fMCK		12.288		MHz
Master Clock Output Timing					
Output Frequency	fMCKO	-	-	24.576	MHz
Duty Cycle (Note 28)	dMCKO	-	50	-	%
LRCK/BCLK Input Timing (Slave mode)					
LRCK Input Timing					
Frequency	fs	8	-	192	kHz
High Time	tLRH	1 / (128 fs)	-	-	nsec
Low Time	tLRL	1 / (128 fs)	-	-	nsec
BCLK Input Timing					
Frequency (Note 29)	fBCK	0.256	-	24.576	MHz
BCLK Pulse Width Low	tBCKL	0.4 x tBCK	-	-	nsec
BCLK Pulse Width High	tBCKH	0.4 x tBCK	-	-	nsec
LRCK/BCLK Output Timing (Master mode)					
LRCK Output Timing					
Frequency	fs	8	-	192	kHz
Pulse Width High					
PCM Mode	tLRH	-	tBCK	-	nsec
Except PCM Mode	tLRH	-	50	-	%
BCLK Output Timing					
Frequency (Note 29)	fBCK	0.256	-	24.576	MHz
Duty	dBCK	-	50	-	%

Note 28. Valid when (MDIV + 1) is 1 or an even number. When (MDIV + 1) = 3, duty cycle will be 67 % (Typ.). When MDIV and FS bits are set such that PLLCLK is divided by 1.5, duty cycle will be 67 % (Typ.).

Note 29. The value must satisfy this conditional expression “(fBCK) ≥ 2 x fs x (bit depth)”.

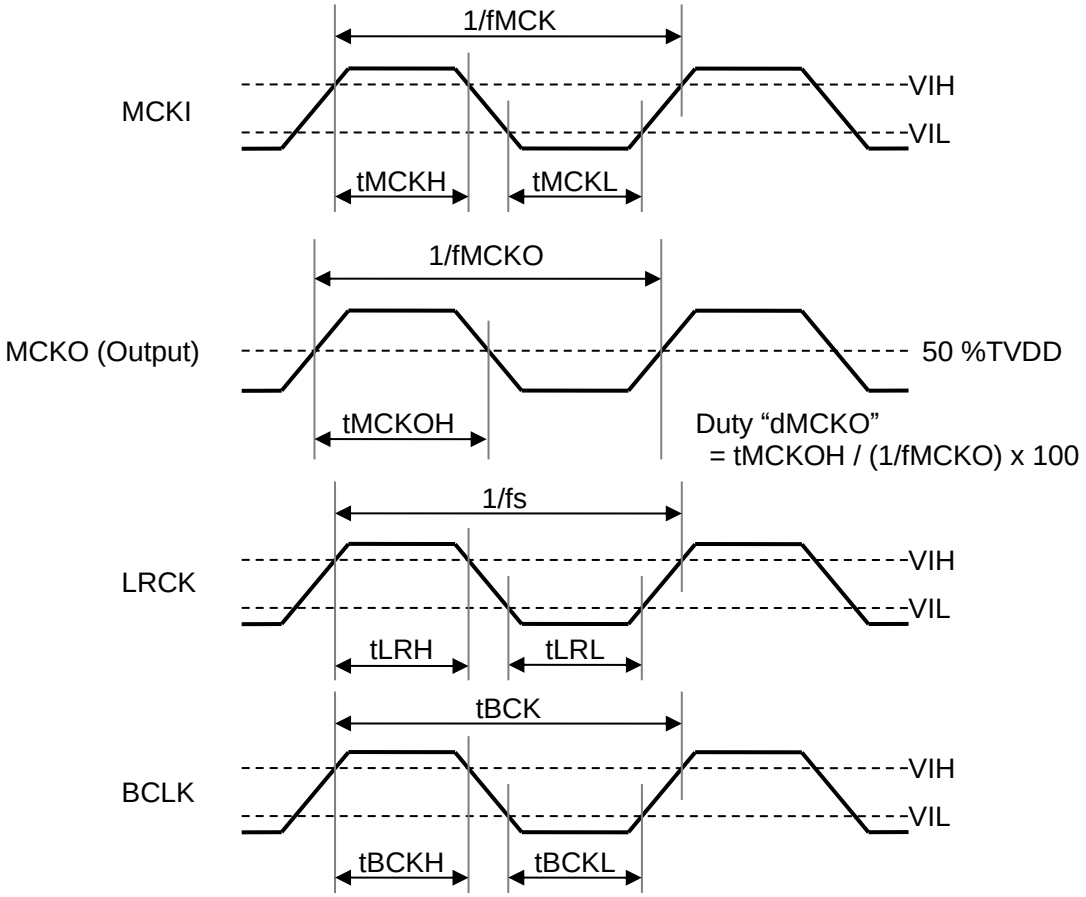


Figure 2. System Clock (Slave Mode)

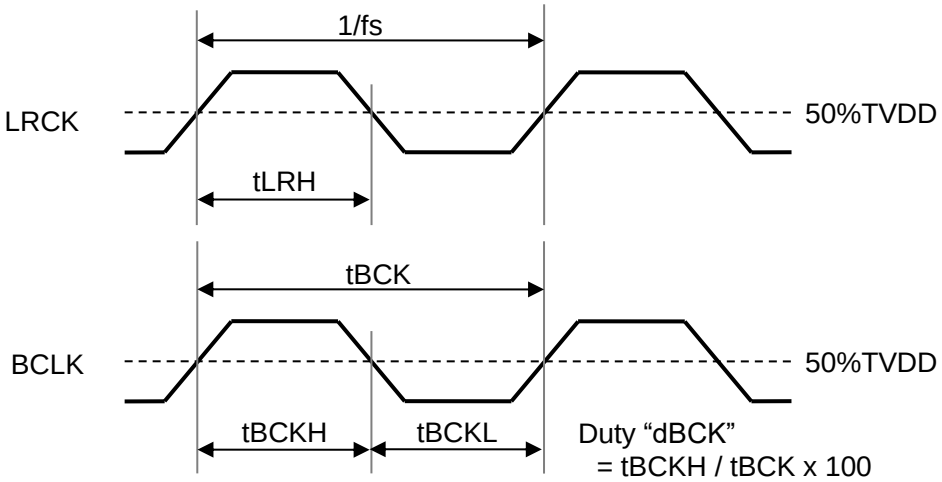


Figure 3.System Clock (Master Mode)

<Audio Interface>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)					
Delay Time from BCLK "↑" to LRCK (Note 30)	tBLRD	10	-	-	nsec
Delay Time from LRCK to BCLK "↑" (Note 30)	tLRBD	10	-	-	nsec
TDMIN Setup Time	tBSIDS	10	-	-	nsec
TDMIN Hold Time	tBSIDH	5	-	-	nsec
Delay Time from BCLK "↓" to SDTO (Note 31, Note 33)	tBSOD1	-	-	20	nsec
Delay Time from BCLK "↑" to SDTO (Note 30)	tBSOD2	5	-	30	nsec
Audio Interface Timing (Master mode)					
BCLK Frequency	fBCK	-	32 48 64 128 256 512	-	fs
BCLK Duty	dBCK	-	50	-	%
Delay Time from BCLK "↓" to LRCK (Note 31)	tMBL	–10	-	10	nsec
TDMIN Setup Time	tBSIDS	10	-	-	nsec
TDMIN Hold Time	tBSIDH	10	-	-	nsec
Delay Time from BCLK "↓" to SDTO (Note 31, Note 32)	tBSOD	-	-	10	nsec
Delay Time from TDMIN/ADC/DMIC1/DMIC2 to SDTO (Note 33)	tIOD	-	2	-	1/fs

Note 30. When the polarity of BCLK is inverted by BCKP bit = "1", delay time starts from BCLK "↓".
Note 31. When the polarity of BCLK is inverted by BCKP bit = "1", delay time starts from BCLK "↑".
Note 32. When BCLK input frequency is 12.288 MHz or more, SDOPH bit should be set to "1" in slave mode. In master mode, SDOPH bit should always be set to "0".
Note 33. This parameter is measured from the time that the data of TDMIN, ADC, DMIC1 or DMIC2 reaches the Audio Hub's data bus until this data is output from the SDTO pin.

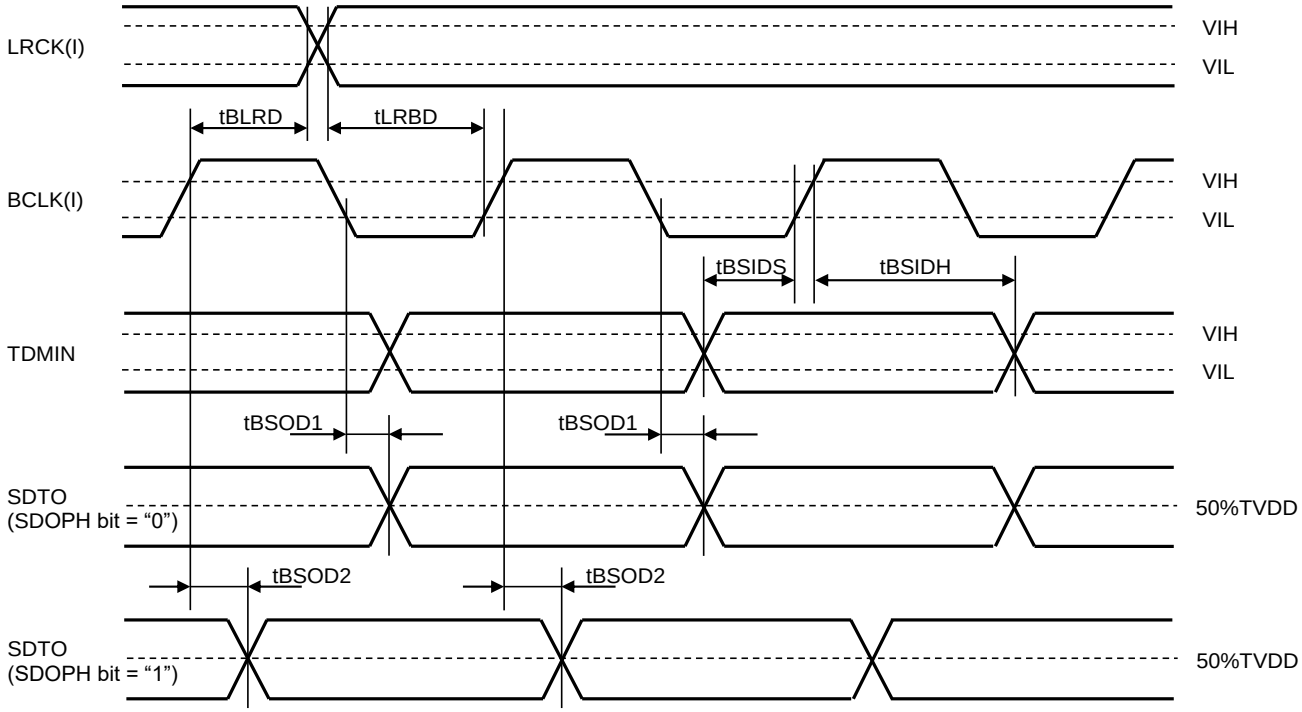


Figure 4. Audio Interface Timing (Slave Mode)

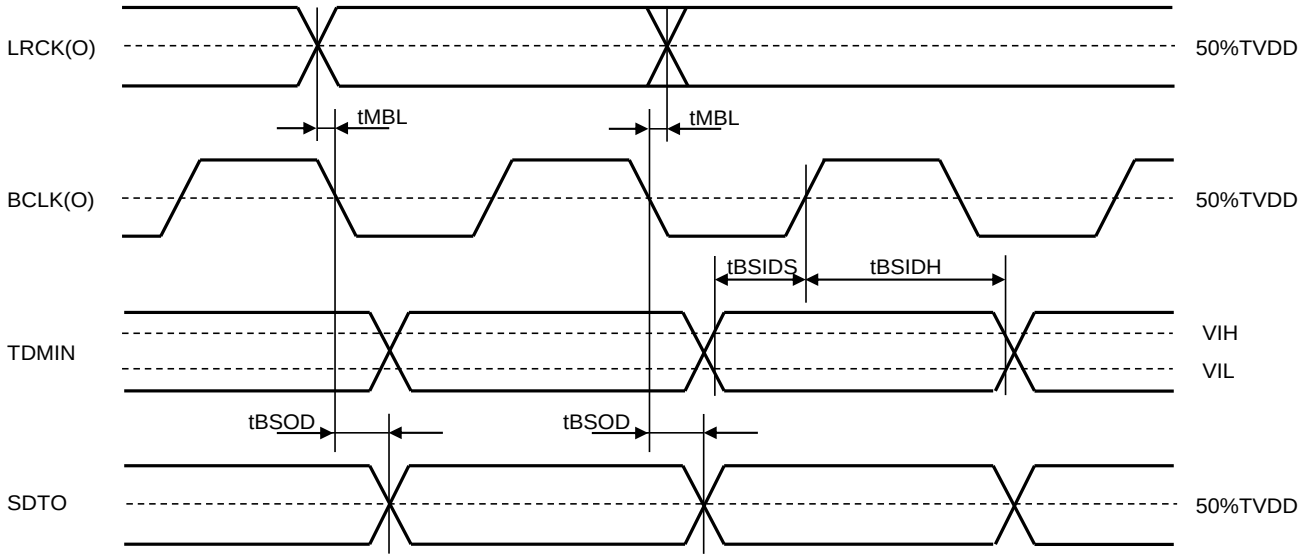
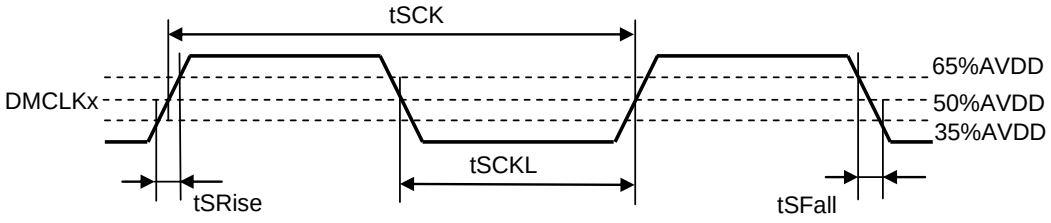


Figure 5. Audio Interface Timing (Master mode)

<Digital Mic Interface>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Audio Interface Timing: C_L = 100 pF					
DMCLK1/2 Output Timing					
Period	tSCK	-	1 / (64 fs) 1 / (48 fs) 1 / (32 fs) 1 / (24 fs)	-	nsec
Rise time	tSRise	-	-	10	nsec
Fall time	tSFall	-	-	10	nsec
Duty Cycle	dSCK	45	50	55	%
Audio Interface Timing (DMCLK1/2, DMDAT1/2 pins)					
DMDAT1/2 Setup Time	tDMS	50	-	-	nsec
DMDAT1/2 Hold Time	tDMH	0	-	-	nsec



dSCK = 100 x tSCKL / tSCK

Figure 6. DMCLK1/2 Output Timing

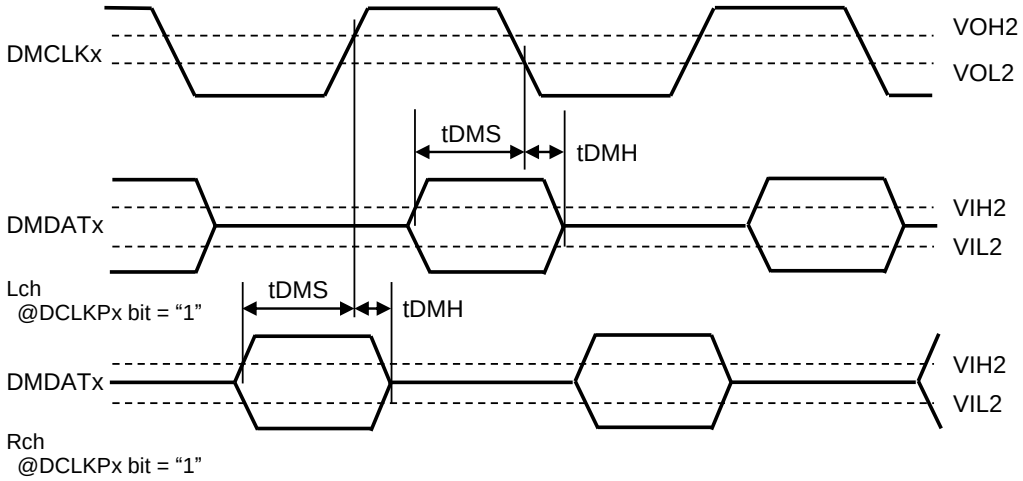


Figure 7. Audio Interface Timing

<I²C-bus: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing: (Note 34)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µsec
Clock Low Time	tLOW	1.3	-	-	µsec
Clock High Time	tHIGH	0.6	-	-	µsec
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µsec
SDA Hold Time from SCL Falling (Note 35)	tHD:DAT	0	-	-	µsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µsec
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µsec
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µsec
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µsec
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	µsec

Note 34. I²C-bus is a registered trademark of NXP B.V.

Note 35. Data must be held long enough to bridge the 300 nsec-transition time of SCL.

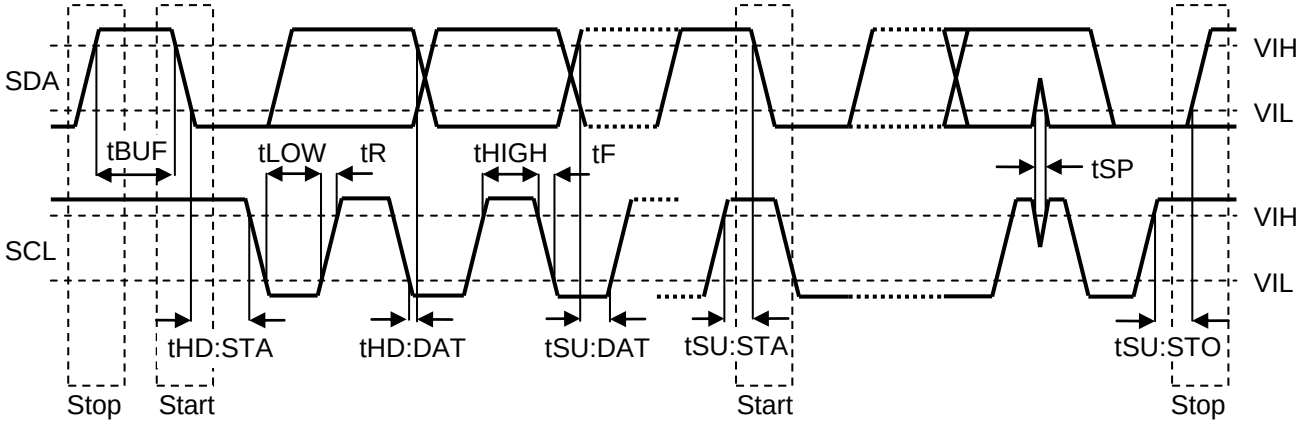


Figure 8. I²C-bus Mode Timing

<SPI Interface>

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK					
Frequency	fSCLK	-	-	13	MHz
Duty Cycle	dSCLK	45	50	55	%
CSN					
High Level Width	tWRQH	160	-	-	nsec
From PDN "↑" to CSN "↓"	tIRRQ	20	-	-	msec
From CSN "↓" to SCLK "↑"	tWSC	160	-	-	nsec
From SCLK "↑" to CSN "↑"	tSCW	160	-	-	nsec
SI, DCSI					
Latch Setup Time	tSIS	12	-	-	nsec
Latch Hold Time	tSIH	32	-	-	nsec
SO					
Delay Time from SCLK "↓"to SO	tSOS	-	-	24	nsec
Hold Time from SCLK "↑" to SO (Note 36)	tSOH	32	-	-	nsec
CSN "↓" to SO ("L") (SOCFG bit = "1")	tDCD	-	-	140	nsec
CSN "↑" to SO (Hi-Z) (SOCFG bit = "1")	tCCZ	-	-	140	nsec

Note 36. Except when inputting the 8th bit of the command code.

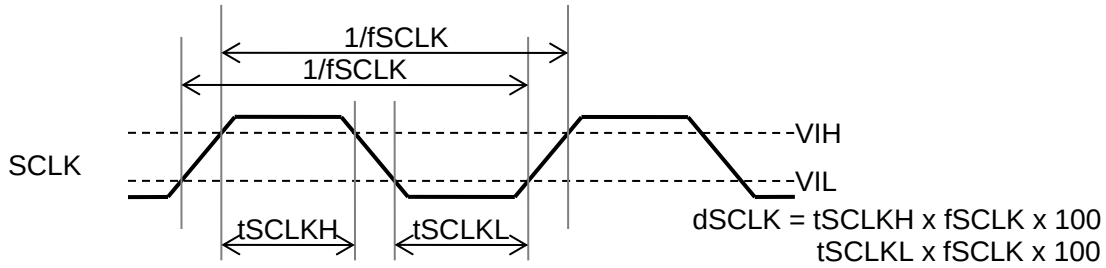


Figure 9. SPI Interface SCLK

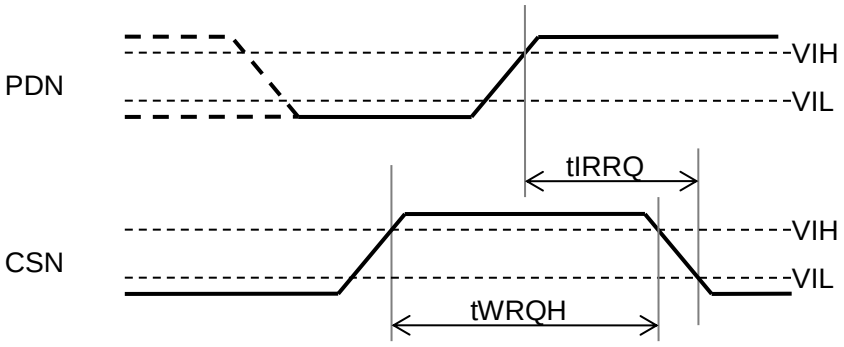


Figure 10. SPI Interface CSN/PDN

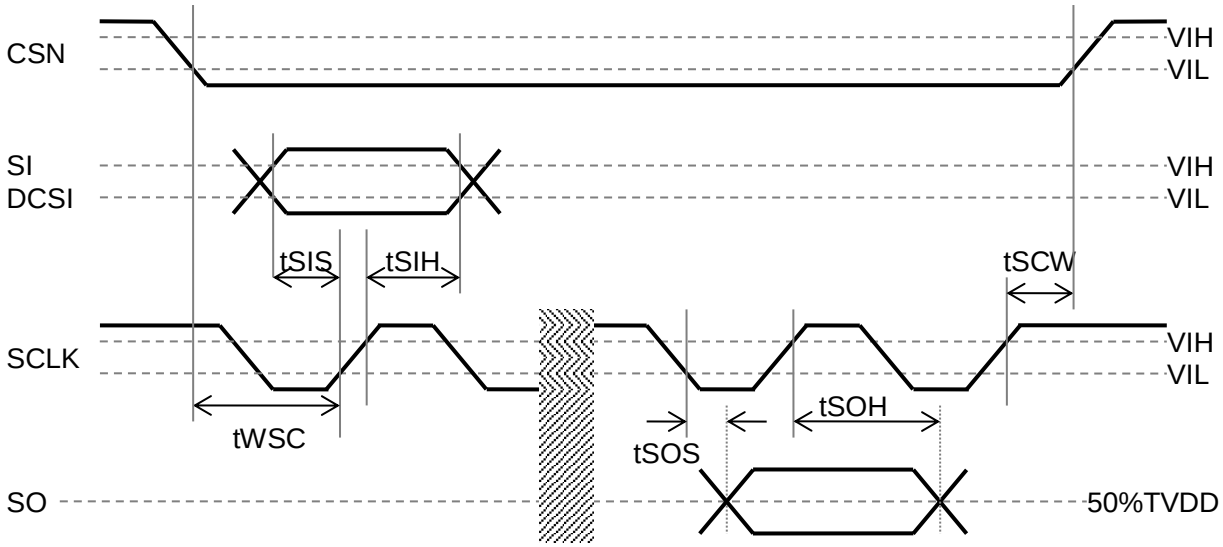


Figure 11. SPI Interface (SI/SO)

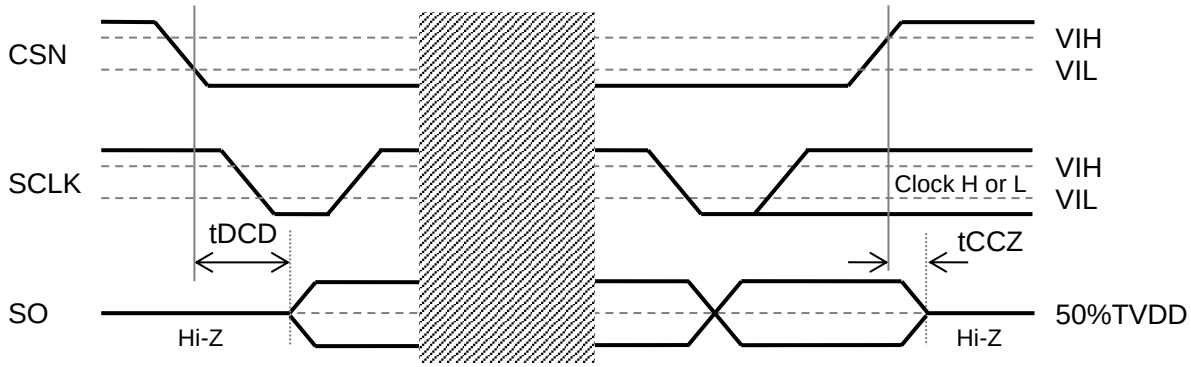


Figure 12. SPI Interface (SO) @ SOCFG bit = “1”

Parameter	Symbol	Min.	Typ.	Max.	Unit
Noise Filter (EXTTRIG pin)					
Accept Pulse Width	tTRG	1000	-	-	nsec
Reject Pulse Width	tRTP	-	-	50	nsec

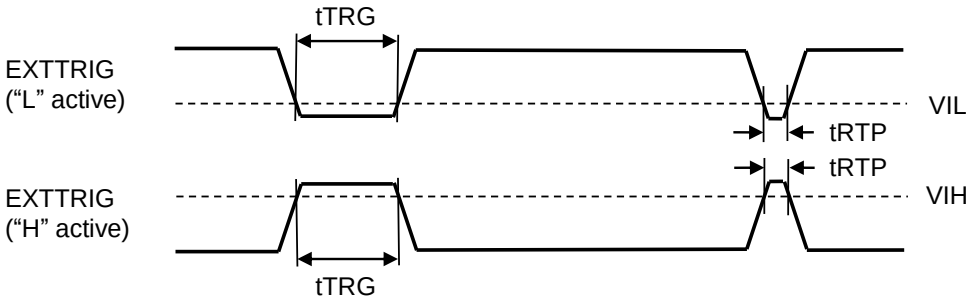


Figure 13. Noise Filter (EXTTRIG pin)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-down & Reset Timing (x = 1, 2)					
PDN Accept Pulse Width (Note 37)	tPDN	1	-	-	msec
PMAD1/2 bit = “1” to SDTO valid (Note 38)					
ADRST[2:0] bits = “000”	tPDV	-	1058	-	1/fs
ADRST[2:0] bits = “001”	tPDV	-	266	-	1/fs
ADRST[2:0] bits = “010”	tPDV	-	2114	-	1/fs
ADRST[2:0] bits = “011”	tPDV	-	530	-	1/fs
ADRST[2:0] bits = “100”	tPDV	-	4226	-	1/fs
ADRST[2:0] bits = “101”	tPDV	-	10	-	1/fs
ADRST[2:0] bits = “110”	tPDV	-	18	-	1/fs
ADRST[2:0] bits = “111”	tPDV	-	34	-	1/fs
PMDMxA/B bit = “1” to SDTO valid (Note 39)					
ADRST[2:0] bits = “000”	tPDV	-	1058	-	1/fs
ADRST[2:0] bits = “001”	tPDV	-	266	-	1/fs
ADRST[2:0] bits = “010”	tPDV	-	2114	-	1/fs
ADRST[2:0] bits = “011”	tPDV	-	530	-	1/fs
ADRST[2:0] bits = “100”	tPDV	-	4226	-	1/fs
ADRST[2:0] bits = “101”	tPDV	-	10	-	1/fs
ADRST[2:0] bits = “110”	tPDV	-	18	-	1/fs
ADRST[2:0] bits = “111”	tPDV	-	34	-	1/fs

Note 37. The PDN pin must held “L” for a period greater than or equal to tPDN. The AK5706 will not be reset by a “L” pulse less than or equal to 50 nsec.

Note 38. This is the count of LRCK “↑” from PMAD1/2[1:0] bits = “01”.

Note 39. This is the count of LRCK “↑” from PMDMxA/B[1:0] bits = “01”.

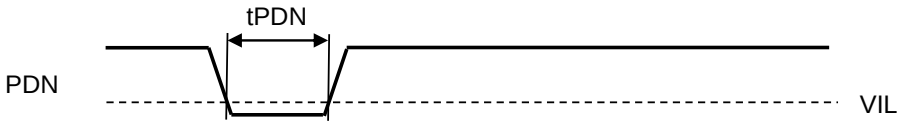


Figure 14. Power Down & Standby

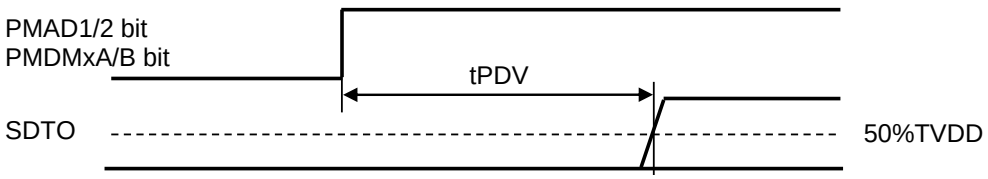
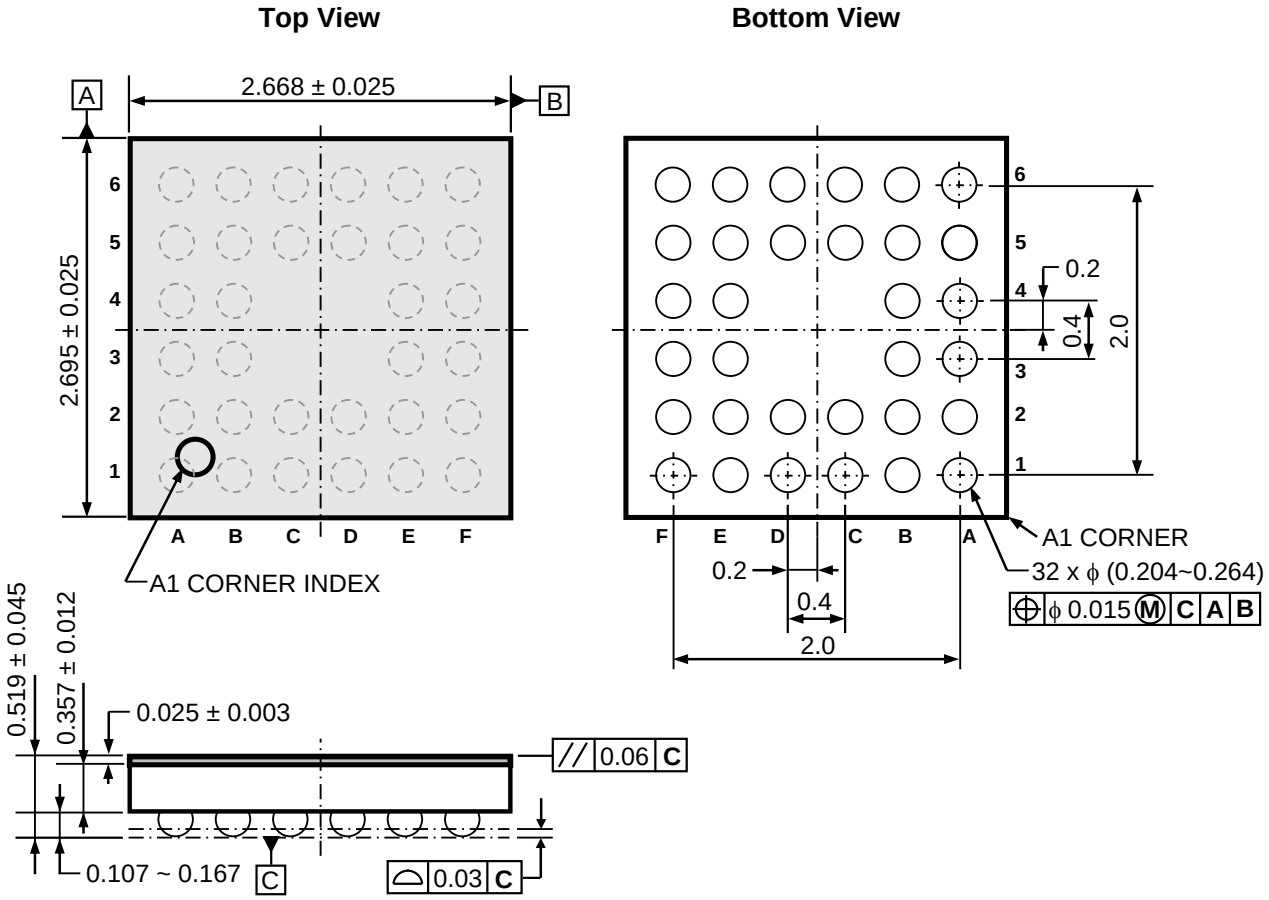


Figure 15. ADC, DMIC1/2 Power Up Timing

9. Package

9.1. Outline Dimensions

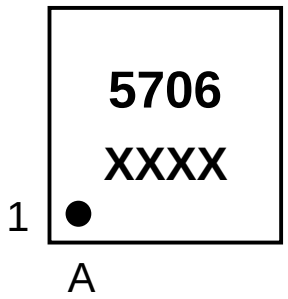
32-pin CSP (2.668 x 2.695 mm, 0.4 mm pitch)



9.2. Material & Lead finish

Package molding compound: Epoxy, Halogen (Br and Cl) free
Solder ball material: SnAgCu

9.3. Marking



XXXX: Date code (4 digits)
Pin #A1 indication

10. Ordering Guide

AK5706ECB −40 to +85˚C 32-pin CSP (0.4mm pitch)
AKD5706 Evaluation board for AK5706

11. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
20/05/15	00	First Edition		

Thank you for your access to AKM product information.
More detail product information is available, please contact our sales office or authorized distributors.

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.

Rev.1