AK5730

4-Channel Differential Audio ADC for Line & Mic Inputs

GENERAL DESCRIPTION

The AK5730 is a 4-channel ADC with SAR ADC for DC measurement. The ADC supports Line and Microphone inputs, making it ideal for microphone array applications. TDM audio format makes it easy to connect with DSP.

FEATURES

1. Audio ADC
   - 4-Channel Audio ADC
   - Full-differential Input and Single-ended Input
   - Input Voltage:
     Microphone: 1.65Vrms,
     LINE and Phone: 3Vrms (with external resistors) programmable
     Boost input: 11.7Vrms (with external resistors) programmable
   - ADC Performance:
     S/(N+D): typ 92dB
     DR, S/N: typ 100dB
   - Digital HPF for DC-offset cancellation: fc=1Hz with individual on/off
2. Sampling Rate: 8kHz ~ 48kHz
3. Master Clock: 256fs, 384fs, 512fs or Internal PLL
4. Master/Slave mode
5. Audio Interface Format: MSB First, 2's complement
   - 24bit I^2S
   - 24bit TDM interface up to 2 ICs cascade
6. SAR ADC
   - 1ch SAR ADC with 9:1 MUX
   - Reference Voltage: Ground
7. Channel Independent Microphone Diagnostics
   - open microphone
   - shorts to battery
   - shorts to ground
   - shorts across inputs
   - microphone bias over current
   - over temperature
8. Programmable Microphone Bias: 5V to 9V with 0.5V step
9. μP I/F: I^2C Bus (Ver 1.0, 400kHz Mode) or SPI
10. Power Supply: VDD = 3.0 to 3.6V
11. Operating Temperature : Ta = –40 to 105°C
12. Package: 48pin LQFP

■ Block Diagram

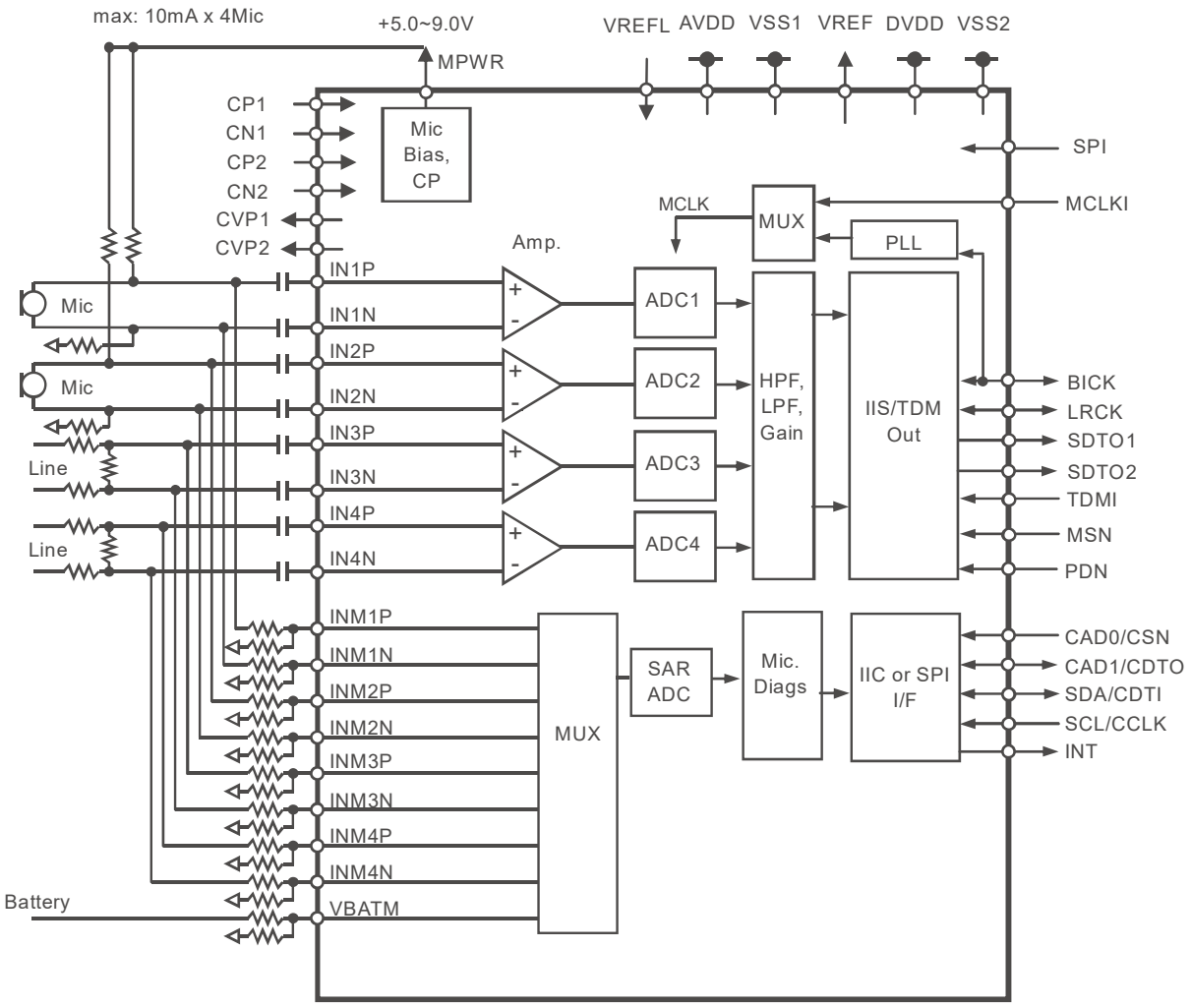
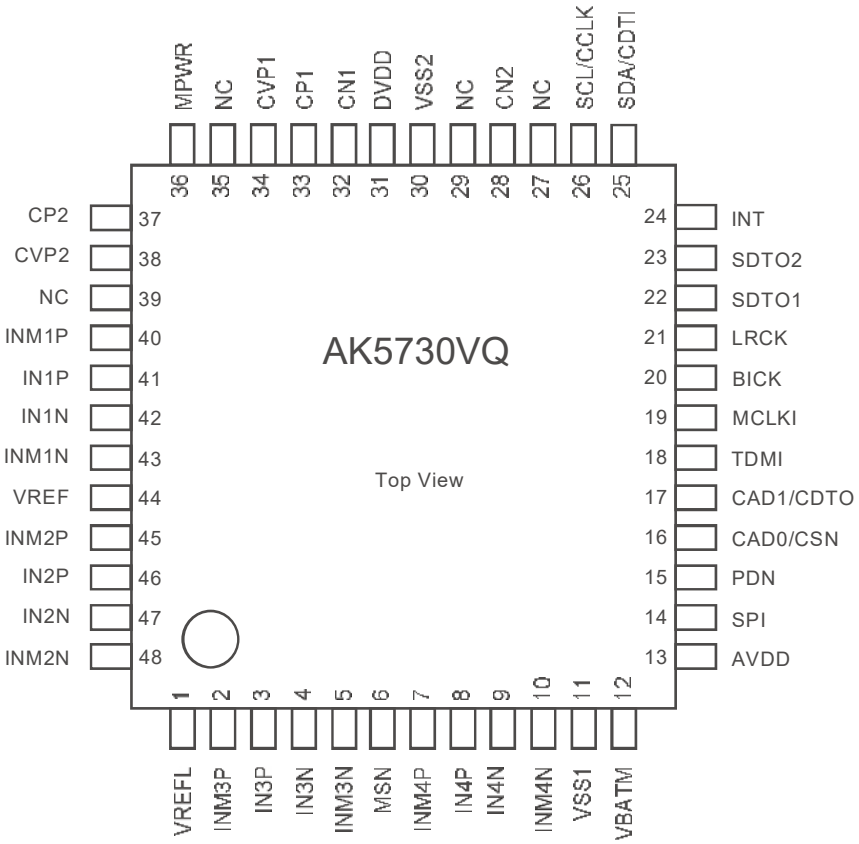


Figure 1. Block Diagram

■ Pin Layout


AK5730VQ
Top View
1 VREFL
2 INM3P
3 IN3P
4 IN3N
5 INM3N
6 MSN
7 INM4P
8 IN4P
9 IN4N
10 INM4N
11 VSS1
12 VBATM
13 AVDD
14 SPI
15 PDN
16 CAD0/CSN
17 CAD1/CDTO
18 TDMI
19 MCLKI
20 BICK
21 LRCK
22 SDTO1
23 SDTO2
24 INT
25 SDA/CDTI
26 SCL/CCLK
27 NC
28 CN2
29 NC
30 VSS2
31 DVDD
32 CN1
33 CP1
34 CVP1
35 NC
36 MPWR
37 CP2
38 CVP2
39 NC
40 INM1P
41 IN1P
42 IN1N
43 INM1N
44 VREF
45 INM2P
46 IN2P
47 IN2N
48 INM2N

PIN/FUNCTION

No.	Pin Name	I/O	Function	Power Down Status
1	VREFL	I	ADC Reference Pin. 0V	-
2	INM3P	I	Ch3 Positive Input Monitor Pin	Hi-z
3	IN3P	I	Ch3 Positive Input Pin (with DC cut capacitor)	Hi-z
4	IN3N	I	Ch3 Negative Input Pin (with DC cut capacitor)	Hi-z
5	INM3N	I	Ch3 Negative Input Monitor Pin	Hi-z
6	MSN	I	Master/Slave Control Pin	Hi-z
7	INM4P	I	Ch4 Positive Input Monitor Pin	Hi-z
8	IN4P	I	Ch4 Positive Input Pin (with DC cut capacitor)	Hi-z
9	IN4N	I	Ch4 Negative Input Pin (with DC cut capacitor)	Hi-z
10	INM4N	I	Ch4 Negative Input Monitor Pin	Hi-z
11	VSS1	-	Ground Pin 1. 0V	-
12	VBATM	I	Battery Power Monitor Pin	Hi-z
13	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V Normally connected to VSS1 with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.	-
14	SPI	I	Control Mode Select Pin "L": I^2C Bus control mode, "H": 4-wire serial control mode	Hi-z
15	PDN	I	Power-Down Mode Pin When at "L", the AK5730 is in the power-down mode and is held in reset. The AK5730 should always be reset upon power-up.	Hi-z
16	CAD0	I	(SPI pin = "L") Chip Address 0 Pin	Hi-z
	CSN	I	(SPI pin = "H") Chip Select Pin in serial control mode	
17	CAD1	I	(SPI pin = "L") Chip Address 1 Pin	Hi-z
	CDTO	O	(SPI pin = "H") Control Data Output Pin	
18	TDMI	I	TDM Data Input Pin	Hi-z
19	MCLKI	I	Master Clock Input Pin	Hi-z
20	BICK	I/O	Audio Serial Data Clock Pin	Hi-z (Slave) L Output (Master)
21	LRCK	I/O	Channel Clock Pin	Hi-z (Slave) L Output (Master)
22	SDTO1	O	ADC Audio Serial Data Output1 Pin	L Output
23	SDTO2	O	ADC Audio Serial Data Output2 Pin	L Output
24	INT	O	Interrupt Signal Output Pin Normally connected to DVDD(3.3V) with an external 10kΩ resistor.	Hi-z
25	SDA	I/O	(SPI pin = "L") Control Data Input/Output Pin	Hi-z
	CDTI	I	(SPI pin = "H") Control Data Input Pin	
26	SCL	I	(SPI pin = "L") Control Data Clock Pin	Hi-z
	CCLK	I	(SPI pin = "H") Control Data Clock Pin	
27	NC	-	This pin should be connected to VSS1.	-

No.	Pin Name	I/O	Function	Power Down Status
28	CN2	I	Negative Charge Pump Capacitor Terminal 2 Connect to CP2 with a 2.2μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the CP2 pin. Non-polarized capacitors can also be used. * The maximum bias voltage of this pin is 7.2V. The capacitance variation of an external capacitor should be in the range of 2.2μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	10kΩ Connect to VSS
29	NC	-	This pin should be connected to VSS1.	-
30	VSS2	-	Digital Ground Pin and Charge Pump Ground Pin , 0V	-
31	DVDD	-	Digital Power Supply Pin and Charge Pump Circuit Positive Power Supply Pin 3.0V~3.6V Normally connected to VSS2 with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.	-
32	CN1	I	Negative Charge Pump Capacitor Terminal 1 Connect to CP1 with a 2.2μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the CP1 pin. Non-polarized capacitors can also be used. * The maximum bias voltage of this pin is 3.6V. The capacitance variation of an external capacitor should be in the range of 2.2μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	10kΩ Connect to VSS
33	CP1	I	Positive Charge Pump Capacitor Terminal 1 Connect to CN1 with a 2.2μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the CP1 pin. Non-polarized capacitors can also be used. * The maximum bias voltage of this pin is 3.6V. The capacitance variation of an external capacitor should be in the range of 2.2μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	50kΩ Connect to VSS
34	CVP1	O	Charge Pump Circuit Positive Voltage Output Pin 1 Connect to VSS2 with a 2.2μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the negative polarity pin should be connected to the VSS2 pin. Non-polarized capacitors can also be used. * The maximum bias voltage of this pin is 7.2V. The capacitance variation of an external capacitor should be in the range of 2.2μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	50kΩ Connect to AVDD
35	NC	-	This pin should be connected to VSS1.	-
36	MPWR	O	MIC Power Supply Pin Normally connected to VSS1 with a 1μF ceramic capacitor. * The maximum bias voltage of this pin is 10V. The capacitance variation of an external capacitor should be in the range of 1μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	Hi-z

No.	Pin Name	I/O	Function	Power Down Status
37	CP2	I	Positive Charge Pump Capacitor Terminal Pin 2 Connect to CN2 with a 2.2μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the CP2 pin. Non-polarized capacitors can also be used. * The maximum bias voltage of this pin is 7.2V. The capacitance variation of an external capacitor should be in the range of 2.2μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	5kΩ Connect to CVP1
38	CVP2	O	Charge Pump Circuit Positive Voltage Output Pin 2 Connect to VSS2 with a 2.2μF low ESR (Equivalent Series Resistance) capacitor over temperature. When this capacitor is polarized, the negative polarity pin should be connected to the VSS2 pin. Non-polarized capacitors can also be used. * The maximum bias voltage of this pin is 14.4V. The capacitance variation of an external capacitor should be in the range of 2.2μF +20% and -40% including the difference by a tolerance, a rate of temperature change and a bias voltage.	5kΩ Connect to CVP1
39	NC	-	This pin should be connected to VSS1.	-
40	INM1P	I	Ch1 Positive Input Monitor Pin	Hi-z
41	IN1P	I	Ch1 Positive Input Pin (with DC cut capacitor)	Hi-z
42	IN1N	I	Ch1 Negative Input Pin (with DC cut capacitor)	Hi-z
43	INM1N	I	Ch1 Negative Input Monitor Pin	Hi-z
44	VREF	O	Voltage Reference Pin for MPWR. Normally connected to VSS1 with a 1.0μF ceramic capacitor.	1MΩ Connect to AVDD
45	INM2P	I	Ch2 Positive Input Monitor Pin	Hi-z
46	IN2P	I	Ch2 Positive Input Pin (with DC cut capacitor)	Hi-z
47	IN2N	I	Ch2 Negative Input Pin (with DC cut capacitor)	Hi-z
48	INM2N	I	Ch2 Negative Input Monitor Pin	Hi-z

Note 1. All digital input pins should not be left floating.
NC Pin (No internal bonding).

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	0.3	4.6	V
	Digital, Charge Pump	DVDD	0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	–0.3	CVP1+0.3	V
Digital Input Voltage		VIND	0.3	DVDD+0.3	V
Operating Temperature (powered applied)		Ta	–40	105	°C
Storage Temperature		Tstg	65	150	°C

Note 2. All voltages with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 3. CVP1: CVP1 pin voltage.
The internal positive power supply generating circuit provides positive power supply (CVP1).

Mode	CVP1 pin Voltage
Power-down (PDN pin and RSTN bit control)	AVDD
Normal operation	1.67 x AVDD

CVP1 pin voltage

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2 =0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies	Analog	AVDD	3.0	3.3	3.6	V
(Note 4)	Digital, Charge Pump	DVDD	3.0	3.3	3.6	V

Note 2. All voltages with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 4. The AVDD, DVDD must be the same voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD =3.3V; VSS1=VSS2 =0V; MCLK =512fs, fs=48kHz, BCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified; GAIN bit = "0")

Parameter		min	typ	max	Unit
ADC Analog Characteristics (AC):					
Resolution		-	-	24	Bits
Input Voltage	Differential (Note 5)	1.55	1.65	1.75	Vrms
	Single-ended (Note 6)	0.77	0.82	0.87	Vrms
	Gain mode (Note 7)	0.51	0.55	0.59	Vrms
Input Impedance		1.0	1.4		MΩ
S/(N+D)	–0.5dBFS Differential	86	92	-	dB
	0.5dBFS Single-ended	86	92	-	dB
	–0.5dBFS Gain mode	86	92		dB
Dynamic Range	–60dBFS, A-weighted Differential	93	100	-	dB
	–60dBFS, A-weighted Single-ended	92	99	-	dB
	–60dBFS, A-weighted Gain mode	92	98		dB
S/N	A-weighted Differential	93	100	-	dB
	A-weighted Single-ended	92	99	-	dB
	10mVrms input, A-weighted Gain mode	57	63	-	dB
Interchannel Isolation		90	100	-	dB
Interchannel Gain Mismatch			0	0.3	dB
CMRR	1kHz, Differential (Note 8)	70	85		dB
	20kHz, Differential (Note 8)	70	85		dB
	1kHz, Single-ended (Note 8)	65	80		dB
	20kHz, Single-ended (Note 8)	55	65		dB
	1kHz, Gain mode (Note 9)	65	80		dB
	20kHz, Gain mode (Note 9)	65	80		dB
PSRR (1kHz, Note 10)			50		dB
MIC Power Supply:					
Output DC Voltage (Note 11)	MBS3-0 bits= "0000"	4.90	5	5.10	V
	MBS3-0 bits= "0001"	5.39	5.5	5.61	V
	MBS3-0 bits= "0010"	5.88	6	6.12	V
	MBS3-0 bits= "0011"	6.37	6.5	6.63	V
	MBS3-0 bits= "0100"	6.86	7	7.14	V
	MBS3-0 bits= "0101"	7.35	7.5	7.65	V
	MBS3-0 bits= "0110"	7.84	8	8.16	V
	MBS3-0 bits= "0111"	8.33	8.5	8.67	V
	MBS3-0 bits= "1000"	8.78	9	9.22	V
Microphone Current (for 4 channels)		0.1		40	mA
Output Noise Level (A-weighted)			-100	-94	dBV
SAR ADC Characteristics (DC):					
Resolution		-	-	12	Bits
Input Voltage (Note 12)		3.2	3.3	3.4	V
Integral Nonlinearity (INL) Error		-4		+5	LSB
Differential Nonlinearity (DNL) Error		-2		+2	LSB

Note 5. The voltage difference between IN*P and IN*N pins. Input Voltage should be adjusted with external resistors. Input voltage is proportional to AVDD voltage. Vin = 0.5 × AVDD Vrms (typ). (*=1,2,3,4)

Note 6. In single-ended input mode, IN*P pin, IN*N pin must be connected to signal common. Input Voltage should be adjusted with external resistors. When STD* bit = "1", Input voltage is proportional to AVDD voltage. (*=1,2,3,4) Vin = 0.25 × AVDD Vrms (typ).

Note 7. The voltage difference between IN*P and IN*N pins. Input Voltage should be adjusted with external resistors. When GAIN* bit = "1", Input Voltage = 0.55Vrms = 0.167 × AVDD Vrms (typ). (*=1,2,3,4)

Note 8. The 1kHz, 1.0Vpp signal is applied to IN*N and IN*P with same phase. CMRR is measured as the attenuation level from 0dB = -7.5dBFS(since the normal 1Vpp= -7.5dBFS). (*=1,2,3,4)

Note 9. The 1kHz, 0.5Vpp signal is applied to IN+. An IN- pin must be connected to the signal common. CMRR is measured as the attenuation level from 0dB = -4dBFS(since the normal 1Vpp=-4dBFS).

Note 10. The PSRR is applied to AVDD and DVDD with 1kHz, 100mVpp.

Note 11. When MBS3-0 bits = "0000" / "0001" / "0010" / "0011" / "0100" / "0101" / "0110" / "0111"/ "1000", the output DC Voltage(typ) is 1.52 / 1.67 / 1.82 / 1.97 / 2.12 / 2.27 / 2.42 / 2.58/ 2.73 × AVDD(V), respectively.
when MBS3-0 bits = "0000" / "0001" / "0010" / "0011" / "0100" / "0101" / "0110" / "0111", the output DC Voltage (min, max) is ±2.0% of Output DC Voltage(typ).
when MBS3-0 bits = "1000", Output DC Voltage(min, max) is ±2.5% of Output DC Voltage (typ).

Note 12. Input Voltage should be adjusted with external resistors. The input voltage range is from 0 to AVDD. Vin = 1.00 × AVDD (Vpp). The SAR ADC operates at more than 100 mV.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0~3.6V; VSS1=VSS2 =0V; fs=48kHz)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.13dB	PB	0		18.0	kHz
	-0.2dB		-	19.4	-	kHz
	-3.0dB		-	22.8	-	kHz
Stopband		SB	28	-	-	kHz
Passband Ripple		PR	-	-	±0.04	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 14)		GD	-	16.4	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	-3dB	FR	-	1.0	-	Hz
	-0.1dB		-	7.1	-	Hz

Note 13. The passband and stopband frequencies scale with fs.
For example, 19.4kHz (@-0.2dB)=0.404 × fs

Note 14. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register.

DC CHARACTERISTICS

(Ta=-40 ~+105°C; AVDD=DVDD=3.0~3.6V; VSS1=VSS2 =0V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 400μA(except SDA, INT pin), 3mA(SDA, INT pin))	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	±10	μA

(Ta=25°C; AVDD=DVDD=3.3V; VSS1=VSS2 =0V)

Power Supplies				
Parameter	**min**	**typ**	**max**	**Unit**
Power Supply Current				
Normal Operation (PDN pin = "H")				
DVDD (Microphone Current=40mA)	-	183	225	mA
DVDD (Microphone Current=100uA)	-	22	36	mA
AVDD	-	9	13.5	mA
Power-Down Mode (PDN pin = "L"; Note 15)				
DVDD	-	3	20	μA
AVDD	-	0	20	μA

Note 15. All digital inputs including clock pins (MCLKI, BICK, LRCK and TDMI) are held at DVDD or VSS2.

SWITCHING CHARACTERISTICS

(Ta=-40~+105°C; AVDD=DVDD=3.0~3.6V; VSS1=VSS2 =0V; C_L=20pF)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
External Clock					
256fs:	fCLK	2.048	-	12.288	MHz
Pulse Width Low	tCLKL	32	-	-	ns
Pulse Width High	tCLKH	32	-	-	ns
384fs:	fCLK	3.072	-	18.432	MHz
Pulse Width Low	tCLKL	22	-	-	ns
Pulse Width High	tCLKH	22	-	-	ns
512fs:	fCLK	4.096	-	24.576	MHz
Pulse Width Low	tCLKL	16	-	-	ns
Pulse Width High	tCLKH	16	-	-	ns
LRCK Timing (Slave mode)					
Stereo mode (TDM1/0 bit = "00")					
frequency	fs	8	-	48	kHz
Duty Cycle	Duty	45	-	55	%
TDM256 mode (Note 16) **(TDM1/0 bit = "01")**					
LRCK frequency	fs	8	-	48	kHz
"H" time	tLRH	1/256fs	-	-	ns
"L" time	tLRL	1/256fs	-	-	ns
LRCK Timing (Master Mode)					
Stereo mode (TDM1/0 bit = "00")					
Normal Speed Mode	fs	8	-	48	kHz
Duty Cycle	Duty	-	50	-	%
TDM256 mode (Note 16) **(TDM1/0 bit = "01")**					
LRCK frequency	fs	8	-	48	kHz
"H" time (Note 17)	tLRH	-	1/8fs	-	ns

Note 16. Master clock should be input the 256fs/512fs in Master mode.
Note 17. If the format is I^2S, it is "L" time.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1/0 bit = "00")					
BICK Period	tBCK	320	-	-	ns
BICK Pulse Width Low	tBCKL	128	-	-	ns
Pulse Width High	tBCKH	128	-	-	ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	20	-	-	ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	20	-	-	ns
LRCK Edge to SDTO(MSB)(Except I^{2}S mode)	tLRS	-	-	20	ns
BICK "↓" to SDTO	tBSD	-	-	20	ns
TDM256 mode (TDM1/0 bit = "01")					
BICK Period	tBCK	80	-	-	ns
BICK Pulse Width Low	tBCKL	32	-	-	ns
Pulse Width High	tBCKH	32	-	-	ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	20	-	-	ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	20	-	-	ns
SDTO Setup time BICK "↑"	tBSS	16.3	-	-	ns
SDTO Hold time BICK "↑"	tBSH	16.3	-	-	ns
TDMI Hold Time	tSDH	10	-	-	ns
TDMI Setup Time	tSDS	10	-	-	ns
Audio Interface Timing (Master mode)					
Stereo mode (TDM1/0 bit = "00")					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–20	-	20	ns
BICK "↓" to SDTO	tBSD	–20	-	20	ns
TDM256 mode (TDM1/0 bit = "01")					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-20		20	ns
SDTO Setup time BICK "↑"	tBSS	16.3	-	-	ns
SDTO Hold time BICK "↑"	tBSH	16.3	-	-	ns
TDMI Hold Time	tSDH	10	-	-	ns
TDMI Setup Time	tSDS	10	-	-	ns

Note 18. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (4-wire serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
CCLK Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	50	-	-	ns
CDTI Hold Time	tCDH	50	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
CDTO Delay	tDCD	-	-	45	ns
CSN "↑" to CDTO Hi-Z	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU :STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 19)	tHD :DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU :DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP :I^2C	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 20)	tPD	150	-	-	ns
PDN "↑" to SDTO valid (FS1/0bit="00") (Note 21)	tPDV	-	3153	-	1/fs
PDN "↑" to SDTO valid (FS1/0bit="01") (Note 21)		-	2098	-	1/fs
PDN "↑" to SDTO valid (FS1/0bit="10") (Note 21)		-	1729	-	1/fs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP :PD	0	-	20	ns

Note 19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 20. The AK5730 can be reset by setting the PDN pin to "L" upon power-up.
Note 21. These cycles are the numbers of LRCK rising edges from the PDN pin rising.
Note 22. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

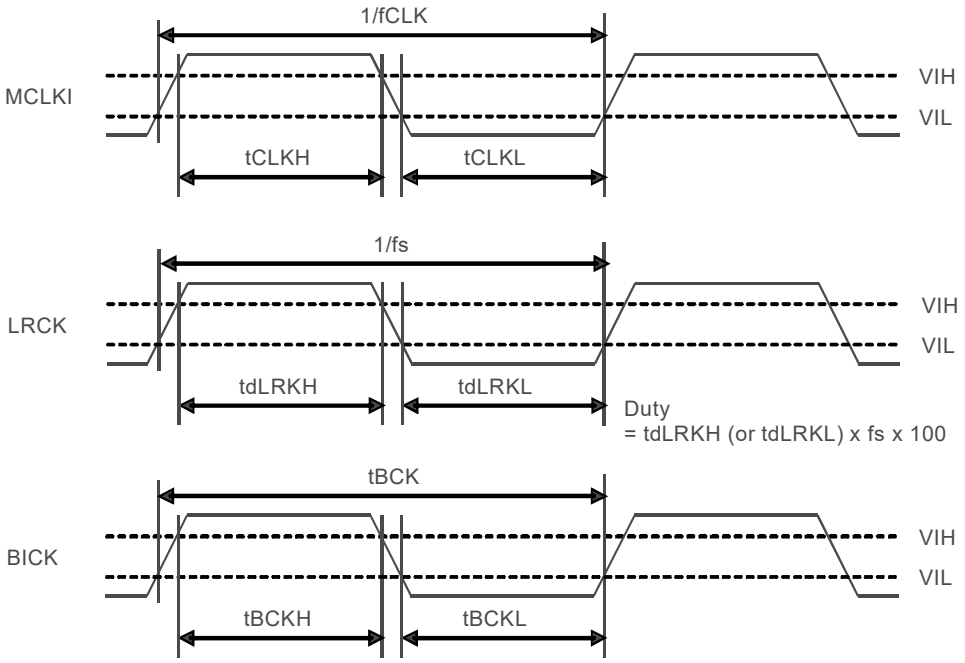


Figure 2. Clock Timing (TDM1/0 bits = "00" & Slave mode)

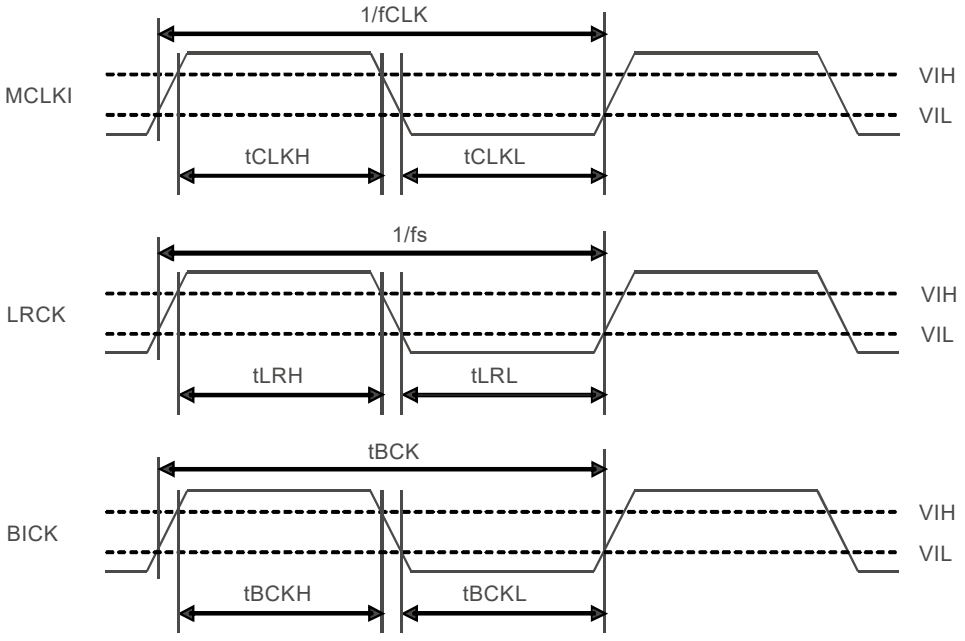


Figure 3. Clock Timing (Except TDM1/0 bits = "00" & Slave mode)

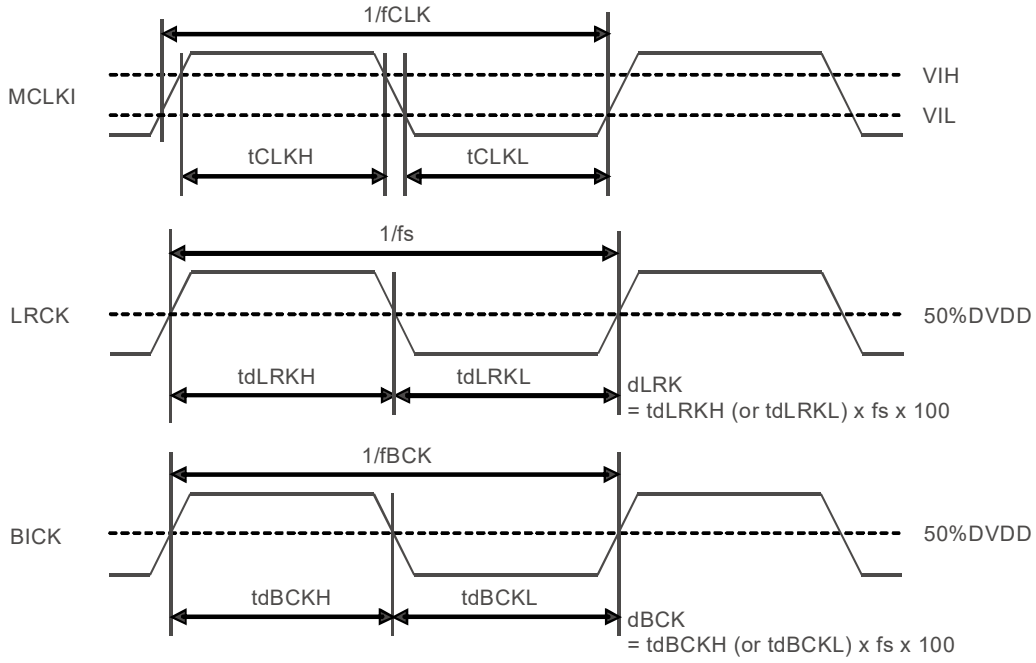


Figure 4. Clock Timing (TDM1/0 bits = "00" & Master mode)

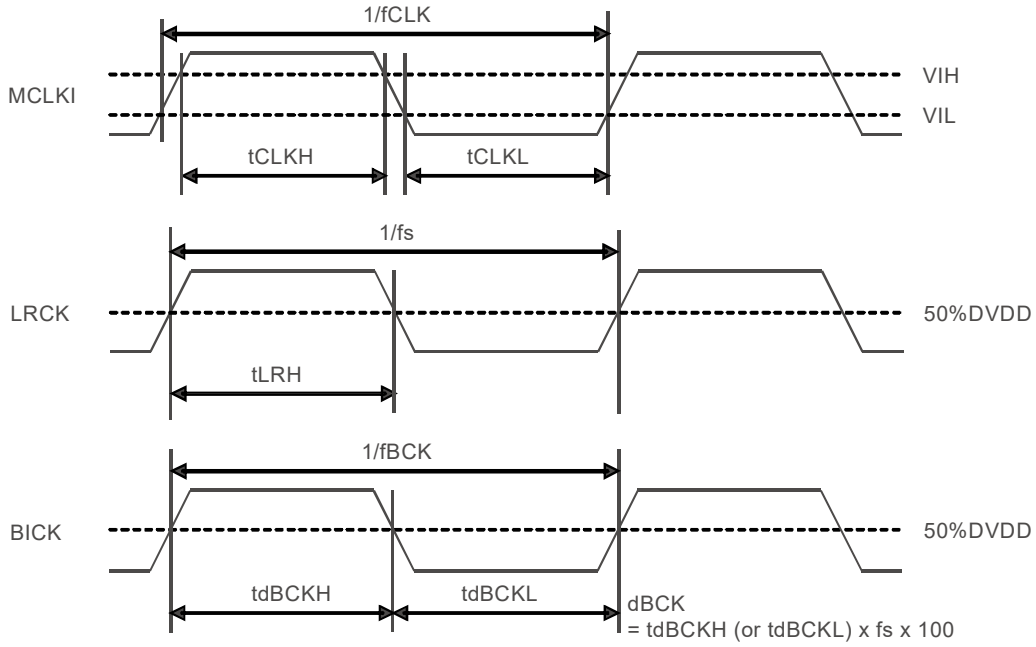


Figure 5. Clock Timing (Except TDM1/0 bits = "00" & Master mode)

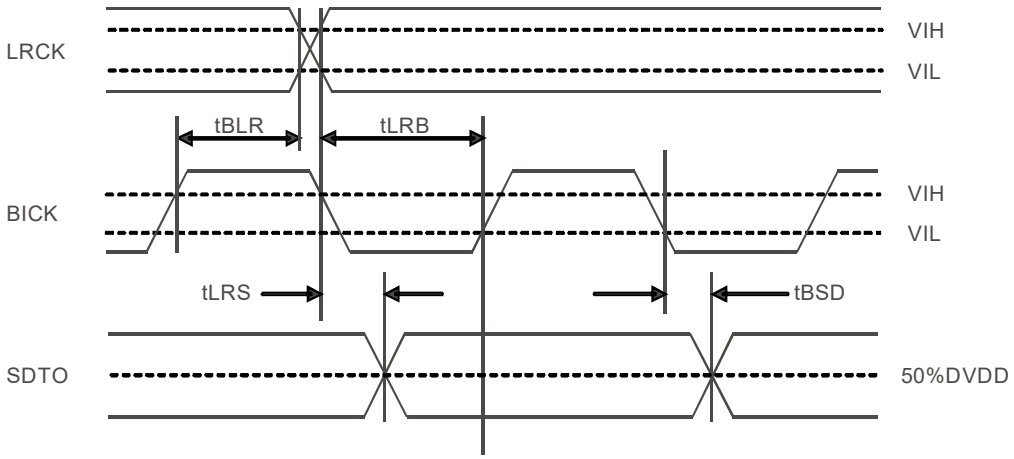


Figure 6. Audio Interface Timing (TDM1/0 bits = "00" & Slave mode)

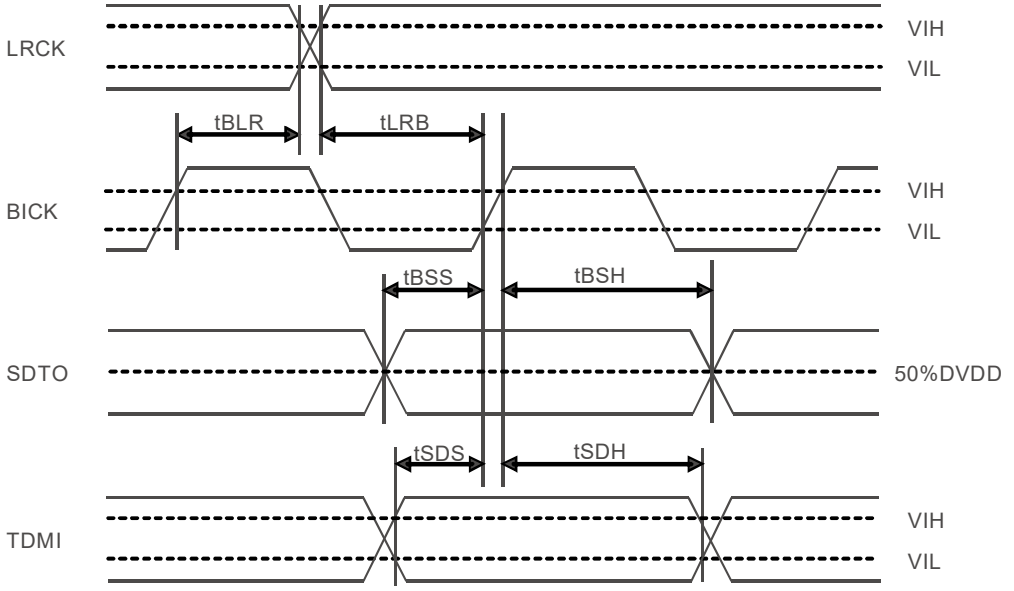


Figure 7. Audio Interface Timing (Except TDM1/0 bits = "00" & Slave mode)

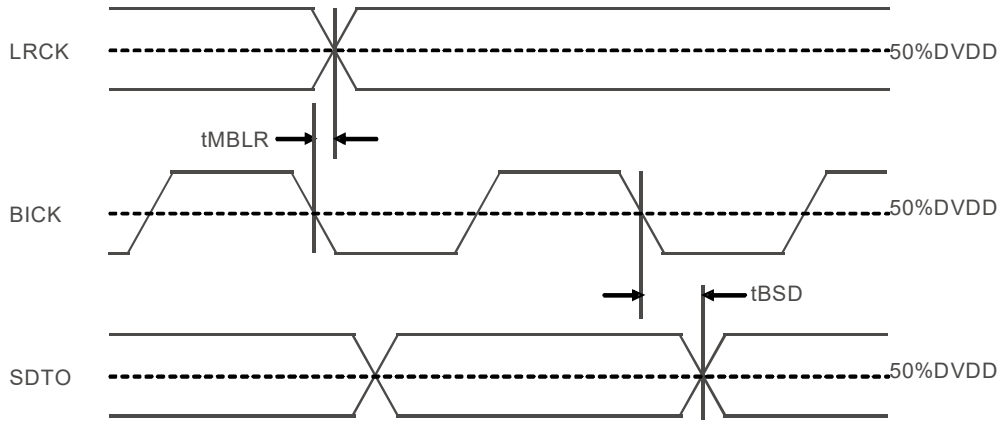


Figure 8. Audio Interface Timing (TDM1/0 bits = "00" & Master mode)

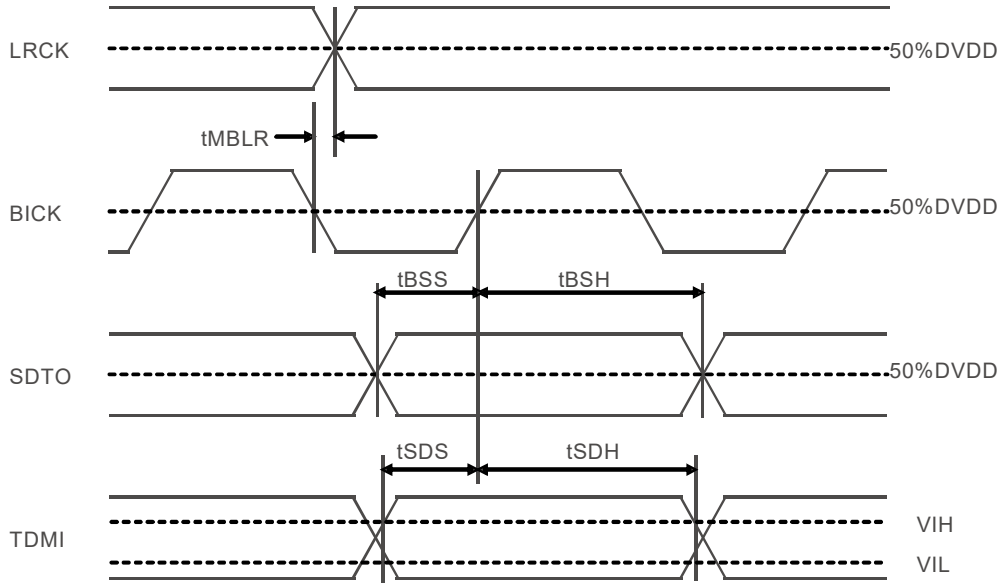


Figure 9. Audio Interface Timing (Except TDM1/0 bits = "00" & Master mode)

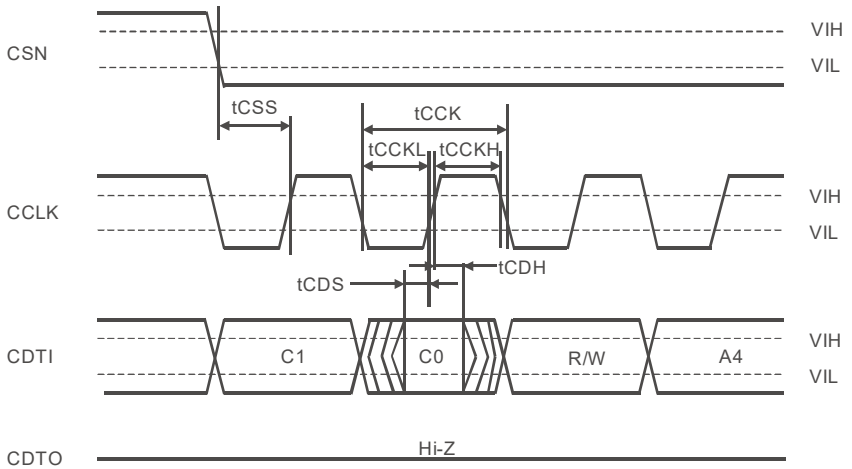


Figure 10. WRITE/READ command input timing (4-wire serial mode)

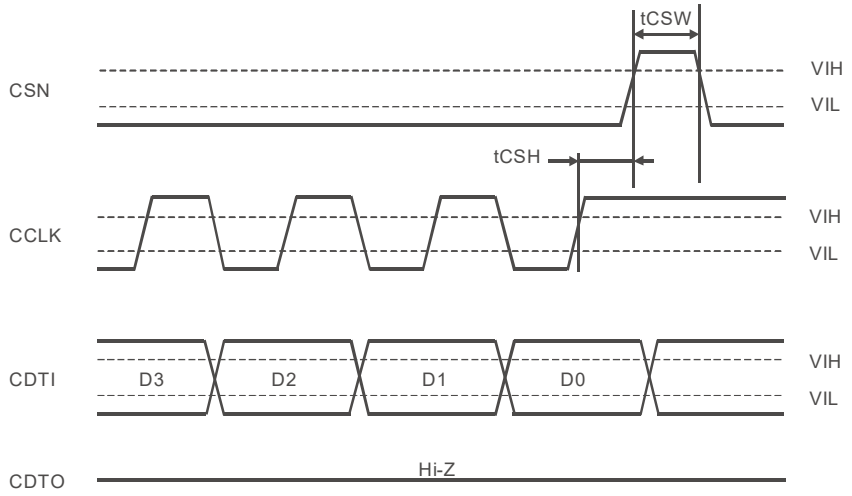


Figure 11. WRITE data input timing (4-wire serial mode)

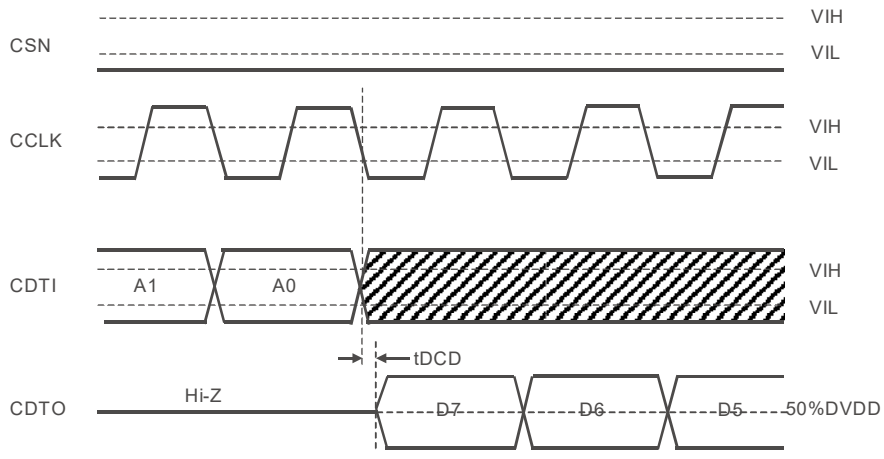


Figure 12. READ data output timing 1 (4-wire serial mode)

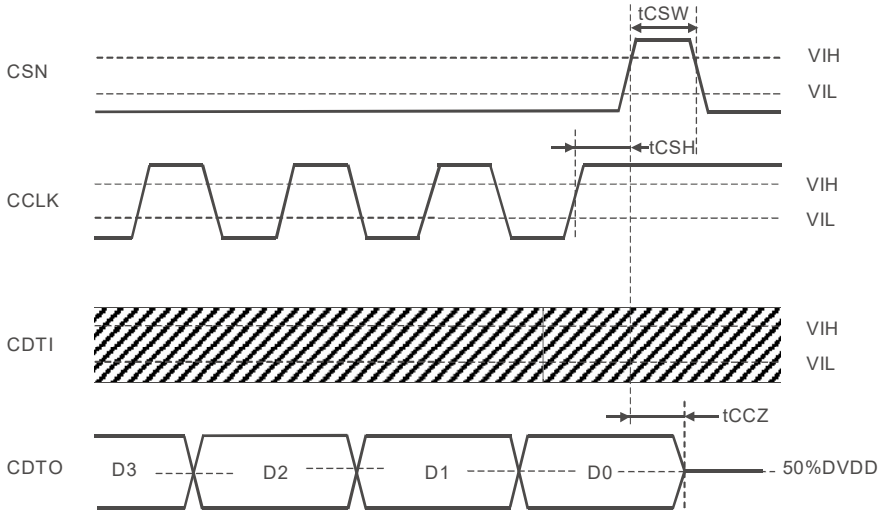


Figure 13. READ data output timing 2 (4-wire serial mode)

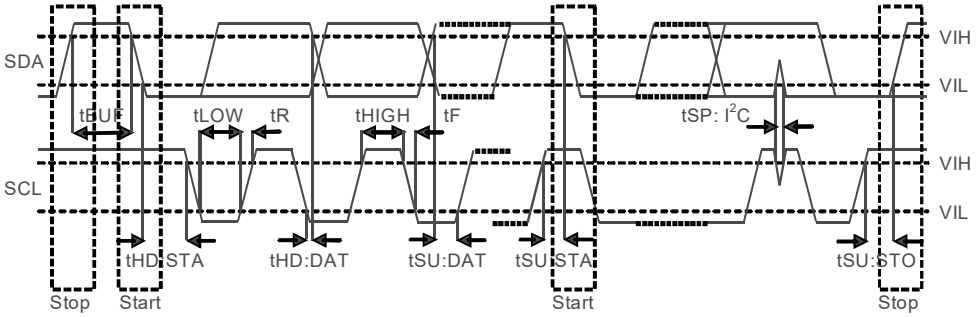


Figure 14. I^2C Bus Timing

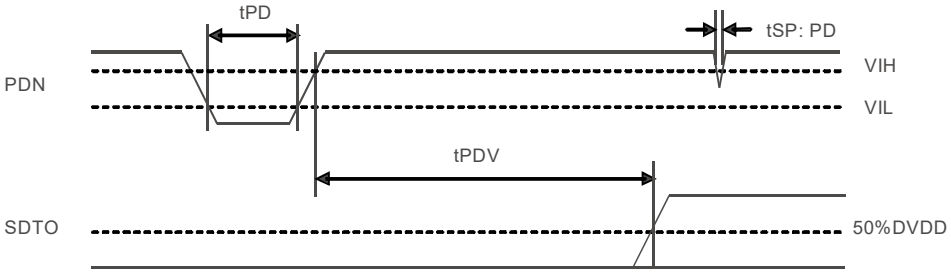


Figure 15. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The MSN pin selects either master or slave mode. MSN pin = "H" selects master mode and "L" selects slave mode.

In slave mode, required clocks depend on use of the internal PLL (PLL1-0 bits).

(1) Not using PLL
MCLK, BICK and LRCK (fs) are required. MCLKI should be synchronized with LRCK but the phase is not critical. After exiting reset at power-up in slave mode, the AK5730 is in power-down mode until MCLK, LRCK and BICK are input.

(2) Using PLL
BICK and LRCK are required. After exiting reset at power-up in master mode, the AK5730 is in power-down mode until MCLKI are input.

Table 1 shows the relationship between the sampling rate and the frequencies of MCLK and BICK. The sampling speed is set by FS0 and FS1 bits (Table 3).

In master mode, only MCLKI is required. Master Clock Input Frequency should be set with the CKS1-0 bits (Table 2), and the sampling speed should be set by the FS1-0 bits. After exiting reset at power-up in master mode, the AK5730 is in power-down mode until MCLKI are input. In TDM256 mode, the master clock should be 256fs.

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
8kHz	2.048	3.072	4.096	0.512
32kHz	8.192	12.288	16.384	2.048
44.1kHz	11.2896	16.9344	22.5792	2.8224
48kHz	12.288	18.432	24.576	3.072

Table 1. System Clock Example

CKS1 bit	CKS0 bit	Clock Speed	
0	0	256fs	
0	1	384fs	
1	0	512fs	(default)
1	1	(reserved)	

Table 2. Master Clock Control (Master Mode)

FS1 bit	FS0 bit	Sampling Rate	
0	0	24kHz – 48kHz	(default)
0	1	12kHz – 24kHz	
1	0	8kHz – 12kHz	
1	1	8kHz – 12kHz (reserved)	

Table 3. Sampling Rate (fs)

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the MSN pin. (“H”=Master Mode, “L”=Slave Mode)
In master mode (MSN pin= “H”), LRCK pin and BICK pin are output pins.
In slave mode (MSN pin= “L”), LRCK pin and BICK pins are input pins

PLL1-0 bits control the PLL modes which generates the internal MCLK from BICK.

PDN	MSN pin	PLL1 bit	PLL0 bit	LRCK pin	BICK pin
L	L	*	*	Input	Input
L	H	*	*	“L” Output	“L” Output
H	L	0	0	Input	Input (PLL off)
H	L	0	1	Input	64fs Input (PLL mode)
H	L	1	0	Input	256fs Input (PLL mode)
H	L	1	1	Input	512fs Input (PLL mode)
H	H	*	*	Output	Output

(*: Don’t Care)

Table 4. LRCK and BICK pins

■ Digital High Pass Filter (HPF)

The ADC has digital high pass filters for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and scales with the sampling rate (fs).

HPFs are controlled by the HPE4-1 bits.

HPE1 bit	HPF	
L	ADC1 HPF off	
H	ADC1 HPF on	(default)

HPE2 bit	HPF	
L	ADC2 HPF off	
H	ADC2 HPF on	(default)

HPE3 bit	HPF	
L	ADC3 HPF off	
H	ADC3 HPF on	(default)

HPE4 bit	HPF	
L	ADC4 HPF off	
H	ADC4 HPF on	(default)

Table 5. HPF Operation Setting

■ Audio Serial Interface Format

Four types of the date formats are available and selected by setting the DIF bit and the TDM1-0 bits. In all modes, the serial data is MSB first, 2`s complement format. LRCK and BICK are output in master mode, input in slave mode.
In slave mode, the MCLKI clock frequency is allowed 256fs and 512fs. In master mode, the MCLKI clock frequency should be 256fs.

Mode	DIF bit	TDM1 bit	TDM0 bit	BICK	Data Format	
0	0	0	0	64fs	Stereo Mode (I^2S)	(default)
1	0	0	1	256fs	TDM256 Mode(I^2S)	
-	0	1	0	-	(Reserved)	
-	0	1	1	-	(Reserved)	
3	1	0	0	64fs	Stereo Mode (Left Justified)	
4	1	0	1	256fs	TDM256 Mode (Left Justified)	
-	1	1	0	-	(Reserved)	
-	1	1	1	-	(Reserved)	

Table 6. TDM Mode Setting

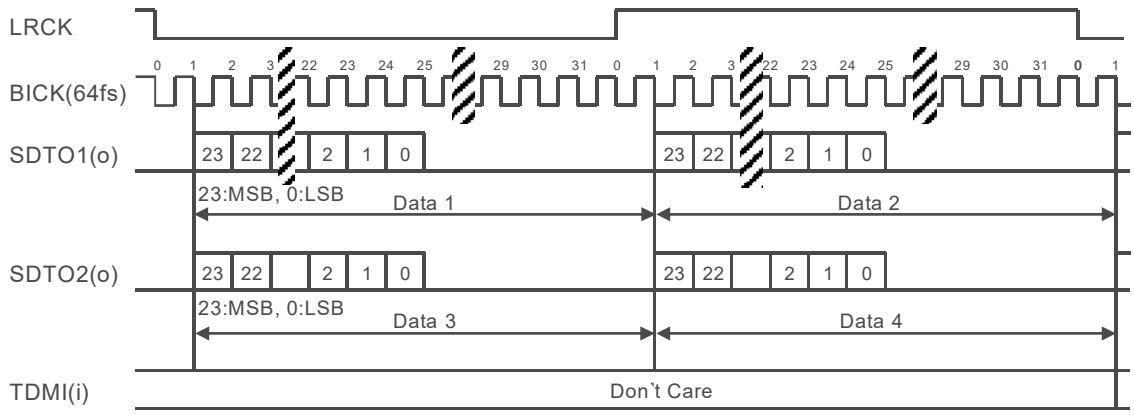


Figure 16. Mode 0 Timing (Stereo Mode (I^2S))

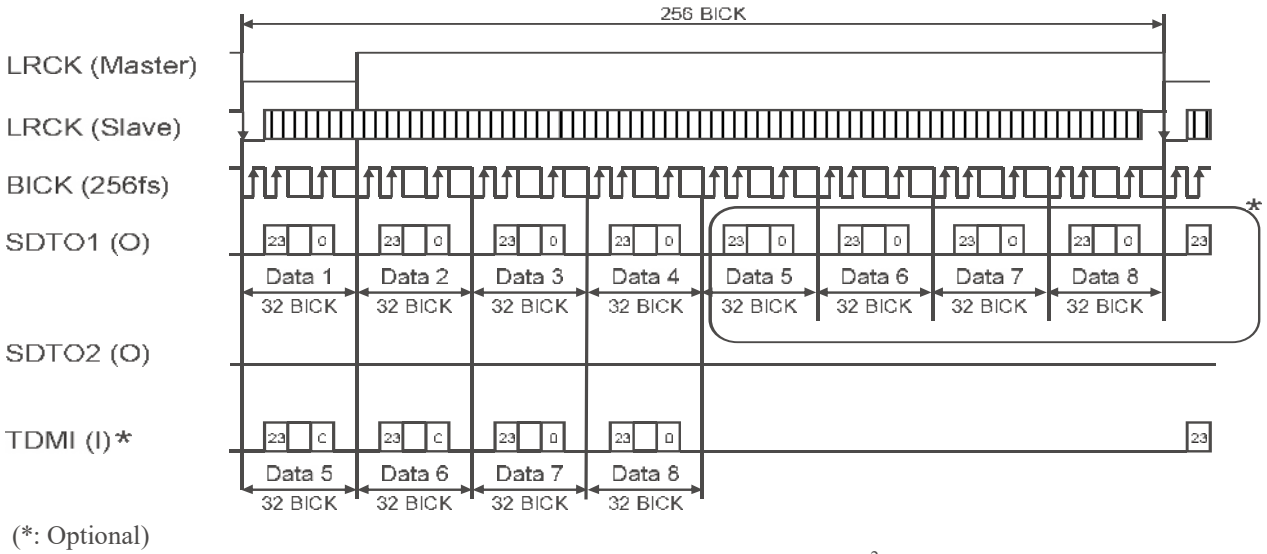


Figure 17. Mode1 Timing (TDM256 Mode (I^2S))

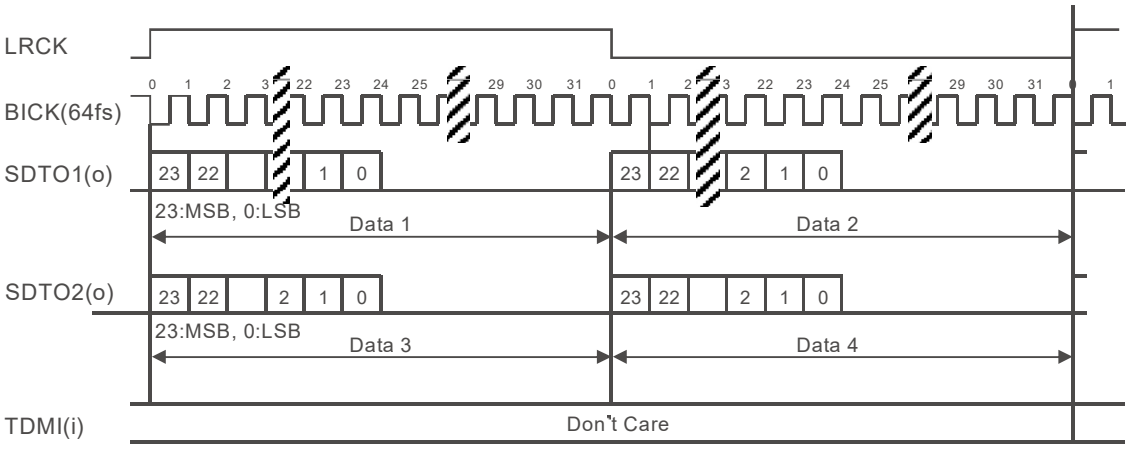


Figure 18. Mode3 Timing (Stereo Mode (Left Justified))

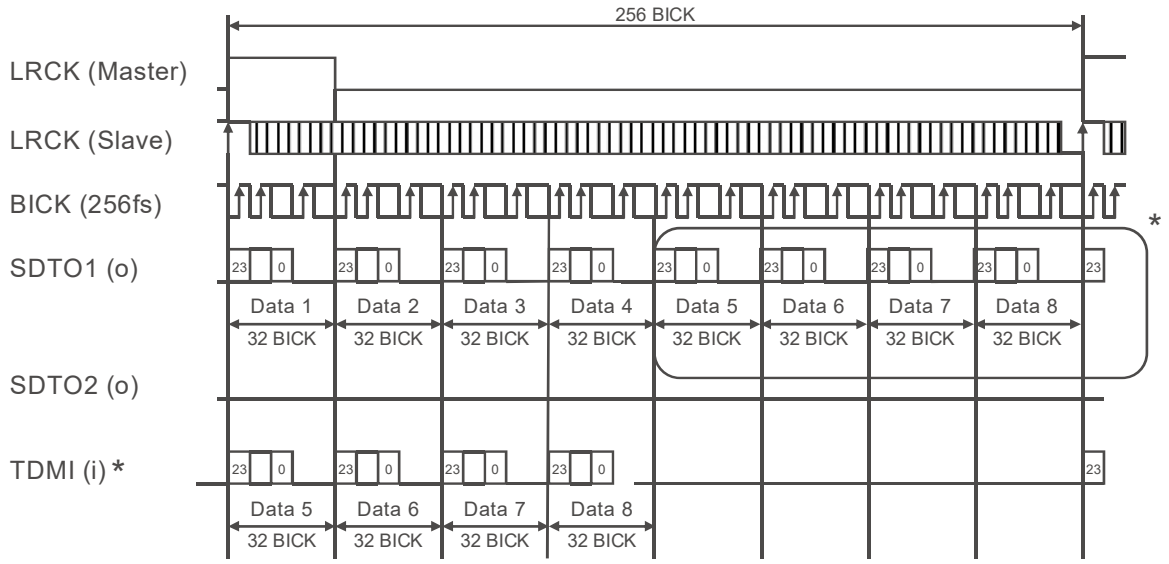
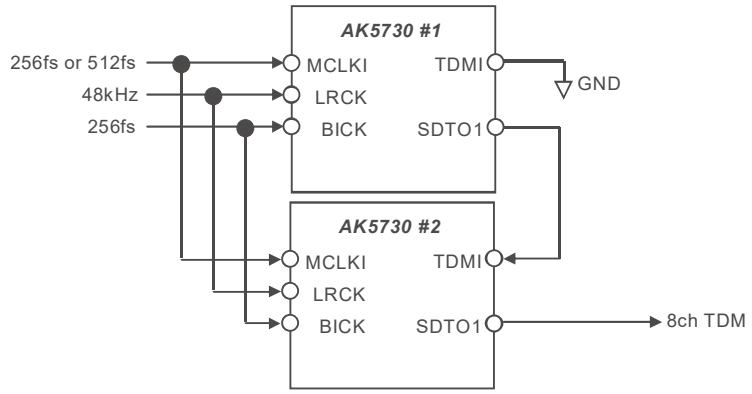


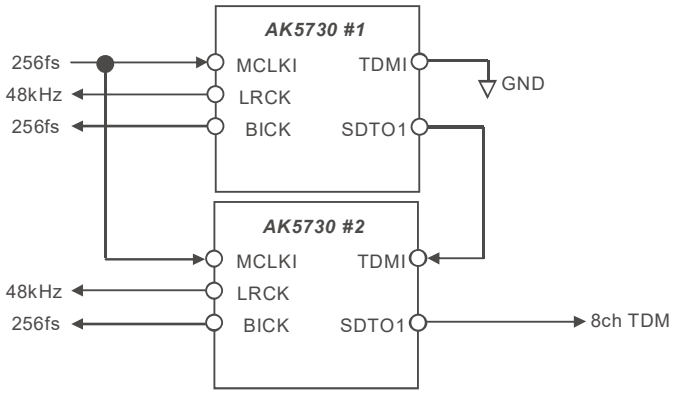
Figure 19. Mode4 Timing (TDM256 Mode (Left Justified))

■ TDM Cascade Mode

TDM256 mode
Two devices can be connected in cascades at the TDM256 mode. In Figure 20, the SDTO1 pin of device #1 is connected with the TDMI pin of device #2. It is possible to output 8channel TDM data from the SDTO1 pin of device # 2 as shown in Figure 17 and Figure 19.



(1) Slave Mode



(2) Master Mode

Figure 20. Cascade TDM Connection Diagram (TDM256 mode)

■ System Reset

The AK5730 should be reset once by bringing the PDN pin = "L" upon power-up. The AK5730 is powered up and the internal timing starts clocking by LRCK "↑" after exiting the power down state of reference voltage (such as VREF) by MCLKI. In slave mode, the AK5730 is in power-down mode until MCLK, BICK and LRCK are input. In master mode, the AK5730 is in power-down mode until MCLKI is input. Following all clock inputs, set RSTN bit to "1" after setting microphone bias voltage (MBS3-0 bits).

■ Digital Attenuator

The AK5730 has a channel-independent digital attenuator (256 levels, 0.5dB step). Attenuation level of each channel can be set by each the ATT7-0 bits (Table 7).

ATT7-0	Attenuation Level
00H	+12dB
01H	+11.5dB
:	:
18H	0dB(default)
19H	-0.5dB
1AH	-1.0dB
	:
FEH	-115.0dB
FFH	MUTE (-∞)

Table 7. Attenuation level of digital attenuator

Transition time between set values of ATT7-0 bits can be selected by ATS1-0 bits (Table 8). Transition between set values is the soft transition eliminating a switching noise in the transition.

Mode	ATS1	ATS0	ATT speed	
0	0	0	3712/fs	(default)
1	0	1	928/fs	
2	1	0	1856/fs	
3	1	1	7424/fs	

Table 8. Transition Time between Set Values of ATT7-0 bits

The transition between set values is a soft transition of 3712 levels in mode 0. It takes 3712/fs (77.3ms@fs=48kHz) from 00H(+12dB) to FFH(MUTE). If the PDN pin goes to "L", the ATTs are initialized to18H. The ATTs also become 18H when RSTN bit = "0", and fade to their current value when RSTN bit returns to "1".

■ Analog Input Mode

The AK5730 has 4 Analog Input modes. Analog Input mode is controlled by LIN*1-0 bits. The input mode is fixed by each set. The AC signal is input from IN*P/N, and the DC signal is input from INM*P/N. Except for Microphone Input mode, the input voltage of IN*P/N(=1.65Vrms (Typ.), Differential) should be adjusted with external resistors. As for the accuracy of external resistance, 0.1% is required for CMRR.

The input voltage of INM*P/N(=AVDD) should be adjusted with external resistors. Fault conditions are calculated digitally, so the value of external resistance is fixed to 7:3. The input voltage of INM*P/N becomes 30% of VDC+/-. As for the accuracy of external resistance, 0.1% is required for the accuracy of SAR.
The full scale of SAR is normalized to 11V (@AVDD=3.3V) for calculations of Fault Condition detection.

(A) Microphone Input Mode (LIN*1-0 bits = "00")
The microphones are connected in a fully balanced manner. A separate cable shield for each microphone may be connected to chassis ground. In this use case, a gain correction of 9.5dB by GAIN* bit = "1" is available.

Parameter	Specification	Remarks
Mic Impedance	1 - 2kΩ, 10kΩ(max)	
Mic Audio Output	10...100mVrms, 1.75Vrms(max)	
Interchannel Isolation(max) of Microphone inputs	70dB	
Mic Phantom Voltage(Vbias)	5V - 9V	depending on type of microphone
Mic Supply Current	0.1 - 10mA	per microphone depending on type of microphone
Resistors (symmetrical)	200 - 10k	

Table 9. Specification(Microphone Input mode)

The maximum interchannel isolation of microphone inputs is 70dB.The isolation depends on MPWR common impedance. In Figure 21, the microphone impedance and the microphone bias resistance is 2kΩ and MPWR voltage is 8.0V. At this time, MPWR common impedance should be 0.2Ω or less.

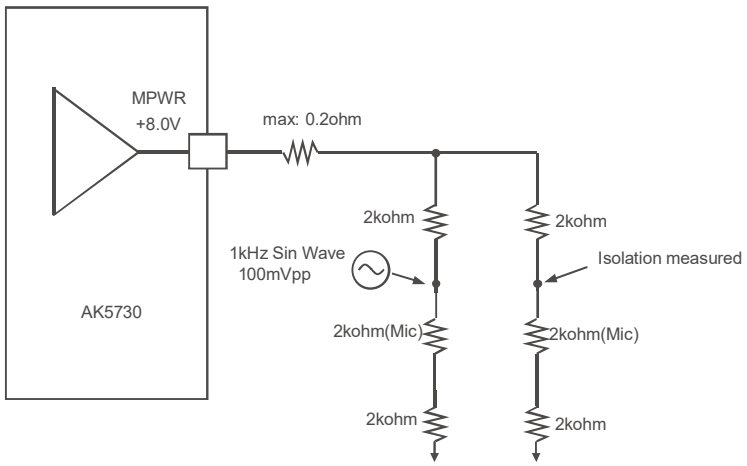


Figure 21. Interchannel Isolation of Microphone Inputs

Different types of microphones can be connected at the same time, with the same phantom voltage.

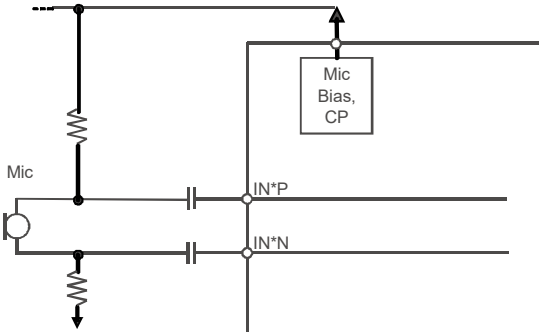


Figure 22. Microphone Input Mode(IN*P/N pins)

For Fault Conditions, refer to Table 10 and Figure 23.

Fault Conditions	Conditions
Positive/Negative input shorted to VBAT	VDC+/- ≥Vbias + Vth
Positive/Negative input shorted to GND	VDC+/- ≤ Vth
Pos. and neg. inputs shorted	|VDC+ - VDC-| ≤ Vth
Positive input open	Vbias - Vth ≤ VDC+ ≤ Vbias + Vth
Negative input open	VDC+/- ≤ Vth

Note 23. It is not possible to distinguish "Positive/Negative input shorted to GND" and "Negative input open".
Vth: Error Monitor Threshold Voltage. Vth is set by Table 18.

Table 10. Fault Conditions (Microphone Input Mode)

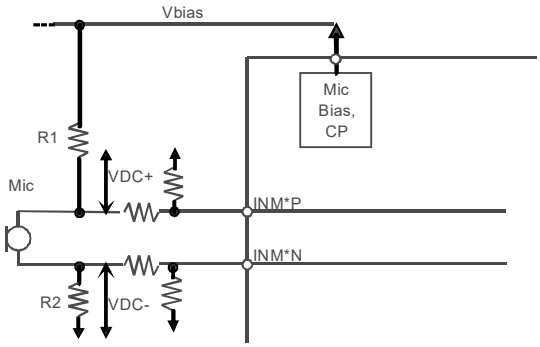


Figure 23. Microphone Input Mode (IN*MP/N pins)

(B) LINE and Phone Input Mode (LIN*1-0 bits = "01")

The stereo line input is a quasi-differential input. Line return, phone return and head unit ground may be isolated from each other. Also combinations of two stereo line inputs, one stereo line and one stereo phone inputs are possible.

Parameter	Specification	Remarks
Stereo Line Input Voltage	1 - 3V RMS	(depending on customer)
Phone Input Voltage	0.1 - 3V RMS	(depending on customer)

Table 11 Specification (LINE and Phone Input mode)

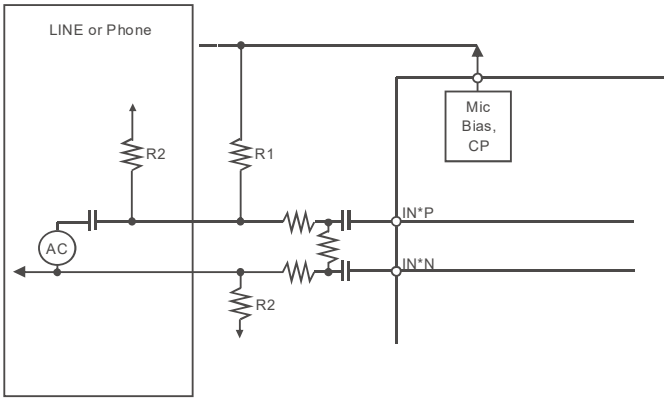


Figure 24. LINE and Phone Input Mode(IN*P/N pins)

For Fault Conditions, refer to Table 12 and Figure 25. The "Pos. and neg. inputs shorted State (R2/(2R1+R2)) * Vbias" is detected based on SAR Threshold A(THA12-01 bits).
The threshold A is a 12bit straight binary code which the full scale is 11V.

Fault Conditions	Conditions
Positive/Negative input short to VBAT	VDC+/- ≥ Vbias + Vth
Positive/Negative input short to GND	VDC+/- ≤ Vth
Pos. and neg. inputs short	R2/(2R1+R2) * Vbias –Vth ≤ VDC+ ≈ VDC- ≤ R2/(2R1+R2) * Vbias + Vth
Positive input open	Vbias - Vth ≤ VDC+ ≤ Vbias + Vth
Negative input open	VDC+/- ≤ Vth

Note 23. It is not possible to distinguish "Positive/Negative input shorted to GND" and "Negative input open".
Note 24. The "Pos. and neg. inputs short" is a condition that occurs when there is no input signal, and DC voltage is not supplied by the input signal.

Table 12. Fault Conditions (LINE and Phone Input Mode)

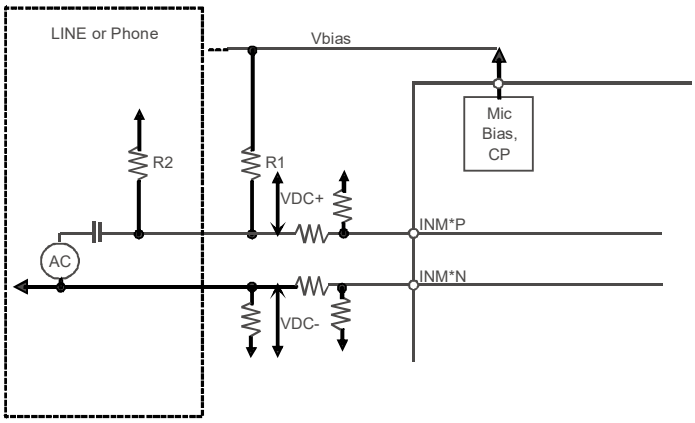


Figure 25. LINE and Phone Input Mode (IN*MP/N pins)

(C) Booster Input Mode (LIN*1-0 bits = "10")
The booster inputs are directly driven by a standard automotive power amp, either by a class AB, a class SB (I) or even by a class D amplifier. The connection is made in a fully balanced manner. In case of using a class SB (I) amplifier, the input voltage may contain common mode signal inside the audio bandwidth due to switching from bridge to single ended mode and vice versa. Booster inputs may share a Quad-ADC with any other input type (line, phone and microphone).

Parameter	Specification	Remarks
Input voltage typ.	10.0V RMS	@ battery voltage <14.4V
Input voltage max.	11.7V RMS	@ battery voltage =16.5V

Table 13 Specification (Booster Input mode)

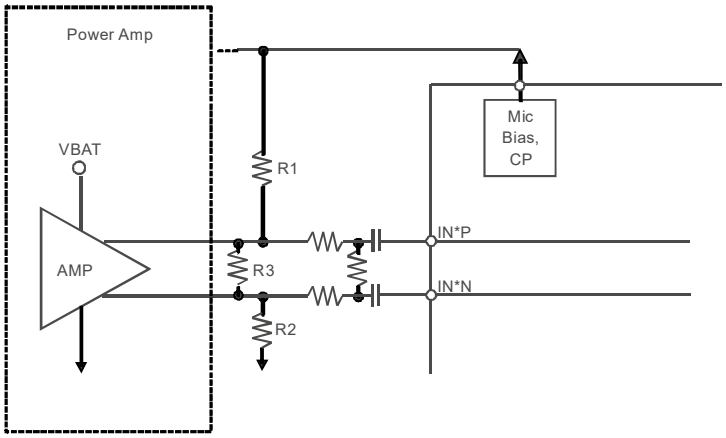


Figure 26. Booster Input mode (IN*P/N pins)

Diagnostic functions are performed by the external amplifier. A simple check can be made, whether the input is connected or not. Input is connected to amp output: VDC+ = VDC- = VBAT / 2. Refer to Note 25 and Figure 27 about Fault Conditions. The "Input open State ((R2+R3)/(R1+R2+R3) * Vbias) and (R2/(R1+R2+R3) * Vbias)" are detected based on SAR threshold B and C (THB12-01 bits, THC12-01 bits). The threshold B and C are 12bit straight binary codes, which the full scale is 11V (Typ.).

Fault Conditions	Conditions
Positive input open	(R2+R3)/(R1+R2+R3) * Vbias –Vth ≤ VDC+ ≤ (R2+R3)/(R1+R2+R3) * Vbias +Vth
Negative input open	R2/(R1+R2+R3) * Vbias – Vth ≤ VDC- ≤ R2/(R1+R2+R3) * Vbias + Vth

Note 25. Positive/Negative input open conditions are statuses when there is no input signal and DC voltage is not supplied by the input signal.

Table 14 Fault Conditions (Booster Input mode)

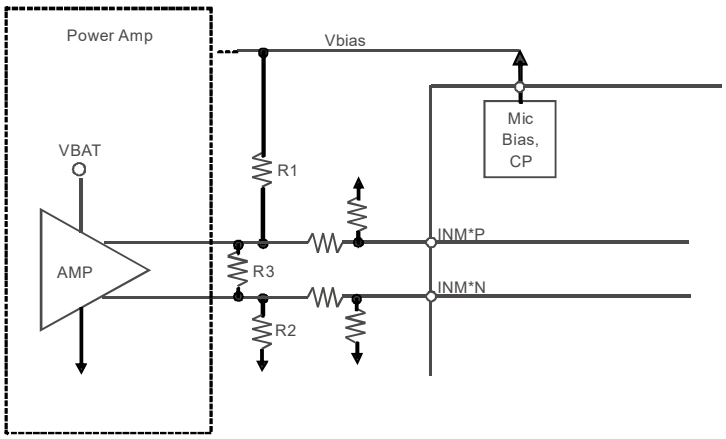


Figure 27. Booster Input Mode (INM*P/N pins)

(D) Internal Unbalanced Source Mode (LIN*1-0 bits = "11")
Max. unbalanced input voltage < 2V RMS
In this mode, No diagnosis is performed for internal connections.

■ VBATM pin

The input voltage of the VBATM pin should be adjusted with external resistors as below.
The input voltage range is 0 to AVDD. When the input is AVDD voltage (=3.3V typ.), the SAR outputs Full-scale data(typ.)

ex.) AVDD=3.3V
R1=2 MΩ, R2=360kΩ

When Battery voltage is 21.6V, the voltage at VBATM pin becomes 3.3V and the SAR outputs Full-scale data.
Battery = 21.6V → Full-scale

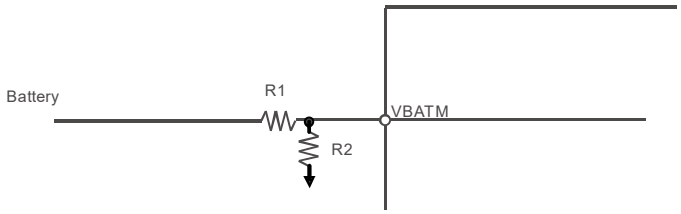


Figure 28. VBATM pin

■ Error Detection

The following seven events cause the INT pin to show the status of the fault condition. When the PDN pin is "L", the INT pin goes to "Hi-z".

1. OPEN: Open circuit
2. SHTD: Short between the positive and negative microphone input
3. SHTG: Short to ground
4. SHTV: Short to VBAT
5. OVCR1: Mic Bias Over-current(90mA(typ)) of booster
6. OVCR2: Charge Pump Over-current(600mA(typ)) of booster
7. OVTP: Over-temp(165 degrees(typ)) of booster

The INT pin outputs an ORed signal based on the above seven interrupt events. When error information is masked, the interrupt event does not affect the operation of the INT pin. This pin should be connected to DVDD (typ. 3.3V) or lower voltage via a 10kΩ resistor.

Once the INT pin goes to "L", it remains "L" until writing INTR bit = "1". After writing "1" to INTR bit, it automatically returns to "0".

OPEN, SHTD, SHTG, SHTV, OVCR and OVTP bits in Address 07-0BH indicate the interrupt status events above in real time. Once they go to "1", it stays "1" until writing INTR bit = "1".

When MSHTV*, MSHTG*, MSHTD*, MOPEN* (*: 1-4) bits (Address=0C-0FH) go to "1", error information at SHTV*, SHTG*, SHTD*, OPEN* bits can not be masked but does not affect the operation of the INT pin. (Table 16)

When over-temperature (OVTP) or over-current (OVCR1, OVCR2) is detected, the AK5730 disables the block listed on Table 15. Unless the error is due to over-temperature or over-current, error detection is restarted by writing INTR bit = "1". When the error is due to over-temperature or over-current, restart the AK5730 by the PDN pin or RSTN bit.

INT detection	CPUIF	PLL	CP	MIC Bias	ADC	SAR ADC	MIC Diags
SAR ERR	A	A	A	A	A	A	A
TSD Overtemp.	A	A	L	A	-	A	A
MIC overcurrent +	A	A	L	A	-	A	A
MIC overcurrent -	A	A	-	-	-	-	-
CP overcurrent	A	A	L	A	-	-	-

A: Active Block, L: Active in Low Power Mode, ×: Power Down

Table 15. Block Conditions on Error Detection

Unmasked Event	Masked Event	INT pin
Not detected	Not detected	Hi-Z
	DETECTED	
DETECTED		L (goes "Hi-Z" after writing INTR bit = "1")

Table 16. Error Handling in Serial Control Mode

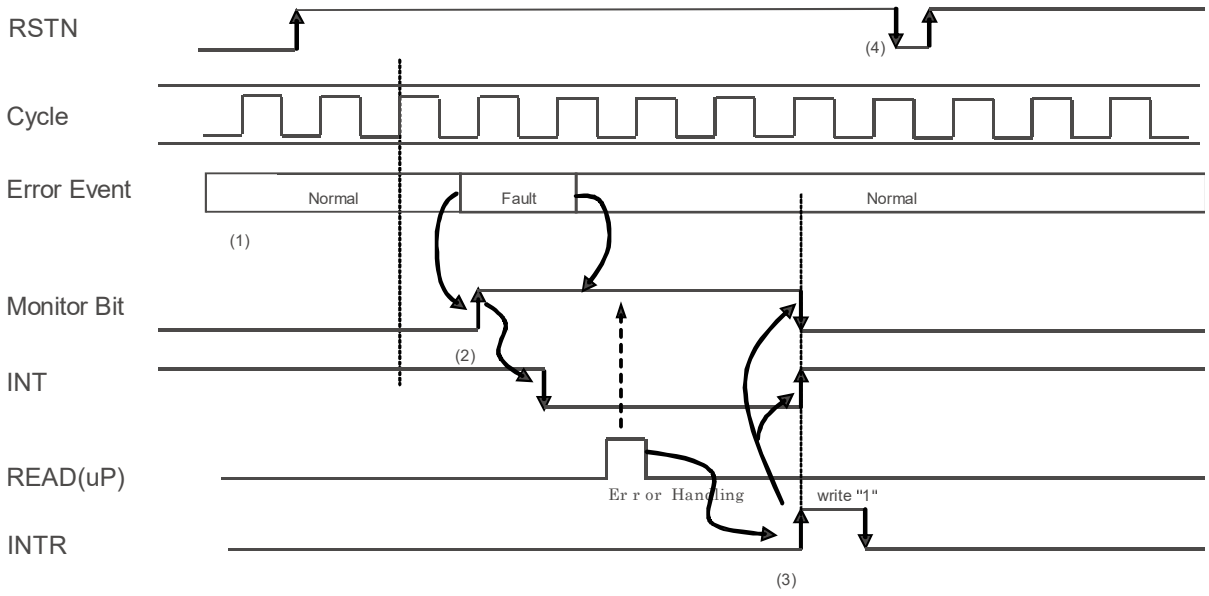


Figure 29. Error Detection Timing

Notes:

(1) Execute error detection from 1ch to 8ch (IN1P~IN4P, IN1N~IN4N pins) in this order.

(2) After the error detection from 1ch to 8ch, the error detection results are ORed and reflected to INT pins. Indication of INT pins can be masked by MSHTV*, MSHTG*, MSHTD*, MOPEN* (*: 1-4) bits (Address= 0C-0FH).

(3) Error monitor registers are reset by setting INTR bit to "1" after all error conditions are removed.

(4) When the detected error is due to over-temperature or over-current, restart the AK5730 by the PDN pin or RSTN bit.

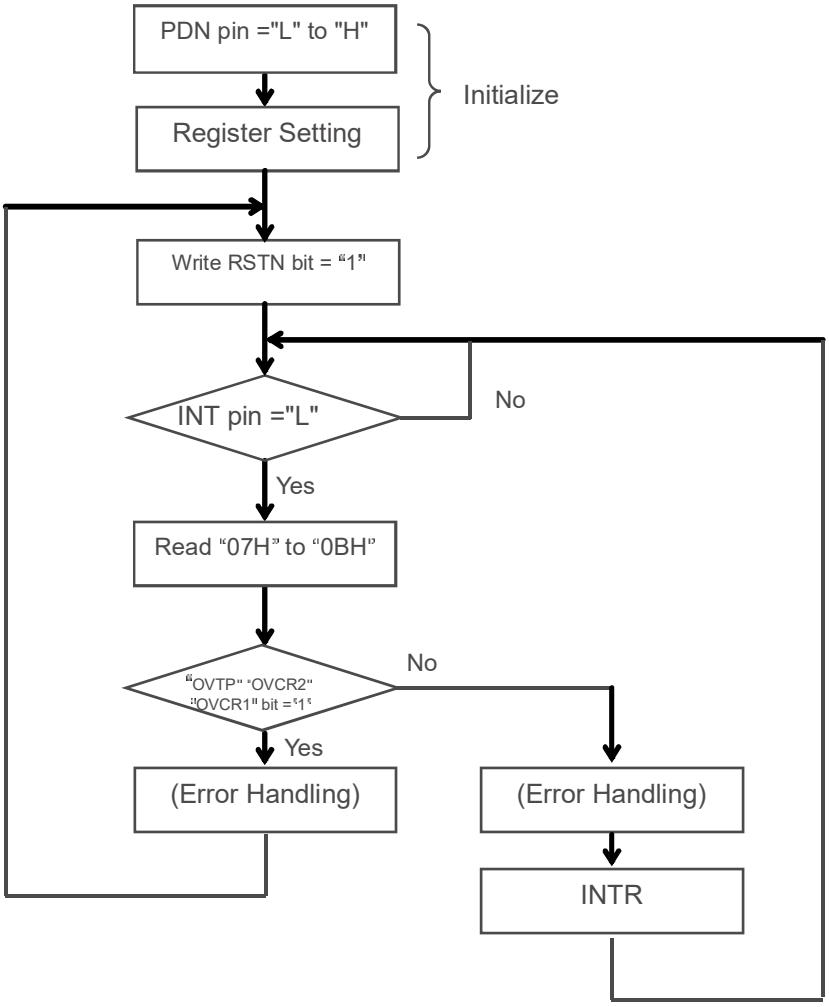


Figure 30. Error Handling Sequence Example

■ Power Up/Down Sequence

The each block of the AK5730 is placed in power-down mode by bringing the PDN pin to "L" and both digital filters are reset at the same time. The PDN pin ="L" also resets the control registers to their default values. In power-down mode, the SDTO pin goes to "L". This reset must always be executed after power-up.

In slave mode, after exiting reset at power-up and etc., the ADC starts operation from the rising edge of LRCK after MCLKI inputs. The AK5730 is in power-down mode until MCLK and LRCK and BICK are input.

The analog initialization cycle of ADC starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 1041/fs cycles of LRCK clock. Figure 31 shows the sequences of the power-down and the power-up.

When RSTN bit = "0", all circuits are powered-down but the internal register are not initialized.

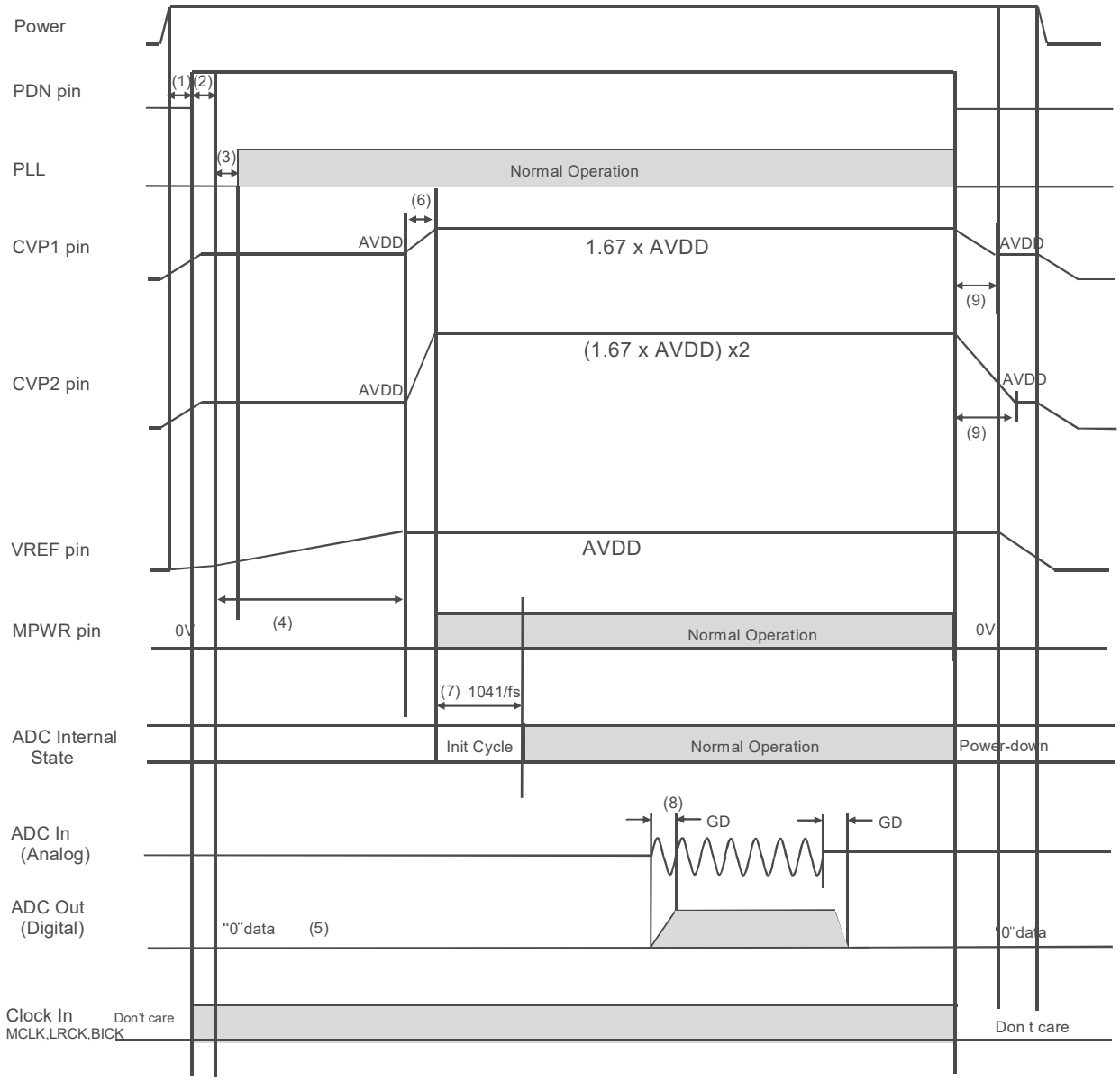


Figure 31 Power-up/down Sequence Example

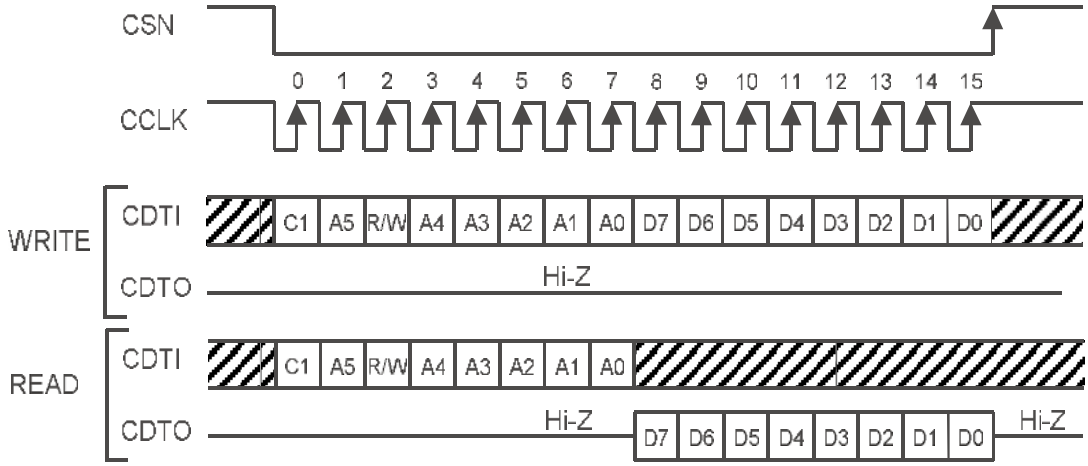
Notes:

(1) Power-up the AK5730 during the PDN pin = "L". The PDN pin should be set to "H" after all powers (DVDD, AVDD) are supplied. The AK5730 requires 150ns or longer "L" period for a certain reset.
(2) Set RSTN bit to "1" after setting microphone bias voltage (MBS3-0 bits).
(3) Power-on the PLL circuit:(PLL mode)
PLL1-0 bits = "01" or "10" or "11", & BICK is input.
PLL is locked within 1 - 2ms
(4) Power-on the Vref circuit:
The CVP1 pin and CVP2 pin are charged up.
The VREF pin becomes AVDD within about 20 - 40ms.
(5) ADC outputs "0" data in power-down state.
(6) Power-on the charge pump circuit1/2:
(Normal mode) PDN pin = "L" → "H"(or PLL is locked) & MCLKI, BICK, LRCK is input.(normal mode)
(PLL mode) PLL is locked.
The CVP1 pin becomes 1.67 x AVDD within about 4 - 8ms.
The CVP2 pin becomes (1.67 x AVDD) x 2 within about 4 - 8ms.
(7) The analog block of ADC is initialized after exiting the power-down state.
(8) Digital outputs corresponding to analog inputs-has group delay (GD).
(9) Charge pump circuit power down:
PDN pin = "H" → "L"
The CVP1/2 pin becomes AVDD according to a flying capacitor and internal resistor. The internal resistor is 50kΩ (typ). Therefore, when the CVP1/2 pin has a flying capacitor of 2.2μF, the time constant is 110ms (typ).

■ Serial Control Interface

(1) 4-wire Serial Control Mode (SPI pin = "H")

The internal registers may be either written or read by the 4-wire µP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (1bit, C1 is fixed to "1"), Read/Write (1bit), Register address (MSB first, 6bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. The PDN pin= "L" resets the registers to their default values.



C1: Chip Address (Fixed to "1")
R/W: READ/WRITE (0:READ, 1:WRITE)
A5-A0: Register Address
D7-D0: Control Data

Figure 32. 4-wire Serial Control I/F Timing

(2). I^2C bus control mode (SPI pin = "L")

The AK5730 supports the fast-mode I^2C-bus (max: 400kHz).

(2)-1. WRITE Operations

Figure 33 shows the data transfer sequence of the I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 39). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pins (CAD1/0 pins) set these device address bits (Figure 34). If the slave address matches that of the AK5730, the AK5730 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 40). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5730. The format is MSB first, and those most significant 2-bits are fixed to zeros (Figure 35). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 36). The AK5730 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 39).

The AK5730 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5730 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 2DH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 41) except for the START and STOP conditions.

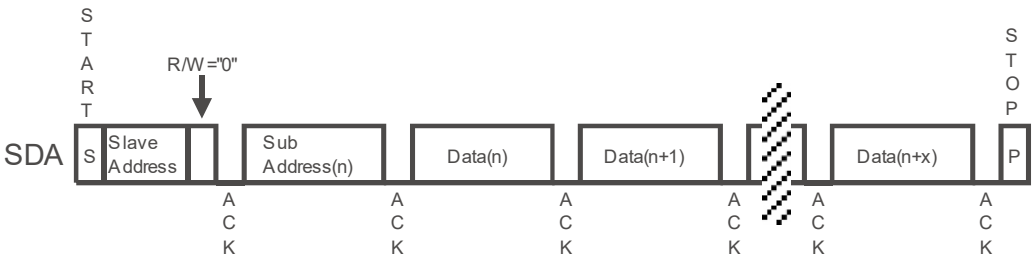


Figure 33. Data Transfer Sequence at The I^{2}C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)

Figure 34. The First Byte

0	0	A5	A4	A3	A2	A1	A0

Figure 35. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 36. Byte Structure after The Second Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK5730. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 2DH prior to generating a stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK5730 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK5730 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK5730 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5730 ceases transmission.

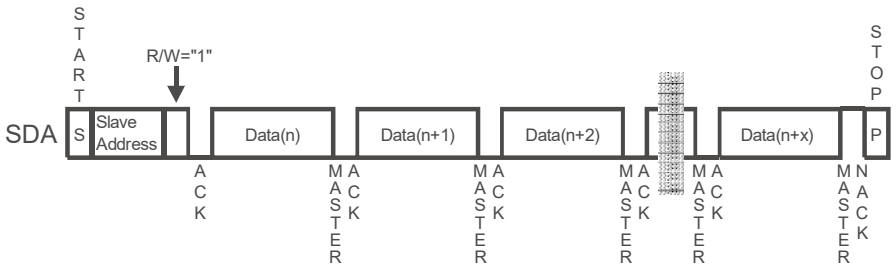


Figure 37. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK5730 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5730 ceases transmission.

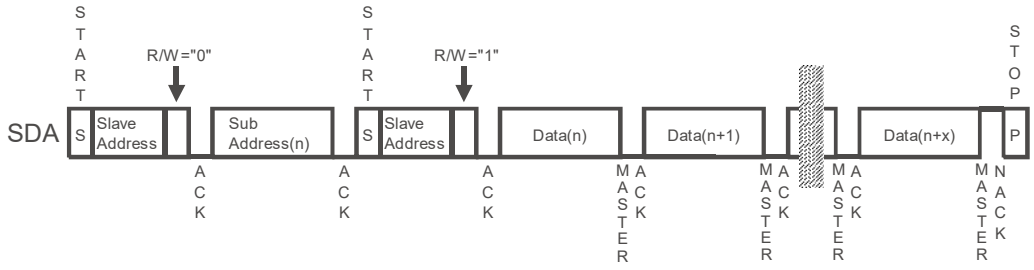


Figure 38. RANDOM ADDRESS READ

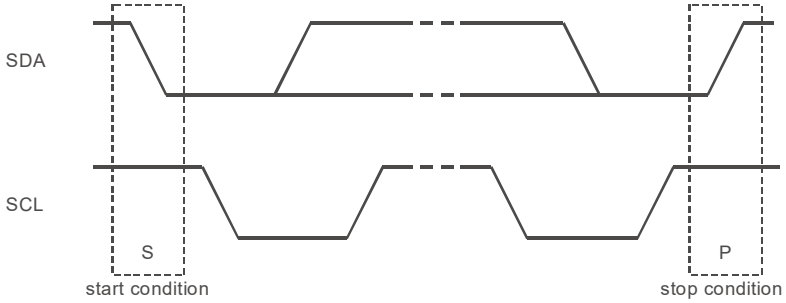


Figure 39. START and STOP Conditions

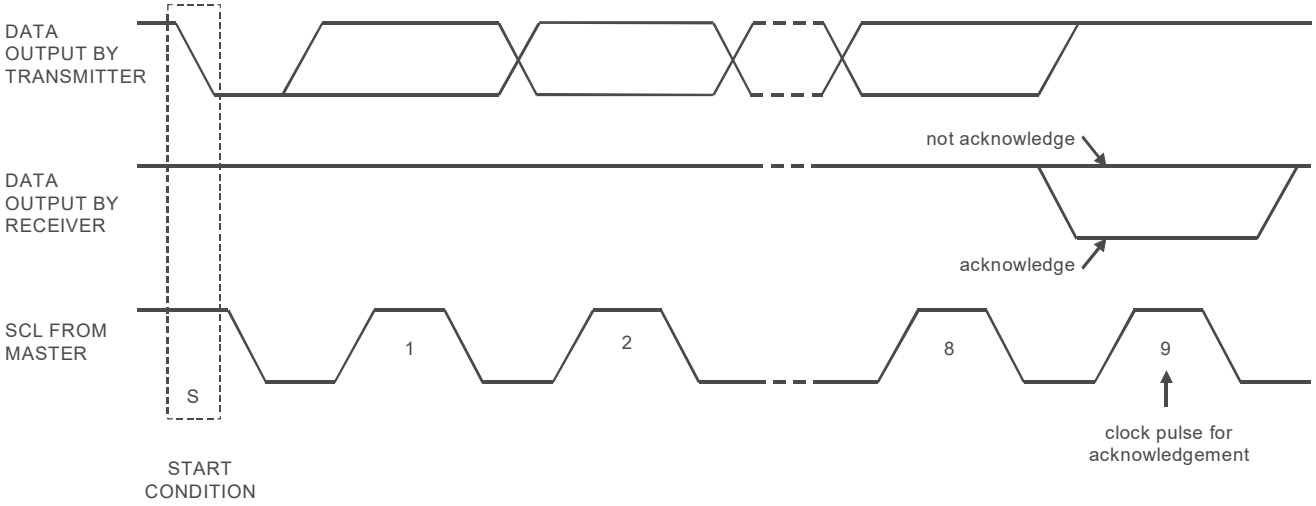


Figure 40. Acknowledge on the I^2C-Bus

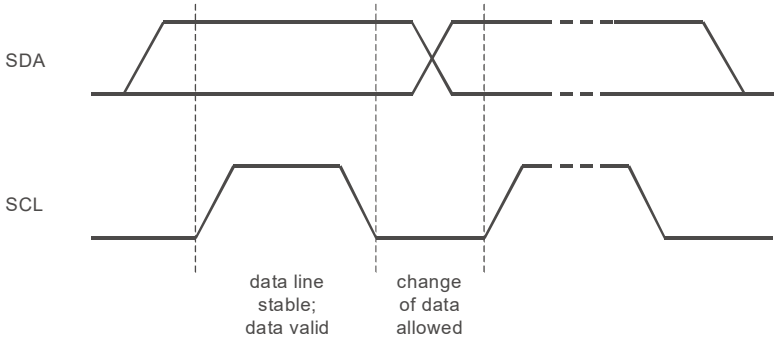


Figure 41. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	General Setting 1	CKS1	CKS0	ATS1	ATS0	DIF	TDM1	TDM0	RSTN
01H	General Setting 2	MBS3	MBS2	MBS1	MBS0	FS1	FS0	PLL1	PLL0
02H	Input mode	LIN41	LIN40	LIN31	LIN30	LIN21	LIN20	LIN11	LIN10
03H	ADC1 Volume Control	ATT17	ATT16	ATT15	ATT14	ATT13	ATT12	ATT11	ATT10
04H	ADC2 Volume Control	ATT27	ATT26	ATT25	ATT24	ATT23	ATT22	ATT21	ATT20
05H	ADC3 Volume Control	ATT37	ATT36	ATT35	ATT34	ATT33	ATT32	ATT31	ATT30
06H	ADC4 Volume Control	ATT47	ATT46	ATT45	ATT44	ATT43	ATT42	ATT41	ATT40
07H	Monitor Summary	0	0	0	0	ADC4	ADC3	ADC2	ADC1
08H	Monitor ADC1	0	OVTP	OVCR2	OVCR1	SHTV1	SHTG1	SHTD1	OPEN1
09H	Monitor ADC2	0	0	0	0	SHTV2	SHTG2	SHTD2	OPEN2
0AH	Monitor ADC3	0	0	0	0	SHTV3	SHTG3	SHTD3	OPEN3
0BH	Monitor ADC4	0	0	0	0	SHTV4	SHTG4	SHTD4	OPEN4
0CH	Mask ADC1	0	0	0	0	MSHTV1	MSHTG1	MSHTD1	MOPEN1
0DH	Mask ADC2	0	0	0	0	MSHTV2	MSHTG2	MSHTD2	MOPEN2
0EH	Mask ADC3	0	0	0	0	MSHTV3	MSHTG3	MSHTD3	MOPEN3
0FH	Mask ADC4	0	0	0	0	MSHTV4	MSHTG4	MSHTD4	MOPEN4
10H	Threshold setting OPEN	0	0	0	0	TOP4	TOP3	TOP2	TOP1
11H	Threshold setting SHTD	0	0	0	0	TSD4	TSD3	TSD2	TSD1
12H	Threshold setting SHTG	0	0	0	0	TSG4	TSG3	TSG2	TSG1
13H	Threshold setting SHTV	0	0	0	0	TSV4	TSV3	TSV2	TSV1
14H	INT setting	STD4	STD3	STD2	STD1	0	0	0	INTR
15H	ADC HPF	GAIN4	GAIN3	GAIN2	GAIN1	HPF4	HPF3	HPF2	HPF1
16H	SAR Thresh A High byte	THA12	THA11	THA10	THA09	THA08	THA07	THA06	THA05
17H	SAR Thresh A Low byte	THA04	THA03	THA02	THA01	0	0	0	0
18H	SAR Thresh B High byte	THB12	THB11	THB10	THB09	THB08	THB07	THB06	THB05
19H	SAR Thresh B Low byte	THB04	THB03	THB02	THB01	0	0	0	0
1AH	SAR Thresh C High byte	THC12	THC11	THC10	THC09	THC08	THC07	THC06	THC05
1BH	SAR Thresh C Low byte	THC04	THC03	THC02	THC01	0	0	0	0
1CH	SAR IN1+ High byte	1P12	1P11	1P10	1P09	1P08	1P07	1P06	1P05
1DH	SAR IN1+ Low byte	1P04	1P03	1P02	1P01	0	0	0	0
1EH	SAR IN1- High byte	1N12	1N11	1N10	1P09	1N08	1N07	1N06	1N05
1FH	SAR IN1- Low byte	1N04	1N03	1N02	1N01	0	0	0	0
20H	SAR IN2+ High byte	2P12	2P11	2P10	2P09	2P08	2P07	2P06	2P05
21H	SAR IN2+ Low byte	2P04	2P03	2P02	2P01	0	0	0	0
22H	SAR IN2- High byte	2N12	2N11	2N10	2N09	2N08	2N07	2N06	2N05
23H	SAR IN2- Low byte	2N04	2N03	2N02	2N01	0	0	0	0
24H	SAR IN3+ High byte	3P12	3P11	3P10	3P09	3P08	3P07	3P06	3P05
25H	SAR IN3+ Low byte	3P04	3P03	3P02	3P01	0	0	0	0
26H	SAR IN3- High byte	3N12	1N11	3N10	3P09	3N08	3N07	3N06	3N05
27H	SAR IN3- Low byte	3N04	3N03	3N02	3N01	0	0	0	0
28H	SAR IN4+ High byte	4P12	4P11	4P10	4P09	4P08	4P07	4P06	4P05
29H	SAR IN4+ Low byte	4P04	4P03	4P02	4P01	0	0	0	0
2AH	SAR IN4- High byte	4N12	4N11	2N10	4N09	4N08	4N07	4N06	4N05
2BH	SAR IN4- Low byte	4N04	4N03	4N02	4N01	0	0	0	0
2CH	SAR VBAT High byte	VB12	VB11	VB10	VB09	VB08	VB07	VB06	VB05
2DH	SAR VBAT Low byte	VB04	VB03	VB02	VB01	0	0	0	0

Note: For addresses from 2EH to 3FH, data is not written.
When the PDN pin goes to “L”, all registers are initialized to their default values.
When RSTN bit is set to “0”, the internal timing is reset, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	General Setting	CKS1	CKS0	ATS1	ATS0	DIF	TDM1	TDM0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

RSTN: Internal timing reset
0: Reset. Registers are not initialized. (default)
1: Normal operation

TDM1-0: TDM Mode Select (Table 6)
00: Normal mode. (default)
01: TDM256 mode
10: Reserved
11: Reserved

DIF: Data format setting (Table 6)
0: I^2S. (default)
1: Left Justified

ATS1-0: Digital attenuator transition time setting (Table 8)
Default: "00", mode 0

CKS1-0: Master Clock setting in Master mode. Refer to Table 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	General Setting 2	MBS3	MBS2	MBS1	MBS0	FS1	FS0	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PLL1-0: PLL mode setting (Table 4)
00: Normal mode. PLL off. (default)
01: PLL mode (BICK=64fs)
10: PLL mode (BICK=256fs)
11: PLL mode (BICK=512fs)

FS1-0: Sampling Frequency setting (Table 3)
00: 24k-48kHz (default)
01: 12k-24kHz
10: 8k-12kHz
11: (Reserved)

MBS3-0: Mic bias voltage setting

MBS3-0	Bias Voltage	
00H	5V	(default)
01H	5.5V	
02H	6V	
03H	6.5V	
04H	7V	
05H	7.5V	
06H	8V	
07H	8.5V	
08H	9V	
09H	Hi-Z	
0AH-0FH	(reserved)	

Table 17. MIC Bias Voltage Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Input mode	LIN41	LIN40	LIN31	LIN30	LIN21	LIN20	LIN11	LIN10
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LIN*1-*0: Mic/Line select for each ADC*

00: Mic mode (Default)
01: LINE and Phone mode
10: Booster input mode
11: Internal unbalanced sources mode. No diagnosis is performed for internal connections.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	ADC1 Volume Control	ATT17	ATT16	ATT15	ATT14	ATT13	ATT12	ATT11	ATT10
04H	ADC2 Volume Control	ATT27	ATT26	ATT25	ATT24	ATT23	ATT22	ATT21	ATT20
05H	ADC3 Volume Control	ATT37	ATT36	ATT35	ATT34	ATT33	ATT32	ATT31	ATT30
06H	ADC4 Volume Control	ATT47	ATT46	ATT45	ATT44	ATT43	ATT42	ATT41	ATT40
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

ATT*7-*0: ADC* Volume Control
Refer to Table 7.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Monitor Summary	0	0	0	0	ADC4	ADC3	ADC2	ADC1
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

ADC4-1: Error Monitor for each ADC

0: No error detected.
1: Error detected. Returns to "L" when INTR bit = "1".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Monitor ADC1	0	OVTP	OVCR2	OVCR1	SHTV1	SHTG1	SHTD1	OPEN1
09H	Monitor ADC2	0	0	0	0	SHTV2	SHTG2	SHTD2	OPEN2
0AH	Monitor ADC3	0	0	0	0	SHTV3	SHTG3	SHTD3	OPEN3
0BH	Monitor ADC4	0	0	0	0	SHTV4	SHTG4	SHTD4	OPEN4
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

Error Monitor.
0: No error detected.
1: Error detected. Set ADCx bit "1" if unmasked.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Mask ADC1	0	0	0	0	MSHTV1	MSHTG1	MSHTD1	MOPEN1
0DH	Mask ADC2	0	0	0	0	MSHTV2	MSHTG2	MSHTD2	MOPEN2
0EH	Mask ADC3	0	0	0	0	MSHTV3	MSHTG3	MSHTD3	MOPEN3
0FH	Mask ADC4	0	0	0	0	MSHTV4	MSHTG4	MSHTD4	MOPEN4
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Error Monitor Mask.
0: No mask.
1: Mask error.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Threshold setting OPEN	0	0	0	0	TOP3	TOP2	TOP1	TOP0
11H	Threshold setting SHTD	0	0	0	0	TSD3	TSD2	TSD1	TSD0
12H	Threshold setting SHTG	0	0	0	0	TSG3	TSG2	TSG1	TSG0
13H	Threshold setting SHTV	0	0	0	0	TSV3	TSV2	TSV1	TSV0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

Error Monitor Threshold Setting
Threshold Voltage is proportional to AVDD voltage. This value is set in digital code.

The threshold voltage is a 12bit straight binary code which the full scale is AVDD/0.3 (11V@AVDD=3.3V). The monitored voltage is multiplied by 0.3 by an external resistor and input to the voltage monitoring pin. Therefore, the threshold voltage range is from +100mV x 0.3 (=+30mV) to +900mV x 0.3 (=+270mV) at the input pin.

bit3-0	Threshold Voltage	
00H	+100mV	
01H	+200mV	
02H	+300mV	(default)
03H	+400mV	
04H	+500mV	
05H	+600mV	
06H	+700mV	
07H	+800mV	
08H	+900mV	
09H-0FH	(Reserved)	

Table 18. Error Monitor Threshold Setting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	INT setting	STD4	STD3	STD2	STD1	0	0	1	INTR
R/W		R/W	R/W	R/W	R/W	RD	RD	RD	R/W
Default		0	0	0	0	0	0	1	0

INTR: INT pin reset
0: Normal operation (default)
1: Reset. Error Monitor Registers(07-0BH) are initialized.

STD1-4: ADC1-4 Mode setting
0: Differential mode (default)
1: Single-ended mode.
When STD* bit = "1", Single-ended IN*P pin, IN*N pin must be connected to signal common.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	ADC HPF	GAIN4	GAIN3	GAIN2	GAIN1	HPF4	HPF3	HPF2	HPF1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

HPF4-1: ADC1-4 HPF on/off (Table 5)
0:ADC* HPF off
1:ADC* HPF on (default)

GAIN4-1: ADC1-4 Differential input Voltage setting
0: 1.65Vrms (default)
1: 0.55Vrms.
When GAIN*bit = "1", input voltage is amplified threefold (+9.5dB)
In order to adjust full scale range to that of the default condition,
attenuation level of each channel should be set at -9.5dB by the ATT7-0 bits (Table 7).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	SAR Thresh A High byte	THA12	THA11	THA10	THA09	THA08	THA07	THA06	THA05
17H	SAR Thresh A Low byte	THA04	THA03	THA02	THA01	0	0	0	0
18H	SAR Thresh B High byte	THB12	THB11	THB10	THB09	THB08	THB07	THB06	THB05
19H	SAR Thresh B Low byte	THB04	THB03	THB02	THB01	0	0	0	0
1AH	SAR Thresh C High byte	THC12	THC11	THC10	THC09	THC08	THC07	THC06	THC05
1BH	SAR Thresh C Low byte	THC04	THC03	THC02	THC01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SAR Raw Data Threshold A/B/C.
A: Pos. and neg. inputs shorted in LINE and Phone mode.
B: Input open in Booster input mode.
C: Input open in Booster input mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	SAR IN1+ High byte	1P12	1P11	1P10	1P09	1P08	1P07	1P06	1P05
1DH	SAR IN1+ Low byte	1P04	1P03	1P02	1P01	0	0	0	0
1EH	SAR IN1- High byte	1N12	1N11	1N10	1P09	1N08	1N07	1N06	1N05
1FH	SAR IN1- Low byte	1N04	1N03	1N02	1N01	0	0	0	0
20H	SAR IN2+ High byte	2P12	2P11	2P10	2P09	2P08	2P07	2P06	2P05
21H	SAR IN2+ Low byte	2P04	2P03	2P02	2P01	0	0	0	0
22H	SAR IN2- High byte	2N12	2N11	2N10	2N09	2N08	2N07	2N06	2N05
23H	SAR IN2- Low byte	2N04	2N03	2N02	2N01	0	0	0	0
24H	SAR IN3+ High byte	3P12	3P11	3P10	3P09	3P08	3P07	3P06	3P05
25H	SAR IN3+ Low byte	3P04	3P03	3P02	3P01	0	0	0	0
26H	SAR IN3- High byte	3N12	1N11	3N10	3P09	3N08	3N07	3N06	3N05
27H	SAR IN3- Low byte	3N04	3N03	3N02	3N01	0	0	0	0
28H	SAR IN4+ High byte	4P12	4P11	4P10	4P09	4P08	4P07	4P06	4P05
29H	SAR IN4+ Low byte	4P04	4P03	4P02	4P01	0	0	0	0
2AH	SAR IN4- High byte	4N12	4N11	2N10	4N09	4N08	4N07	4N06	4N05
2BH	SAR IN4- Low byte	4N04	4N03	4N02	4N01	0	0	0	0
2CH	SAR VBAT High byte	VB12	VB11	VB10	VB09	VB08	VB07	VB06	VB05
2DH	SAR VBAT Low byte	VB04	VB03	VB02	VB01	0	0	0	0
R/W		**RD**	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**
Default		0	0	0	0	0	0	0	0

SAR Raw Data Readout.

When reading these registers, always read the high byte first. The low byte is only updated when the high byte is read.

SYSTEM DESIGN

Figure 42 shows the system connection diagram example.

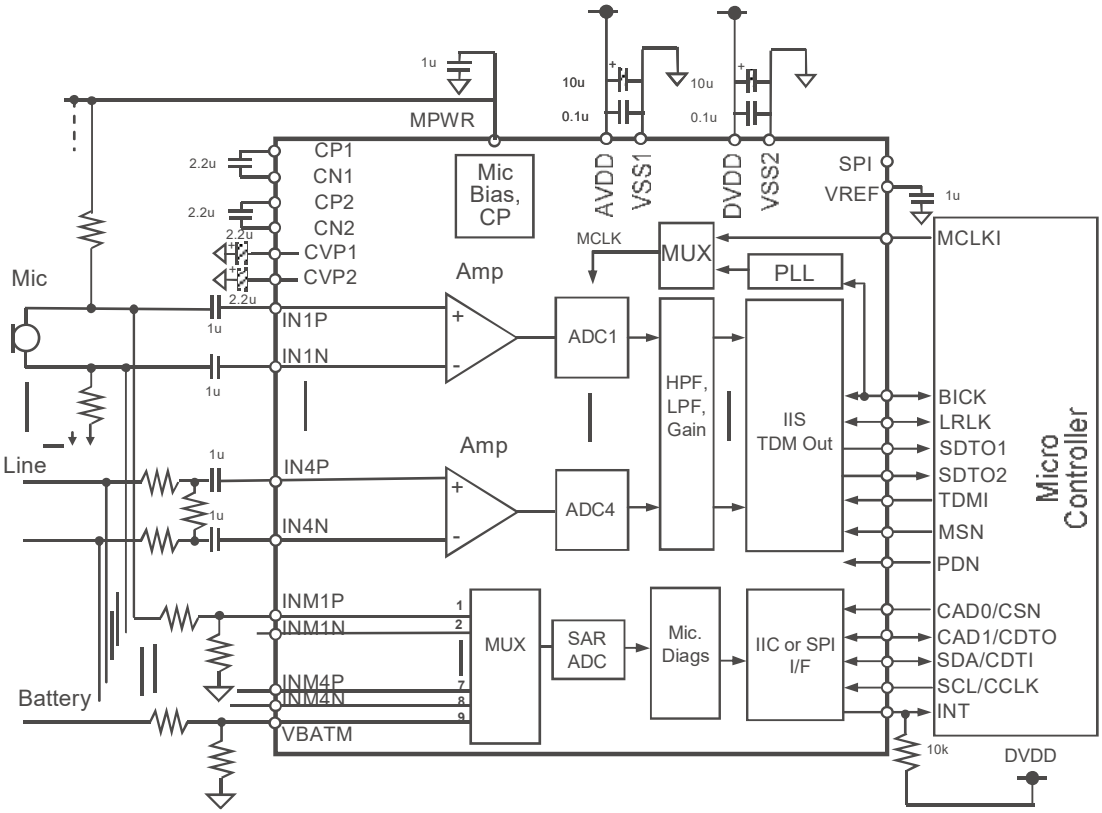


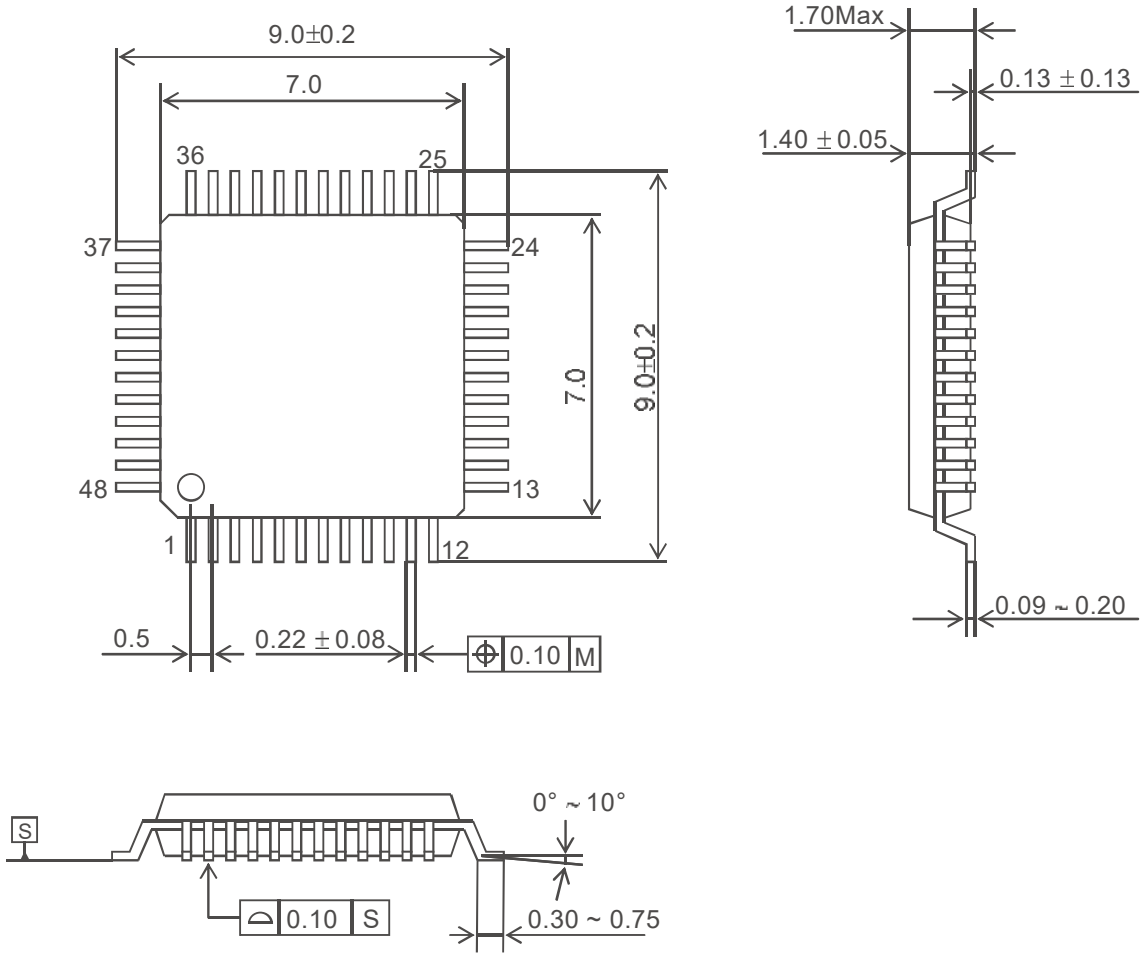
Figure 42. Typical Connection Diagram

■ Grounding and Power Supply Decoupling

AVDD should be supplied from an analog supply unit with low impedance and be separated from system digital supply. An electrolytic capacitor of 10μF parallel with a 0.1μF ceramic capacitor should be attached between AVDD and VSS1 pins, and DVDD and VSS2 pins to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitor should be placed as close to VDD (AVDD, DVDD) as possible.

PACKAGE

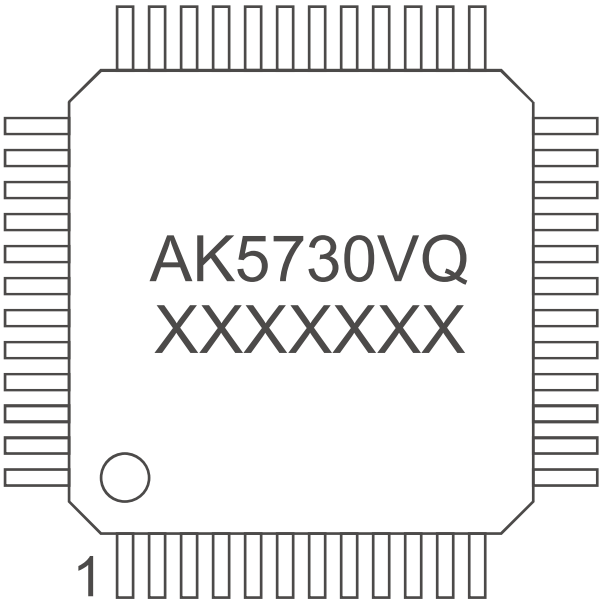
48pin LQFP(Unit: mm)



■ Package & Lead Frame Material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Marking Code: AK5730VQ
3) Date Code: XXXXXXX (7 digits)

ORDERING GUIDE

AK5730VQ	-40 ~ +105°C	48pin LQFP (0.5mm pitch)
AKD5730	Evaluation Board for AK5730	

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page/Line	Contents
13/10/16	00	First Edition		
13/12/19	01	Specification Change	11,12, 22, 23, 24, 41	TDM512 mode was deleted.
13/07/08	02	Improvement	2	Block Diagram was improved.
		Error Correction	6	Pin No.38 CVP2 The maximum bias voltage was changed. : 7.2V → 14.4V
15/11/24	03	Specification Change	12	Slave TDM256 mode SDTO Setup time BICK"↑" (min.) 12ns → 16.3ns SDTO Hold time BICK"↑" (min.) 10ns → 16.3ns TDMI Hold time (min.) 20ns → 10ns TDMI Setup time (min.) 20ns → 10ns Master TDM256 mode SDTO Setup time BICK"↑" (min.) 12ns → 16.3ns (max.) 20ns→ Deleted SDTO Hold time BICK"↑" (min.) 10ns → 16.3ns TDMI Hold time (min.) 20ns → 10ns TDMI Setup time (min.) 20ns → 10ns
		Description Addition	20	System Clock Add "In TDM256 mode, the master clock should be 256fs."
			22	Audio Serial Interface Format Add "In slave mode, the MCLKI clock frequency is allowed 256fs and 512fs. In master mode, the MCLKI clock frequency should be 256fs."
			24	Add a figure of master mode to the Cascade TDM Connection Diagram.
		Error Correction	43	Register Definitions Address 08H, D6 "0" → "OVTP" Address 08H, D5 "OVTP1" → "OVCR2"
			44	Register Definitions GAIN4-1 0: 1.68Vrms → 1.65Vrms 1: 0.56Vrms → 0.55Vrms
			46	SYSTEM DESIGN ・Add a 1uF capacitor to MPWR pin ・MCLK → MCLKI
		Description Addition	48	Add ordering guide

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