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AK5736

6-Channel Differential Audio ADC with Diagnostics

1. General Description

The AK5736 is a 6-channel ADC that supports line and microphone inputs with an SAR ADC for error detection. The error detection function monitors connection status of line and microphone inputs. The AK5736 has Pre-Gain Amplifiers (PGA) for microphone and Microphone bias (MIC bias) voltage sources. These functions make it ideal for microphone array applications such as automotive ANC, (Active Noise Cancelation), etc. The TDM audio format makes it easy to connect with a DSP.

2. Features

1. **Audio ADC**
   - **6-Channel Audio ADC**
   - **Full-differential Input and Single-ended Input**
   - **PGA for Microphone: 0dB or 6dB ~ 20dB (1dB step)**
   - **Input Voltage: 2.0 V_{RMS}**
   - **ADC Performance:**
     S/(N+D): typ 92B
     DR, S/N: typ 100dB
   - **4 Types of LPF**
     - **Sharp Roll Off Filter**
     - **Slow Roll Off Filter**
     - **Short Delay Sharp Roll Off Filter (GD=4.9/fs)**
     - **Short Delay Slow Roll Off Filter (GD=4.3/fs)**
   - **Digital Volume: MUTE, -115dB ~ +52dB (1dB step)**
   - **Digital HPF for DC-offset cancellation: fc=2Hz**
2. **Sampling Rate: 8kHz ~ 192kHz**
3. **Master Clock: 128fs, 192fs, 256fs, 384fs, 512fs**
4. **Master/Slave Mode**
5. **Audio Interface Format: MSB First, 2's complement**
   - **24bit I^2S**
   - **24bit Left justified**
   - **24bit TDM interface up to 16ch cascade connection**
6. **SAR ADC**
   - **1ch SAR ADC for Error Detection**
7. **Error Detect Function**
   - **Open**
   - **Short across Inputs**
   - **Short to Ground**
   - **Short to MIC Bias Voltage**
   - **Short to Battery**
   - **MIC Bias Over Current/Voltage**
   - **Charge Pump Under Voltage**
   - **Over Temperature**
8. **Programmable MIC Bias Voltage: 5V ~ 9V (0.5V step)**
9. **µP I/F: I^2C-Bus (Ver 1.0, 400kHz mode) or SPI**
10. **Power Supply:**
    - **AVDD= 3.0 ~ 3.6V (typ. 3.3V)**
    - **DVDD = 3.0~3.6V (typ. 3.3V) or 1.7~1.98V (typ. 1.8V)**
    - **CPVDD = 3.0~3.6V (typ. 3.3V)**
11. **Operating Temperature Range: Ta = –40 ~ 105°C**
12. **Package: 48-pin QFN**

3. Table of Contents

4. Block Diagram

■ Block Diagram

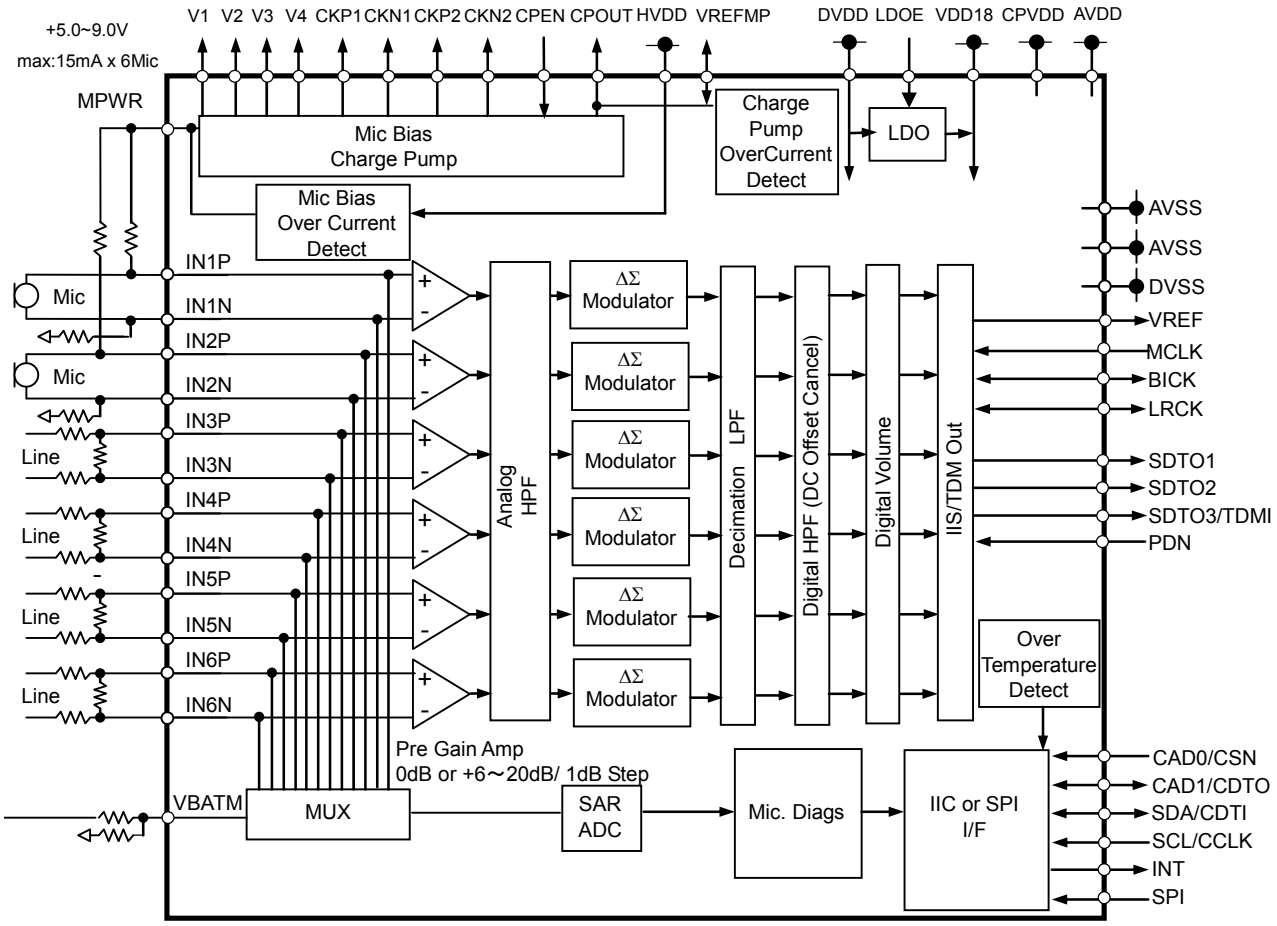
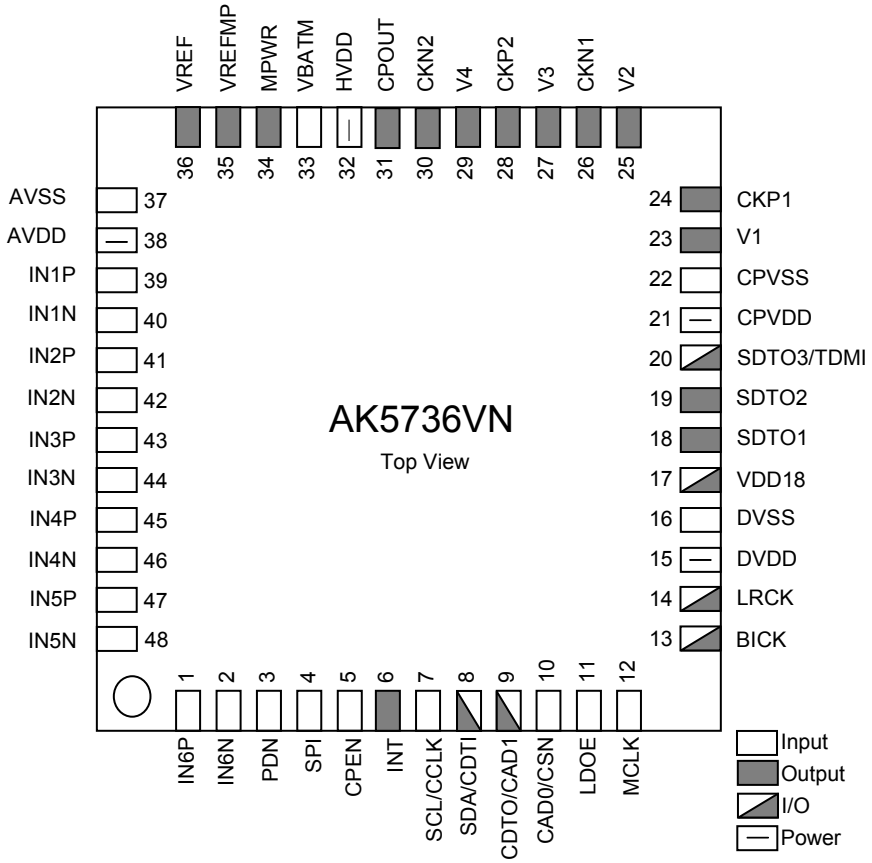


Figure 1. AK5736 Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations



■ **Pin Functions**

No.	Pin Name	I/O	Function	Power Down Status
1	IN6P	I	Ch6 Positive Input Pin	Pull down
2	IN6N	I	Ch6 Negative Input Pin	Pull down
3	PDN	I	Power-Down Mode Pin The AK5736 is in power-down mode and it is held at reset when the PDN pin = "L". It should always be reset upon power-up by the PDN pin. The AK5736 normally operates when the PDN pin ="H".	Hi-z
4	SPI	I	Control Mode Select Pin "L": I²C Bus control mode, "H": 4-wire serial control mode	Hi-z
5	CPEN	I	Internal Charge Pump Enable/Disable Pin. "L": Enable, Voltage that is boosted by internal charge pump is supplied from the CPOUT pin to the HVDD pin. Connect CPOUT pin to the HVDD pin externally. "H": Disable, Internal charge pump is powered down. An external voltage should be supplied to the HVDD pin. In this case, connect AVDD to the CPVDD pin externally.	Hi-z
6	INT	O	Interrupt Signal Output Pin (Active "L") Connect this pin to DVDD via an external 10kΩ resistor.	Hi-z
7	SCL	I	(SPI pin = "L") Control Data Clock Pin in I²C Bus control mode	Hi-z
	CCLK		(SPI pin = "H") Control Data Clock Pin in 4-wire serial control mode	
8	SDA	I/O	(SPI pin = "L") Control Data Input/Output Pin in I²C Bus control mode	Hi-z
	CDTI	I	(SPI pin = "H") Control Data Input Pin in 4-wire serial control mode	
9	CAD1	I	(SPI pin = "L") Chip Address 1 Pin in I²C Bus control mode	Hi-z
	CDTO	O	(SPI pin = "H") Control Data Output Pin in 4-wire serial control mode	
10	CAD0	I	(SPI pin = "L") Chip Address 0 Pin in I²C Bus control mode	Hi-z
	CSN		(SPI pin = "H") Chip Select Pin in serial control mode in 4-wire serial control mode	
11	LDOE	I	LDO Enable Pin "L": LDO Disable, "H": LDO Enable	Hi-z
12	MCLK	I	Master Clock Input Pin	Hi-z
13	BICK	I/O	Audio Serial Data Clock Pin	Pull down by 100kΩ
14	LRCK	I/O	Channel Clock Pin	Pull down by 100kΩ
15	DVDD	-	Digital Power Supply Pin and Charge Pump Circuit Positive Power Supply Pin 3.0V~3.6V or 1.7V~1.98V Connect this pin to DVSS via a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.	-
16	DVSS	-	Digital Ground Pin 0V	-
17	VDD18	-	Digital Core Power Supply Pin, 1.7-1.98V (LDOE pin= "L")	-
		O	LDO Stabilization Capacitor Connect Pin. (LDOE pin= "H") Connect a 4.7μF -40% ~ +20% ceramic capacitor to this pin.	Pull down

No.	Pin Name	I/O	Function	Power Down Status
18	SDTO1	O	Audio Serial Data Output1 Pin	"L"
19	SDTO2	O	Audio Serial Data Output2 Pin	"L"
20	SDTO3	O	Audio Serial Data Output3 Pin	Pull-down
	TDMI	I	TDM Data Input Pin in TDM mode	
21	CPVDD	-	Charge Pump Power Supply Pin, 3.0 ~ 3.6V Connect this pin to CPVSS via a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.	-
22	CPVSS	-	Charge Pump Ground Pin, 0V	-
23	V1	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% ~ +20% capacitor between the CKP1 pin and this pin.	Pull-up to CPVDD
24	CKP1	O	Charge Pump Clock pin	"L"
25	V2	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% ~ +20% capacitor between the CKN1 pin and this pin.	Pull-up to CPVDD
26	CKN1	O	Charge Pump Clock pin	"H"(CPVDD)
27	V3	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% ~ +20% capacitor between the CKP2 pin and this pin.	Pull-up to CPVDD
28	CKP2	O	Charge Pump Clock pin	"L"
29	V4	O	Charge Pump Boost Pin Do not connect this pin to an external device to draw current. Connect a 2.2uF-40% ~ +20% capacitor between the CKN2 pin and this pin.	Pull-up to CPVDD
30	CKN2	O	Charge Pump Clock pin	"H"(CPVDD)
31	CPOUT	O	Charge Pump Output Pin Connect HVDD to this pin externally when using the internal charge pump (CPEN pin = "L"). This pin should also be connected to AVSS via a 10uF ceramic capacitor. This pin should be open when not using the internal charge pump (CPEN pin = "H").	Pull-up to CPVDD
32	HVDD	I	High voltage power input pin Connect this pin to a load dump protected 12V~16V. When CPEN pin="H", HVDD voltage, not a charge pump, makes the analog voltage like a MIC bias voltage and Pre Gain Amp etc.	-
33	VBATM	I	Battery Power Monitor Pin	Pull down

No.	Pin Name	I/O	Function	Power Down Status
34	MPWR	O	MIC Bias Voltage Output Pin Normally, connect this pin to AVSS via a 1ohm resistor and a 10μF ceramic capacitor. * The maximum bias is 9V. The capacitance of the connecting external capacitor must be a minimum of 3.5uF, including variation tolerance, including temperature change and bias voltage difference. The external capacitor must be mounted as close as possible to the MPWR pin. A variation of a 1ohm external resistor must be within ±10% including allowable value and temperature drift. At startup, a maximum of 500mA current may flow.	Pull down
35	VREFMP	O	Voltage Reference Pin for MPWR. Connect this pin to AVSS via a 2.2μF capacitor.	Pull down
36	VREF	O	Voltage Reference Decoupling Pin Connect this pin to AVSS via a 1.0μF capacitor.	Pull down
37	AVSS	-	Analog Ground pin 0V	-
38	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V Normally, connect this pin to AVSS via a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.	-
39	IN1P	I	Ch1 Positive Input Pin	Pull down
40	IN1N	I	Ch1 Negative Input Pin	Pull down
41	IN2P	I	Ch2 Positive Input Pin	Pull down
42	IN2N	I	Ch2 Negative Input Pin	Pull down
43	IN3P	I	Ch3 Positive Input Pin	Pull down
44	IN3N	I	Ch3 Negative Input Pin	Pull down
45	IN4P	I	Ch4 Positive Input Pin	Pull down
46	IN4N	I	Ch4 Negative Input Pin	Pull down
47	IN5P	I	Ch5 Positive Input Pin	Pull down
48	IN5N	I	Ch5 Negative Input Pin	Pull down

Note 1. All digital input pins should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be connected appropriately.

Classification	Pin Name	Setting
Analog	IN1-6P, IN1-6N	Open
	V1,V2,V3,V4,CPOUT,CKP1,CKN1,CKP2,CKN2	Open
	MPWR, VBATM, INT, CDTO	Open
Digital	SDTO1-3	Open

Data is output from unused channels. Mute the unused channels via the digital volume function. The TDM format does not change, even with unused channels. When not using the internal charge pump and the MPWR pin, power up the AK5736 after setting the register address 5EH[7:0] = 7FH and RSTN bit = "1". In register control mode, AK5736's roll over address is 4BH, therefore set the address to 5EH directly.

6. Absolute Maximum Ratings

(AVSS = DVSS = CPVSS = 0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog (AVDD pin)	AVDD	−0.3	5.5	V
	Digital Interface (DVDD pin)	DVDD	−0.3	5.5	V
	Digital Core (VDD18 pin)(Note 3)	VDD18	−0.3	1.98	V
	Charge Pump Power Supply Pin	CPVDD	−0.3	5.5	V
	High voltage Supply Pin	HVDD	−0.3	18	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
IN1-6P, IN1-6N Input Voltage		VINA	−0.3	10.1	V
VBATM	(ATT_VB bit = "0" (default))	VINBAT	−0.3	18	V
	(ATT_VB bit = "1")		−0.3	10.1	
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages are with respect to ground. AVSS, DVSS and CPVSS must be connected to the same analog ground plane.

Note 3. When an external power supply is connected to the VDD18 and the 1.8V LDO is Off, (LDOE pin="L").

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = CPVSS = 0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog (AVDD pin)	AVDD	3.0	3.3	3.6	V
	(LDOE pin= "L") (Note 4)					
	Digital Interface (DVDD pin) (Note 5)	DVDD	1.7	1.8	1.98	V
	Digital Core (VDD18 pin)	VDD18	1.7	1.8	1.98	V
	(LDOE pin= "H") (Note 6)					
	Digital Interface (DVDD pin)	DVDD	3.0	3.3	3.6	V
	Charge Pump (CPVDD pin) (Note 7)	CPVDD	3.0	3.3	3.6	V
	Analog (HVDD pin) (Note 8)	HVDD	12	14.5	16	V

Note 2. All voltages are with respect to ground. AVSS, DVSS and CPVSS must be connected to the same analog ground plane.

Note 4. DVDD must be powered up before or at the same time as VDD18 when the LDOE pin="L". The power up sequence between AVDD and DVDD, AVDD and VDD18 are not critical.

Note 5. DVDD should be in the range of VDD18 ±0.1V when the LDOE pin= "L".

Note 6. The internal LDO outputs 1.8V when the LDOE pin="H". The power up sequence between DVDD and AVDD is not critical.

Note 7. Connect the CPVDD pin to AVDD when the CPEN pin="H". If the CPEN pin is "L", the voltage difference between CPVDD and AVDD should be less than 0.1V.

Note 8. When an external power supply is supplied to the HVDD pin and the Internal charge pump is not used, the AK5736 should be reset by setting RSTN bit="0" or PDN pin="L", if the HVDD voltage drops to a value lower than recommended operating conditions or has an instantaneous interruption to avoid clicking noises.

Note 9. Exposed Pad on the back surface of the package must be connected to ground. It is recommended to have at least 24 thermal via holes when solid ground is applied on one layer and 8 or more via holes are recommended when solid ground is applied on two layers.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Analog Characteristics

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; Signal Frequency = 1kHz; 24bit Data; Measurement frequency = 20Hz ~ 20kHz; HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"); IN*P DC level = 6.0V / IN*N DC level = 3.0V(Differential *:1, 2, ⋯,6), IN*P DC level = 4.5V / IN*N DC level = 0V(Single-end *:1, 2, ⋯,6); unless otherwise specified)

Parameter				Min.	Typ.	Max.	Unit
ADC Analog Characteristics							
Resolution				-	-	24	Bit
Input Voltage		PGA 0dB	Differential (Note 10)	1.9	2.0	2.1	Vrms
			Single-ended	0.95	1.0	1.05	Vrms
		PGA 20dB	Differential (Note 10)	0.18	0.2	0.22	Vrms
			Single-ended	0.091	0.1	0.109	Vrms
PGA(Pre Gain Amp) Gain step Error				-0.3	0	0.3	dB
Input Impedance				0.8	1.48	2	MΩ
S/(N+D)	fs=48kHz	0dB	−0.5dBFS Differential	86	92	-	dB
			−0.5dBFS Single-ended	86	92	-	
		20dB	−0.5dBFS Differential	81	87	-	
			−0.5dBFS Single-ended	78	84	-	
	fs=96kHz, 192kHz (Note 11)	0dB	−0.5dBFS Differential	85	91	-	dB
			−0.5dBFS Single-ended	84	90	-	
		20dB	−0.5dBFS Differential	79	85	-	
			−0.5dBFS Single-ended	75	81	-	
S/N	fs=48kHz	0dB	A-weighted Differential	95	100	-	dB
			A-weighted Single-ended	94	99	-	
		20dB	A-weighted Differential	90	96	-	
			A-weighted Single-ended	85	91	-	
	fs=96kHz, 192kHz (Note 11)	0dB	Flat Differential	90	95	-	dB
			Flat Single-ended	89	94	-	
		20dB	Flat Differential	81	87	-	
			Flat Single-ended	75	81	-	
Dynamic Range		0dB	−60dBFS, A-weighted Differential	95	100	-	dB
			−60dBFS, A-weighted Single-ended	94	99	-	
		20dB	−60dBFS, A-weighted Differential	90	96	-	
			−60dBFS, A-weighted Single-ended	85	91	-	
Interchannel Isolation		0dB		90	100	-	dB
		20dB		70	80	-	
Interchannel Gain Mismatch		0dB		-	0	0.2	dB
		20dB		-	0	0.3	
Peak Input Voltage (Note 12)				0	-	9.5	V

Note 10. The voltage difference between IN*P and IN*N pins. Input voltage is not proprtional to AVDD.

Note 11. The mesurement conditions when fs = 96kHz and 192kHz are frequency = 20Hz ~ 20kHz and MCLK = 256fs(fs = 96kHz) or 128fs(fs = 192kHz).

Note 12. It is the input voltage range of IN*P and IN*N (*1,2,…,6) pins that satisfy the above analog characteristics.

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; Signal Frequency = 1kHz; 24bit Data; Measurement frequency = 20Hz ~ 20kHz;, HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V (CPEN pin = "H"); IN*P DC level = 6.0V / IN*N DC level = 3.0V (Differential mode *:1, 2, ⋯, 6), IN*P DC level = 4.5V / IN*N DC level = 0V (Single-ended mode *:1, 2, ⋯,6), unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
CMRR (Note 13)	0dB	Differential (1kHz, 20kHz)	70	85	-	dB
	20dB	Differential (1kHz, 20kHz)	70	85	-	
PSRR (Note 14)	0dB	Differential / Single-end	-	80	-	dB
	20dB	Differential / Single-end	-	80	-	
PSMR (Note 15)	0dB	100mVpp, 1kHz, Differential / Single-end	-	-100	-	dB
CMMR (Note 16)	0dB	100mVpp, 1kHz, Differential	-	-100	-	
Analog HPF Cutoff Frequency			1.8	4	10	Hz
Peak Input Voltage (Note 17)			0	-	9.5	V

Note 13. Input conditions are 1.0 Vpp, (Gain = 0 dB), or 0.1 Vpp, (Gain = 20 dB), signal to the IN*P pin and the IN*N pin with the same phase and an input DC level = 4.5 V.

Note 14. PSRR is applied to AVDD and DVDD with 1kHz, 20mVpp.

Note 15. This value shows the level of the modulation wave, [dBFS], that appears on, "1kHz input signal ± superimposed noise frequency of the power supply", when a sine wave of 0.1 Vpp is superimposed on the AVDD pin and the DVDD pin, inputting a 1 kHz/- 0.5 dB sine wave to the IN*P and the IN*N pins, (* = 1, 2, ..., 6). The superimposed noise frequency is 0.1kHz, 0.5kHz or 15.5kHz.

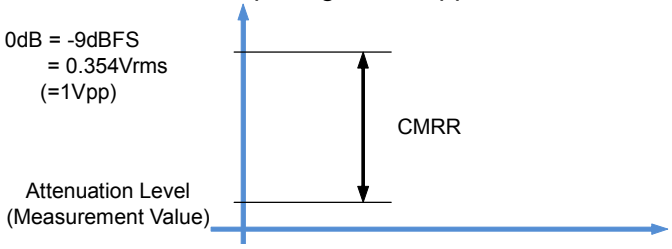
Note 16. This value shows the level of the modulation wave, [dBFS], that appears on, "1kHz input signal ± common mode noise frequency", when a sine wave of 1 kHz / - 0.5 dB is input to the IN*P and the IN*N pins, (* 1, 2, ..., 6), in the same phase while the input DC level = 4.5 V, inputting a 0.1 Vpp sine wave to the IN*P and the IN*N pins. The common mode noise frequency is 0.1kHz, 0.5kHz or 15.5kHz.

Note 17. The input voltage range of the IN*P and the IN*N pins, (*1, 2, …, 6), that satisfies the above analog characteristics.

Definition of CMRR

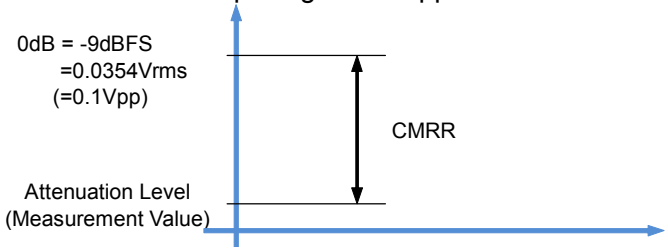
1. When Setting Gain = 0dB

CMRR is measured by inputting a 1kHz or 20kHz, 1.0Vpp signal to both the IN*P and the IN*N pins in phase. CMRR represents the ratio of the input signal 1.0Vpp and the attetuation level.



2. When Setting Gain = 20dB

CMRR is measured by inputting a 1kHz or 20kHz, 0.1Vpp signal to both the IN*P and the IN*N pins in phase. CMRR represents the ratio of the input signal 0.1Vpp and the attetuation level.



(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; HVDD = CPOUT (CPEN pin = "L"), HVDD = 14.5V(CPEN pin ="H"))

Parameter		Min.	Typ.	Max.	Unit
MIC Bias Voltage:					
Output DC Voltage (Note 18)	MBS3-0 bits= "0000"	4.90	5	5.10	V
	MBS3-0 bits= "0001"	5.39	5.5	5.61	V
	MBS3-0 bits= "0010"	5.88	6	6.12	V
	MBS3-0 bits= "0011"	6.37	6.5	6.63	V
	MBS3-0 bits= "0100"	6.86	7	7.14	V
	MBS3-0 bits= "0101"	7.35	7.5	7.65	V
	MBS3-0 bits= "0110"	7.84	8	8.16	V
	MBS3-0 bits= "0111"	8.33	8.5	8.67	V
	MBS3-0 bits= "1000"	8.78	9	9.22	V
Microphone Current (for 6 channels)		-	-	90	mA
Output Noise Level (A-weighted)		-	-100	-94	dBV

Note 18. When MBS3-0 bits = "0000"/"0001"/"0010"/"0011"/"0100"/"0101"/"0110"/"0111"/"1000", the DC output voltage (typ.) is 1.515/1.667/1.818/1.969/2.121/2.272/2.424/2.575/2.727 × AVDD(V), respectively.
When MBS3-0 bits = "0000"/"0001"/"0010"/"0011"/"0100"/"0101"/"0110"/"0111", the DC output voltage (Min, Max) is ±2.0% of typical DC output voltage.
When MBS3-0 bits = "1000", the DC output voltage, (Min, Max), is ±2.5% of typical DC output voltage.

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.0～3.6V; AVSS = DVSS = CPVSS = 0V; MCLK = 512fs, fs = 48kHz, BCLK = 64fs, CPEN pin = "L")

Parameter		min	typ	max	Unit
MIC Bias Voltage:					
Microphone Current (for 6 channels total)	MBS3-0 bits = "0000"	-	-	50	mA
	MBS3-0 bits = "0001"	-	-	55	mA
	MBS3-0 bits = "0010"	-	-	60	mA
	MBS3-0 bits = "0011"	-	-	65	mA
	MBS3-0 bits = "0100"	-	-	70	mA
	MBS3-0 bits = "0101"	-	-	75	mA
	MBS3-0 bits = "0110"	-	-	80	mA
	MBS3-0 bits = "0111"	-	-	78	mA
	MBS3-0 bits = "1000"	-	-	66	mA

Note 19. Voltage difference between CPVDD and AVDD should be less than 0.1V.

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.0~3.6V; HVDD = 12.0~16.0V; AVSS = DVSS = CPVSS = 0V; MCLK = 512fs, fs = 48kHz, BCLK = 64fs, CPEN in = "H")

Parameter		min	typ	max	Unit
MIC Bias Voltage:					
Microphone Current (for 6 channels total)	MBS3-0 bits = "0000"	-	-	50	mA
	MBS3-0 bits = "0001"	-	-	55	mA
	MBS3-0 bits = "0010"	-	-	60	mA
	MBS3-0 bits = "0011"	-	-	65	mA
	MBS3-0 bits = "0100"	-	-	70	mA
	MBS3-0 bits = "0101"	-	-	75	mA
	MBS3-0 bits = "0110"	-	-	80	mA
	MBS3-0 bits = "0111"	-	-	85	mA
	MBS3-0 bits = "1000"	-	-	90	mA

(Ta = 25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = 0V; MCLK = 512fs, fs = 48kHz, BICK = 64fs; HVDD = CPOUT (CPEN pin = “L”), HVDD = 14.5V (CPEN pin = ”H”))

Parameter		Min.	Typ.	Max.	Unit
SAR ADC Characteristics (DC):					
Resolution		-	-	12	Bit
IN*P&IN*N pin Input Voltage (Note 20)		0	-	10.1	V
VBATM pin Input Voltage (Note 21)	ATT_VB bit = “0”	0	14.5	18	V
VBATM pin Input Voltage (Note 21)	ATT_VB bit = “1”	0	-	10.1	V
Integral Nonlinearity (INL) (Note 22)		-4	-	+5	LSB
Differential Nonlinearity (DNL) A (Note 22)		-4	-	+4	LSB
IN*P&IN*N pin Attenuation error		-1.4	-	1.4	%
VBATM pin Attenuation error	ATT_VB bit = “0”	-1.8	-	+1.8	%
	ATT_VB bit = “1”	-1.4	-	+1.4	%
MPWR pin Attenuation error		-1.4	-	+1.4	%

Note 20. Input signals of IN*P and IN*N pins are attenuated by 30% via internal resistance and input to the SARADC. The SARADC operates with an input voltage to IN*P, IN*N pins greater than 330mV. Input signals recognized as full scale code are proportional to AVDD, and it is at the full scale if 10V is input when AVDD = 3.0V. The full-scale input voltage will be 11V when AVDD = 3.3V however do not input a voltage more than 10.1V since it exceeds the absolute maximum rating. The internal path connected to the MIC Bias Voltage is also attenuated by 30%.

Note 21. When ATT_VB bit = “0” (default), input signal of the VBATM pin is attenuated by 10% via internal resistance and input to the SARADC.
The attenuation ratio will be 30% when ATT_VB bit = “1”.

Note 22. The IN*P, IN*N and VBATM pins should be within the conditions stated below to guarantee the characteristics.

- IN*P, IN*N pin ≥ 330mV
- (ATT_VB bit = 0): VBATM pin ≥1V,
  (ATT_VB bit = 1): VBATM pin ≥330mV

(Ta=25°C; AVDD = DVDD = CPVDD = 3.3V; AVSS = DVSS = CPVSS = 0V)

Parameter	Min.	Typ.	Max.	Unit
Power Supplies				
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "H" CPEN pin = "L")				
AVDD	-	10	14	mA
DVDD (fs = 48kHz)	-	19	27	mA
DVDD (fs = 96kHz)	-	28	39	mA
DVDD (fs = 192kHz)	-	28	39	mA
CPVDD (MIC bias current = 90mA)	-	500	550	mA
Power down (PDN pin = "L" , LDOE pin = "H") (Note 23)				
AVDD+DVDD+CPVDD		1	100	μA
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "L" CPEN pin = "L")				
AVDD	-	10	14	mA
DVDD+VDD18 (fs = 48kHz)	-	19	27	mA
DVDD+VDD18 (fs = 96kHz)	-	28	39	mA
DVDD+VDD18 (fs = 192kHz)	-	28	39	mA
CPVDD (MIC bias current = 90mA)	-	500	550	mA
Power down (PDN pin = "L" , LDOE pin = "L") (Note 23)				
AVDD+DVDD+CPVDD+VDD18		1	100	μA
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "H" CPEN pin = "H")				
AVDD+CPVDD	-	10	14	mA
DVDD (fs = 48kHz)	-	19	27	mA
DVDD (fs = 96kHz)	-	28	39	mA
DVDD (fs = 192kHz)	-	28	39	mA
HVDD (MIC bias current =90mA)	-	110	116	mA
Power down (PDN pin = "L" , LDOE pin = "H") (Note 23)				
AVDD+DVDD+CPVDD+HVDD		1	300	μA
Power Supply Current				
Normal operation (PDN pin = "H", LDOE pin = "L" CPEN pin = "H")				
AVDD+CPVDD	-	10	14	mA
DVDD+VDD18 (fs = 48kHz)	-	19	27	mA
DVDD+VDD18 (fs = 96kHz)	-	28	39	mA
DVDD+VDD18 (fs = 192kHz)	-	28	39	mA
HVDD (MIC bias current = 90mA)	-	110	116	mA
Power down (PDN pin = "L" , LDOE pin = "L") (Note 23)				
AVDD+DVDD+CPVDD+VDD18+HVDD		1	300	μA

Note 23. All digital input pins are fixed to DVDD or DVSS. The power supply current of DVDD is in TDM mode.

Note 24. Power consumption of DVDD in normal operation is measured when 1kHz sine wave is input to the IN1P, IN3P, IN5P, IN1N, IN3N and IN5N pins and a sine wave that is shifted 180° input to the IN2P, IN4P, IN6P, IN2N, IN4N and IN6N pins.

9. Filter Characteristics

■ ADC Filter Characteristics (fs = 48kHz)

(Ta = -40 ~ +105°C; AVDD = 3.0~3.6V, DVDD = 1.7~1.98V (LDOE pin = "L"), 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V (LDOE pin = "L"), HVDD = CPOUT(CPEN pin = "L") / HVDD = 12~16V(CPEN pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 2) (SD bit = "0", SLOW bit = "0")						
Passband (Note 25)	+0.001/–0.06dB –6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 25)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 3) (SD bit= "0", SLOW bit="1")						
Passband (Note 25)	+0.001/–0.076dB –6.0dB	PB	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 25)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	6.6	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 4) (SD bit= "1", SLOW bit= "0")						
Passband (Note 25)	+0.001/–0.06dB –6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 25)		SB	27.9		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 26)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 5) (SD bit="1", SLOW bit="1")						
Passband (Note 25)	+0.001/–0.076dB –6.0dB	PB -	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 25)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 26)		GD	-	4.3	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 25)	–3.0dB –0.5dB –0.1dB	FR	- - -	2.0 5.0 13.0	- - -	Hz Hz Hz

Note 25. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.06dB) =0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.076dB) =0.26 × fs (SLOW ROLL-OFF).

Note 26. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO.

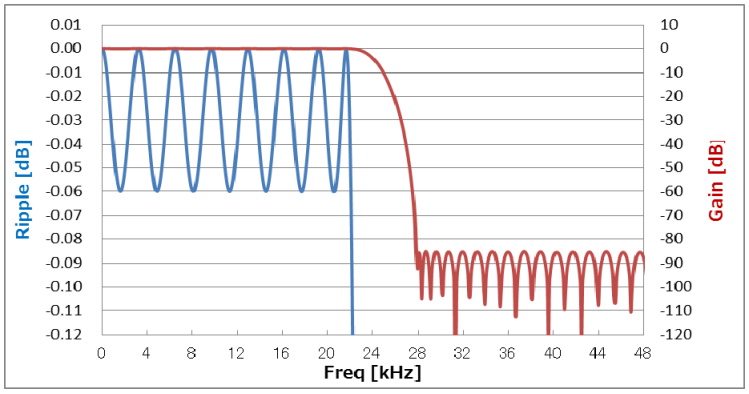


Figure 2. SHARP ROLL-OFF (fs=48kHz)

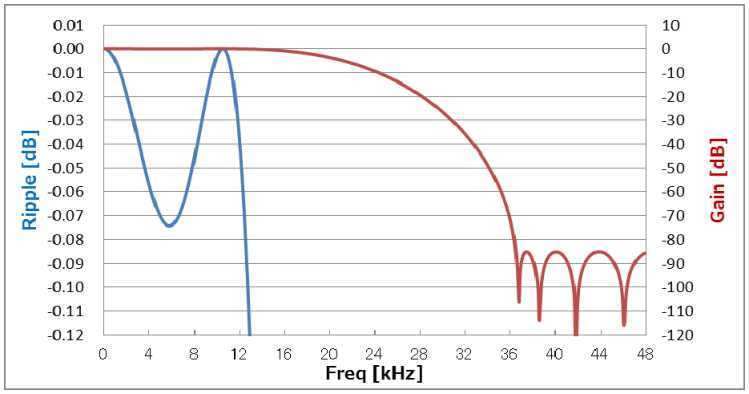


Figure 3. SLOW ROLL-OFF (fs=48kHz)

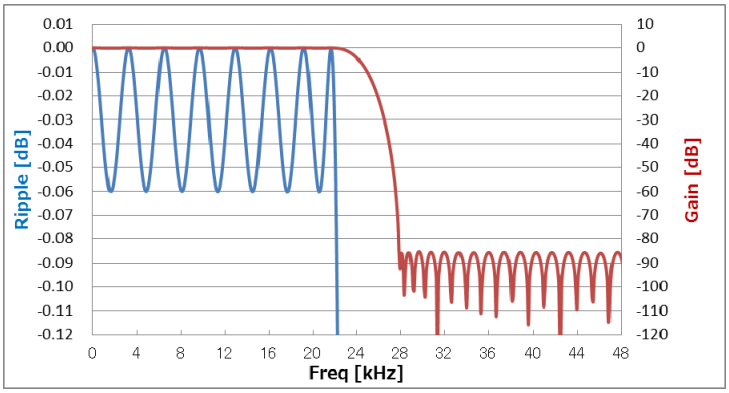


Figure 4. SHORT DELAY SHARP ROLL-OFF (fs=48kHz)

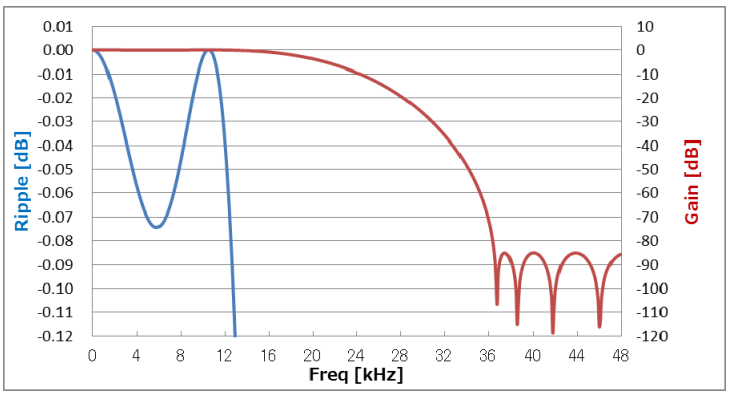


Figure 5. SHORT DELAY SLOW ROLL-OFF (fs=48kHz)

■ ADC Filter Characteristics (fs = 96kHz)

(Ta = -40 ~ +105°C; AVDD = 3.0~3.6V, DVDD = 1.7~1.98V (LDOE pin = "L"), 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V (LDOE pin = "L"), HVDD = CPOUT(CPEN pin = "L") / HVDD = 12~16V(CPEN pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 6) (SD bit="0", SLOW bit="0")						
Passband (Note 25)	0.001dB/–0.06dB –6.0dB	PB	0	- 48.8	44.1	kHz kHz
Stopband (Note 25)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 7) (SD bit="0", SLOW bit="1")						
Passband (Note 25)	+0.001dB/–0.076dB –6.0dB	PB	0 -	- 43.8	25	kHz kHz
Stopband (Note 25)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	6.6	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF (Figure 8) (SD bit="1", SLOW bit="0")						
Passband (Note 25)	+0.001dB/–0.06dB –6.0dB	PB	0 -	- 48.8	44.1 -	kHz kHz
Stopband (Note 25)		SB	55.7		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 26)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 9) (SD bit="1", SLOW bit="1")						
Passband (Note 25)	+0.001dB/–0.076dB –6.0dB	PB	0 -	- 43.8	25 -	kHz kHz
Stopband (Note 25)		SB	73	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 26)		GD	-	4.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 25)	–3.0dB –0.5dB –0.1dB	FR	- - -	2.0 5.0 13.0	- - -	Hz Hz Hz

Note 25. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.06dB) =0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.076dB) =0.26 × fs (SLOW ROLL-OFF).

Note 26. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO.

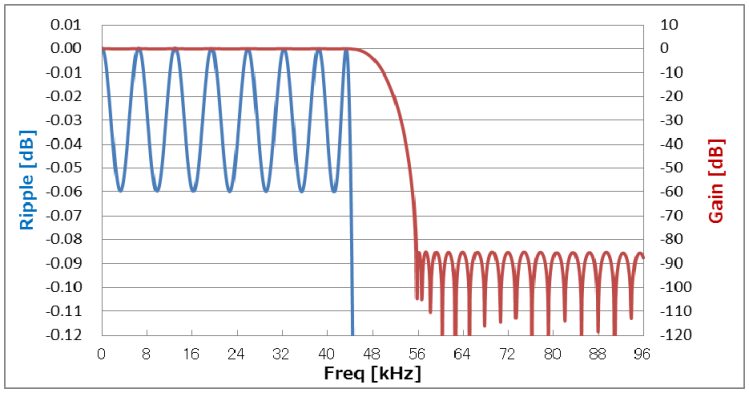


Figure 6. SHARP ROLL-OFF (fs=96kHz)

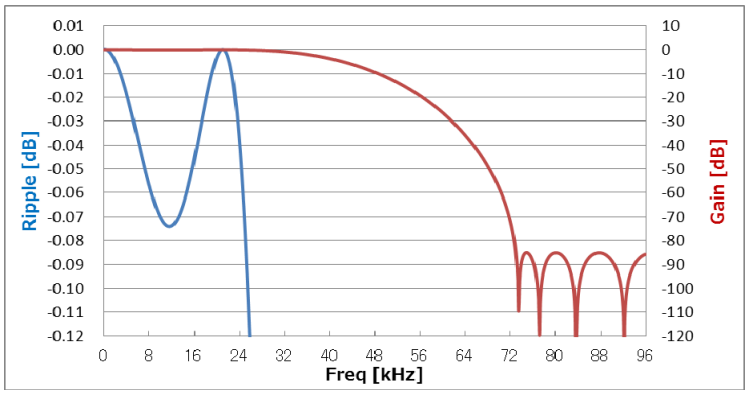


Figure 7. SLOW ROLL-OFF (fs=96kHz)

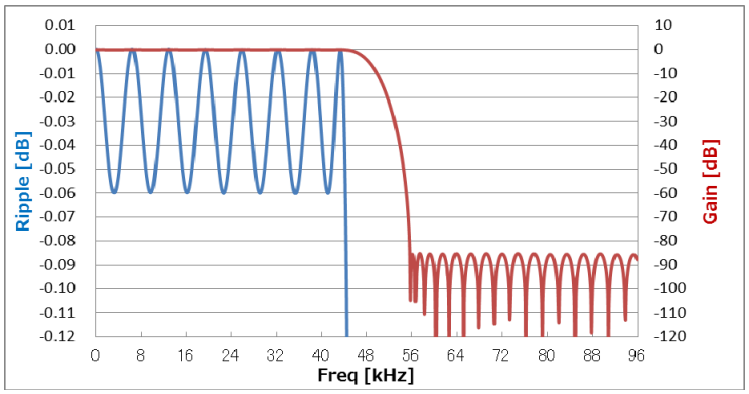


Figure 8. SHORT DELAY SHARP ROLL-OFF (fs=96kHz)

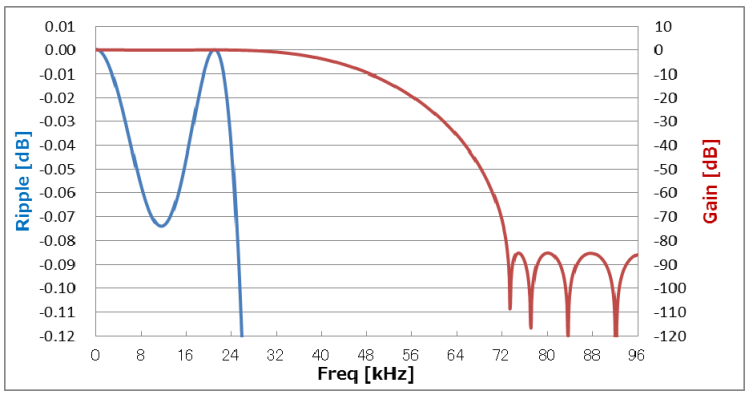


Figure 9. SHORT DELAY SLOW ROLL-OFF (fs=96kHz)

■ ADC Filter Characteristics (fs = 192kHz)

(Ta = -40 ~ +105°C; AVDD = 3.0~3.6V, DVDD = 1.7~1.98V (LDOE pin = "L"), 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V (LDOE pin = "L"), HVDD = CPOUT(CPEN pin = "L") / HVDD = 12~16V(CPEN pin = "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 10) (SD bit= "0", SLOW bit= "0")						
Passband (Note 25)	+0.001B/–0.037dB –6.0dB	PB	0	- 100.2	83.7	kHz kHz
Stopband (Note 25)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	14.4	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 11) (SD bit= "0", SLOW bit= "1")						
Passband (Note 25)	0.001dB/–0.1dB –6.0dB	PB	0	- 75.2	31.5	kHz kHz
Stopband (Note 25)		SB	146	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	7.3	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 12) (SD bit= "1", SLOW bit= "0")						
Passband (Note 25)	+0.001B/–0.037dB –6.0dB	PB	0 -	- 100.2	83.7 -	kHz kHz
Stopband (Note 25)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 26)		GD	-	6.0	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (Figure 13) (SD bit "1", SLOW bit= "1")						
Passband (Note 25)	+0.001dB/–0.1dB –6.0dB	PB	0 -	- 75.2	31.5 -	kHz kHz
Stopband (Note 25)		SB	146	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.4	1/fs
Group Delay (Note 26)		GD	-	5.8	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 25)	–3.0dB –0.5dB –0.1dB	FR	- - -	2.0 5.0 13.0	- - -	Hz Hz Hz

Note 25. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.037dB) =0.436 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.1dB) = 0.164 × fs (SLOW ROLL-OFF).

Note 26. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO.

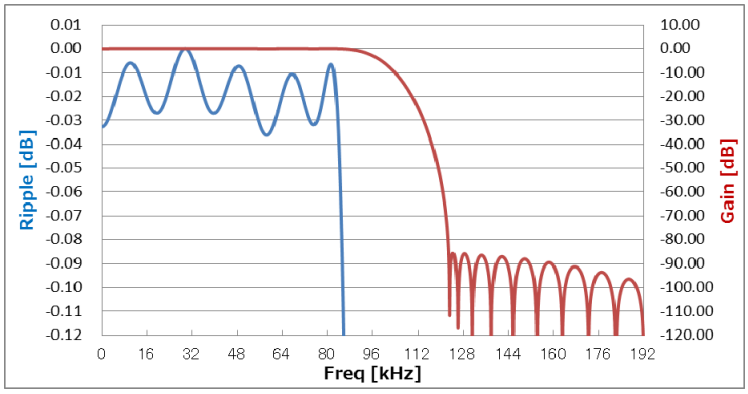


Figure 10. SHARP ROLL-OFF (fs=192kHz)

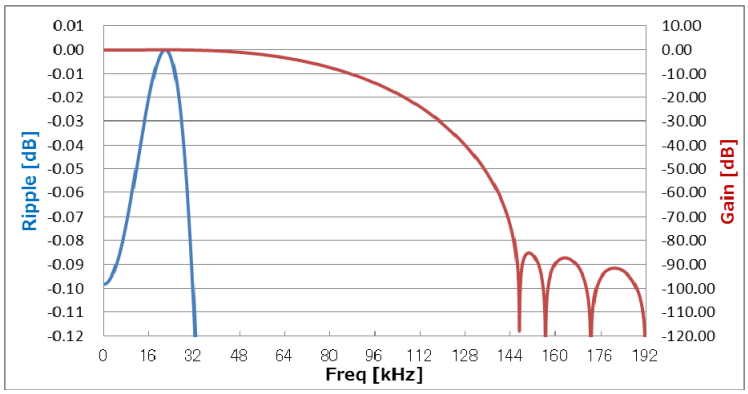


Figure 11. SLOW ROLL-OFF (fs=192kHz)

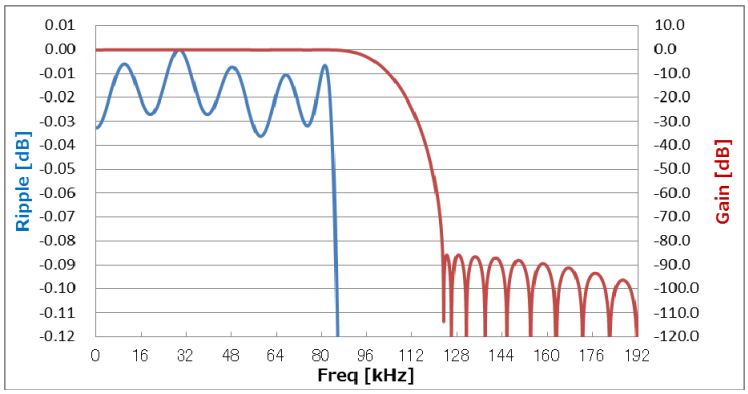


Figure 12. SHORT DELAY SHARP ROLL-OFF (fs=192kHz)

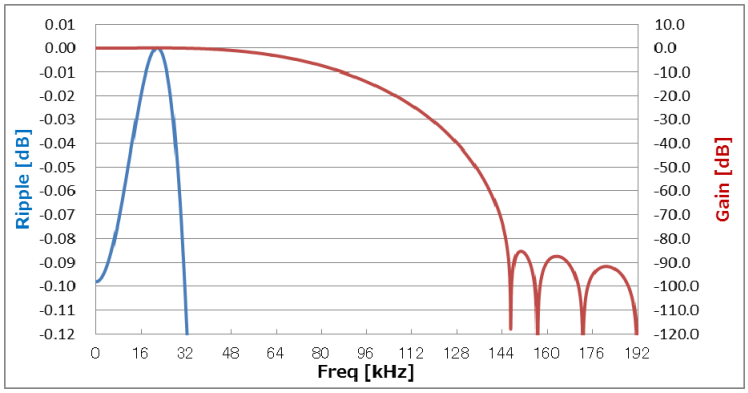


Figure 13. SHORT DELAY SLOW ROLL-OFF (fs=192kHz)

10. DC Characteristics

(Ta = −40~105°C; AVDD = 3.0~3.6V, DVDD = 1.7~1.98V (LDOE pin = "L"), 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V (LDOE pin = "L"), CPVDD = 3.0~3.6V, HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V(CPEN pin = "H"))

Parameter	Symbol	Min.	Typ.	Max.	Unit
DVDD=3.0V ~ 3.6V (LDOE pin= "H")					
High-Level Input Voltage (Note 27)	VIH	70%DVDD	-		V
Low-Level Input Voltage (Note 27)	VIL		-	30%DVDD	V
High-Level Output Voltage (Note 28) (Iout=−100μA)	VOH	DVDD−0.5	-		V
Low-Level Output Voltage (Note 28) (except SDA, INT pin: Iout= 100μA)	VOL	-		0.5	V
(SDA, INT pin: Iout= 3mA)	VOL	-		0.4	V
DVDD=1.7 ~ 1.98V (LDOE pin= "L")					
High-Level Input Voltage (Note 27)	VIH	80%DVDD	-		V
Low-Level Input Voltage (Note 27)	VIL	-	-	20%DVDD	V
High-Level Output Voltage (Note 28) (Iout=−100μA)	VOH	DVDD-0.3	-	-	V
Low-Level Output Voltage (Note 28) (except SDA, INT pin: Iout= 100μA)	VOL		-	0.3	V
(SDA, INT pin: Iout= 3mA)	VOL		-	20%DVDD	V
Input Leakage Current	Iin	-	-	±10	μA

Note 27. MCLK, PDN, BICK (Slave Mode), LRCK (Slave Mode), SPI, LDOE, CAD0/CSN, SCL/CCLK, CPEN, CAD1 (I^2C mode), TDMI (TDM mode), SDA/CDTI

Note 28. BICK (Master Mode), LRCK (Master Mode), SDTO1, SDTO2, TDMI (Stereo mode), INT, SDA/CDTI (I^2C mode), CDTO (4-wire mode)

Note 29. Pull-up resister of pins mentioned in INT pin and SDA pin should be connected to a voltage less than DVDD+0.3V.

11. Switching Characteristics

■ System Clocks

□ Slave Mode

[Ta = –40~+105°C; AVDD = 3.0~3.6V, 1.7~1.98V, (LDOE pin = "L"), DVDD = 3.0~3.6V, (LDOE pin = "H"), VDD18 = 1.7~1.98V, (LDOE pin = "L"), CPVDD = 3.0~3.6V, HVDD = CPOUT, (CPEN pin = "L"), / HVDD = 14.5V, (CPEN pin = "H"), C_L = 20pF]

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
(Note 30)					
Frequency	fMCLK	4.096	-	36.864	MHz
Pulse Duty Low	tMCLKL	40	-	60	%
Pulse Duty High	tMCLKH	40	-	60	%
LRCK Input Timing					
Stereo Mode					
Frequency					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	48	kHz
MCLK 384fs		8	-	48	kHz
Double Speed	fsd				
MCLK 256fs		48	-	96	kHz
MCLK 384fs		48	-	96	kHz
Quad Speed	fsq				
MCLK 128fs		96	-	192	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK	45	-	55	%
TDM128 Mode					
Frequency					
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Quad Speed	fsd	96	-	192	kHz
Pulse Width Low	tLRCKL	1/(128fsn)	-	-	s
		1/(128fsd)	-	-	s
		1/(128fsq)	-	-	s
Pulse Width High	tLRCKH	1/(128fsn)	-	-	s
		1/(128fsd)	-	-	s
		1/(128fsq)	-	-	s

Note 30. Refer to Table 4 for checking the available MCLK in each operation mode.

LRCK Input Timing (Continued)						
TDM256 Mode						
Frequency						
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Pulse Width Low	tLRCKL	1/(256fsn)	-	-	s
		1/(256fsd)	-	-	s
Pulse Width High	tLRCKH	1/(256fsn)	-	-	s
		1/(256fsd)	-	-	s
TDM512 Mode						
Frequency						
Normal Speed	fsn	8	-	48	kHz
Pulse Width Low	tLRCKL	1/(512fsn)	-	-	s
Pulse Width High	tLRCKH	1/(512fsn)	-	-	s
BICK Input Timing						
Stereo Mode						
Period	tBICK	-		-	
Normal Speed		1/(64fsn)	-	-	s
Double Speed		1/(64fsd)	-	-	s
Quad Speed		1/(64fsq)	-	-	s
Duty Cycle	dBICK	-	50	-	%
TDM128 Mode						
Period	tBICK				
Normal Speed		-	1/(128fsn)	-	s
Double Speed		-	1/(128fsd)	-	s
Quad Speed		-	1/(128fsq)	-	s
Pulse Width Low	tBICKL				
Normal Speed		66	-	-	ns
Double Speed		33	-	-	ns
Quad Speed		17	-	-	ns
Pulse Width High	tBICKH				
Normal Speed		66	-	-	ns
Double Speed		33	-	-	ns
Quad Speed		17	-	-	ns
TDM256 Mode						
Period	tBICK				
Normal Speed		-	1/(256fsn)	-	s
Double Speed		-	1/(256fsd)	-	s
Pulse Width Low	tBICKL				
Normal Speed		33	-	-	ns
Double Speed		17	-	-	ns
Pulse Width High	tBICKH				
Normal Speed		33	-	-	ns
Double Speed		17	-	-	ns
TDM512 Mode						
Period	tBICK				
Normal Speed		-	1/(512fsn)	-	s
Pulse Width Low	tBICKL				
Normal Speed		17	-	-	ns
Pulse Width High	tBICKH				
Normal Speed		17	-	-	ns

Note 31. BICK rising edge must not occur at the same time as LRCK edge.

□ **Master Mode**

(Ta = -40~+105°C; AVDD = 3.0~3.6V, 1.7~1.98V(LDOE pin = "L"), DVDD = 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V(LDOE pin = "L"), CPVDD = 3.0~3.6V, HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V(CPEN pin = "H"), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
(Note 32, Note 33)					
Frequency	fMCLK	4.096	-	36.864	MHz
Pulse Width Low	tMCLKL	40		60	%
Pulse Width High	tMCLKH	40		60	%
LRCK Output Timing					
Stereo Mode					
Frequency					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	48	kHz
MCLK 384fs		8	-	48	kHz
Double Speed	fsd				
MCLK 256fs		48	-	96	kHz
MCLK 384fs		48	-	96	
Quad Speed	fsq				
MCLK 128fs		96	-	192	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK		50		%
TDM128 Mode (Note 34)					
Frequency					
Normal Speed	fsn	8	-	48	kHz
Double Speed	Fsd	48	-	96	kHz
Quad Speed	fsq	96	-	192	kHz
Pulse Width Low	tLRCKL	-	1/(4fsn)	-	s
		-	1/(4fsd)	-	s
		-	1/(4fsq)	-	
Pulse Width High	tLRCKH	-	1/(4fsn)	-	s
		-	1/(4fsd)	-	s
		-	1/(4fsq)	-	

Note 32. Refer to Table 4 for checking the available MCLK in each operation mode.
Note 33. The minimum value of "Pulse Width Low/High" is inversely proportional to the MCLK frequency on the basis of "11ns" that is the minimum ones when MCLK is 36.864MHz.
ex) When MCLK = 18.432 MHz, the minimum value of "Pulse Width Low/High" is 11 × 36.864/18.432 = 22ns.

LRCK Output Timing (Continued)						
TDM256 Mode (Note 34)						
Frequency						
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Pulse Width Low	tLRCKL	-	1/(8fsn)	-	s
		-	1/(8fsd)	-	s
Pulse Width High	tLRCKH	-	1/(8fsn)	-	s
		-	1/(8fsd)	-	s
TDM512 Mode (Note 34)						
Frequency						
Normal Speed		8		48	kHz
Pulse Width Low	tLRCKL	-	1/(16fsn)	-	s
Pulse Width High	tLRCKH	-	1/(16sn)	-	s
BICK Output Timing						
Stereo Mode						
Period	tBICK	-	1/(64fs)	-	s
Duty Cycle	dBICK	-	50	-	%
TDM128 Mode						
Period	tBICK	-	1/(128fs)	-	s
Duty Cycle	dBICK	-	50	-	%
TDM256 Mode						
Period	tBICK	-	1/(256fs)	-	s
Duty Cycle (MCLK=512fs)	dBICK	-	50	-	%
Duty Cycle (MCLK=256fs)	dBICK	-	50	-	%
TDM512 Mode						
Period	tBICK	-	1/(512fn)	-	s
Duty Cycle	dBICK	-	50	-	%

Note 34. BICK duty depends on MCLK duty in TDM mode.

■ Audio Interface

□ **External Slave Mode**(Ta = -40~+105°C; AVDD = 3.0~3.6V, 1.7~1.98V(LDOE pin = "L"), DVDD = 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V(LDOE pin = "L"), CPVDD = 3.0~3.6V, HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V(CPEN pin = "H"), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed, Double Speed, Quad Speed Mode					
DVDD=1.7V~1.98V					
LRCK to BICK "↑"	tLRB	30	-	-	ns
BICK "↑" to LRCK	tBLR	30	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	30	ns
BICK "↓" to SDTO	tBSD	-	-	30	ns
DVDD=3.0V~3.6V					
LRCK to BICK "↑"	tLRB	33	-	-	ns
BICK "↑" to LRCK	tBLR	33	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	28	ns
BICK "↓" to SDTO	tBSD	-	-	28	ns
TDM128, (Normal Speed Mode, Double Speed Mode), TDM256 (Normal Speed Mode)					
DVDD=1.7V~1.98V					
LRCK to BICK "↑"	tLRB	33	-	-	ns
BICK "↑" to LRCK	tBLR	33	-	-	ns
BICK "↑" to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns
DVDD=3.0V~3.6V					
LRCK to BICK "↑"	tLRB	33	-	-	ns
BICK "↑" to LRCK	tBLR	33	-	-	ns
BICK "↓" to SDTO	tBSD	-	-	14	ns
TDMI Setup time to BICK "↑"	tSDS	5	-		ns
TDMI Hold time to BICK "↑"	tSDH	5	-		ns
TDM128 Mode					
Quad Speed Mode					
LRCK to BICK "↑"	tLRB	16	-	-	ns
BICK "↑" to LRCK	tBLR	16	-	-	ns
BICK "↑" to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns
TDM256 Mode					
Double Speed Mode					
LRCK to BICK "↑"	tLRB	16	-	-	ns
BICK "↑" to LRCK	tBLR	16	-	-	ns
BICK "↑" to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns
TDM512 Mode					
Normal Speed Mode					
LRCK to BICK "↑"	tLRB	16	-	-	ns
BICK "↑" to LRCK	tBLR	16	-	-	ns
BICK "↑" to SDTO	tBSDD	5	-	30	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns

Note 35. It is a case that when the duty of MCLK is 50%.

□ **External Master Mode**

(Ta=–40~+105°C; AVDD = 3.0~3.6V, 1.7~1.98V(LDOE pin = "L"), DVDD = 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V(LDOE pin = "L"), CPVDD = 3.0~3.6V, HVDD = CPOUT(CPEN pin = "L") / HVDD = 14.5V(CPEN pin = "H"), C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed, Double Speed, Quad Speed Mode					
DVDD=1.7V~1.98V					
BICK "↓" to LRCK	tMBLR	-10	-	10	ns
LRCK to SDTO (MSB Justified)	tLRS	-20	-	20	ns
BICK "↓" to SDTO	tBSD	-20	-	20	ns
DVDD=3.0V~3.6V					
BICK "↓" to LRCK	tMBLR	-10	-	10	ns
LRCK to SDTO (MSB Justified)	tLRS	-20	-	20	ns
BICK "↓" to SDTO	tBSD	-20	-	20	ns
TDM128, TDM256 Mode, TDM512 Mode					
Normal Speed, Double Speed, Quad Speed Mode					
BICK "↓" to LRCK	tMBLR	-6		6	ns
BICK "↓" to SDTO	tBSD	-10	-	10	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns

■ I²C Bus, Power-down, Reset

(Ta = –40~105°C; AVDD = 3.0~3.6V, DVDD = 1.7~1.98V (LDOE pin = "L"), 3.0~3.6V (LDOE pin = "H"), VDD18 = 1.7~1.98V (LDOE pin = "L")), CPVDD=3.0～3.6V, HVDD = 14.5V (CPEN pin = "H"), HVDD = CPOUT(CPEN pin = "L")

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (4-wire Mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
CCLK pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CCSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 36)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 36)	tCSH	50	-	-	ns
CCLK "↓" to CDTO, (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTO (Hi-z), (at Read Command), (Note 37)	tCCZ	-	-	70	ns
Control Interface Timing (I2C Bus):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time, (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling, (Note 38)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width, (Note 39)	tAPD	150	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns
RSTN bit "1" to SDTO valid (CPEN pin = "H"), (Note 40)	tRSTNV	-	2262	-	1/fs
RSTN bit "1" to SDTO valid (CPEN pin = "L"), (Note 40)	tRSTNV	-	3224	-	1/fs

Note 36. CCLK rising edge must not occur at the same time as CSN edge.

Note 37. Hi-z level is defined at the point when the CDTO pin voltage is changed for 10% from "L" level while it is pulled up to DVDD by 1kΩ.

Note 38. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 39. The AK5736 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must be held "L", for more than 150ns for a certain reset. The AK5736 is not reset by an "L" pulse less than 30ns.

Note 40. This cycle is the number of LRCK rising edges from writing RSTN bit = "1" when MSN bit is set to "0". It will be -3/fs times shorter if MSN bit is set to "1".

■ Timing Diagram

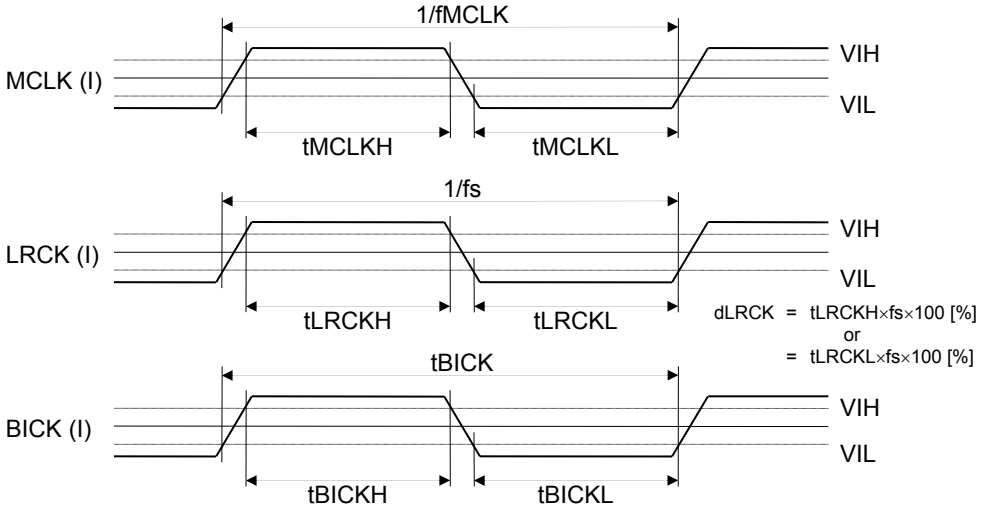


Figure 14. Clock Timing (External Slave Mode)

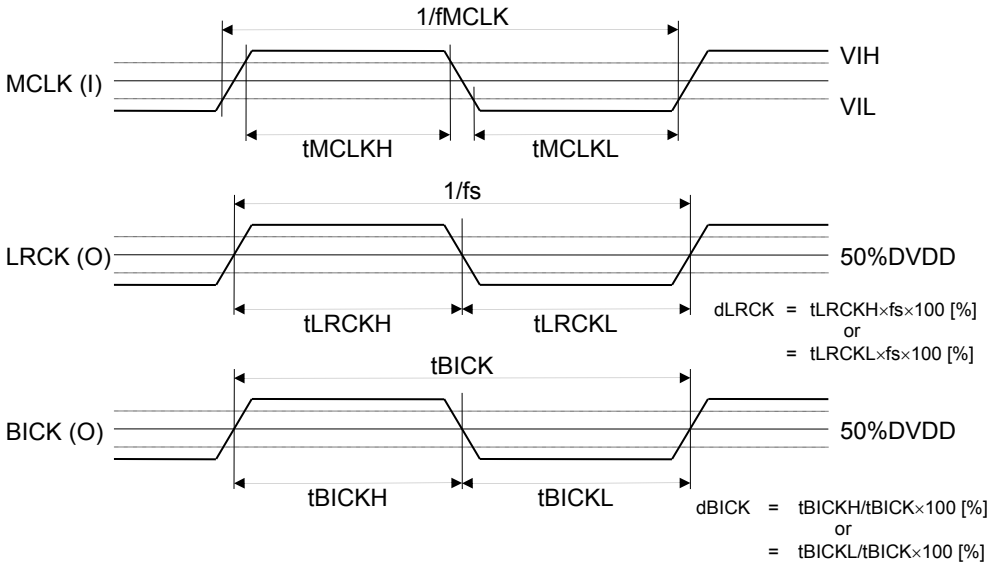


Figure 15. Clock Timing (External Master Mode)

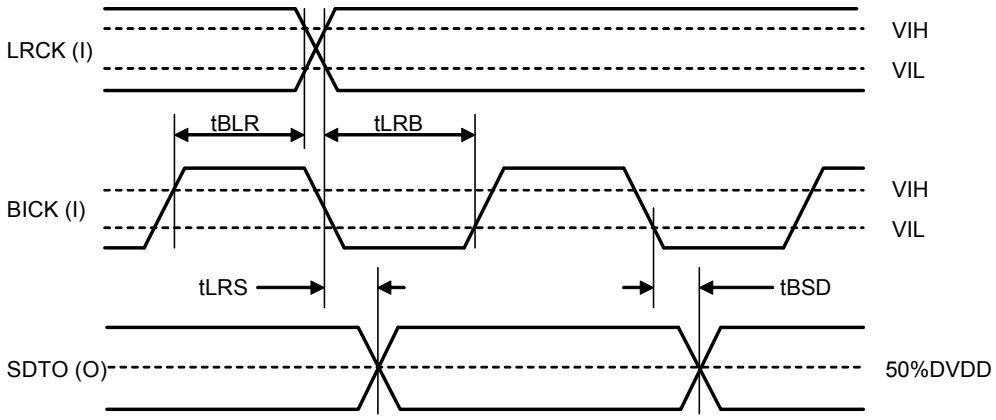


Figure 16. Audio Interface Timing (External Slave Mode)

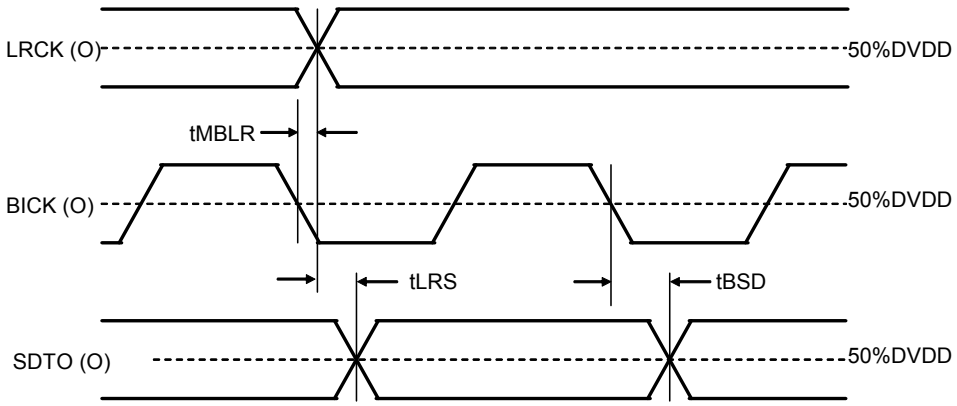


Figure 17. Audio Interface Timing (External Master Mode)

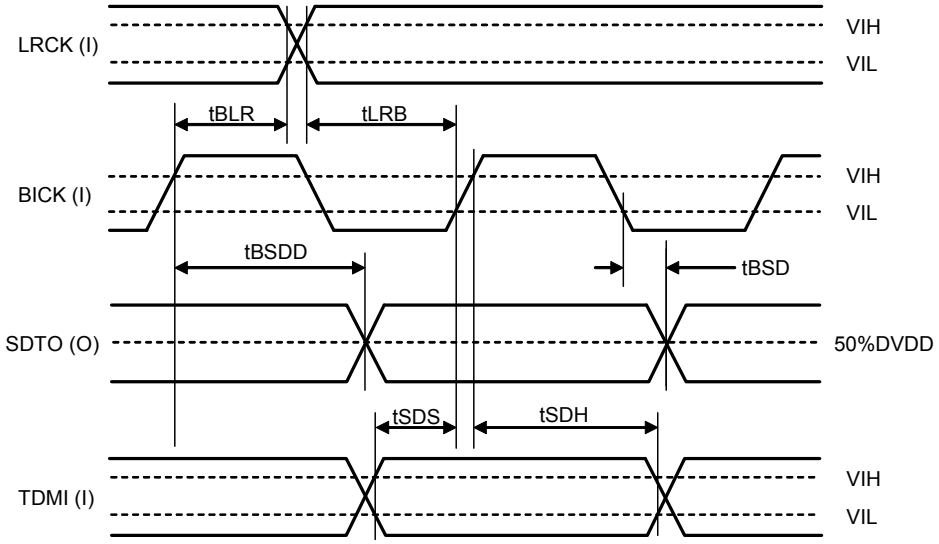


Figure 18. Audio Interface Timing (TDM mode & Slave mode)

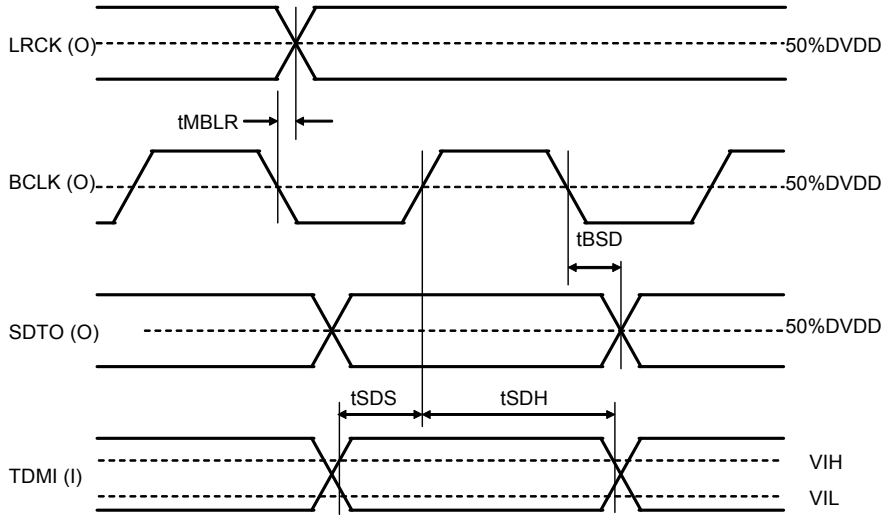


Figure 19. Audio Interface Timing (TDM mode & Master mode)

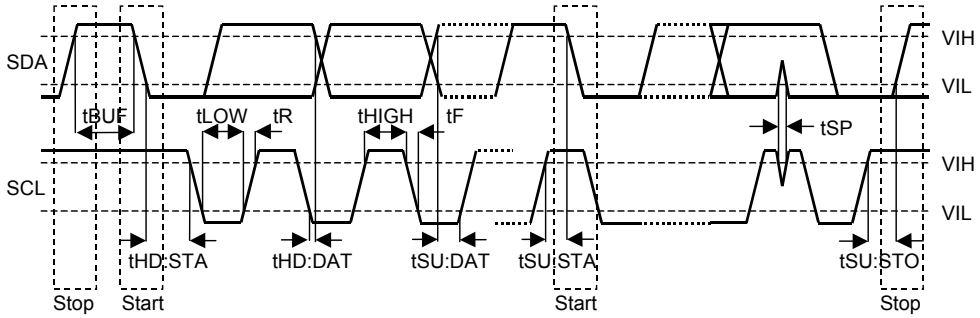


Figure 20. I^{2}C Bus Timing

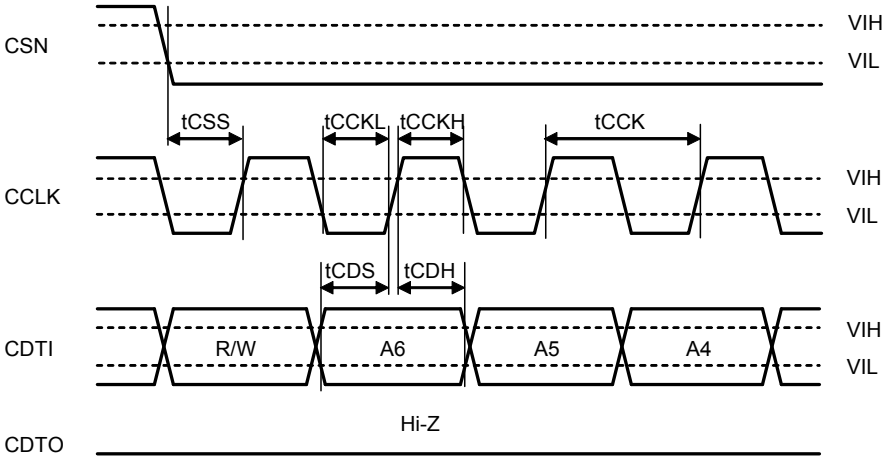


Figure 21. WRITE/READ Command Input Timing (4-wire serial mode)

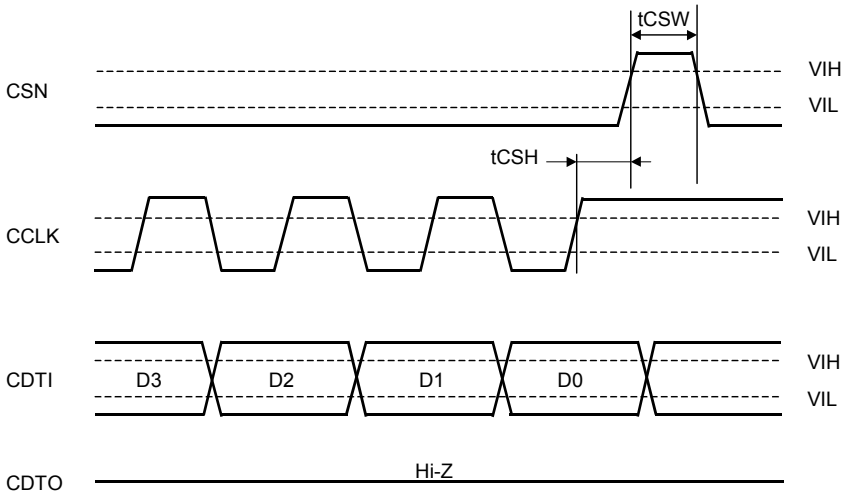


Figure 22. WRITE Data Input Timing (4-wire serial mode)

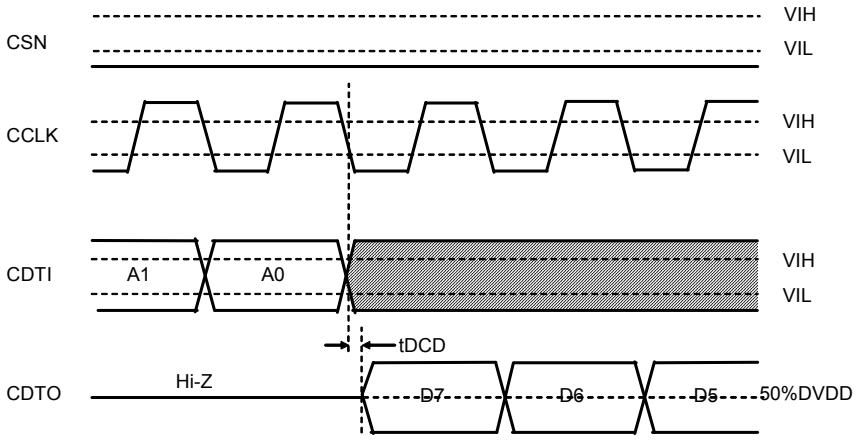


Figure 23. READ Rata output timing 1 (4-wire serial mode)

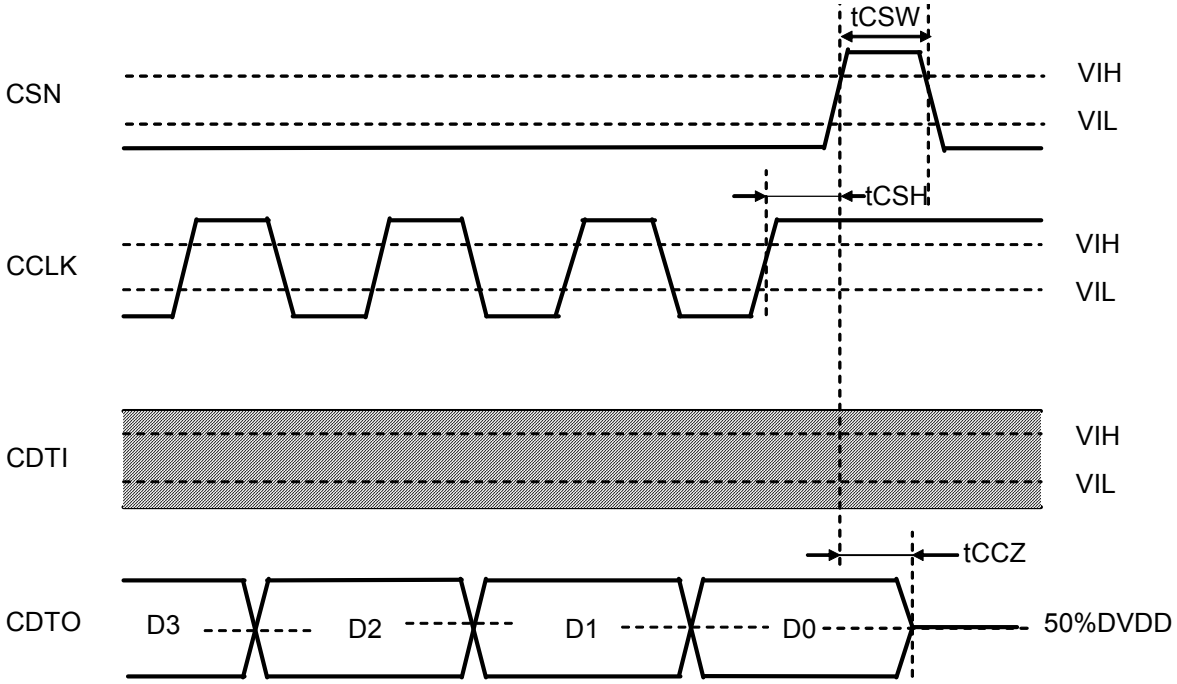


Figure 24. READ Data Output Timing 2 (4-wire serial mode)

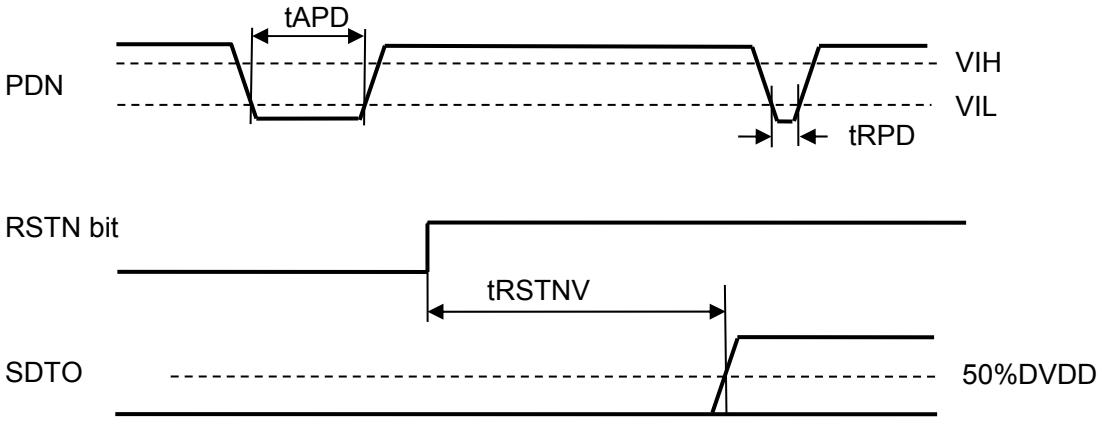


Figure 25. Power-down & Reset Timing

12. Functional Descriptions

■ Digital Core Power Supply

The digital core of the AK5736 operates with a 1.8V power supply. This 1.8V is generated from DVDD, (3.3V), by an internal LDO regulator. The LDO is powered ON by setting the LDOE pin = "H" and OFF by setting the LDOE pin = "L". When using a 1.8V power supply for DVDD, set the LDOE pin = "L" and input the 1.8V power to the VDD18 pin. A wait time more than 2msec is necessary to access control registers after setting the PDN pin = "L" → "H" for power-up.

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the MSN bit. ["1" = Master Mode, "0" = Slave Mode (default)]. In Master mode, the LRCK pin and the BICK pin become output pins. In Slave mode, the LRCK pin and the BICK pins become input pins.

Clock Mode	MSN bit	Clock Pin Status			Connection Diagram
		MCLK	BICK	LRCK	
Master	1	In	Out	Out	Figure 26
Slave	0	In	In	In	Figure 27

Table 1. Clock Mode

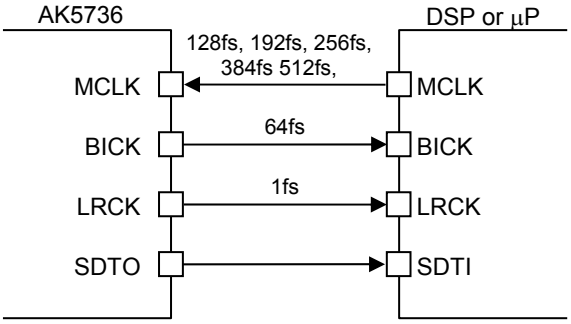


Figure 26: Master Mode

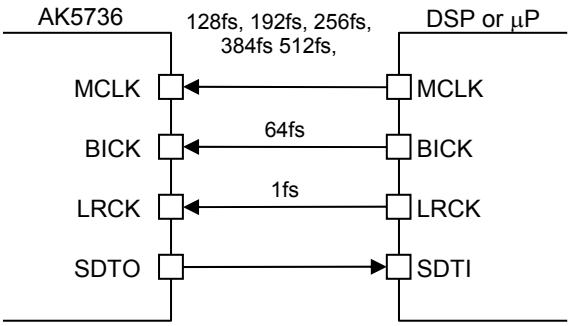


Figure 27. Slave Mode

■ System Clock

System clock of the AK5736 is controlled by CKS2-0 bits and FS2-0 bits.

CKS2 bit	CKS1 bit	CKS0 bit	Clock Speed	
0	0	0	128fs	
0	0	1	192fs	
0	1	0	256fs	
0	1	1	384fs	
1	0	0	512fs	(default)

Table2: Master Clock Control

FS2 bit	FS1 bit	FS0 bit	Sampling Rate	
0	0	0	8kHz ≤ fs ≤ 12kHz	
0	0	1	12kHz < fs ≤ 24kHz	
0	1	0	24kHz < fs ≤ 48kHz	(default)
0	1	1	48kHz < fs ≤ 96kHz	
1	0	0	96kHz < fs ≤ 192kHz	

Table 3. Master Mode Setting (Serial Control Mode)

LRCK	MCLK (MHz)				
fs	128fs	192fs	256fs	384fs	512fs
8kHz	-	-	-	-	4.096
12kHz	-	-	-	-	6.144
16kHz	-	-	4.096	6.144	8.192
24kHz	-	-	6.144	9.216	12.288
32kHz	-	-	8.192	12.288	16.384
44.1kHz	-	-	11.2896	16.9344	22.5792
48kHz	-	-	12.288	18.432	24.576
72kHz	-	-	18.432	27.648	-
96kHz	-	-	24.576	36.864	-
144kHz	18.432	27.648	-	-	-
192kHz	24.576	36.864	-	-	-

(-: Not available)

Table 4. System Clock Example

Input 512fs MCLK if the sampling frequency is 8kHz ~ 12kHz.
Relationship between MCLK and TDM mode in TDM master mode is shown in Table 5. The MCLK is divided by 2 and output as BICK in modes described with a white dot. In these modes, BICK duty cycle is typically 50%. In modes described with a black dot, BICK duty cycle depends on the duty cycle of the MCLK input. Modes described with, "-", are not available since the clock frequency of MCKI input is slower than BICK output.

MCLK Speed	TDM128	TDM256	TDM512
128fs	●	-	-
192fs	-	-	-
256fs	○	●	-
384fs	-	-	-
512fs	○	○	●

(-: Not available)

Table 5. Relationship between MCKI and TDM Modes

■ Clock Stop Detection Circuit

The AK5736 has MCLK, BICK and LRCK stop detection circuits. The MCLK stop detection circuit works when the MCLK frequency drops under 660kHz. In this case, internal circuits except for clock detection circuits, control registers, bias generation circuit and LDO, (when LDOE pin = "H"), are stopped.
BICK, LRCK stop detection circuits work when BICK or LRCK is stopped and MCLK is input for 2048 cycles. In this case, internal circuits except for clock detection circuits, control registers, the bias generation circuit, and LDO, (when LDOE pin = "H"), are stopped.

■ Audio Interface Formats

Eight types of audio interface formats are selectable with the DIF bit and TDM1-0 bits. In all modes the serial data format is MSB first, 2's complement.

Available audio interface formats are different depending on the operation mode, (Normal, Double or Quad). Modes described as, "Yes", in the table below are available in each mode.
In TDM128 or TDM256 mode, the AK5736 supports up to 8ch outputs, (6ch AK5736 + 2ch external device). In TDM512 mode, the AK5736 supports up to 16ch outputs (6ch AK5736 + 10ch external device).
*SDTO1~3 data should be captured on a rising edge of BICK.

Mode	DIF bit	TDM1 bit	TDM0 bit	BICK	Normal	Double	Quad	Data Format	
0	0	0	0	64fs	Yes	Yes	Yes	Stereo Mode (I^2S)	(default)
1	0	0	1	128fs	Yes	Yes	Yes	TDM128 Mode(I^2S)	
2	0	1	0	256fs	Yes	Yes	-	TDM256 Mode(I^2S)	
3	0	1	1	512fs	Yes	-	-	TDM512 Mode(I^2S)	
4	1	0	0	64fs	Yes	Yes	Yes	Stereo Mode (MSB Justified)	
5	1	0	1	128fs	Yes	Yes	Yes	TDM128 Mode (MSB Justified)	
6	1	1	0	256fs	Yes	Yes	-	TDM256 Mode (MSB Justified)	
7	1	1	1	512fs	Yes	-	-	TDM512 Mode (MSB Justified)	

(-: Not available)

Table 6. Audio Data Interface Modes Setting

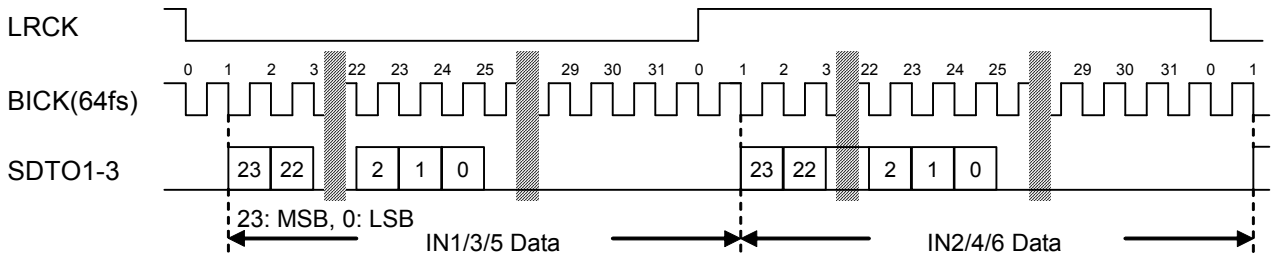


Figure 28. Mode 0 Timing (Stereo Mode (I^2S))

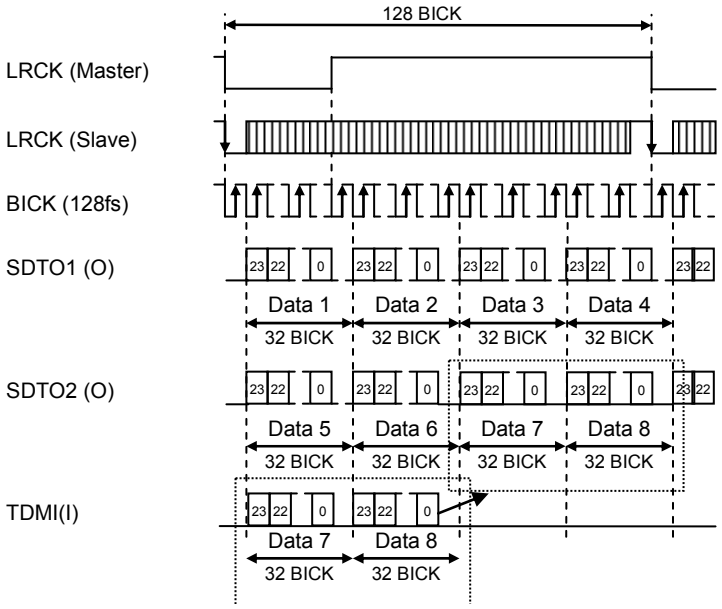


Figure 29 Mode 1 Timing (TDM128 Mode, I²S Compatible)

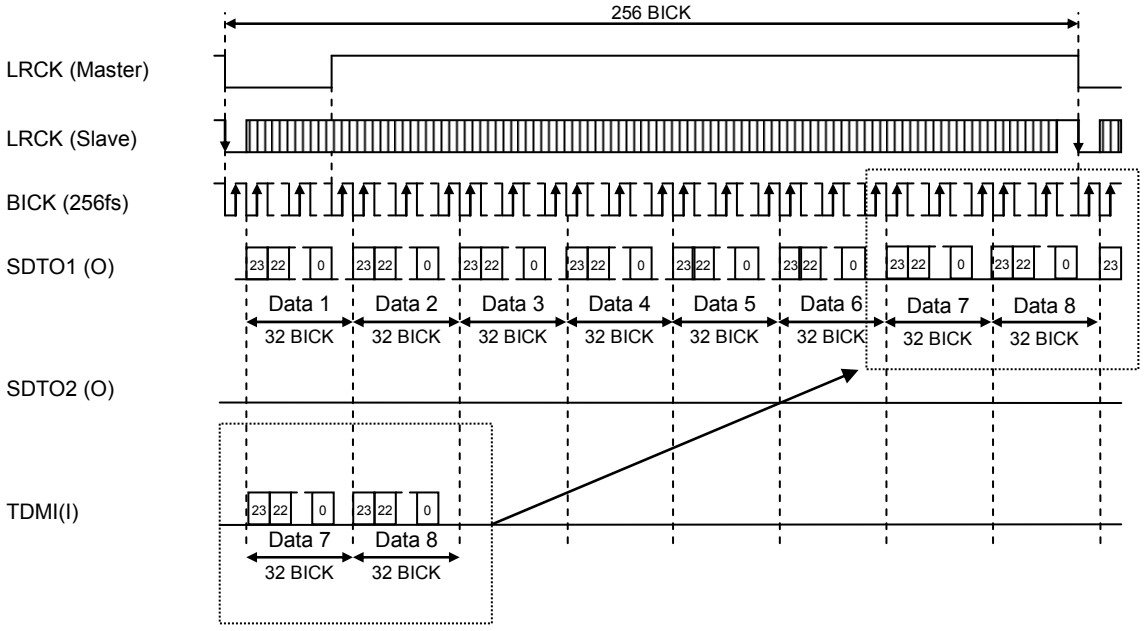


Figure 30. Mode2 Timing (TDM256 Mode, I²S Compatible)

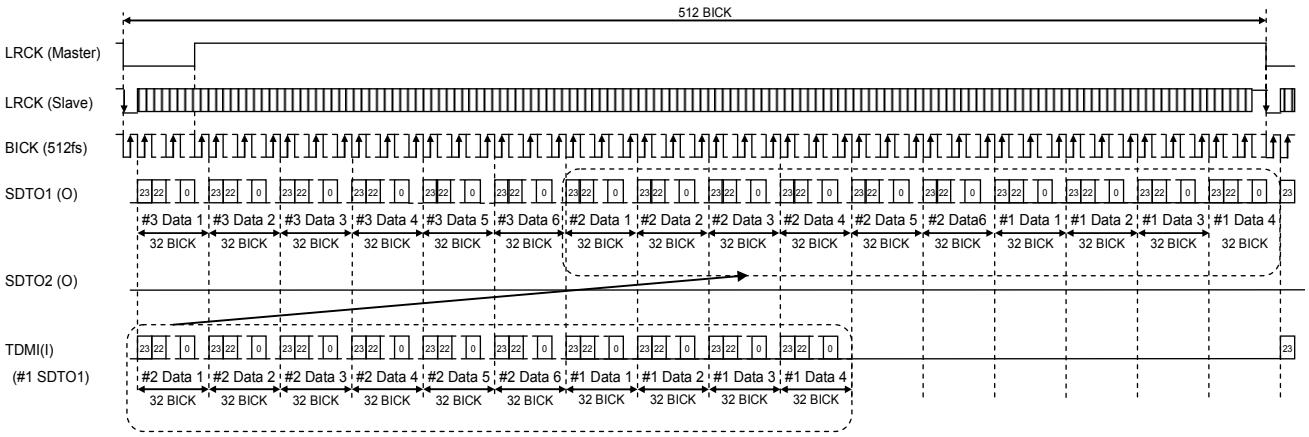


Figure 31. Mode3 Timing, (TDM512 Mode, I²S Compatible)

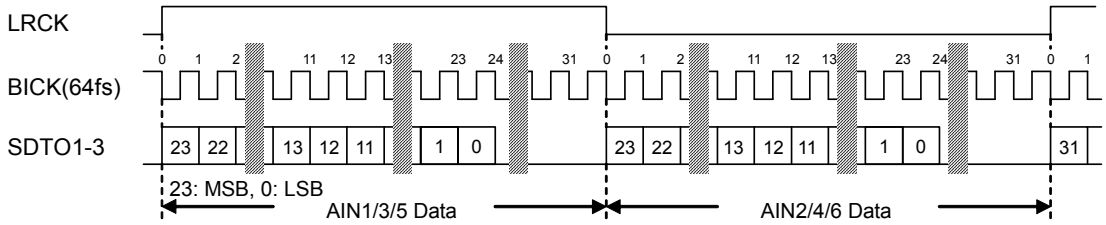


Figure 32. Mode4 Timing, (Stereo Mode, MSB Justified)

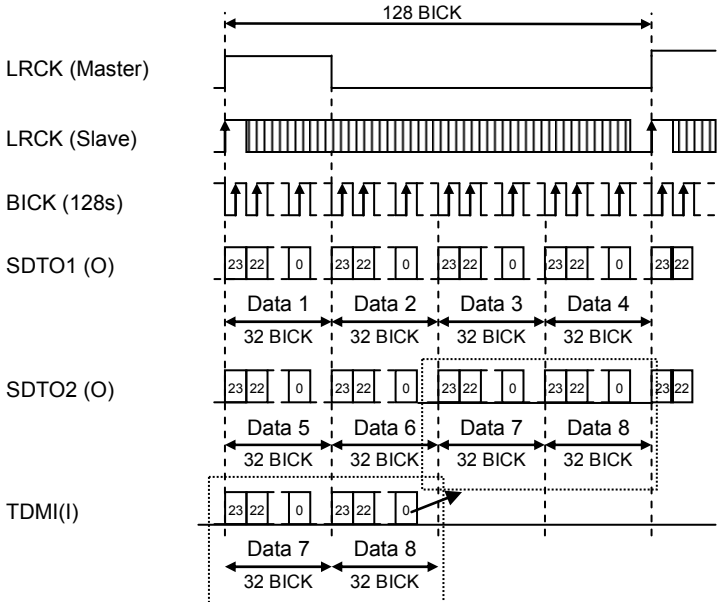


Figure 33. Mode 5 Timing, (TDM128 mode, MSB justified)

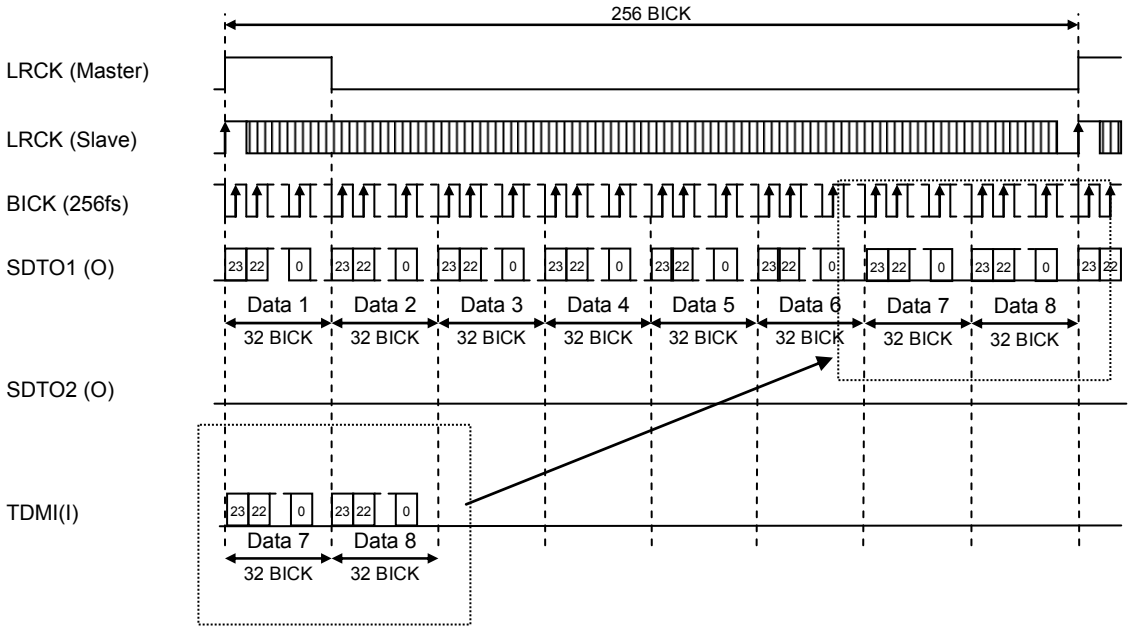


Figure 34. Mode 6 Timing, (TDM256 Mode, MSB Justified)

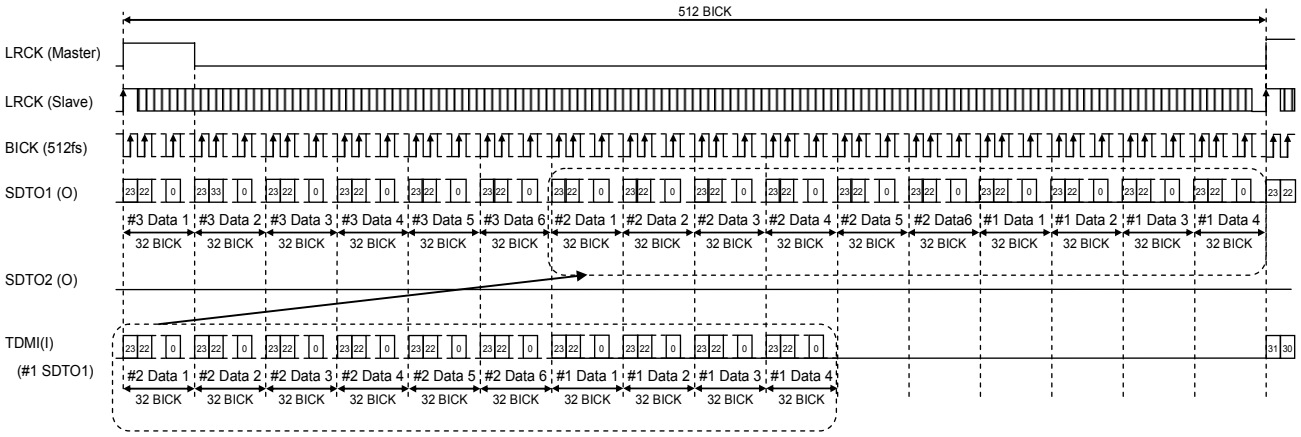


Figure 35. Mode7 Timing, (TDM512 Mode (MSB Justified))

■ Synchronization with Audio System (SYNCDET)

The AK5736 has a SYNCDET circuit for phase synchronization of the data output since it is assumed that multiple AK5736's will be used.

When the clock frequency is changed during operation, phase mismatch may occur between external LRCK and data transferring clock that has the same frequency as the internal LRCK generated from external LRCK.
The SYNCDET circuit resets the internal counter and adjusts the phase between LRCK and FsCLK automatically. Then the clocks for the charge pump, ΔΣADC and SARADC may stop and detect errors.

Change the operation clock setting when RSTN bit = "0" and stable clock should be input while RSTN bit = "1".

■ Cascade Connection in TDM Mode

The AK5736 supports a cascade connection of two devices in TDM512 mode. Figure 36 shows a connection example. All A/D converted data of connected AK5736's is output from the SDTO pin of the last AK5736 via cascade connection.

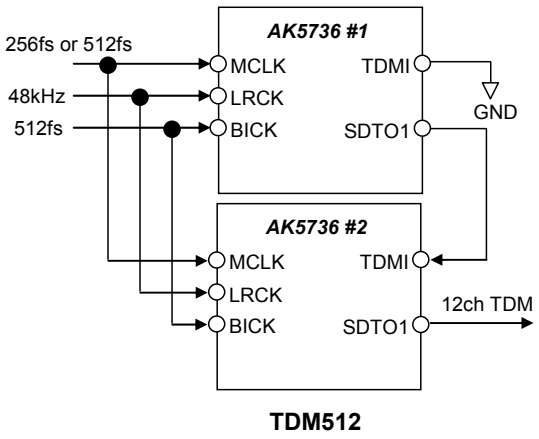


Figure 36. Cascade Connection

■ Digital HPF

The AK5736 has a digital high-pass filter (HPF) for DC offset cancellation. The cut-off frequency of the high-pass filter is 2.0Hz with the maximum sampling frequency in each operation mode that is set by FS[2:0] bits.

<FS[2:0] bits = “000”> When fs: 8kHz ≤ fs ≤ 12kHz,
Cutoff Frequency fc = 2Hz @ fs=12kHz

< FS[2:0] bits = “001”> When fs: 12kHz < fs ≤ 24kHz,
Cutoff Frequency fc = 2Hz @ fs=24kHz

< FS[2:0] bits = “010”> When fs: 24kHz < fs ≤ 48kHz,
Cutoff Frequency fc = 2Hz @ fs=48kHz

< FS[2:0] bits = “011”> When fs: 48kHz < fs ≤ 96kHz,
Cutoff Frequency fc = 2Hz @ fs=96kHz

< FS[2:0] bits = “100”> When fs: 96kHz < fs ≤ 192kHz,
Cutoff Frequency fc = 2Hz @ fs=192kHz

The cut-off frequency, (fc), is proportional to the sampling frequency, (fs), in each setting of FS[2:0] bits. For example: When FS[2:0] bits = “011” and fs= 44.1kHz, the cutoff frequency “fc” = 2Hz x 44.1/48 = 1.84Hz.

■ Digital Filter Setting

The AK5736 has four types of digital filters. They are selected by the SD bit and SLOW bit.

SD bit	SLOW bit	Filter	
0	0	Sharp Roll-off Filter	(default)
0	1	Slow Roll-off Filter	
1	0	Short Delay Sharp Roll-off Filter	
1	1	Short Delay Slow Roll-off Filter	

Table 7. Digital Filter Setting

■ Digital Volume

The AK5736 has a digital volume setting, (168 levels, 1dB per step), that can control each channel independently. The digital volume of each channel can be set via the register ATT17-10 bits (1ch), ATT27-20 bits (2ch), …, ATT67-60 bits (6ch), (Table 8). A value that is set during RSTN bit = "0" will be the default value of the digital volume. The AK5736 starts operation from this default value by setting RSTN bit = "1". ATT* bits, (*=1~6ch), setting is initialized and set to ATT* bits, (*=1~6ch)=34H by setting the PDN pin to "L".

ATT* bits (*1~6ch)	Volume	
00H	52dB	
01H	51dB	
:	:	
32H	2dB	
33H	1dB	
34H	0dB	(default)
35H	-1dB	
36H	-2dB	
37H	-3dB	
:	:	
A6H	-114dB	
A7H	-115dB	
A8H	MUTE	
A9H	MUTE	
:	MUTE	
FFH	MUTE	

Table 8. Attenuation Level of Digital Attenuator

Digital volume transition time is set by ATS[1:0] bits (Table 9). Volume transition by ATT* bits (*=1~6ch) is a soft transition, thus no switching noise occurs during the transition.

Mode	ATS1	ATS0	ATT speed	
0	0	0	5376/fs	(default)
1	0	1	2688/fs	
2	1	0	672/fs	
3	1	1	336/fs	

Table 9. Transition Time between Set Values of ATT* bits (*=1~6ch)

In Mode0, the volume transition by ATT* bits, (*=1~6ch), has 5376/fs in soft transition. It takes 5376/fs (112ms@fs=48kHz), to change the volume from 00H, (+52dB), to FFH, (MUTE).

■ Power Up/Down Sequence Example

In slave mode, the reset state is released by setting RSTN bit = “1” after MCLK, BICK and LRCK inputs following the PDN pin = “H”. After that, power down state is released by detecting a rising edge of LRCK following a rising edge of MCLK.
In master mode, the reset state is released by detecting a rising the edge of MCLK following RSTN bit = “1” and MCLK input after setting the PDN pin = “H”.
After releasing power down state, the initialization cycle starts. When the CPEN pin = ”L”, output data “SDTO” is determined in 3324 × 1/fs, (in slave mode), or 3321 × 1/fs, (in master mode), after setting RSTN bit = “1”. When the CPEN pin = “H”, the output data “SDTO” is determined in 2262 × 1/fs, (in slave mode), or 2259 × 1/fs, (in master mode), after setting RSTN bit = “1”. During initialization, the ADC output data is “0” in 2’s complement and it settles to the data corresponding to the analog input signal after the initialization, (It takes about the group delay time).

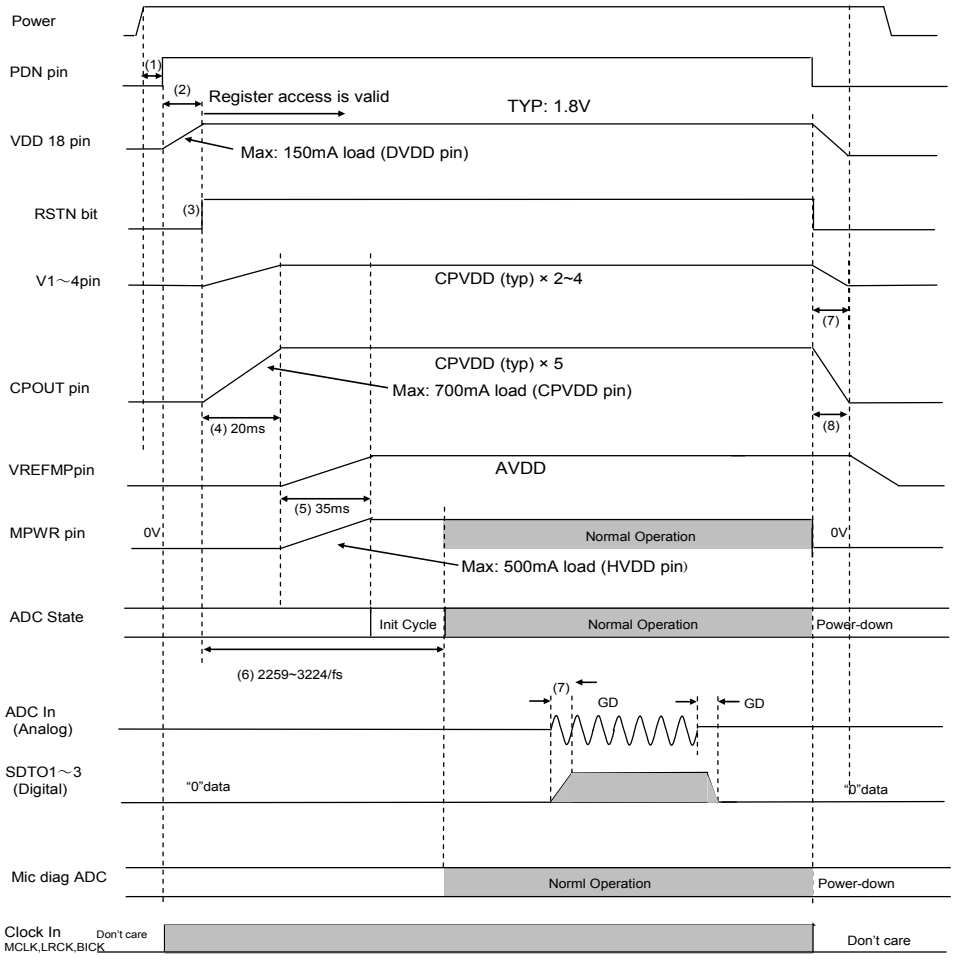


Figure 37. Power Up/Down Sequence, (LDOE pin = “H”, CPEN pin = “L”)

(1) Set the PDN pin = “L” → “H” after powering on all the power supplies. The PDN pin must be held at “L” at least 150ns before setting to “H” after all power is supplied.
(2) Internal LDO is powered up after setting the PDN = “H”, and register access will be available in 2ms.
(3) After LDO starts up, set RSTN bit = "1" after setting necessary registers such as for clock, audio interface, error diagnosis function, and the output level of the MIC bias voltage settings.

(4) The internal charge pump powers up after 20msec when the CPEN pin = “L” and fs = 48kHz. With a 48kHz based sampling frequency, 12kHz, 24kHz, 48kHz, 96kHz, and 192kHz power up time is 20msec. With a 32kHz based sampling frequency, 8kHz, 16kHz, 32kHz, 72kHz, and 144kHz time becomes 30msec. When fs = 44.1kHz, time is 21.8ms.
The internal charge pump will not be powered up when the CPEN pin = “H”. This power-up time is not necessary when not using the internal charge pump and supplying HVDD externally.

(5) When fs = 48kHz, the MPWR pin and the VREFMP pin rise in 35ms after the internal charge pump is powered up. With a 48kHz based sampling frequency,12kHz, 24kHz, 48kHz, 96kHz, and 192kHz power up time is 35msec. With a 32kHz based sampling frequency, 8kHz, 16kHz, 32kHz, 72kHz and 144kHz, this becomes 52.5msec. When fs = 44.1kHz, the time is 38.1ms.

(6) The AK5736 outputs data and error detections become enabled after 67ms, (max. @fs=48kHz), by setting the RSTN bit = “1” when the CPEN pin = “L”. It will be after 47ms (max. @fs=48kHz) if the CPEN pin = “H”.

(7) There is a Group Delay, (GD), on the SDTO output from the ADC input.

(8) All circuits are powered down by setting the PDN pin = “H” → “L”.

Note: The wait time of, (7), is inversely proportional to the maximum sampling frequency, “fs”, of the operation mode set by FS[2:0] bits. The wait time until data is output is defined as the time from the input timing of the analog signal to the output timing of the MSB at L channel of the SDTO output.

Example: When the CPEN pin = "L" and Fs = 32 kHz, a wait time of 67 ms × (48/32) = 100.5 ms is required. The reference wait time at 48 kHz is 67 ms. When the CPEN pin = "L" and fs = 16 kHz, a wait time of 79 ms × (24/16) = 118.5 ms is required. The reference wait time at 24 kHz is 79 ms.

FS2	FS1	FS0	fs	Wait time until Output
0	0	0	8kHz ≤ fs ≤ 12kHz	103 ms @ 12kHz
0	0	1	12kHz < fs ≤ 24kHz	79 ms @ 24kHz
0	1	0	24kHz < fs ≤ 48kHz	67 ms @ 48kHz
0	1	1	48kHz < fs ≤ 96kHz	61 ms @ 96kHz
1	0	0	98kHz < fs ≤ 192kHz	58 ms @ 192kHz

Table 10. Wait Time until Data is Output, (CPEN pin = “L”)

FS2	FS1	FS0	fs	Wait time until Output
0	0	0	8kHz ≤ fs ≤ 12kHz	83 ms @ 12kHz
0	0	1	12kHz < fs ≤ 24kHz	59 ms @ 24kHz
0	1	0	24kHz < fs ≤ 48kHz	47 ms @ 48kHz
0	1	1	48kHz < fs ≤ 96kHz	41 ms @ 96kHz
1	0	0	98kHz < fs ≤ 192kHz	38 ms @ 192kHz

Table 11. Wait Time until Data is Output, (CPEN pin = “H”)

■ Analog Input Connection

The analog input connection method is shown in this section. The AK5736 supports line and microphone inputs. 6 differential analog input channels are available. AC or DC connections are selectable at each channel by setting the AC6-1 bits. Analog signals are input into the PGA via differential input pins of each channel. The voltage difference of IN*P and IN*N pins will be the input voltage (* = 1~6). The ADC input range is 2.0Vrms (typ.).

The Input DC operating point of the IN*P pin must be higher than the IN*N pin.

1. Microphone Inputs

The connection method for a microphone input application and the AK5736 is shown below. Please follow the diagram of the connected ECM for the MIC bias voltage and the baias voltage. The AK5736 is capable of supplying 5 ~ 9V, (in 0.5V steps). Voltage is supplied from the MPWR pin. In the use case of connecting multiple microphones, you must not exceed the maximum current of the MIC Power Supply.

1-1: Electric Condenser Microphone (ECM) Differential Input (DC Connection)

Set AC6-1 bits = “0” when using a DC connection. Normally, the output signal amplitude is proportional to MIC bias voltage with an electric capacitor microphone (ECM). When supplying 9V to the MIC bias voltage, the 2Vrms differential signal can be output from the ECM. In this case, 1Vrms, (2.8V p-p), is input to both the IN*P pin and the IN*N pin of the AK5736. Common voltage depends on the connected ECM but normally it will be equivalent to, “2/3 x MIC bias voltage”, at the IN*P pin and, “1/3 x MIC bias voltage”, at the IN*N pin.

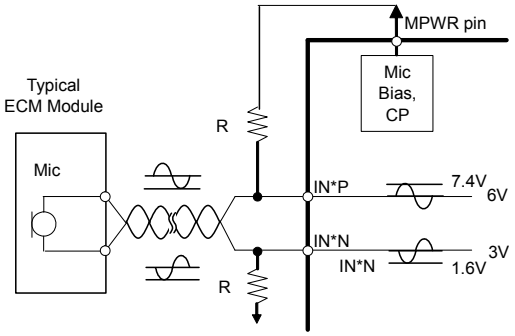


Figure 38. Differential Input DC Connection, (IN*P/N pins)

1-2: Dynamic MIC Differential Input, (AC Connection)

Set AC6-1 bits = “1” when using AC connection. Common voltage is 2.5V, (typ.), and generated internally.

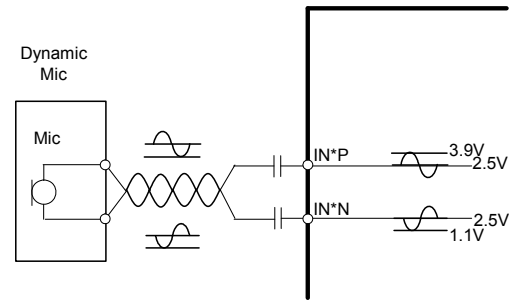


Figure 39. Differential Input AC Connection (IN*P/N pins)

1-3: ECM Single-ended Input (DC connection)

Set AC6-1 bits = “0” when using a DC connection. With single-ended input, signal amplitude will be half of the differential input since a signal is input to the IN*P pin. The available input signal amplitude of the IN*P pin is 1Vrms (typ.) Common voltage depends on the connected ECM but normally it will be about “1/2 x MIC bias voltage”.

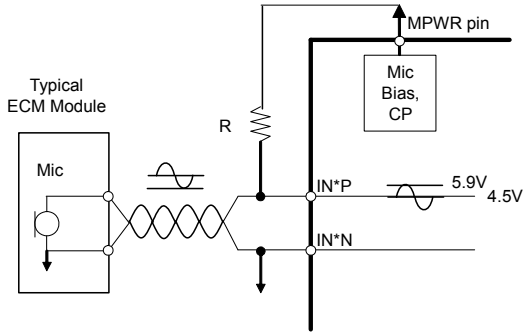


Figure 40. Single-ended Input DC Connection, (IN*P/N pins)

1-4: Dyamic MIC Single-ended Input, (AC Connection)

Set AC6-1 bits = “1” when using an AC connection. Common voltage is 2.5V, (typ.) and generated internally.

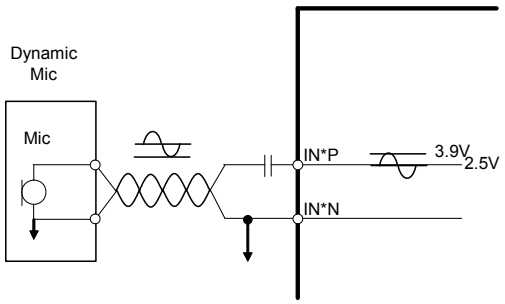


Figure 41. Single-ended Input AC Connection, (IN*P/N pins)

2. Line Input

Normally the output amplitude of an automotive power amplifier is about 10 Vrms (differential), and common voltage is about 7.2V, (assuming a BTL connection with a 14.4 V battery). In this case, the input signal amplitude of each IN*P pin and IN*N pin is 5 Vrms, (14.14 V p-p), and common voltage is 7.2 V. The amplitude range is from, “(7.2V + 7.07V) = +14.27V ”, to, “(7.2 V − 7.07 V) = 0.13 V”. External resistance values, (R1 and R2), should be adjusted so that the input signal to IN*P pin and IN*N pin will not exceed 2.0Vrms.

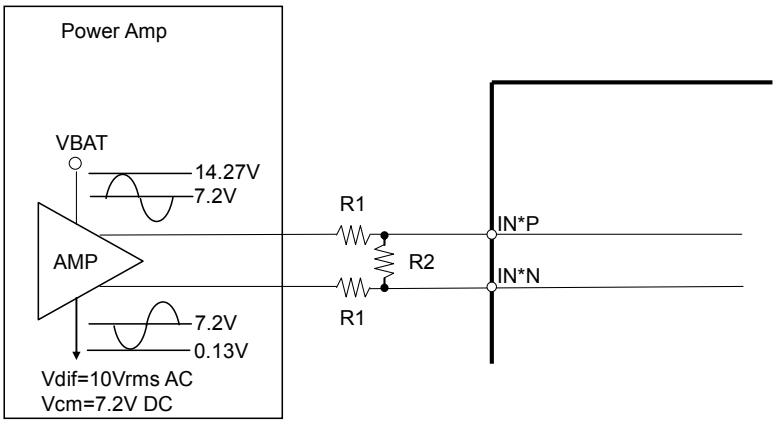


Figure 42. Differential Input DC Connection, (IN*P/N pins)

■ Full Scale Clip Function

As shown in Figure 43, the output becomes full scale code when the analog input is over 0dBFS.

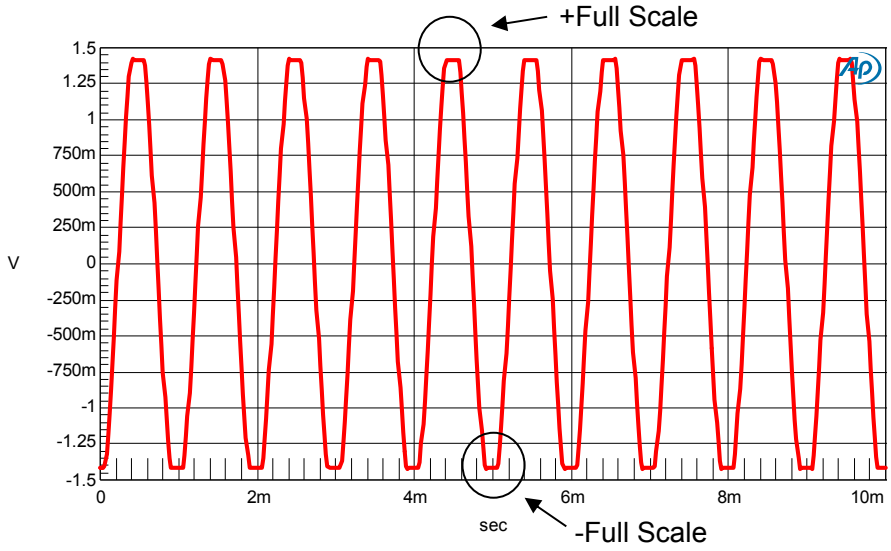


Figure 43: Output Signal with an input of 1kHz 2.3Vrms Signal (2Vrms = 0dBFS)

■ Pre Gain Amplifier (PGA) for MIC Input

The AK5736 has a PGA for microphone input. Each microphone input gain can be set with the PG13-10 bits, (1ch), PG23-20 bits (2ch), …, PG63-60 bits (6ch) in the range of 0dB, +6dB ~ +20dB, (1dB Step). Set the PG* bits, (*=1~6ch), so that the input voltage to the ADC block will not exceed 2.0 Vrms, (ADC full-scale).

PG*3	PG*2	PG*1	PG*0	Input Gain	
0	0	0	0	0dB	(default)
0	0	0	1	6dB	
0	0	1	0	7dB	
0	0	1	1	8dB	
0	1	0	0	9dB	
0	1	0	1	10dB	
0	1	1	0	11dB	
0	1	1	1	12dB	
1	0	0	0	13dB	
1	0	0	1	14dB	
1	0	1	0	15dB	
1	0	1	1	16dB	
1	1	0	0	17dB	
1	1	0	1	18dB	
1	1	1	0	19dB	
1	1	1	1	20dB	

Table 12. PGA for Microphone Input Gain Setting (*channel number)

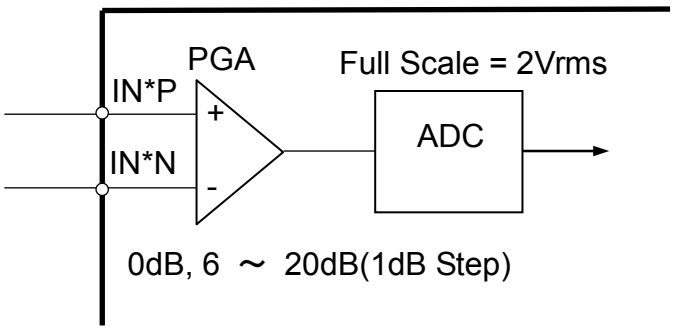


Figure 44. Input Step Construction

■ Charge Pump

The AK5736 integrates a charge pump circuit. The charge pump oscillation frequency is 512kHz or 768kHz. At 512kHz sampling frequency is 32kHz. At 768kHz, sampling frequency is 48kHz.

The internal charge pump boosts the CPVDD voltage to generate the MIC bias voltage and analog voltage such as for a PGA, etc. Boosted voltage is output from the CPOUT pin. When using the charge pump, set the CPEN pin = "L" (Internal Generation Mode), and connect the CPOUT pin with the HVDD pin. The charge pump is not powered up when setting the CPEN pin = "H" (Outside Supply Mode). In this case, the external power supply should be connected to the HVDD pin. External capacitors should be connected to as shown in Figure 45.

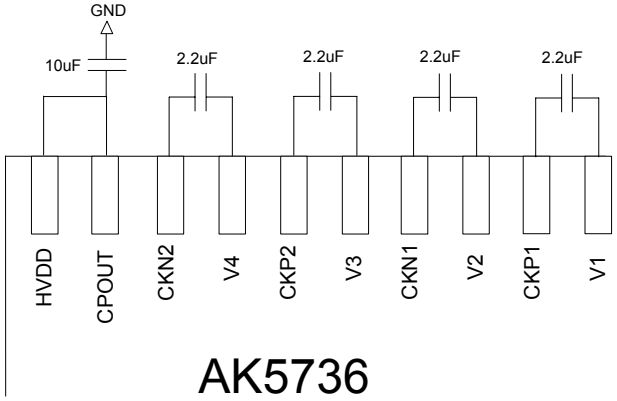


Figure 45. Charge Pump Connection Diagram (CPEN pin = "L")

When the CPEN pin = "L" (Internal Generation Mode), it is recommended that the trace which connects the CPOUT pin with the HVDD pin is close as physically possible to a 10uF capacitor.

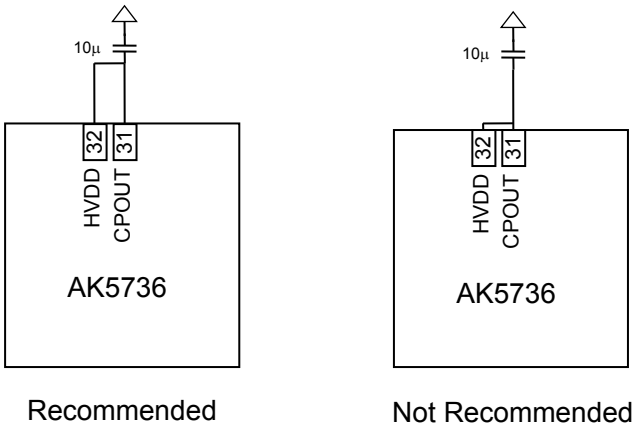


Figure 46. Recommended Pattern (CPEN pin = "L")

Handling of HVDD Pin and CPOUT pin

1. Internal Charge Pump is Enabled (CPEN pin = “L”)

Pin Name	Action
HVDD	Connect to the CPOUT pin externally.
CPOUT	Connect to the HVDD pin externally.

2. Internal Charge Pump is Disabled (CPEN pin = “H”)
The CPVDD pin must be connected to the AVDD pin externally.

Pin Name	Action
HVDD	Connect to the HVDD pin externally.
CPOUT	OPEN

■ MIC Bias Voltage

MIC bias voltage is controlled by the MBS[3:0] bits in a range of 5 ~ 9 V, (0.5V steps), with output from the MPWR pin. The MPWR pin should be connected to AVSS via a 1Ω resistor and a 10μF ceramic capacitor. The VREFMP pin should be connected to AVSS via a 2.2μF ceramic capacitor. (Figure 68)

MBS3-0	Bias Voltage	
00H	5V	(default)
01H	5.5V	
02H	6V	
03H	6.5V	
04H	7V	
05H	7.5V	
06H	8V	
07H	8.5V	
08H	9V	
09H-0FH	Typ 4.5kΩ pulldown (Power down state)	

Table 13. MIC Bias Voltage Setting

■ Error Detection Function

The AK5736 outputs, “L”, to the INT pin when one of following nine errors are detected. Error status registers, (11H ~ 17H), that reflect the ADC input error status are updated simultaneously. Errors 1-5 are detectable only in DC connection mode. Errors 6-9 can be detected at any time. The INT pin outputs an ORed signal based on the below nine interrupt events. However, error conditions can be masked by setting each mask bit 18H~1DH and the masked error will not be reflected at the INT pin. The INT pin should be connected to DVDD via a 10kΩ resistor.

Table 14: Error Statuses, Error Status Registers, and Mask Registers

No.	Error Status	Error Status Register	Mask Register
1	OPEN: Input Open	OPEN* (*1~6)	MOPEN* (*1~6)
2	SHTD: Short between Positive and Negative Inputs	SHTD* (*1~6)	MSHTD* (*1~6)
3	SHTG: Short to Ground	SHTG* (*1~6)	MSHTG* (*1~6)
4	SHMB: Short to MIC Bias Voltage	SHMB* (*1~6)	MSHMB* (*1~6)
5	SHTV: Short to Battery	SHTV* (*1~6)	MSHTV* (*1~6)
6	OVDET: MIC Bias Overvoltage [11.9V (typ.), not depending on the setting of MIC bias voltage level, (MBS3-0 bits)]	OVDET	-
7	OIDET: MIC Bias Overcurrent, [Threshold: 350mA (typical)]	OIDET	-
8	OVCP: Charge Pump Under Voltage [CPOUT Voltage = 5~7V (typical)]	OVCP	-
9	OVTP: Over temperature (Threshold: 160ºC or more)	OVTP	-

Note 41. When the mask register is set to, “0”, there is a, “1”, in the error status register detecting an error. If the mask register is set to, “1”, there is a, “0”, in the error status register detecting an error.

Table 15. Detectable Error Status

No.	Error Status	DC Connection (Differential/Single-end)	AC Connection (Differential/Single-end)
1	OPEN	Yes	N/A
2	SHTD	Yes	N/A
3	SHTG	Yes	N/A
4	SHMB	Yes	N/A
5	SHTV	Yes	N/A
6	OVDET	Yes	Yes
7	OIDET	Yes	Yes
8	OVCP	Yes	Yes
9	OVTP	Yes	Yes

N/A: Not Available

<Internal Circuit State at Error Detection and Error Status Release>
1. Errors 1-5
Internal circuits are not powered down when errors are detected. These error statuses can be released by setting INTR bit = “1”, or RSTN bit = ”0”.

2. Errors 6-8
The error status of internal circuits is selected by ERRPDSEL bit (2EH).
If ERRPDSEL bit = “0”, internal circuits are not powered down when errors are detected. It is recommended that the ERRPDSEL bit is changed during RSTN bit = “0”. These error statuses can be released by setting INTR bit = “1”, or RSTN bit = “L”.

If ERRPDSEL bit = “1”, internal circuits are powered down when errors are detected. In this mode, error status registers are not reset since control registers are not powered down. The INT pin outputs a, “L“. These error statuses can be released by setting RSTN bit = “0” or PDN pin = “L”.

3. Error 9
Internal circuits are powered down when this error is detected. At this time, error status registers are not reset since control registers are not powered down, and the INT pin outputs “L“. This error status can be released by setting RSTN bit = “0”, or PDN pin = “L”.

Table 16: State of the Internal Circuit and How to Reset Error Status

No	Error Status	Internal Circuit States of Error Status	Error Release Conditions
1 - 5	OPEN, SHTD, SHTG, SHMB, SHTV	Not powered down	INTR bit = “1” or RSTN bit =”0”
6 - 8	OVDET, OIDET, OVCP	① Case: ERRPDSEL bit = “0” Not powered down ② Case: ERRPDSEL bit = “1” Powered down	① Case: ERRPDSEL bit = “0” INTR bit = “1” or RSTN bit = “0” ② Case: ERRPDSEL bit = “1” RSTN bit = “0” or PDN pin = “L”
9	OVTP	Powered down	RSTN bit = “0” or PDN pin = “L”

Note 42. The internal circuit includes the ADC, Error detection circuits 1-8, MIC bias voltage generator, and charge pump.

1. Detectable Error State

The integrated error detection circuit detects connection errors for the microphone by monitoring the DC level of the microphone input signal. The detectable error status is described below.

1-1. Input Open

An Input Open is detected when the voltage of an IN*P pin approaches the MPWR pin level, (MIC bias voltage), and the electrical potential of an IN*N pin approaches GND level. The error status is detected when the voltage of an IN*P pin is within the range of MPWR ± Vth and the voltage of an IN*N pin is under Vth. The threshold voltage (Vth) can be set via register address 1FH [3:0] bits for simple detection (SARTH bit = "0"), and is set from register address 24H [7:0] and 25H [7:4] bits for high accuracy detection (SARTH bit = "1").

Short to MIC Bias Voltage, (1-4 SHMB), is detected If only IN*P pin is open. Short to ground, (1-3 SHTG) is detected if only IN*N pin is open.

Error detection criteria is the readout value of MPWR (Address: 4AH and 4BH) when REFSEL bit = "0" (Address: 08H, D1)

Fault Conditions	Conditions
Positive and Negative Input Open	MPWR - Vth ≤ IN*P ≤ MPWR + Vth and IN*N ≤ Vth

Error detection criteria is the readout value of VBATM voltage, (Address: 48H and 49H), when the REFSEL bit = "1", (Address: 08H, D1).

Fault Conditions	Conditions
Positive and Negative Input Open	VBATM - Vth ≤ IN*P ≤ VBATM + Vth and IN*N ≤ Vth

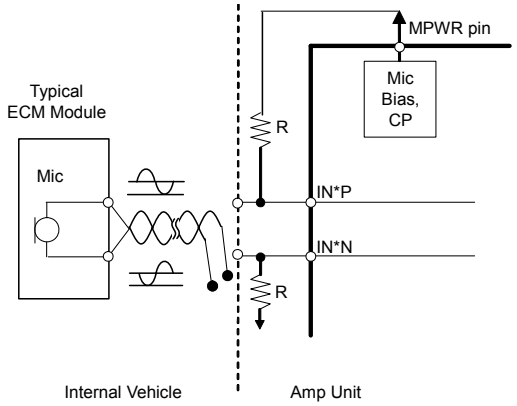
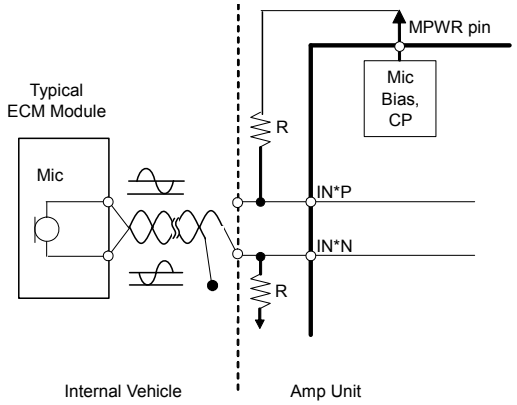
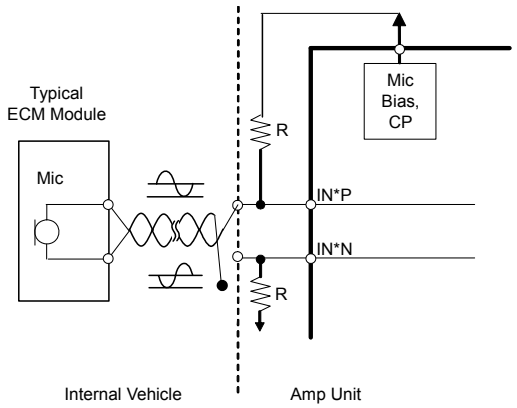


Figure 47. Positive and Negative Input OPEN



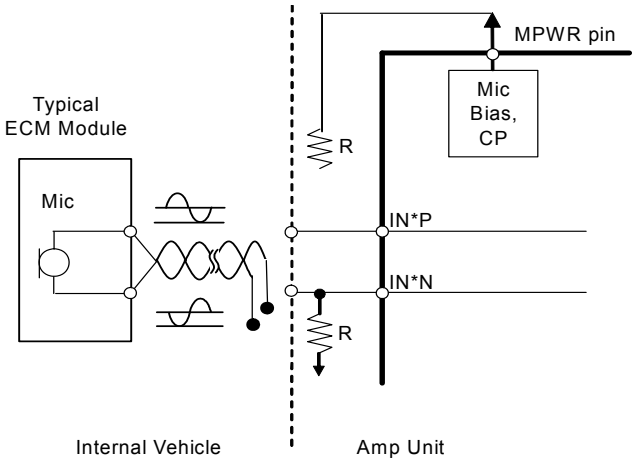
Note: Short to MIC Bias Voltage, (1-4. SHMB), is detected if only an IN*P pin is open.

Figure 48. Positive Input OPEN



Note: Short to Ground, (1-3. SHTG), is detected if only an IN*N pin is open.

Figure 49. Negative Input OPEN



If both resistance elements that are connected to microphone input and MPWR pin are open, the INT pin is pulled down by internal resistance, (Typ. 1.4 MΩ), and short to ground is detected.

Figure 50: Positive and Negative Input OPEN with MPWR pin Open

1-2. SHTD: Short between Positive and Negative Inputs

The voltage of each pin will be equal to, (“MIC bias voltage”/2), when the positive input pin, (IN*P pin), and a negative input pin, (IN*N pin), are shorted together. The error status is detected when the voltage difference of IN*P and IN*N pins goes below the threshold voltage, (Vth), set in the register settings. The threshold voltage can be set via register address 20H, [3:0] bits for simple detection, (SARTH bit = “0”) and set by register address 27H, [7:0] bits and 28H, [7:4] bits for high accuracy detection (SARTH bit = “1”).

Fault Condition	Condition
Short Between Positive and Negative Inputs	|IN*P – IN*N| ≤ Vth

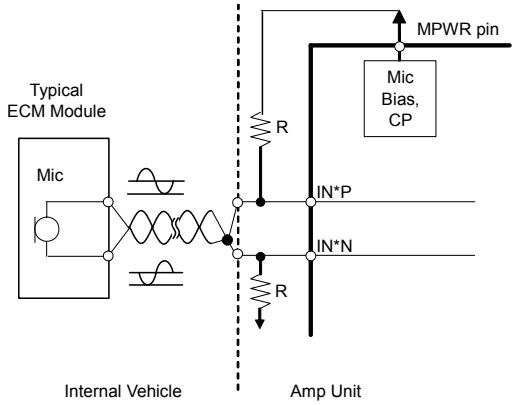


Figure 51. Positive and Negative Input Shorted

1-3. SHTG: Short to Ground

When input pins, (IN*P/N pins), are shorted to ground, the voltage approaches 0V. An error status is detected if the voltage of the pin goes under the threshold voltage, (Vth). The threshold voltage, (Vth), can be set via register address 21H [3:0] bits for simple detection (SARTH bit = "0") and it is set by register address 28H [7:0] and 29H [7:4] bits for high accuracy detection (SARTH bit = "1").

Fault Condition	Condition
Positive Input Short to Ground	IN*P ≤ Vth

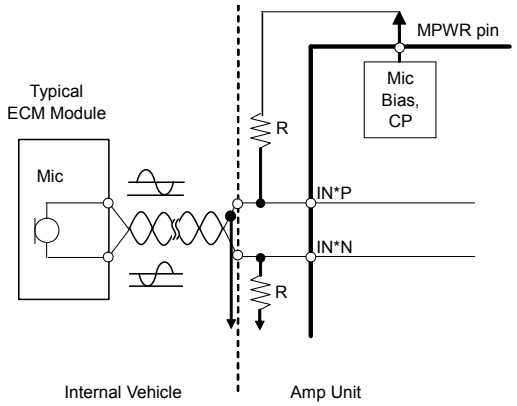


Figure 52. Positive Input Short to GND

Fault Condition	Condition
Negative Input Short to Ground	IN*N ≤ Vth

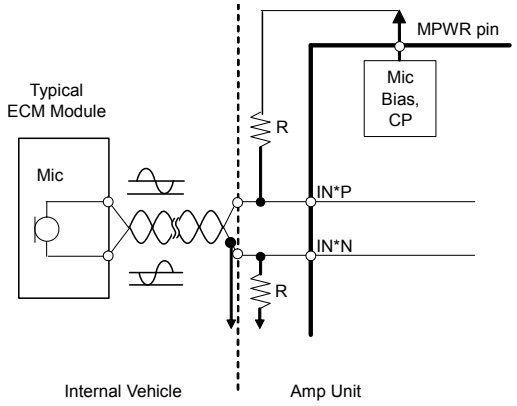


Figure 53. Negative Input Short to GND

1-4. SHMB: Short to MIC Bias Voltage

When input pins, (IN*P/N pins), are shorted to MPWR, (MIC bias voltage), the voltage travels to the MIC bias voltage. An error status is detected if the voltage of the pin goes higher than, “MPWR – Vth”. The threshold voltage, (Vth), can be set via register address 22H [3:0] bits for simple detection, (SARTH bit = “0”), and it is set by register address 2CH [7:0] and 2DH [7:4] bits for high accuracy detection, (SARTH bit = “1”).

Error detection criteria for the read value of MPWR, (Address: 4AH and 4BH), when REFSEL bit = “0”, (Address: 08H, D1)

Fault Conditions	Conditions
Short to MIC bias voltage	INP/N ≥ MPWR - Vth

Error detection criteria for the readout value of VBATM voltage, (Address: 48H and 49H), when REFSEL bit = “1” (Address: 08H, D1).

Fault Conditions	Conditions
Short to MIC bias voltage	IN*P/N ≥ VBATM - Vth

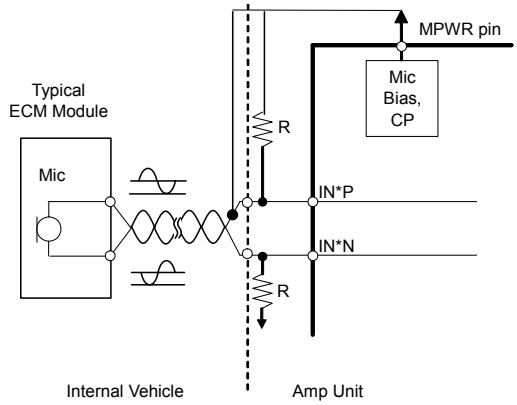


Figure 54. Short to Mic Bias Voltage

1-5. SHTB: Short to Battery

When the input pins, (IN*P/N pins), are shorted to the battery, their voltage moves to battery voltage. An error status is detected if the voltage at the pin becomes higher than, “MPWR – Vth”. The threshold voltage, (Vth) can be set via register address 23H [3:0] bits for simple detection, (SARTH bit = “0”), and set via register address 2AH [7:0] and 2BH [7:4] bits for high accuracy detection, (SARTH bit = “1”). To avoid electric stress to the device, it is necessary to have protection circuits that limit the input voltage to IN*P and IN*N pins to 10V or less if expecting short to battery. In this case, connect a Zener diode via limiting resistors around 500Ω as shown below.

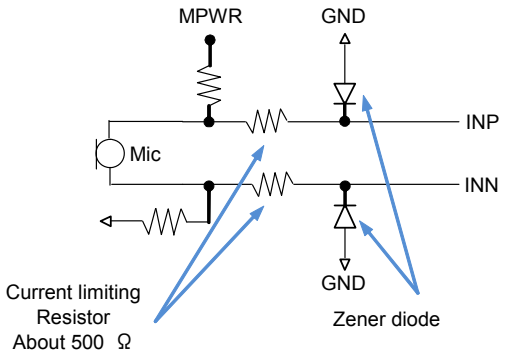


Figure 55. External Protection Circuit for Battery Short

Error detection criteria for the read value of MPWR voltage, (Address: 4AH and 4BH), when REFSEL bit = “1” (Address: 08H, D1)

Fault Conditions	Conditions
Short to Battery	INP/N ≥ MPWR + Vth

Error detection criteria for the read value of VBATM voltage, (Address: 48H and 49H), when REFSEL bit = “1” (Address: 08H, D1)

Fault Conditions	Conditions
Short to Battery	IN*P/N ≥ VBATM - Vth

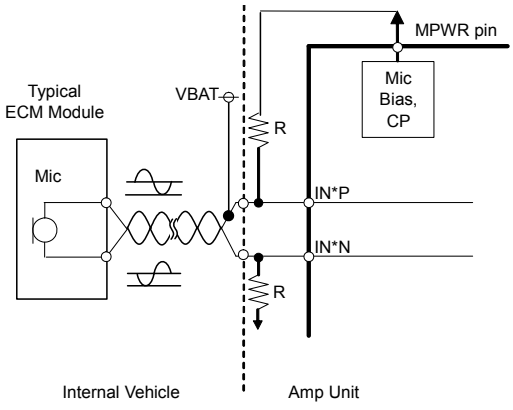


Figure 56. Short to Battery

2. Error Detection Settings

There are two ways to determine the threshold voltage, (Vth), for error detection. When SARTH bit = "0", nine threshold voltage settings (Table 17) are available by setting TOP3-0, TSD3-0, TSG3-0, TSB3-0 and TSV3-0 bits. When the SARTH bit = "1", threshold Voltage can be set with a 12-bit straight binary code with full scale of AVDD for high accuracy error detection.

2-1. Threshold Voltage Setting

Simple Error Detection with Nine Threshold Steps (SARTH bit = "0")

Threshold voltage, (Vth), for error detection can be set from the TOP3-0, TSD3-0, TSG3-0, TSB3-0 and TSV3-0 bits. Input signals to the IN*P pin and IN*N pin will be attenuated by 0.3 times the internal resistance and input to the ADC. Therefore, the threshold voltage at SAR ADC input ranges from, "100mV × 0.3 = (30mV)" to "900mV × 0.3 = (270mV)".

bit3-0	Threshold Voltage	
00H	100mV	
01H	200mV	
02H	300mV	(default)
03H	400mV	
04H	500mV	
05H	600mV	
06H	700mV	
07H	800mV	
08H	900mV	
09H-0FH	(Reserved)	

Table 17. Error Monitor Threshold Setting

High Accuracy Setting via 12-bit Code (SARTH bit = "1")

The threshold voltage in the high accuracy mode can be set from a 12-bit straight binary code, (Address: 24H-2DH), which the full scale is AVDD. When AVDD = 3.3V, the minimum value of the threshold voltage is 3.3V/4095 = 0.81mV. Vth becomes "n/4095× 3.3V". "n" is the set value in 24H-2DH.
e.g.) When THOP12-1 bits is, "000000000011", Vth = 3/4095 × 3.3 = 2.43mV.

2-2. Continuous Error Detection Setting

To prevent false triggering of a fault event, continuous detection times to distinguish the error status can be set. The AK5736 detects error status when detecting an error for the number of times set by INT1-0 bits, and outputs the status to Error Monitor Registers, (11-17H), and, (30-4BH). In this case, the INT pin becomes "L".

INT1 bit	INT0 bit	Error Detection Number	
0	0	Error determination is made by 1 times Detection	(default)
0	1	Error determination is made by 5 times Detection	
1	*	Error determination is made by 10 times Detection	

(*: Don't care)

Table 18. Number of Times for Continuous Error Detection

3. Error Detection Sequence

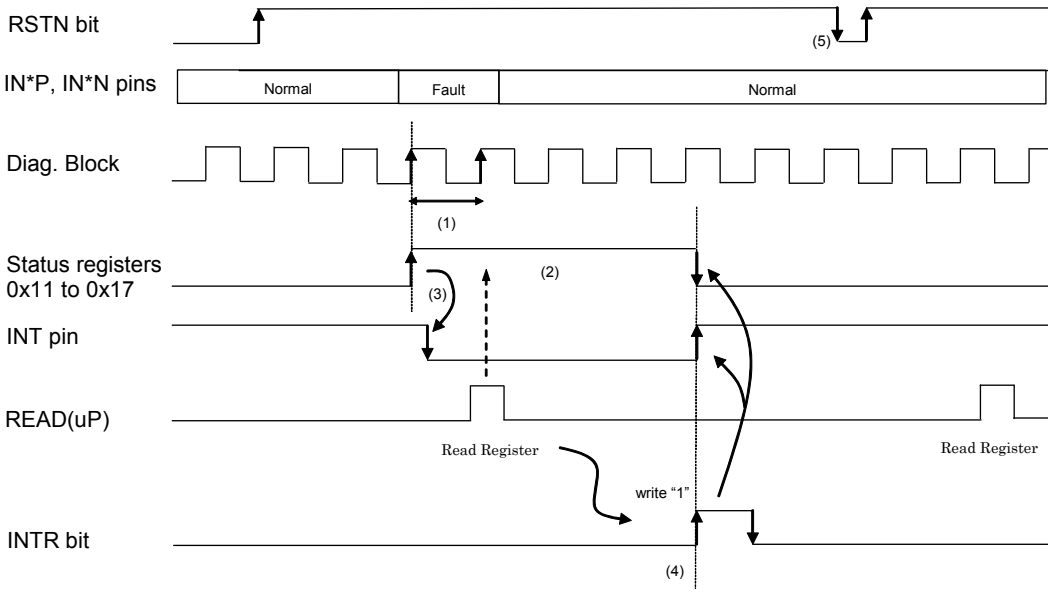


Figure 57. Error Detection Timing

Notes:

(1) The AK5736 executes error detection on 1ch - 14ch, (VBATM, MPWR, IN1P, IN1N, IN2P, IN2N • • • IN6P, IN6N) in this order. The detection cycle of the error detection circuit, "T (ch→2ch→…→14ch→1ch)" depends on the sampling frequency (fs).
fs: 8kHz ≤ fs ≤ 48kHz, T = 23×1/fs[sec]
fs: 48kHz < fs ≤ 96kHz, T = 45×1/fs[sec]
fs: 96kHz < fs ≤ 192kHz, T = 89×1/fs[sec]

(2) The error status register becomes, "1", when an error status is detected at the input pin, MIC bias, charge pump, or over temperature. Once the error status register becomes, "1", it keeps the status until being reset by the INTR bit = "1". In this case, the internal ADC is not reset by INTR bit = "1".

(3) An ORed result is output to the INT pin when error detection is executed on analog input 1ch - 14ch. Detection result can be masked via MSHTV*, MSHTG*, MSHMB*, MSHTD*, and MOPEN* (*: 1-6) bits, (Address = 0C - 0FH), and masked error conditions will not reflect to the error status registers.

(4) Status of the INT pin and error status registers are reset by setting INTR bit = "1" except when MIC bias overvoltage, MIC bias overcurrent, Charge pump under voltage, or over temperature error is detected. When writing, "1" to the INTR bit or setting RSTN bit = "0", the INTR bit automatically will return to, "0" within one cycle of error detection (1).
When ERRPDSEL bit = "0", errors except for over temperature can be reset by setting INTR bit = "1". Over temperature error can be reset by setting RSTN bit = "0".
When ERRPDSEL bit = "1", errors, MIC bias overvoltage, MIC bias overcurrent, Charge pump under voltage. or over temperature can be reset by setting RSTN bit = "0".

(5) In the case the internal circuit is powered down, (Table 16), reset the AK5736 by setting RSTN bit = "0" or the PDN pin = "L".

■ Register Control Interface

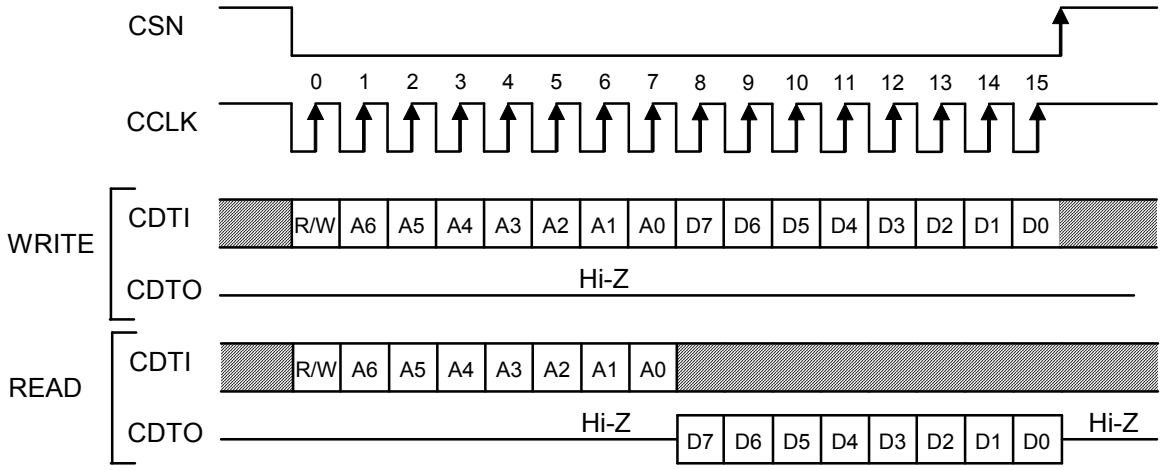
By using the SPI pin, it is possible to switch the operation mode between, “4-wire serial control mode, (SPI pin =’H’)”, and, “I2C Bus control mode, (SPI pin = ‘L’)”. The SPI pin status must not be changed when the AK5736 is in operation.

(1) 4-wire Serial Control Mode, (SPI pin = “H”)

The internal registers may be either written or read from the 4-wire µP interface pins: CSN, CCLK, CDTI & CDTO. The data consists of Chip address, (1bit, C1 is fixed to “1”), Read/Write (1bit), Register address (MSB first, 7bits) and Control data (MSB first, 7bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is written on a rising edge of CSN after the 16th rising edge of CCLK counting from a falling edge of CSN. For read operations, the CDTO output goes to high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. Setting the PDN pin= “L” resets the registers to their default values.

Data will not be written with a format other than 16 times CCLK while CSN is, “L”, such as 15 times CCLK or 17 times CCLK.

For read operations, data will be output after a rising edge of CSN if CCLK is not transitioned 16 times while CSN is “L”. The AK5736 outputs data until D1, (Figure 58), if the CCLK cycle is finished in 15 times and CSN rises.



R/W: READ/WRITE (0: READ, 1: WRITE)
A6-A0: Register Address
D7-D0: Control Data

Figure 58. 4-wire Serial Control I/F Timing

(2). I²C Bus Control Mode (SPI pin = "L")

The AK5736 supports the fast-mode I²C bus, (max: 400kHz).

(2)-1. WRITE Operation

Figure 59 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition, (Figure 65). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0, (device address bits). These bits identify the specific device on the bus. The hard-wired input pins, (CAD1/0 pins), set these device address bits, (Figure 60). If the slave address matches that of the AK5736, the AK5736 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line, (HIGH), during the acknowledge clock pulse, (Figure 66). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5736. The format is MSB first, and those most significant 1-bit is fixed to zero, (Figure 61). The data after the second byte contains control data. The format is MSB first, 8bits, (Figure 62). The AK5736 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, (Figure 65).

The AK5736 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5736 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet, the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds, "4BH", prior to generating a stop condition, the address counter will, "roll over", to, "00H" and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW, (Figure 67), except for the START and STOP conditions.

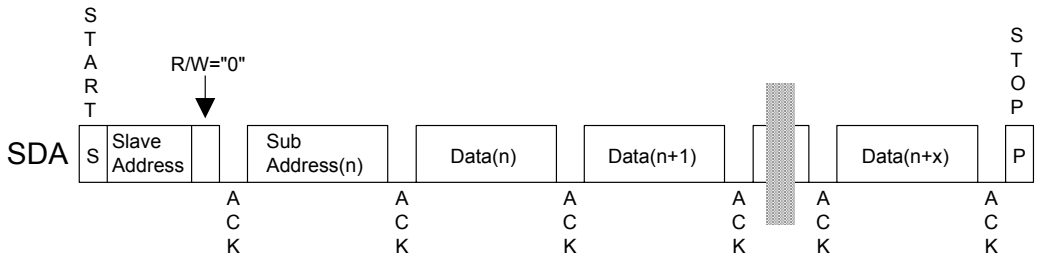


Figure 59: Data Transfer Sequence at the I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD bits are set by the CAD pins)

Figure 60: The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 61. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 62. Byte Structure after the Second Byte

(2)-2. READ Operation
Set the R/W bit = “1” for the READ operation of the AK5736. After transmission of data, the master can read the next address’ data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet, the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds, “4BH”, prior to generating a stop condition, the address counter will “roll over” to “00H” and the data of 00H will be read out.

The AK5736 supports two basic read operations: Current Address Read and Random Address Read.

(2)-2-1. Current Address Read

The AK5736 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access, (either a read or write), was to address, “n”, the next CURRENT READ operation would access data from the address, “n+1”. After receipt of the slave address with R/W bit “1”, the AK5736 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5736 ceases transmission.

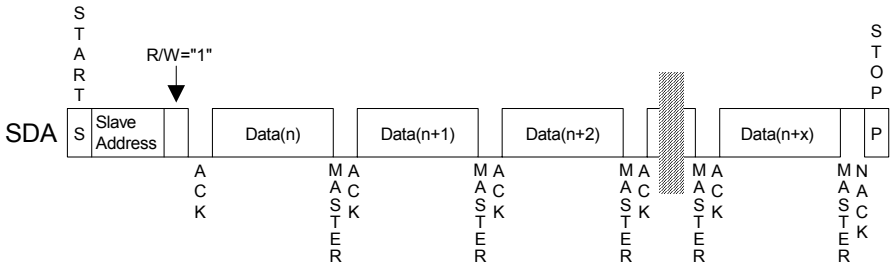


Figure 63. Current Address Read

(2)-2-2. Random Address Read
The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit =“1”, the master must execute a “dummy” write operation first. The master issues a start request, a slave address, (R/W bit = “0”), and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit =“1”. The AK5736 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5736 ceases transmission.

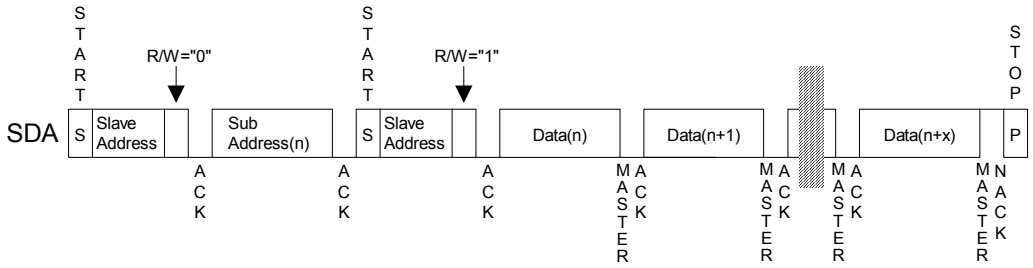


Figure 64. Random Address Read

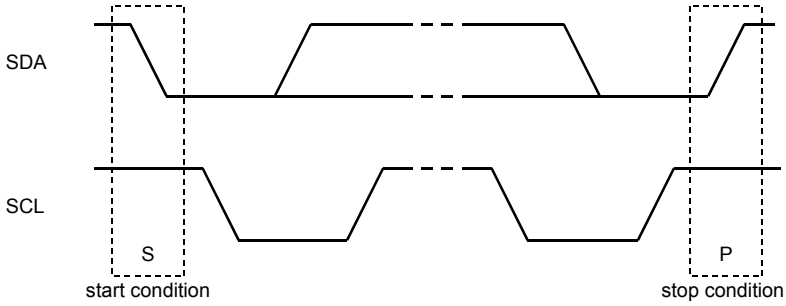


Figure 65: START and STOP Conditions

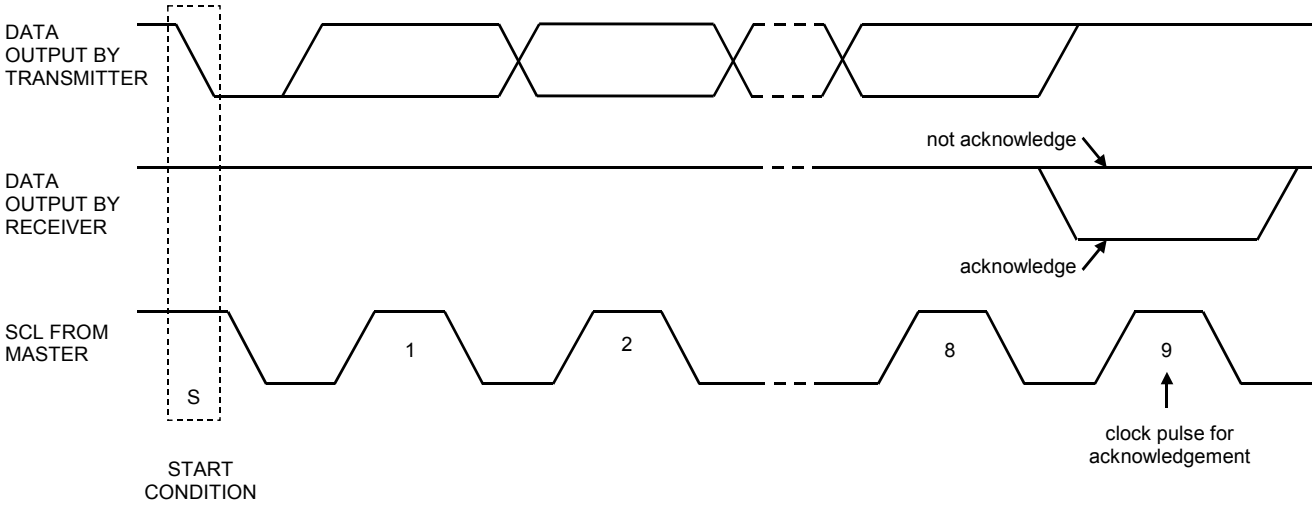


Figure 66. Acknowledge on the I²C-Bus

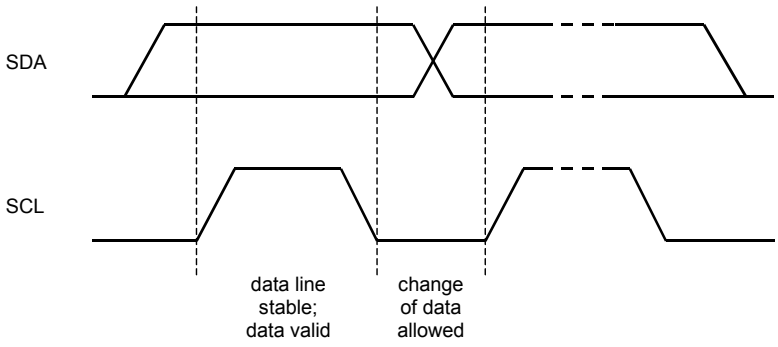


Figure 67. Bit Transfer on the I²C Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	def
00H	Mic. PGA1	0	0	STD1	0	PG13	PG12	PG11	PG10	R/W	00
01H	Mic. PGA2	0	0	STD2	0	PG23	PG22	PG21	PG20	R/W	00
02H	Mic. PGA3	0	0	STD3	0	PG33	PG32	PG31	PG30	R/W	00
03H	Mic. PGA4	0	0	STD4	0	PG43	PG42	PG41	PG40	R/W	00
04H	Mic. PGA5	0	0	STD5	0	PG53	PG52	PG51	PG50	R/W	00
05H	Mic. PGA6	0	0	STD6	0	PG63	PG62	PG61	PG60	R/W	00
06H	General Setting 1	SLOW	SD	ATS1	ATS0	DIF	TDM1	TDM0	RSTN	R/W	00
07H	General Setting 2	0	FS2	FS1	FS0	CKS2	CKS1	CKS0	SARTH	R/W	28
08H	General Setting 3	MBS3	MBS2	MBS1	MBS0	0	0	REFSEL	ATT_VB	R/W	00
09H	Master Slave	0	MSN	0	0	0	0	0	0	R/W	00
0AH	SAR ERR RST	0	0	0	0	0	0	0	INTR	R/W	00
0BH	ADC1 Digital Volume Control	ATT17	ATT16	ATT15	ATT14	ATT13	ATT12	ATT11	ATT10	R/W	34
0CH	ADC2 Digital Volume Control	ATT27	ATT26	ATT25	ATT24	ATT23	ATT22	ATT21	ATT20	R/W	34
0DH	ADC3 Digital Volume Control	ATT37	ATT36	ATT35	ATT34	ATT33	ATT32	ATT31	ATT30	R/W	34
0EH	ADC4 Digital Volume Control	ATT47	ATT46	ATT45	ATT44	ATT43	ATT42	ATT41	ATT40	R/W	34
0FH	ADC5 Digital Volume Control	ATT57	AT56	ATT55	ATT54	ATT53	ATT52	ATT51	ATT50	R/W	34
10H	ADC6 Digital Volume Control	ATT67	ATT66	ATT65	ATT64	ATT63	ATT62	ATT61	ATT60	R/W	34
11H	Monitor Summary	0	0	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	R	00
12H	Monitor ADC1	0	OVDET	OIDET	SHTV1	SHMB1	SHTG1	SHTD1	OPEN1	R	00
13H	Monitor ADC2	0	OVTP	OVCP	SHTV2	SHMB2	SHTG2	SHTD2	OPEN2	R	00
14H	Monitor ADC3	0	0	0	SHTV3	SHMB3	SHTG3	SHTD3	OPEN3	R	00
15H	Monitor ADC4	0	0	0	SHTV4	SHMB4	SHTG4	SHTD4	OPEN4	R	00
16H	Monitor ADC5	0	0	0	SHTV5	SHMB5	SHTG5	SHTD5	OPEN5	R	00
17H	Monitor ADC6	0	0	0	SHTV6	SHMB6	SHTG6	SHTD6	OPEN6	R	00
18H	Mask ADC1	DETST	INT[1]	INT[0]	MSHTV1	MSHMB1	MSHTG1	MSHTD1	MOPEN1	R/W	00
19H	Mask ADC2	0	0	0	MSHTV2	MSHMB2	MSHTG2	MSHTD2	MOPEN2	R/W	00
1AH	Mask ADC3	0	0	0	MSHTV3	MSHMB3	MSHTG3	MSHTD3	MOPEN3	R/W	00
1BH	Mask ADC4	0	0	0	MSHTV4	MSHMB4	MSHTG4	MSHTD4	MOPEN4	R/W	00
1CH	Mask ADC5	0	0	0	MSHTV5	MSHMB5	MSHTG5	MSHTD5	MOPEN5	R/W	00
1DH	Mask ADC6	0	0	0	MSHTV6	MSHMB6	MSHTG6	MSHTD6	MOPEN6	R/W	00

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	def
1EH	Input Mode Select	0	0	AC6	AC5	AC4	AC3	AC2	AC1	R/W	00
1FH	SAR Threshold setting OPEN	0	0	0	0	TOP[3]	TOP[2]	TOP[1]	TOP[0]	R/W	02
20H	SAR Threshold setting SHTD	0	0	0	0	TSD[3]	TSD[2]	TSD[1]	TSD[0]	R/W	02
21H	SAR Threshold setting SHTG	0	0	0	0	TSG[3]	TSG[2]	TSG[1]	TSG[0]	R/W	02
22H	SAR Threshold setting SHMB	0	0	0	0	TSB[3]	TSB[2]	TSB[1]	TSB[0]	R/W	02
23H	SAR Threshold setting SHTV	0	0	0	0	TSV[3]	TSV[2]	TSV[1]	TSV[0]	R/W	02
24H	SAR OPEN Threshold High byte	THOP_12	THOP_11	THOP_10	THOP_09	THOP_08	THOP_07	THOP_06	THOP_05	R/W	06
25H	SAR OPEN Threshold Low byte	THOP_04	THOP_03	THOP_02	THOP_01	0	0	0	0	R/W	F0
26H	SAR P/N SHORT Threshold High byte	THSD_12	THSD_11	THSD_10	THSD_09	THSD_08	THSD_07	THSD_06	THSD_05	R/W	06
27H	SAR P/N SHORT Threshold Low byte	THSD_04	THSD_03	THSD_02	THSD_01	0	0	0	0	R/W	F0
28H	SAR GND SHORT Threshold High byte	THSG_12	THSG_11	THSG_10	THSG_09	THSG_08	THSG_07	THSG_06	THSG_05	R/W	06
29H	SAR GND SHORT Threshold Low byte	THSG_04	THSG_03	THSG_02	THSG_01	0	0	0	0	R/W	F0
2AH	SAR VBAT SHORT Threshold High byte	THSV_12	THSV_11	THSV_10	THSV_09	THSV_08	THSV_07	THSV_06	THSV_05	R/W	06
2BH	SAR VBAT SHORT Threshold Low byte	THSV_04	THSV_03	THSV_02	THSV_01	0	0	0	0	R/W	F0
2CH	SAR VBIAS SHORT Threshold High byte	THSM_12	THSM_11	THSM_10	THSM_09	THSM_08	THSM_07	THSM_06	THSM_05	R/W	06
2DH	SAR VBIAS SHORT Threshold Low byte	THSM_04	THSM_03	THSM_02	THSM_01	0	0	0	0	R/W	F0
2EH	Error State Select	ERRPDSEL	0	0	0	0	0	0	0	R/W	00
2FH	Reserved	0	0	0	0	0	0	0	0	R/W	00
30H	SAR IN1+ High byte	A1P12	A1P11	A1P10	A1P09	A1P08	A1P07	A1P06	A1P05	R	00
31H	SAR IN1+ Low byte	A1P04	A1P03	A1P02	A1P01	0	0	0	0	R	00
32H	SAR IN1- High byte	A1N12	A1N11	A1N10	A1N09	A1N08	A1N07	A1N06	A1N05	R	00
33H	SAR IN1- Low byte	A1N04	A1N03	A1N02	A1N01	0	0	0	0	R	00
34H	SAR IN2+ High byte	A2P12	A2P11	A2P10	A2P09	A2P08	A2P07	A2P06	A2P05	R	00
35H	SAR IN2+ Low byte	A2P04	A2P03	A2P02	A2P01	0	0	0	0	R	00
36H	SAR IN2- High byte	A2N12	A2N11	A2N10	A2N09	A2N08	A2N07	A2N06	A2N05	R	00
37H	SAR IN2- Low byte	A2N04	A2N03	A2N02	A2N01	0	0	0	0	R	00
38H	SAR IN3+ High byte	A3P12	A3P11	A3P10	A3P09	A3P08	A3P07	A3P06	A3P05	R	00
39H	SAR IN3+ Low byte	A3P04	A3P03	A3P02	A3P01	0	0	0	0	R	00
3AH	SAR IN3- High byte	A3N12	1N11	A3N10	A3N09	A3N08	A3N07	A3N06	A3N05	R	00
3BH	SAR IN3- Low byte	A3N04	A3N03	A3N02	A3N01	0	0	0	0	R	00

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	def
3CH	SAR IN4+ High byte	A4P12	A4P11	A4P10	A4P09	A4P08	A4P07	A4P06	A4P05	R	00
3DH	SAR IN4+ Low byte	A4P04	A4P03	A4P02	A4P01	0	0	0	0	R	00
3EH	SAR IN4- High byte	A4N12	A4N11	A4N10	A4N09	A4N08	A4N07	A4N06	A4N05	R	00
3FH	SAR IN4- Low byte	A4N04	A4N03	A4N02	A4N01	0	0	0	0	R	00
40H	SAR IN5+ High byte	A5P12	A5P11	A5P10	A5P09	A5P08	A5P07	A5P06	A5P05	R	00
41H	SAR IN5+ Low byte	A5P04	A5P03	A5P02	A5P01	0	0	0	0	R	00
42H	SAR IN5- High byte	A5N12	A5N11	A5N10	A5N09	A5N08	A5N07	A5N06	A5N05	R	00
43H	SAR IN5- Low byte	A5N04	A5N03	A5N02	A5N01	0	0	0	0	R	00
44H	SAR IN6+ High byte	A6P12	A6P11	A6P10	A6P09	A6P08	A6P07	A6P06	A6P05	R	00
45H	SAR IN6+ Low byte	A6P04	A6P03	A6P02	A6P01	0	0	0	0	R	00
46H	SAR IN6- High byte	A6N12	A6N11	A6N10	A6N09	A6N08	A6N07	A6N06	A6N05	R	00
47H	SAR IN6- Low byte	A6N04	A6N03	A6N02	A6N01	0	0	0	0	R	00
48H	SAR VBAT High byte	VBAT12	VBAT11	VBAT10	VBAT09	VBAT08	VBAT07	VBAT06	VBAT05	R	00
49H	SAR VBAT Low byte	VBAT04	VBAT03	VBAT02	VBAT01	0	0	0	0	R	00
4AH	SAR VBIAS High byte	VBIAS12	VBAIS11	VBIAS10	VBIAS09	VBIAS08	VBIAS07	VBIAS06	VBIAS05	R	00
4BH	SAR VBIAS Low byte	VBIAS04	VBIAS03	VBIAS02	VBIAS01	0	0	0	0	R	00
5AH	Test	0	0	0	0	0	0	0	0	R/W	00
5BH	Test	0	0	0	0	0	0	0	0	R/W	00
5CH	Test	0	0	0	0	0	0	0	0	R/W	00
5DH	Test	0	0	0	0	0	0	0	0	R/W	00
5EH	Power down control	PDMP_N	1	1	1	1	1	1	1	R/W	FF
5FH	Test	1	1	1	1	1	1	1	1	R/W	FF

Note: ・Do not write to the registers called, “Test”, and addresses after “5FH”. Leave them to the default setting. Malfunctions may occur by writing “0” to these bits.
・Auto increment function is valid until the address 4BH, so the address counter will be set to, “00H”, after accessing, “4BH”. Therefore, the address, “5EH”, must be accessed directly.
・Bits indicated as 0 in each address must contain a, “0”, value. Malfunctions may occur by writing, “1”, to those bits. Bits indicated as 1 in each address must contain a, “1”, value. Malfunctions May occur by writing, “0”, to those bits.
・When the PDN pin goes to, “L”, all registers are initialized to their default values.
・When RSTN bit is set to, “0”, the internal timing is reset, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Mic. PGA1	0	0	STD1	0	PG13	PG12	PG11	PG10
01H	Mic. PGA2	0	0	STD2	0	PG23	PG22	PG21	PG20
02H	Mic. PGA3	0	0	STD3	0	PG33	PG32	PG31	PG30
03H	Mic. PGA4	0	0	STD4	0	PG43	PG42	PG41	PG40
04H	Mic. PGA5	0	0	STD5	0	PG53	PG52	PG51	PG50
05H	Mic. PGA6	0	0	STD6	0	PG63	PG62	PG61	PG60
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

STD*: Input Select (single–ended or differential)
0: Differential (default)
1: Single–ended

PGA*3-*0: Microphone Pre-Gain Amplifier Gain Setting, (Table 12)
Default value is “0000” (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	General Setting 1	SLOW	SD	ATS1	ATS0	DIF	TDM1	TDM0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable (Table 7)
0: Sharp roll-off filter (default)
1: Slow roll-off filter

SD: Short delay Filter Enable (Table 7)
0: Sharp roll-off filter (default)
1: Short delay filter

ATS1-0: ADC Digital attenuator transition time setting (Table 9)
Default value is “00”.

DIF: Audio Data Interface Modes (Table 6)
0: IIS (default)
1: Left Justified

TDM: TDM Mode Select (Table 6)
00: Normal mode (default)
01: TDM128 mode
10: TDM256 mode
11: TDM512 mode

RSTN: Internal Timing Reset
0: Reset (default)
Internal clock timings are reset, but all other registers are not reset to their default value and R/W access is still allowed.
1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	General Setting 2	0	FS2	FS1	FS0	CKS2	CKS1	CKS0	SARTH
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	0

SARTH: SAR Error check mode select
0: Simple check mode (4bit code) (default)
1: Highly precise check (12bit code)

CKS[2:0]: Master Clock setting (Table2)
Default value is “00” (512fs).

FS[2:0]: Master Clock setting (Table 3)
Default value is “010” (24kHz < fs ≤ 48kHz).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	General Setting 3	MBS3	MBS2	MBS1	MBS0	0	0	REFSEL	ATT_VB
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATT_VB: VBATM pin Attenuation (Note 21)
0: 10% Attenuation (default)
1: 30% Attenuation

REFSEL: Criteria Setting

0: Using MIC bias voltage for OPEN*, SHMB*, SHTV* error detection (default)

Error Name	Fault Conditions	Conditions
OPEN*	Positive and Negative Input Open	MPWR - Vth ≤ IN*P ≤ MPWR + Vth and IN*N ≤ Vth
SHMB*	Short to MIC Bias Voltage	IN*P/N ≥ MPWR - Vth
SHTV*	Short to Battery	IN*P/N ≥ MPWR + Vth

1: Using VBATM for OPEN*, SHMB*, SHTV* error detection

Error Name	Fault Conditions	Conditions
OPEN*	Positive and Negative Input Open	VBATM - Vth ≤ IN*P ≤ VBATM + Vth and IN*N ≤ Vth
SHMB*	Short to MIC Bias Voltage	IN*P/N ≥ VBATM - Vth
SHTV*	Short to Battery	IN*P/N ≥ VBATM + Vth

MBS[3:0]: MIC Bias Voltage Setting (Table 13)
Default value is “0000” (5V).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Master Slave	0	MSN	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSN: Master & Slave Mode Select (Table 1)
0: Slave Mode (default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	SAR ERR RST	0	0	0	0	0	0	0	INTR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INTR: INT pin Reset
0: Normal Operation (default)
1: Reset
Error Monitor Registers (11-17H) and (30-4BH) are initialized.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ADC1 Digital Volume Control	ATT17	ATT16	ATT15	ATT14	ATT13	ATT12	ATT11	ATT10
0CH	ADC2 Digital Volume Control	ATT27	ATT26	ATT25	ATT24	ATT23	ATT22	ATT21	ATT20
0DH	ADC3 Digital Volume Control	ATT37	ATT36	ATT35	ATT34	ATT33	ATT32	ATT31	ATT30
0EH	ADC4 Digital Volume Control	ATT47	ATT46	ATT45	ATT44	ATT43	ATT42	ATT41	ATT40
0FH	ADC5 Digital Volume Control	ATT57	ATT56	ATT55	ATT54	ATT53	ATT52	ATT51	ATT50
10H	ADC6 Digital Volume Control	ATT67	ATT66	ATT65	ATT64	ATT63	ATT62	ATT61	ATT60
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	1	0	0

ATT[*7:0]: MIC Bias Voltage Setting (Table 8)
Default value is “00110100” (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Monitor Summary	0	0	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

Error Monitor for each ADC

0: No error detected. (default)
1: Error detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Monitor ADC1	0	OVDET	OIDET	SHTV1	SHMB1	SHTG1	SHTD1	OPEN1
13H	Monitor ADC2	0	OVTP	OVCP	SHTV2	SHMB2	SHTG2	SHTD2	OPEN2
14H	Monitor ADC3	0	0	0	SHTV3	SHMB3	SHTG3	SHTD3	OPEN3
15H	Monitor ADC4	0	0	0	SHTV4	SHMB4	SHTG4	SHTD4	OPEN4
16H	Monitor ADC5	0	0	0	SHTV5	SHMB5	SHTG5	SHTD5	OPEN5
17H	Monitor ADC6	0	0	0	SHTV6	SHMB6	SHTG6	SHTD6	OPEN6
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

Error Status Monitor

0: No error detected (default)
1: Error detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Mask ADC1	DETST	INT[1]	INT[0]	MSHTV1	MSHMB1	MSHTG1	MSHTD1	MOPEN1
19H	Mask ADC2	0	0	0	MSHTV2	MSHMB2	MSHTG2	MSHTD2	MOPEN2
1AH	Mask ADC3	0	0	0	MSHTV3	MSHMB3	MSHTG3	MSHTD3	MOPEN3
1BH	Mask ADC4	0	0	0	MSHTV4	MSHMB4	MSHTG4	MSHTD4	MOPEN4
1CH	Mask ADC5	0	0	0	MSHTV5	MSHMB5	MSHTG5	MSHTD5	MOPEN5
1DH	Mask ADC6	0	0	0	MSHTV6	MSHMB6	MSHTG6	MSHTD6	MOPEN46
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSH*, MOPEN*: Error Monitor Mask
0: No mask (default)
1: Mask error

INT[1:0]: Number of Times for Continuous Error Detection (Table 18)

DETST: Operation Setting of Error Detection Circuit
0: Error detection circuit and SAR ADC keep operation after detecting error. (default)
1: Error detection circuit and SAR ADC stop operation after detecting error.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	Input Mode Select	0	0	AC6	AC5	AC4	AC3	AC2	AC1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

AC*: Analog Input Mode (AC or DC Connection) Select
0: DC Connection Mode (default)
1: AC Connection Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1FH	SAR Threshold setting OPEN	0	0	0	0	TOP[3]	TOP[2]	TOP[1]	TOP[0]
20H	SAR Threshold setting SHTD	0	0	0	0	TSD[3]	TSD[2]	TSD[1]	TSD[0]
21H	SAR Threshold setting SHTG	0	0	0	0	TSG[3]	TSG[2]	TSG[1]	TSG[0]
22H	SAR Threshold setting SHMB	0	0	0	0	TSB[3]	TSB[2]	TSB[1]	TSB[0]
23H	SAR Threshold setting SHTV	0	0	0	0	TSV[3]	TSV[2]	TSV[1]	TSV[0]
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

1F-23H: Simple Error Detection Threshold Setting (Table 17)
Default value is “00000010” (300mV).
This setting is valid when SARTH bit = “0”. Nine values of threshold voltage can be selected.
The threshold setting is applied to all channels.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	SAR OPEN Threshold High byte	THOP_12	THOP_11	THOP_10	THOP_09	THOP_08	THOP_07	THOP_06	THOP_05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25H	SAR OPEN Threshold Low byte	THOP_04	THOP_03	THOP_02	THOP_01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	SAR P/N SHORT Threshold High byte	THSD_12	THSD_11	THSD_10	THSD_09	THSD_08	THSD_07	THSD_06	THSD_05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	SAR P/N SHORT Threshold Low byte	THSD_04	THSD_03	THSD_02	THSD_01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	SAR GND SHORT Threshold High byte	THSG_12	THSG_11	THSG_10	THSG_09	THSG_08	THSG_07	THSG_06	THSG_05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
29H	SAR GND SHORT Threshold Low byte	THSG_04	THSG_03	THSG_02	THSG_01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2AH	SAR VBAT SHORT Threshold High byte	THSV_12	THSV_11	THSV_10	THSV_09	THSV_08	THSV_07	THSV_06	THSV_05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2BH	SAR VBAT SHORT Threshold Low byte	THSV_04	THSV_03	THSV_02	THSV_01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	SAR VBIAS SHORT Threshold High byte	THSM_12	THSM_11	THSM_10	THSM_09	THSM_08	THSM_07	THSM_06	THSM_05
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2DH	SAR VBIAS SHORT Threshold Low byte	THSM_04	THSM_03	THSM_02	THSM_01	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	0	0	0

24H-2DH: High Accuracy Error Detection Threshold Setting

Default value of High byte is, “00000110”

Default value of Low byte is, “11110000”

This setting is valid when SARTH bit = “1”. Threshold voltage of the SAR ADC can be set by a 12-bit straight binary code with AVDD full scale. The threshold setting is applied to all channels.

When AVDD = 3.3V, the minimum value of the threshold voltage is 3.3V/4096 = 0.81mV.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2EH	Error State Select	ERRPDSEL	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ERRPDSEL: Error State Select (Table 16)

Error state of internal circuits when MIC bias overvoltage, MIC bias overcurrent or charge pump undervoltage is detected can be selected.

0: Active (default)

1: Power down

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	SAR IN1 +High byte	A1P12	A1P11	A1P10	A1P09	A1P08	A1P07	A1P06	A1P05
31H	SAR IN1 +Low byte	A1P04	A1P03	A1P 02	A1P01	0	0	0	0
32H	SAR IN1 -High byte	A1N12	A1N11	A1N10	A1P09	A1P08	A1P07	A1P06	A1P05
33H	SAR IN1 -Low byte	A1N04	A1N03	A1N02	A1N01	0	0	0	0
34H	SAR IN2 +High byte	A2P12	A2P11	A2P10	A2P09	A2P08	A2P07	A2P06	A2P05
35H	SAR IN2 +Low byte	A2P04	A2P03	A2P 02	A2P01	0	0	0	0
36H	SAR IN2 -High byte	A2N12	A2N11	A2N10	A2P09	A2P08	A2P07	A2P06	A2P05
37H	SAR IN2 -Low byte	A2N04	A2N03	A2N02	A2N01	0	0	0	0
38H	SAR IN3 +High byte	A3P12	A3P11	A3P10	A3P09	A3P08	A3P07	A3P06	A3P05
39H	SAR IN3 +Low byte	A3P04	A3P03	A3P 02	A3P01	0	0	0	0
3AH	SAR IN3 -High byte	A3N12	A3N11	A3N10	A3P09	A3P08	A3P07	A3P06	A3P05
3BH	SAR IN3 -Low byte	A3N04	A3N03	A3N02	A3N01	0	0	0	0
3CH	SAR IN4 +High byte	A4P12	A4P11	A4P10	A4P09	A4P08	A4P07	A4P06	A4P05
3DH	SAR IN4 +Low byte	A4P04	A4P03	A4P 02	A4P01	0	0	0	0
3EH	SAR IN4 -High byte	A4N12	A4N11	A4N10	A4P09	A4P08	A4P07	A4P06	A4P05
3FH	SAR IN4 -Low byte	A4N04	A5N03	A4N02	A4N01	0	0	0	0
40H	SAR IN5 +High byte	A5P12	A5P11	A5P10	A5P09	A5P08	A5P07	A5P06	A5P05
41H	SAR IN5 +Low byte	A5P04	A5P03	A5P 02	A5P01	0	0	0	0
42H	SAR IN5 -High byte	A5N12	A5N11	A5N10	A5P09	A5P08	A5P07	A5P06	A5P05
43H	SAR IN5 -Low byte	A5N04	A5N03	A5N02	A5N01	0	0	0	0
44H	SAR IN6 +High byte	A6P12	A6P11	A6P10	A6P09	A6P08	A6P07	A6P06	A6P05
45H	SAR IN6 +Low byte	A6P04	A6P03	A6P 02	A6P01	0	0	0	0
46H	SAR IN6 -High byte	A6N12	A6N11	A6N10	A6P09	A6P08	A6P07	A6P06	A6P05
47H	SAR IN6 -Low byte	A6N04	A6N03	A6N02	A6N01	0	0	0	0
48H	SAR VBAT High byte	VBAT12	VBAT11	VBAT10	VBAT09	VBAT08	VBAT07	VBAT06	VBAT05
49H	SAR VBAT Low byte	VBAT04	VBAT03	VBAT02	VBAT01	0	0	0	0
4AH	SAR VBIAS High byte	VBIAS12	VBIAS11	VBIAS10	VBIAS09	VBIAS08	VBIAS07	VBIAS06	VBIAS05
4BH	SAR VBIAS Low byte	VBIAS04	VBIAS03	VBIAS02	VBIAS01	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

SAR Law Data Read

Default value is, “00000000”.

Read out Low bytes before High bytes when reading the addresses above. To prevent data mismatch of Low byte and High byte, the AK5736 High byte and Low byte will not be updated once High byte is read until reading other addresses. Therefore, addresses from 30H to 4BH should be read continuously. Do not stop the data read; there is a possibility of data mismatch of High and Low bytes, or the data might not be updated.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5EH	Power down control	PDMP_N	1	1	1	1	1	1	1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

PDMP_N: MIC Bias Voltage Power Down Negative

0: Power down

1: Power up (default)

13. Recommended External Circuits

Figure 68 shows recommended external connection. An evaluation board (AKD5736) is available for fast evaluation as well as suggestions for peripheral circuitry.

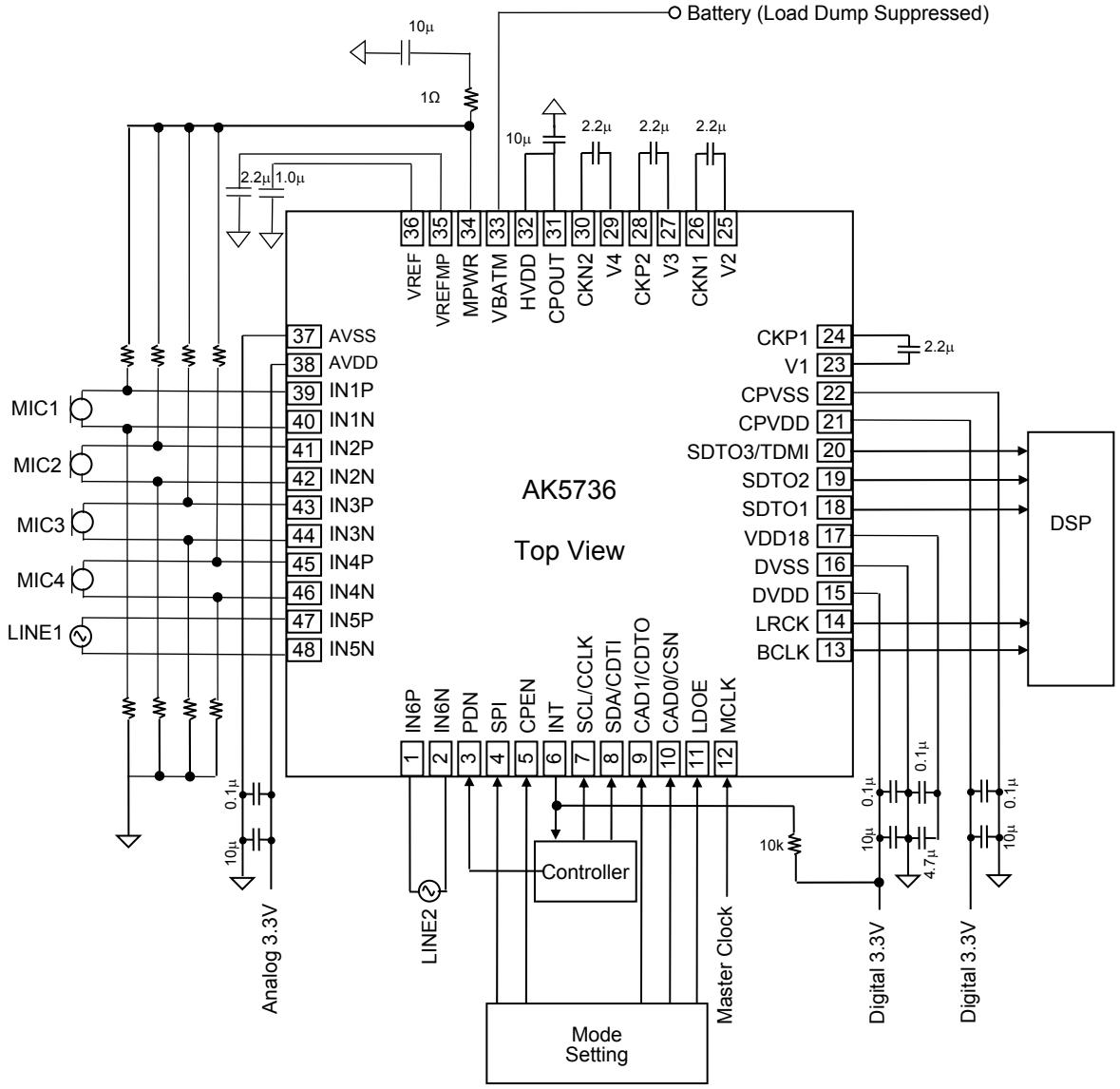
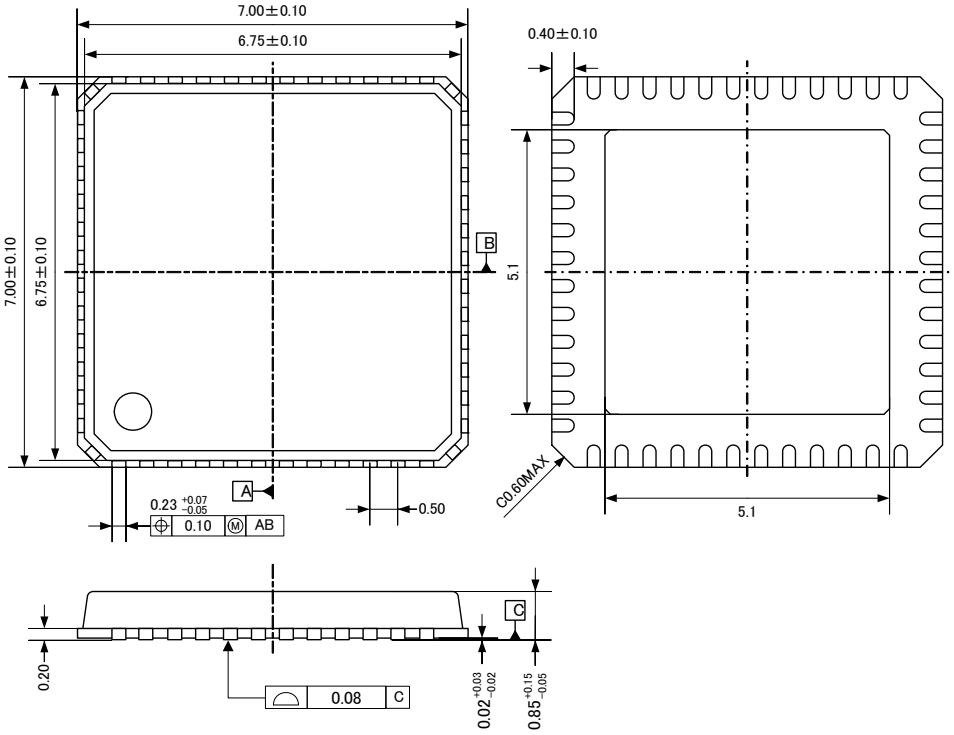


Figure 68. Typical Connection Diagram

14. Package

■ Outline Dimensions

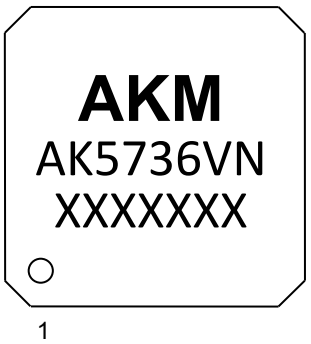
48-pin QFN (Unit: mm)



■ Material & Lead Finish

Package Molding Compound: Epoxy Resin
Lead Frame Material: Cu
Pin Surface Treatment: Solder, (Pb free), Plate

■ Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marketing Code: AK5736VN
4) AKM Logo

15. Ordering Guide

AK5736VN	−40 ~ 105°C	48-pin QFN
AKD5736	Evaluation Board for AK5736	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
18/03/27	00	First Edition		
18/04/12	01	Specification Change	4	MPWR pin : Input →Output
			7	1ohm resistor in parallel with a 10F → 1ohm resistor and a 10F
			8	VINBAT VTT_VB bit = ”H” : 10V →10.1V
		Error Correction	8	VTT_VB bit = ”L” →”0” VTT_VB bit = ”H” →”1”
			11	The below sentence was deleted. The VREFMP pin has an internal resistor, (typ: 187.5kohm, max: 255kohm).
			25	The below sentence was deleted. Note 32-34 The AK5736 should be in Quad/Double/Normal Speed mode.
		Description Addition	25	The below note was added. It is a case that when the duty of MCLK is 50%.
		Error Correction	59	Vth = 3/4095 × 23.3 = 2.43mV. → Vth = 3/4095 × 3.3 = 2.43mV.
19/04/12	02	Error Correction	3	IN5N → IN5P
		Error Correction	12	VBATM pin Attenuation error +186 → +1.8
		Description and Specification Change	21, 23	Specification of MCLK on page 21, 23 and page 34 was unified because there was difference in their description. The specification of Table 4 “System Clock Example” on page 34 was not changed. (Page 21, 23) Description of MCLK input timing was simplified. In master mode, MCLK 3.072MHz is not available when MCLK = 384fs, and MCLK 27.648MHz is not available when MCLK = 512fsn, 256fsd, 128fsq. The minimum MCLK frequency was changed to 4.096MHz. Note 30, 32 and 33 were added.
		Specification Change	39	Mode switching must be executed when RSTN bit =”0”.
		Error Correction	51	Description was changed. “Errors 1-5 are only detectable when the microphone is connected as shown in recommended examples, (Figure38, Figure40).” → “Errors 1-5 are detectable only in DC connection mode.”

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