

AK59256AS / AK59256AG

262,144 Word by 9 bit, CMOS

Dynamic Random Access Memory

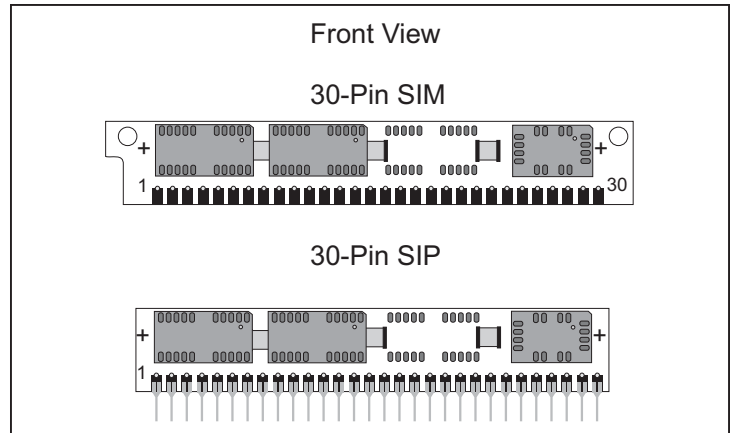
DESCRIPTION

The Accuthek AK59256A high density memory modules is a random access memory organized in 256K x 9 bit words. The assembly consists of two 256K x 4 and one 256K x 1 DRAMs in surface mount packages mounted to the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. This packaging approach provides a better than 6 to 1 density increase over standard DIP packaging.

The operation of the AK59256A is identical to two 256K x 4 DRAMs plus one 256K x 1 DRAM. For the lower eight bits data input is tied to data output and brought out separately for each 256K x 4 device, with common $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ control. The $\overline{\text{OE}}$ pins are tied to V_{ss} which dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable ($\overline{\text{WE}}$) signal must always go low before $\overline{\text{CAS}}$ in a write cycle, Read-Write and Read-Modify-Write operation is not possible. For the ninth bit, the data input (D_9) and data output (Q_9) pins are brought out separately and controlled by a separate $\overline{\text{PCAS}}$ for that bit. Bit nine is generally used for parity.

FEATURES

- 262,144 x 9 bit organization
- Optional 30 Pad SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC standard pinout
- Common $\overline{\text{CAS}}$, $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ control for the lower eight bits
- Separate $\overline{\text{PCAS}}$ control for D_9 and Q_9



- Power:
 - 1.26 Watt Max Active (70 nSEC)
 - 1.10 Watt Max Active (80 nSEC)
 - .935 Watt Max Active (100 nSEC)
 - 22 mWatt Standby (Max)
- Operating free air temperature: 0° to 70°C
- Upward compatible with AK491024, AK591024, AK594096 and AK5916384
- Functionally and Pin compatible with AK49256
- Available with access times of 60 nSEC to 100 nSEC

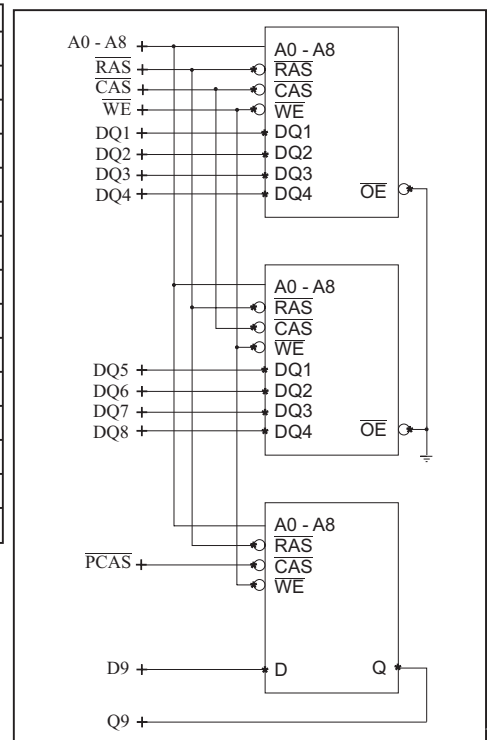
PIN NOMENCLATURE

DQ ₁ - DQ ₈	Data In / Data Out
D ₉	Data In
Q ₉	Data Out
A ₀ - A ₉	Address Inputs
$\overline{\text{CAS}}$, $\overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Write Enable
V _{cc}	5v Supply
V _{ss}	Ground
NC	No Connect

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL
1	V _{cc}	16	DQ ₅
2	$\overline{\text{CAS}}$	17	A ₈
3	DQ ₁	18	NC
4	A ₀	19	NC
5	A ₁	20	DQ ₆
6	DQ ₂	21	$\overline{\text{WE}}$
7	A ₂	22	V _{ss}
8	A ₃	23	DQ ₇
9	V _{ss}	24	NC
10	DQ ₃	25	DQ ₈
11	A ₄	26	Q ₉
12	A ₅	27	$\overline{\text{RAS}}$
13	DQ ₄	28	$\overline{\text{PCAS}}$
14	A ₆	29	D ₉
15	A ₇	30	V _{cc}

FUNCTIONAL DIAGRAM



MODULE OPTIONS

Leadless SIM: AK59256AS
Leaded SIP: AK59256AG

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8																				
1 Product	AK = Accuthek Memory																											
2 Type	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM																											
3 Organization/Word Width	1 = by 1 16 = by 16 4 = by 4 32 = by 32 8 = by 8 36 = by 36 9 = by 9																											
4 Size/Bits Depth	64 = 64K 4096 = 4 MEG 256 = 256K 8192 = 8 MEG 1024 = 1 MEG 16384 = 16 MEG																											
5 Package Type	G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP)																											
6 Special Designation	P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram																											
7 Separator	- = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In																											
8 Speed (first two significant digits)	<table border="0"> <tr> <td>DRAMS</td> <td>SRAMS</td> <td></td> <td></td> </tr> <tr> <td>50 = 50 nS</td> <td>8 = 8 nS</td> <td></td> <td></td> </tr> <tr> <td>60 = 60 nS</td> <td>10 = 10 nS</td> <td></td> <td></td> </tr> <tr> <td>70 = 70 nS</td> <td>12 = 12 nS</td> <td></td> <td></td> </tr> <tr> <td>80 = 80 nS</td> <td>15 = 15 nS</td> <td></td> <td></td> </tr> </table>								DRAMS	SRAMS			50 = 50 nS	8 = 8 nS			60 = 60 nS	10 = 10 nS			70 = 70 nS	12 = 12 nS			80 = 80 nS	15 = 15 nS		
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The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

EXAMPLES:

AK59256AGP-60

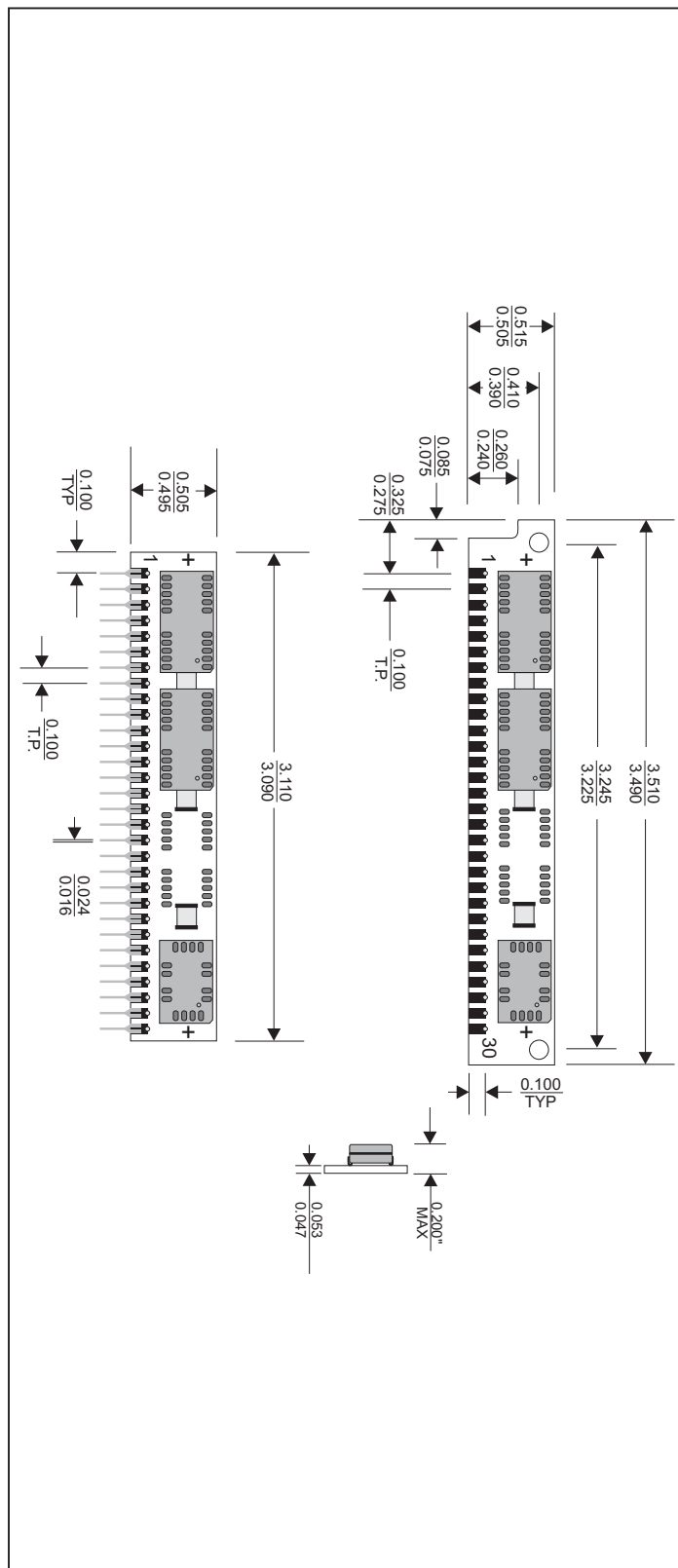
256K x 9, 60 nSEC, DRAM, SIP Configuration, 30 Pin, Page Mode

AK59256ASP-70

256K x 9, 70 nSEC, DRAM, SIM Configuration, 30 Pin, Page Mode

MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.



5 NEW PASTURE ROAD
NEWBURYPORT, MA 01950-4040
PHONE: 978-465-6200 FAX: 978-462-3396
Email: sales@accutekmicro.com
Internet: www.accutekmicro.com