

#### DESCRIPTION

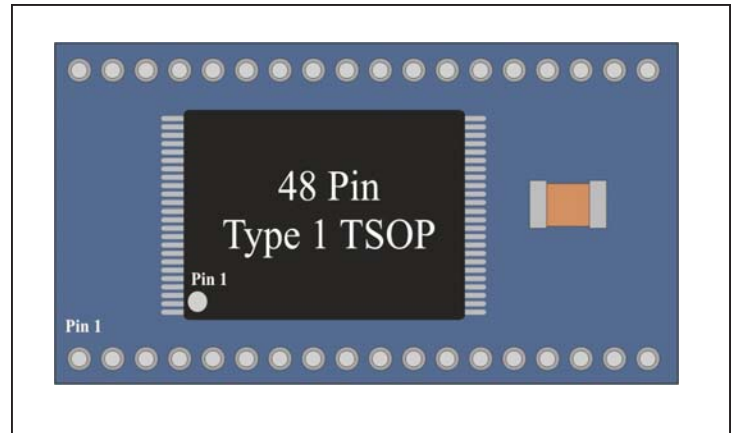
The Accuthek AK682048D high density memory module is a static random access memory organized in 2 Meg x 8 bit words. The assembly consists of one medium speed 2 Meg x 8 SRAM in a Type 1 TSOP package. The module is supplied in a 600 mil wide, 36 pin DIP (Dual In-Line Package) configuration. This pinout is completely compatible with industry standard monolithic designs. These modules are intended for use in applications where limited board space dictates compact module designs.

The operation of the AK682048D is identical to standard monolithic 8 bit word wide SRAMs.

The AK682048D offers the features of low power and medium speed by using CMOS devices and makes high density mounting possible with no surface mount technology.

#### FEATURES

- 2,097,152 x 8 bit organization
- Fast access time: 45 - 70 nSEC
- Completely static RAM, no clock or timing strobe required
- Inputs and outputs TTL compatible
- Conventional 600 mil wide SIP package with industry compatible pinout
- Single 5 volt power supply - AK682048D
- Single 3.3 volt power supply - AK682048D/3.3
- Operating free air temperature 0<sup>0</sup> to 70<sup>0</sup>C



#### ELECTRICAL SPECIFICATIONS

Timing diagrams and basic electrical characteristics are those of the standard 2048 Meg x 8 SRAMs used to construct these modules. Accuthek's module design allows the flexibility of selecting industry-compatible 2048 Meg x 8 SRAMs from any of a number of semiconductor manufacturers.

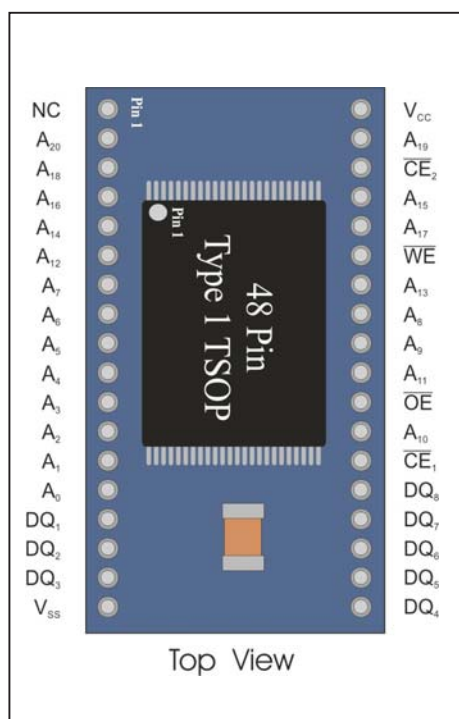
#### PIN NOMENCLATURE

DQ <sub>1</sub> - DQ <sub>8</sub>	Data In/Data Out
A <sub>0</sub> - A <sub>20</sub>	Address Inputs
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
$\overline{WE}$	Write Enable
V <sub>cc</sub>	5v Supply
V <sub>ss</sub>	Ground
$\overline{OE}$	Output Enable

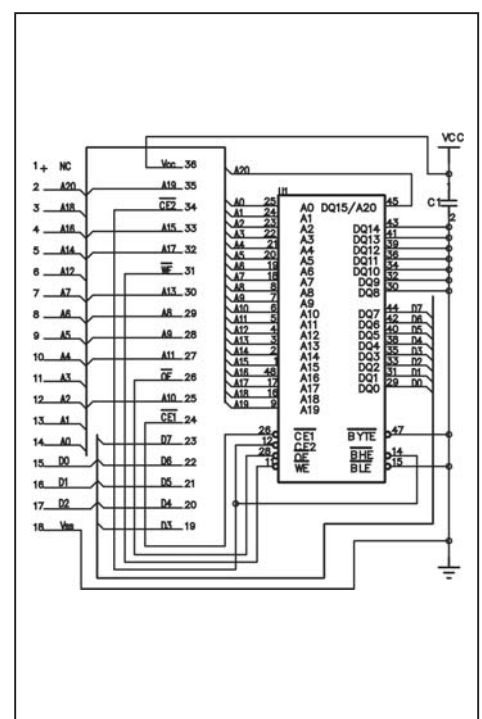
#### TIMING OPTIONS

55 nSEC Access Time
70 nSEC Access Time

#### PIN ASSIGNMENT



#### FUNCTIONAL DIAGRAM



## ORDERING INFORMATION

### PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8
<b>1 Product</b>								
	<b>AK = Accuthek Memory</b>							
<b>2 Type</b>								
	4 = Dynamic RAM							
	5 = CMOS Dynamic RAM							
	6 = Static RAM							
<b>3 Organization/Word Width</b>								
	1 = by 1		16 = by 16					
	4 = by 4		32 = by 32					
	8 = by 8		36 = by 36					
	9 = by 9							
<b>4 Size/Bits Depth</b>								
	32 = 32K		1024 = 1 MEG					
	64 = 64K		4096 = 4 MEG					
	128 = 128K		8192 = 8 MEG					
	256 = 256K		16384 = 16 MEG					
	512 = 512K							
<b>5 Package Type</b>								
	G = Single In-Line Package (SIP)							
	S = Single In-Line Module (SIM)							
	D = Dual In-Line Package (DIP)							
	W = .050 inch Pitch Edge Connect							
	Z = Zig-Zag In-Line Package (ZIP)							
<b>6 Special Designation</b>								
	P = Page Mode							
	N = Nibble Mode							
	K = Static Column Mode							
	W = Write Per Bit Mode							
	V = Video Ram							
<b>7 Separator</b>								
	- = Commercial 0°C to +70°C							
	M = Military Equivalent Screened (-55°C to +125°C)							
	I = Industrial Temperature Tested (-45°C to +85°C)							
	X = Burned In							
<b>8 Speed (first two significant digits)</b>								
	DRAMS		SRAMS					
	50 = 50 nS		8 = 8 nS					
	60 = 60 nS		12 = 12 nS					
	70 = 70 nS		55 = 55 nS					
	80 = 80 nS		70 = 70 nS					

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

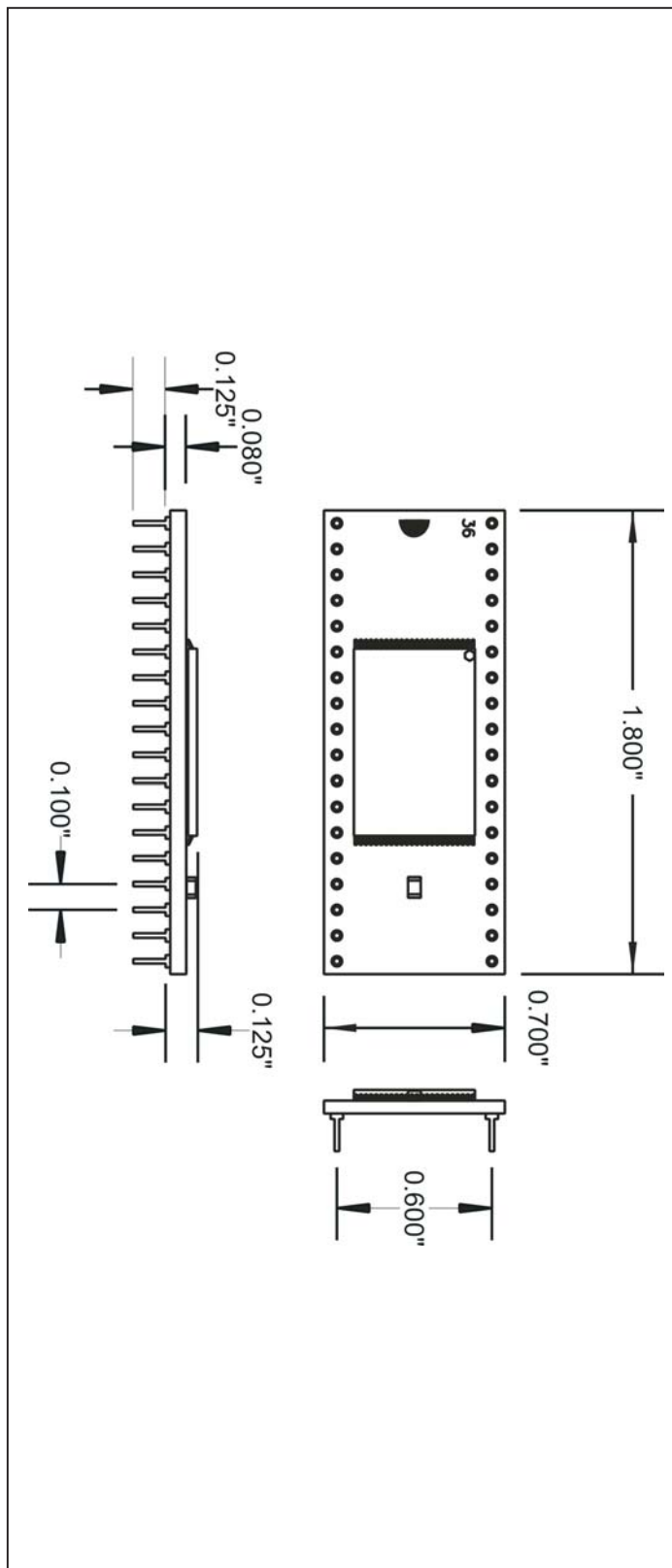
### EXAMPLES:

#### AK682048D-70

2048 x 8, 70 nSEC SRAM Module, DIP Configuration

## MECHANICAL DIMENSIONS

Inches



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Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.