AK7734

Audio DSP with 2-Channel ADC/SRC

GENERAL DESCRIPTION

The AK7734 is a highly integrated audio digital signal processor with integrated 2ch 24bit ADC and 2ch SRC. It includes internal memories for digital audio processing, that allows surround effect process, time alignment and parametric equalizing. More over, the AK7734 can process both data and filter coefficients as floating point data so that high accuracy IIR/FIR filter performance can be achieved easily. The internal SRC has various sampling rate converting modes, corresponds many sampling rates without changing the DSP operating sampling frequency. The AK7734 can operate a hands-free software by AKM, as well as sound processing, by programs downloaded via the microprocessor interface.

FEATURES

[DSP Block]

- **Word length: 24bit (Coefficient RAM & Data RAM: F24 floating point)**
- **Processing Speed: 13.6 ns (1536step/fs; fs = 48kHz)**
- **Multiplication: 20 x 24 → 44-bit Double precision arithmetic available**
- **Divider 20 / 20 → 20bit**
- **ALU: 48bit arithmetic operation (overflow margin 4bit) 20bit floating point arithmetic and logic operation**
- **Program RAM: 3072 x 24bit**
- **Coefficient RAM: 2048 x 24bit (F24 floating point)**
- **Data RAM: 2048 x 24-bit (F24 floating point)**
- **Offset Register: 64 x 13bit**
- **Delay RAM1: 3072 x 24-bit**
- **Delay RAM2: 2048 x 24-bit**
- **Sampling rate: fs= 7.35k ~ 48kHz**
- **Master Clock: 1536fs**
  (generated from 32fs, 48fs, 64fs, 128fs, 256fs, 384fs by internal PLL)
- **Master/Slave Operation**

[ADC Block]

- **64 times Over sampling**
- **24bit 2ch**
- **Sampling rate: 7.35 ~ 48kHz**
- **S/(N+D): 83dB (fs = 48kHz)**
- **DR, S/N: 96dB (fs = 48kHz)**
- **Integrated DC offset canceling High Pass Filter**

[SRC Block]

- **2ch x 1 system**
- **Support frequency: Fin = 7.35kHz ~ 96kHz → Fout = 7.35kHz ~ 48kHz**
  (FSO/FSI = 0.167~ 6.0)

[Digital Interface Input/Output]

- **8ch Serial Data Input**
- **8ch Serial Data Output**

[Micro Computer Interface]

- I^2C Interface or 4-wired Interface

[General]

- Integrated PLL
- Integrated Regulator 3.3V → 1.8V
- Power Supply: 3.3V ± 0.3V
- Operating Temperature Range: -40˚C ~ 85˚C
- 48pin LQFP

■ Block Diagram

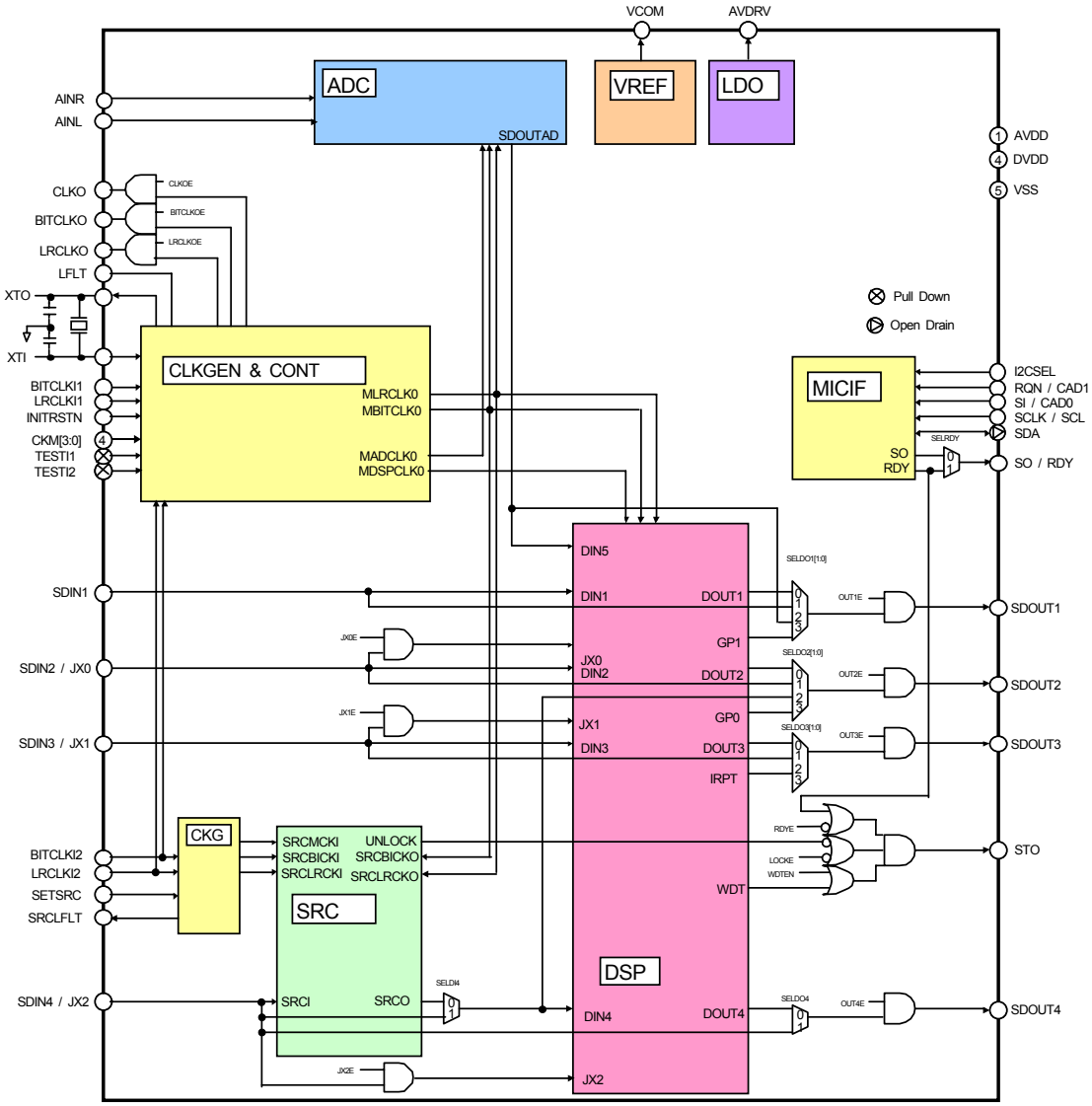


Figure 1. Block Diagram

* Figure 1 shows a simplified diagram of the AK7734, which is not the perfect same as the actual circuit diagram.

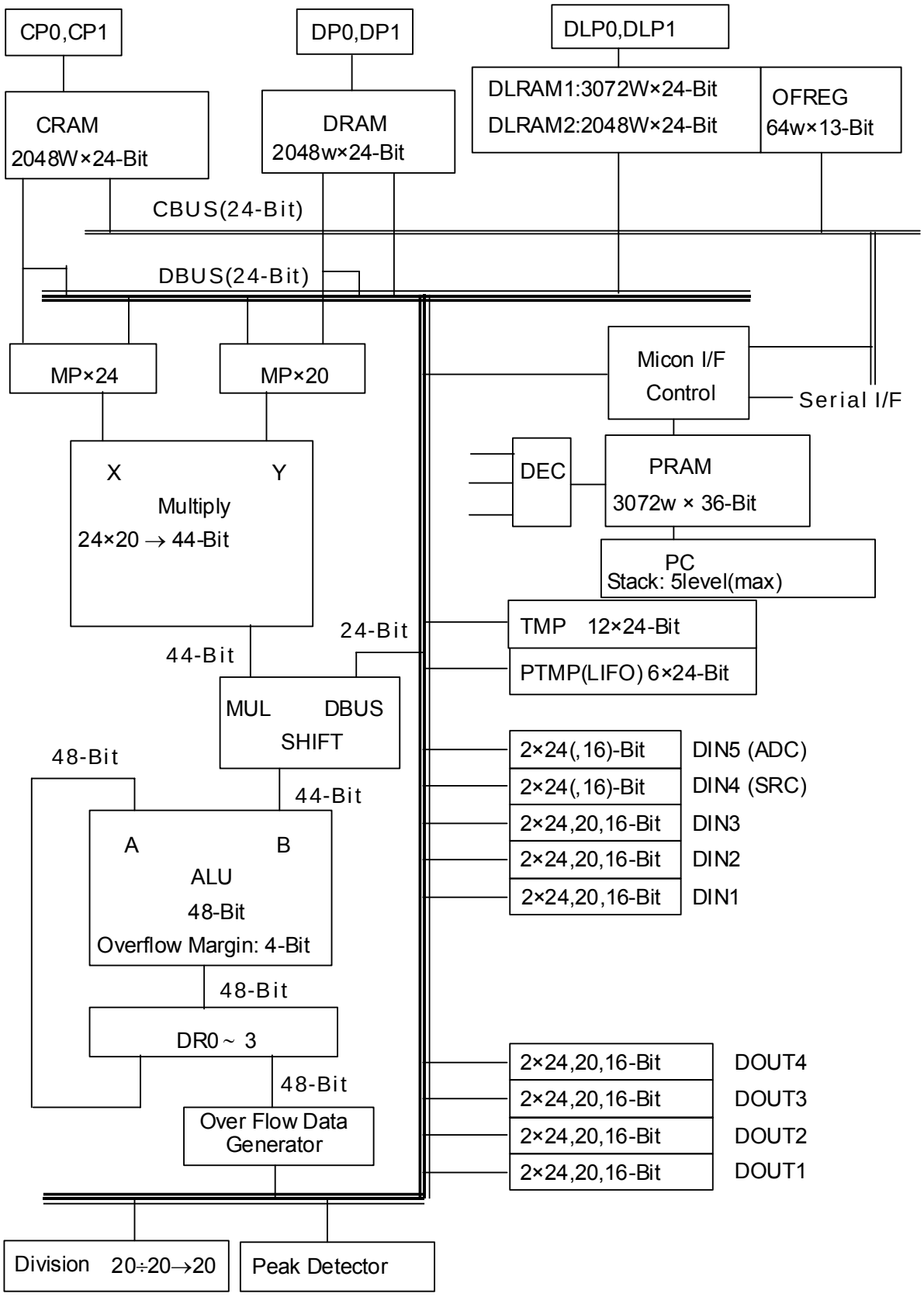
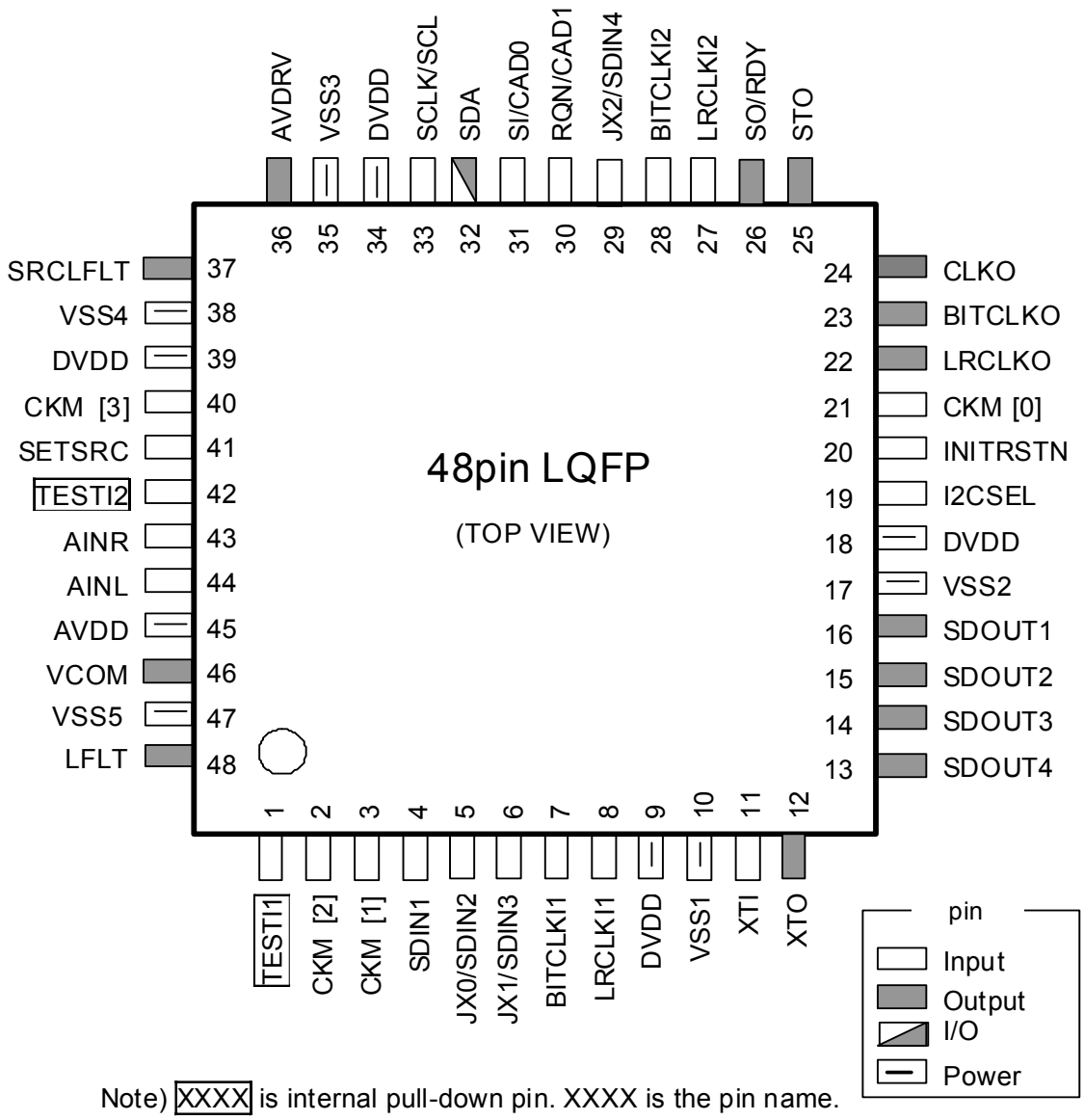


Figure 2. Main DSP Block Diagram of The AK7734

■ Ordering Guide

AK7734XQ	-40 ~ +85°C	48pin LQFP
AKD7734	Evaluation Board for AK7734	

■ Pin Layout



Note) XXXX is internal pull-down pin. XXXX is the pin name.

PIN FUNCTION

No.	Name	I/O	Function	Classification
1	TESTI1	I	Test1 Pin (Internal pull-down) This pin must be connected to VSS.	Test
2	CKM[2]	I	Clock Mode Select Pin2	Mode Select
3	CKM[1]	I	Clock Mode Select Pin1	Mode Select
4	SDIN1	I	Serial Data Input Pin1	Digital Input
5	JX0	I	Conditional Jump Pin0 A conditional jump pin (JX0) is available by setting control register (JX0E) to "1".	Conditional Input
	SDIN2	I	Serial Data Input Pin2	Digital Input
6	JX1	I	Conditional Jump Pin1 A conditional jump pin (JX1) is available by setting control register (JX1E) to "1".	Conditional Input
	SDIN3	I	Serial Data Input Pin2	Digital Input
7	BITCLKI1	I	Serial Bit Clock Input Pin1 Normally connected to the Bluetooth Data Clock line (256kHz/512kHz).	System Clock
8	LRCLKI1	I	LR Channel Select Clock Pin1 Normally connected to the Bluetooth LR Clock line (8kHz).	System Clock
9	DVDD	-	Power Supply for Digital Section 3.0V ~ 3.6V	Digital Power Supply
10	VSS1	-	Ground Pin 0V	Power Supply
11	XTI	I	Crystal oscillator input pin Connect a crystal oscillator between this pin and the XTO pin, or input an external clock to the XTI pin.	Clock
12	XTO	O	Crystal oscillator output pin When a crystal oscillator is used, connect it between XTI and XTO. When an external clock is used, leave this pin open. During initial reset, the output of this pin is not determinable.	Clock
13	SDOUT4	O	Serial Data Output Pin4 Outputs "L" during initial reset.	Digital Output
14	SDOUT3	O	Serial Data Output Pin3 Outputs "L" during initial reset.	Digital Output
15	SDOUT2	O	Serial Data Output Pin2 Outputs "L" during initial reset.	Digital Output
16	SDOUT1	O	Serial Data Output Pin1 Outputs "L" during initial reset.	Digital Output
17	VSS2	-	Ground Pin 0V	Power Supply
18	DVDD	-	Power Supply for Digital Section 3.0V ~ 3.6V	Digital Power Supply
19	I2CSEL	I	I^2C BUS Select Pin (Internal pull-down) I2CSEL pin = "L": 4-wired Interface I2CSEL pin = "H": I2CBus selected mode. SCL and SDA are active. I2CSEL should be connected to "L" (VSS) or "H" (DVDD).	I^2C Select
20	INITRSTN	I	Reset Pin (for initialization) Use to initialize the AK7734. When changing CKM [3:0] and changing XTI or BITCLK input frequency, it is necessary to set this pin.	Reset
21	CKM[0]	I	Clock Mode Select Pin	Mode Select
22	LRCLKO	O	LR Channel Select Clock Pin Outputs "L" during initial reset in master mode.	System Clock Output

No.	Name	I/O	Function	Classification
23	BITCLKO	O	Serial Bit Clock Output Pin Outputs "L" during initial reset in master mode.	System Clock Output
24	CLKO	O	Clock Output Pin Outputs "L" during initial reset.	Clock Output
25	STO	O	Status Output Pin Outputs "H" during initial reset.	Status
26	SO	O	Serial Data Output Pin for Microprocessor Interface Outputs "L" during initial reset.	Microprocessor Interface
	RDY	O	Data Write Ready Output Pin for Microprocessor Interface Outputs RDY when SELRDY bit = "1"	Microprocessor Interface
27	LRCLKI2	I	LR Channel Select Clock Pin2 (for SRC)	System Clock Input
28	BITCLKI2	I	Serial Bit Clock Input Pin2 (for SRC)	System Clock Input
29	JX2	I	Conditional Jump Pin2 A conditional jump pin (JX2) is available by setting control register (JX2E) to "1".	Conditional Input
	SDIN4	I	Serial Data Input Pin4 Normally used for SRC serial data input pin.	Digital Input
30	RQN	I	Microprocessor Interface Write Request Pin (I2CSEL pin = "L") When initial reset state and Microcomputer interface are not in use, leave RQN pin= "H".	Microprocessor Interface
	CAD1	I	I^2C Bus Address Setting Pin 1 (I2CSEL pin = "H")	I^2C
31	SI	I	Serial Data Input Pin for Microprocessor Interface (I2CSEL pin = "L") When SI is not used, tie the SI pin = "L".	Microprocessor Interface
	CAD0	I	I^2C Bus Address Setting Pin 0 (I2CSEL pin = "H")	I^2C
32	SDA	O	I2CSEL pin = "L" Leave this pin Open. SDA outputs "L".	Open
		I/O	I^2C Bus Data Clock Pin (I2CSEL pin = "H") Outputs "Hi-z" during initial reset.	I^2C
33	SCLK	I	Serial Data Clock Pin for Microprocessor Interface (I2CSEL pin = "L") When SCLK is not used, tie the SCLK pin = "H".	Microprocessor Interface
	SCL	I	I^2C Bus Data Clock Pin (I2CSEL pin = "H")	I^2C
34	DVDD	-	Power Supply for Digital Section 3.0V ~ 3.6V	Digital Power Supply
35	VSS3	-	Ground Pin 0V	Power Supply
36	AVDRV	O	AVDRV Pin Connect a 1μF capacitor between this pin and No.35 pin (VSS3). No external circuits should be connected to this pin. This pin outputs "L" during initial reset.	Analog Output
37	SRCLFLT	O	SRC, PLL RC component connect pin Connect a 1μF capacitor between this pin and VSS4. This pin outputs "L" during initial reset.	Analog Output
38	VSS4	-	Ground Pin 0V	Power Supply
39	DVDD	-	Power Supply for Digital Section 3.0V ~ 3.6V	Digital Power Supply
40	CKM[3]	I	Clock Mode Select Pin3	Mode Select
41	SETSRC	I	PLL Reference Clock Select Pin for SRC	Mode Select
42	TESTI2	I	Test2 Pin (Internal pull-down) This pin must be connected to VSS.	Test
43	AINR	I	ADC Single-ended Input Pin for Rch	Analog Input

No.	Name	I/O	Function	Classification
44	AINL	I	ADC Single-ended Input Pin for Lch	Analog Input
45	AVDD	I	Analog Ground 0V	Analog Power Supply
46	VCOM	O	Analog Common Voltage Output pin Connect 0.1μF and 2.2μF capacitors between this pin and No.47 pin (VSS5). No external circuits should be connected to this pin. This pin outputs "L" during initial reset.	Analog Output
47	VSS5	I	Ground Pin 0V	Power Supply
48	LFLT	O	PLL RC component connect pin Connect C=12nF between this pin and No.47 (VSS5). This pin outputs "L" during initial reset.	Analog Output

Note:
- Do NOT leave digital input pins open.
- When analog input pins (AINL, AINR) are not used, leave them open.

■ Handling of Unused Pin

The following table illustrates recommended states for open pins:

Classification	Pin Name	Setting
Analog	AINL, AINR	Leave Open.
Digital	SDOUT1-4, CLKO, LRCLKO, BITCLKO, STO, SO/RDY, XTO	Leave Open.
	TESTI1, TESTI2, SDIN1, JX0-2/SDIN2-4, XTI, BITCLKI1-2, LRCLKI1-2	Connect to VSS.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=VSS5=0V: Note 1)

Parameter	Symbol	min	max	Units
Power Supply Voltage				
Analog	AVDD	-0.3	4.3	V
Digital	DVDD	-0.3	4.3	V
Input Current (except for power supply pin)	IIN	–	±10	mA
Analog Input Voltage AINL pin, AINR pin	VINA	-0.3	AVDD+0.3	V
Digital Input Voltage	VIND	-0.3	DVDD+0.3	V
Operating Ambient Temperature	Ta	-40	85	ºC
Storage Temperature	Tstg	-65	150	ºC

Note 1. All indicated voltages are with respect to ground.
Note 2. VSS1-5 must be connected to the same ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=VSS5=0V: Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply Voltage					
Analog	AVDD	3.0	3.3	3.6	V
Digital	DVDD	3.0	3.3	3.6	V

Note 3. The power supply sequence for AVDD and DVDD is not critical but all power supplies must be On before start operating the AK7734.
Note 4. Do not turn off the power supply of the AK7734 with the power supply of the surrounding device turned on. DVDD must not exceed the pull-up of SDA and SCL of I2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

ELECTRIC CHARACTERISTICS

(1) Analog Characteristics

1) ADC

1-1) fs=8kHz

(Ta=25ºC; AVDD=DVDD=3.3V, BITCLK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~3.4kHz @fs=8kHz; CKM mode0(CKM[3:0]=LLLL) Unless otherwise specified.)

Parameter		min	typ	max	Units
ADC Section	Resolution			24	Bits
	Dynamic Characteristics				
	S/(N+D) (-1dBFS)	76	84		dB
	Dynamic Range (Note 5)	84	92		dB
	S/N	84	92		dB
	Inter-Channel Isolation (fin=1kHz) (Note 6)	90	110		dB
	DC accuracy				
	Channel Gain Mismatch		0.1	0.3	dB
	Analog Input				
	Input Voltage (Note 7)	1.85	2.00	2.15	Vp-p
	Input Impedance	38	58		kΩ

Note 5. - S/(N+D) when -60dB FS signal is applied.
Note 6. Inter-channel isolation between AINR and AINL at –1dB FS signal input.
Note 7. Full scale output voltage is FS=AVDD×2.0/3.3.

1-2) fs=48kHz

(Ta=25ºC; AVDD=DVDD=3.3V, BITCLK=64fs; Signal frequency 1kHz; Measurement frequency =20Hz~20kHz @fs=48kHz; CKM mode0(CKM[3:0]=LLLL) Unless otherwise specified.)

Parameter		min	typ	max	Units
ADC Section	Resolution			24	Bits
	Dynamic Characteristics				
	S/(N+D) (-1dBFS)	75	83		dB
	Dynamic Range (Filter A) (Note 8)	87	96		dB
	S/N (Filter A)	87	96		dB
	Inter-Channel Isolation (fin=1kHz) (Note 9)	90	110		dB
	DC accuracy				
	Channel Gain Mismatch		0.1	0.3	dB
	Analog Input				
	Input Voltage (Note 10)	1.85	2.00	2.15	Vp-p
	Input Impedance	23	35		kΩ

Note 8. - S/(N+D) when -60dBFS signal is applied.
Note 9. Inter-channel isolation between AINR and AINL at –1dB FS signal input.
Note 10. Full scale output voltage is FS=AVDD×2.0/3.3.

(2) SRC

(Ta=25ºC; AVDD = DVDD=3.3V; VSS=0V, data = 24bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Units
Resolution				24	Bits
Input Sample Rate	FSI	7.35		96	kHz
Output Sample Rate	FSO	7.35		48	kHz
THD+N (Input= 1kHz, 0dBFS)					
FSO/FSI=44.1kHz/48kHz			-112		dB
FSO/FSI=44.1kHz/96kHz			-104		dB
FSO/FSI=48kHz/44.1kHz			-112		dB
FSO/FSI=48kHz/96kHz			-112		dB
FSO/FSI=48kHz/8kHz			-111	-103	dB
FSO/FSI=8kHz/48kHz			-113		dB
FSO/FSI=8kHz/44.1kHz			-78		dB
Dynamic Range (Input= 1kHz, -60dBFS)					
FSO/FSI=44.1kHz/48kHz			113		dB
FSO/FSI=44.1kHz/96kHz			113		dB
FSO/FSI=48kHz/44.1kHz			113		dB
FSO/FSI=48kHz/96kHz			113		dB
FSO/FSI=48kHz/8kHz		109	112		dB
FSO/FSI=8kHz/48kHz			113		dB
FSO/FSI=8kHz/44.1kHz			113		dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted					
FSO/FSI=44.1kHz/48kHz			115		dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

(3) DC Characteristics

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Units
High Level Input Voltage (Note 11)	VIH	80%DVDD			V
Low Level Input Voltage (Note 11)	VIL			20%DVDD	V
SCL,SDA High Level Input Voltage	VIH	70%DVDD			V
SCL,SDA Low Level Input Voltage	VIL			30%DVDD	V
High Level Output Voltage Iout=-100µA	VOH	DVDD-0.5			V
Low Level Output Voltage Iout=100µA (Note 12)	VOL			0.5	V
SDA Low Level Output Voltage Iout=3mA	VOL			0.4	V
Input Leak Current (Note 13)	Iin			±10	µA
Input Leak Current (pull-down pin) (Note 14)	Iid		22		µA
Input Leak Current (XTI pin)	Iix		26		µA

Note 11. SCL and SDA pins are not included. (SCLK pins are included)
Note 12. SDA pin is not included.
Note 13. Pull-down pins, and the XTI pin is not included.
Note 14. TESTI1 and TESTI2 pins are internal pulled-down pin. (Typ150kΩ)

(4) Current Consumption

(Ta=25ºC; AVDD=DVDD=3.0~3.6V (when typ=3.3V, max=3.6V))

Parameter	min	typ	max	Units
Power Supply Current (Note 15)				
AVDD		21		mA
DVDD		65		mA
AVDD+DVDD		86	120	mA
INITRSTN pin= "L" (reference) (Note 16)		2		mA

Note 15. The current of DVDD changes depending on the system frequency and contents of the DSP program.

Note 16. This is a reference value when using a crystal oscillator. Since most of the supply current at the initial reset state are in the oscillator section, the value may vary according to the crystal type and the external circuit. This is a "reference data" only.

DIGITAL FILTER CHARACTERISTICS

■ ADC Section

1. fs=8kHz

(Ta=-40ºC ~85ºC, AVDD=DVDD=3.0~3.6V, fs=8kHz; Note 17)

Parameter	Symbol	min	typ	max	Units
Passband (±0.1dB) (Note 18)	PB	0		3.15	kHz
(-1.0dB)			3.63		kHz
(-3.0dB)			3.83		kHz
Stopband	SB	4.66			kHz
Passband Ripple (Note 18)	PR			±0.1	dB
Stopband Attenuation (Note 19, Note 20)	SA	68			dB
Group Delay Distortion	ΔGD		0		μs
Group Delay (Ts=1/fs)	GD		16		Ts

Note 17. Frequency of each amplitude characteristic is in proportion to fs (sampling rate). The characteristic of the high pass filter is not included.

Note 18. The passband is from DC to 3.15kHz when fs=8kHz.

Note 19. The stopband is 4.66kHz to 507.34kHz when fs=8kHz.

Note 20. When fs = 8kHz, the analog modulator samples the input signal at 512kHz. There is no attenuation of an input signal in band (n x 512kHz ±4.66kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

2. fs=48kHz

(Ta=-40ºC~85ºC, AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Units
Passband (±0.1dB) (Note 21)	PB	0		18.9	kHz
(-1.0dB)			20.0		kHz
(-3.0dB)			23.0		kHz
Stopband	SB	28			kHz
Passband Ripple (Note 21)	PR			±0.04	dB
Stopband Attenuation (Note 22,Note 23)	SA	68			dB
Group Delay Distortion	ΔGD		0		μs
Group Delay (Ts=1/fs)	GD		16		Ts

Note 21. The passband is from DC to 18.9kHz when fs=48kHz.

Note 22. The stopband is 28kHz to 3.044MHz when fs=48kHz.

Note 23. When fs = 48kHz, the analog modulator samples the input signal at 512kHz. There is no attenuation of an input signal in band (n x 3.072MHz ±28kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Units
XTI CKM[3:0]=0000, 0001, 0010					
a) with a Crystal Oscillator:					
CKM[3:0]=0000 fs=44.1kHz fs=48kHz	fXTI	-	11.2896 12.288	-	MHz
CKM[3:0]=0001 fs=44.1kHz fs=48kHz	fXTI	-	16.9344 18.432	-	MHz
b) with an External Clock					
Duty Cycle		40	50	60	%
CKM[3:0]=0000, 0010 fs=44.1kHz fs=48kHz	fXTI	11.0	11.2896 12.288	12.4	MHz
CKM[3:0]=0001 fs=44.1kHz fs-48kHz	fXTI	16.5	16.9344 18.432	18.6	MHz
LRCLKI1 Frequency (Note 24)	fs	7.35		48	kHz
BITCLKI1 Frequency					
a) CKM[3:0]=0010			64		fs
High Level Width	tBCLKH	64			ns
Low Level Width	tBCLKL	64			ns
Frequency	fBCLK	0.46	3.072	3.1	MHz
b) CKM[3:0]=0011 (Note 25)			64		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	2.75	3.072	3.1	MHz
c) CKM[3:0]=0100 (Note 26)			32		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	230	256	258	kHz
d) CKM[3:0]=0101 (Note 25)			64		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	460	512	516	kHz
e) CKM[3:0]=1001 (Note 27)			48		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	2.06	2.304	2.32	MHz
f) CKM[3:0]=1010 (Note 27)			48		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	345	384	387	kHz
LRCLKI2 Frequency (Note 24)	fs	7.35		48	kHz
BITCLKI2 Frequency					
a) CKM[3:0]=1011 (Note 25)			64		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	2.75	3.072	3.1	MHz
b) CKM[3:0]=1100 (Note 26)			32		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	230	256	258	kHz
c) CKM[3:0]=1101 (Note 25)			64		fs
Duty Cycle		40	50	60	%
Frequency	fBCLK	460	512	516	kHz

Note 24. LRCK frequency and sampling rate (fs) should be the same.
Note 25. When BITCLK is a source of master clock, it should be 64 times fs correctly. (64fs fixed)
Note 26. When BITCLK is a source of master clock, it should be 32 times fs correctly. (32fs fixed)
Note 27. When BITCLK is a source of master clock, it should be 48 times fs correctly. (48fs fixed)

■ SRC Input Clock

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V; VSS=0V)

Parameter	Symbol	min	typ	max	Units
LRCLKI2 Frequency	fs	7.35		96	kHz
BITCLKI2 Frequency					
Frequency	fBCLK	0.23	3.072	6.144	MHz
High Level Width	tBCLKH	32			ns
Low Level Width	tBCLKL	32			ns

■ Reset

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Units
INITRSTN (Note 28)	tRST	600			ns

Note 28. It must be “L” when power-up the AK7734.

■ Audio Interface (SDIN1-4, SDOUT1-4)

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V, CL=20pF)

Parameter	Symbol	min	typ	max	Units
DSP Section Input SDIN1-4 (Note 29)					
Delay Time from BICLKI1 "↑" to LRCLKI1 (Note 30, Note 31)	tBLRD	20			ns
Delay Time from LRCLKI1 to BITCLKI1 "↑" (Note 30, Note 31)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	80			ns
Serial Data Input Latch Hold Time	tBSIDH	80			ns
SRC Section Input SDIN4 (Note 32)					
Delay Time from BICLKI2 "↑" to LRCLKI2 (Note 33)	tBLRD	20			ns
Delay Time from LRCLKI2 to BITCLKI2 "↑" (Note 33)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	40			ns
Serial Data Input Latch Hold Time	tBSIDH	40			ns
Output SDOUT1-4 (Note 29)					
BITCLKO Frequency	fBCLK		64		fs
BITCLKO Duty Factor			50		%
Delay Time from BITCLKO "↓" to LRCLKO (Note 34)	tBLRD	-20		40	ns
Delay Time from LRCLKI1 to Serial Data Output (Note 35)	tLRD			80	ns
Delay Time from BITCLKI1 to Serial Data Output (Note 31)	tBSOD			80	ns
Delay Time from LRCLKO to Serial Data Output (Note 35)	tLRD			80	ns
Delay Time from BITCLKO to Serial Data Output (Note 31)	tBSOD			80	ns
SDINn →SDOUTn (n=1-4) (Note 36)					
Delay Time from SDINn to SDOUTn Output	tIOD			60	ns

Note 29. In CKM modeB/C/D, LRCLKI2=LRCLKI1, BITCLKI2=BITCLKI1.
Note 30. BITCLKI1 edge must not occur at the same time as LRCLKI1 edge.
Note 31. In PCM mode 0/2, BITCLKI1 is polarity reversal.
Note 32. Except CKM mode B/C/D.
Note 33. BITCLKI2 edge must not occur at the same time as LRCLKI2 edge. When BIEDGE bit= "1", this value is for BITCLKI2 "↓" since BITCLK2 is polarity reversal.
Note 34. When SELBCK bit= "1", this value is for BITCLKO "↑" since BITCLKO is polarity reversal.
Note 35. Except I^2S.
Note 36. When SDIN1 → SDOUT1: Control Register Setting SELDO1[1:0] bit= "01", OUT1E bit= "1"
SDIN2 → SDOUT2: Control Register Setting SELDO2[1:0] bit = "01", OUT2E bit= "1"
SDIN3 → SDOUT3: Control Register Setting SELDO3[1:0] bit= "01", OUT3E bit= "1"
SDIN4 → SDOUT4: Control Register Setting SELDO4 bit= "1", OUT4E bit= "1"

■ Microprocessor Interface

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V; VSS=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Units
Microprocessor Interface Signal					
RQN Fall Time	tWRF			30	ns
RQN Rise Time	tWRR			30	ns
SCLK Fall Time	tSF			30	ns
SCLK Rise Time	tSR			30	ns
SCLK Frequency	fSCLK			2.1	MHz
SCLK Low Level Width SCLK High Level Width	tSCLKL tSCLKH	200 200			ns ns
Microprocessor → AK7734 RQN High Level Width	 tWRQH	 500			 ns
From RQN "↓" to SCLK "↓" From SCLK "↑" to RQN "↑"	tWSC tSCW	500 800			ns ns
SI Latch Setup Time SI Latch Hold Time	tSIS tSIH	200 200			ns ns
AK7734 → Microprocessor					
Deley Time from SCLK "↓"to SO Output	tSOS			200	ns
Hold Time from SCLK "↑" to SO Output (Note 37)	tSOH	200			ns

Note 37. Except for, when writing to 8th bit of command code.

■ I²C BUS Interface

(Ta=-40ºC~85ºC; AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
I²C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 38. I²C-bus is a trademark of NXP B.V.

■ **Timing Diagram**

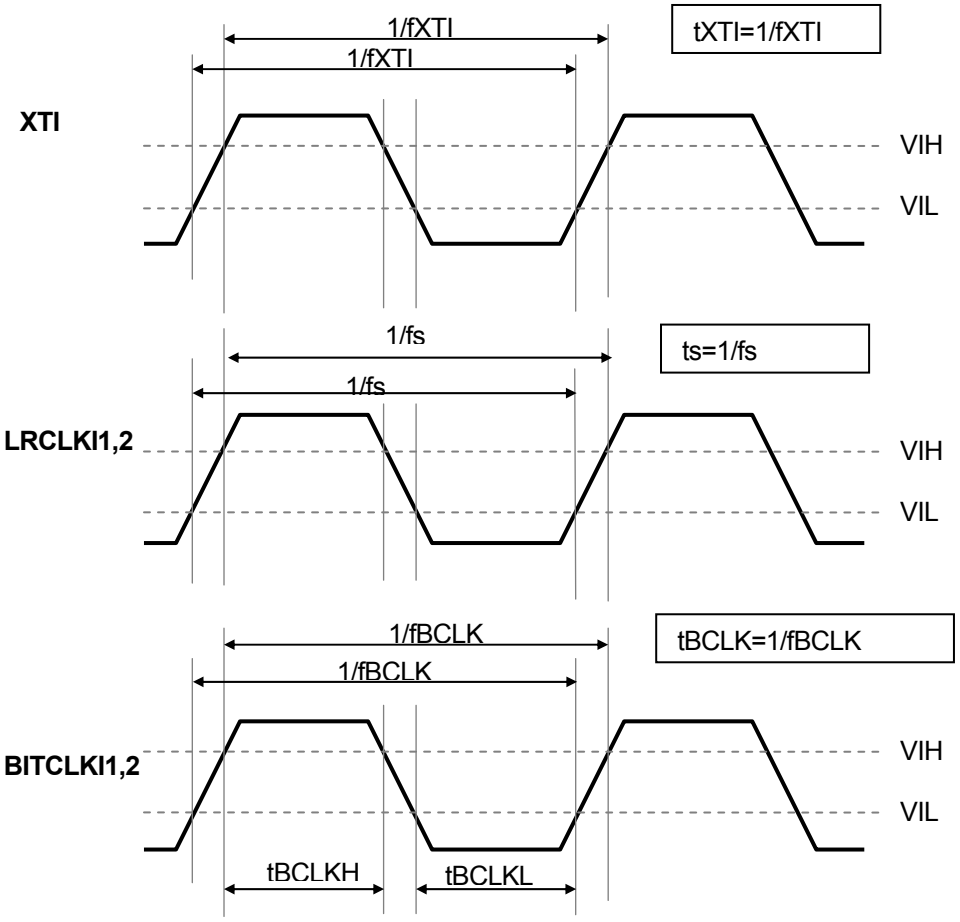


Figure 3. System Clock

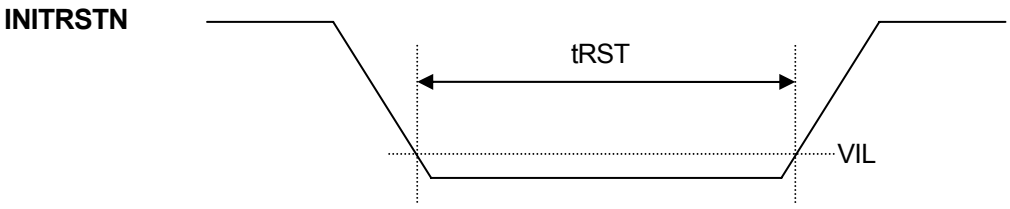


Figure 4. Reset

Note 39. The INITRSTN pin must be "L" when power-up/power-down the AK7734.

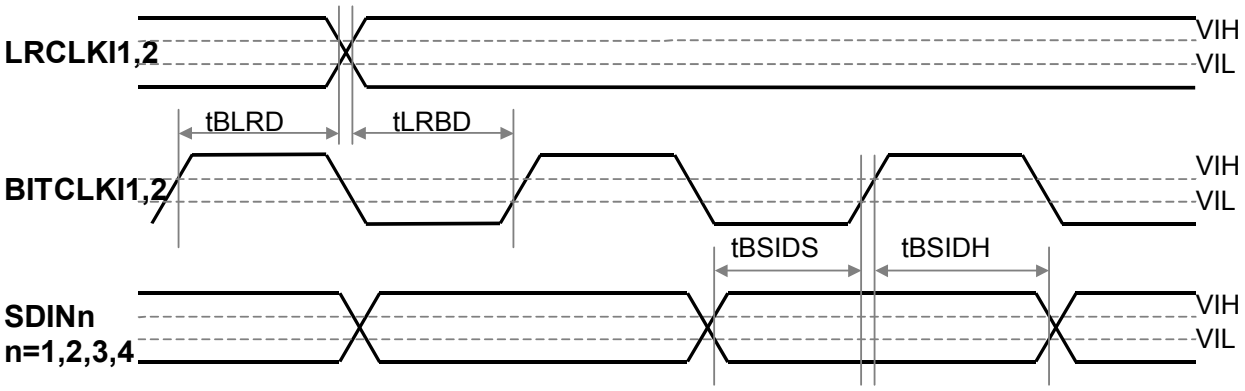


Figure 5. Audio Interface (DSP Section Slave Mode Input)

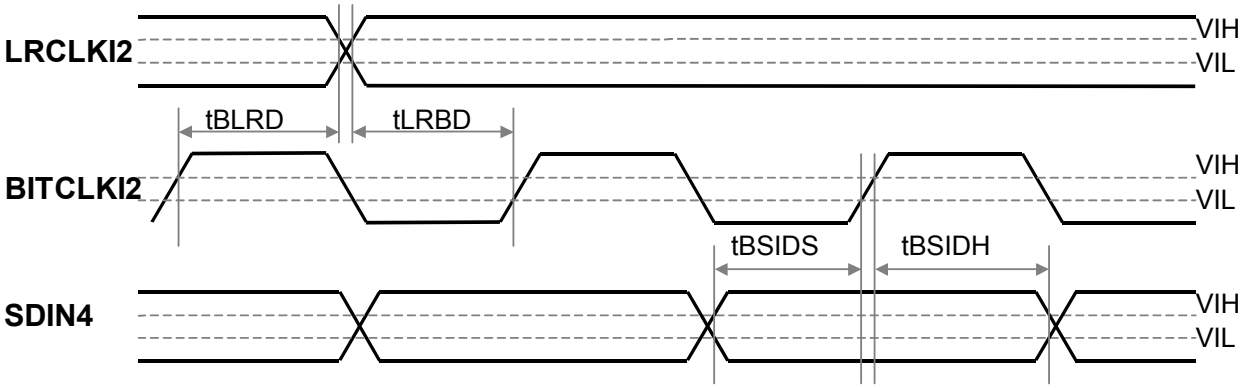


Figure 6. Audio Interface (SRC Section Input)

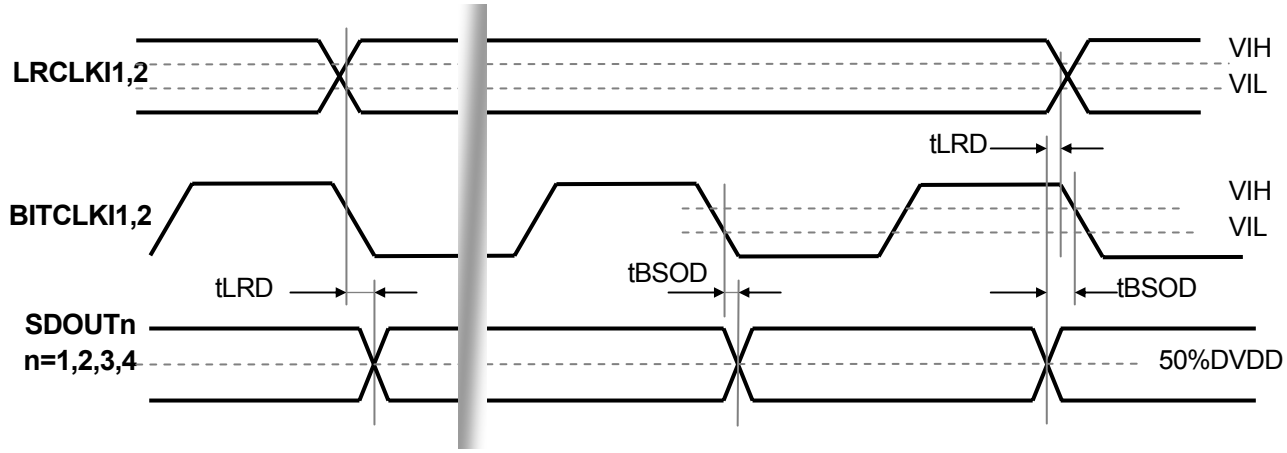


Figure 7. Audio Interface (Slave Mode Output)

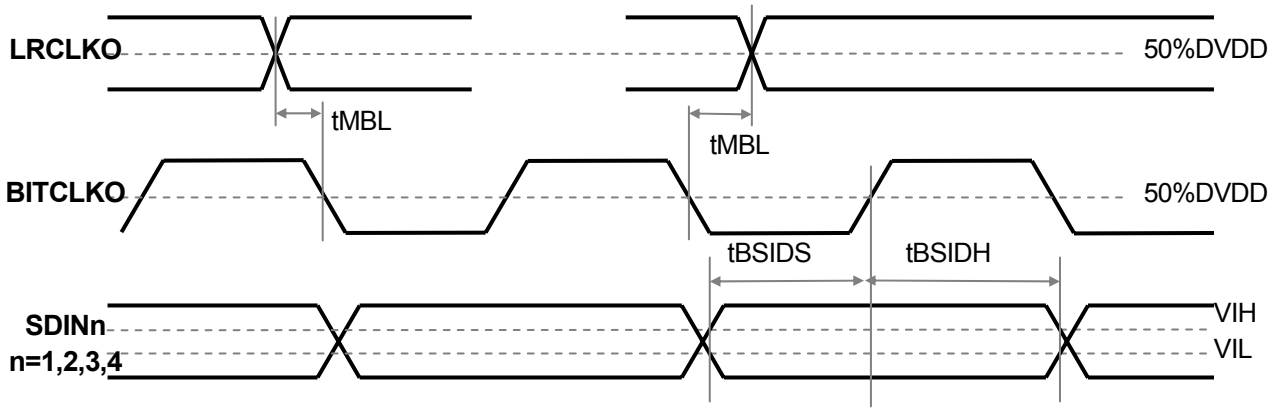


Figure 8. Audio Interface (Master Mode Input)

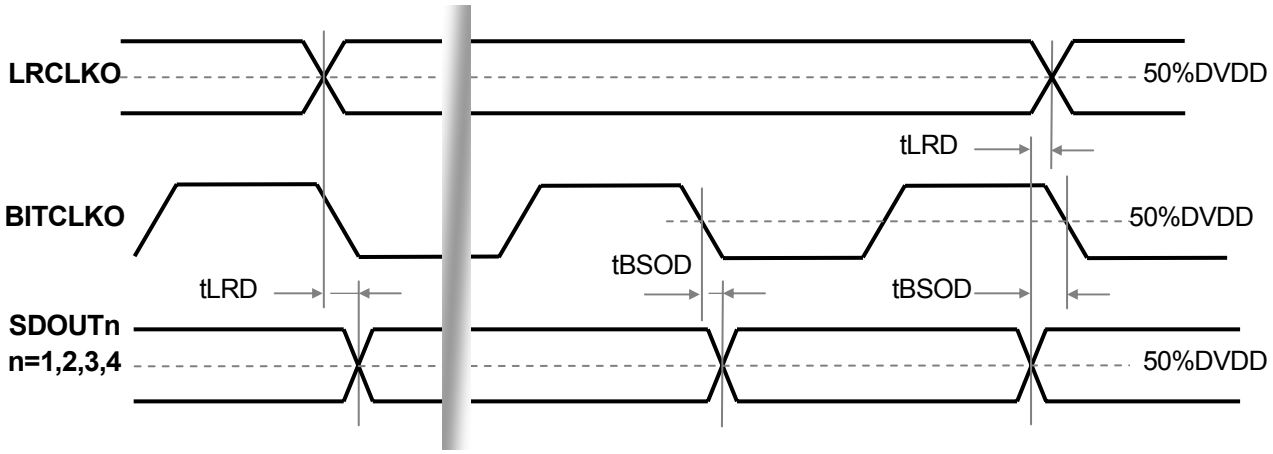


Figure 9. Audio Interface (Master Mode Output)

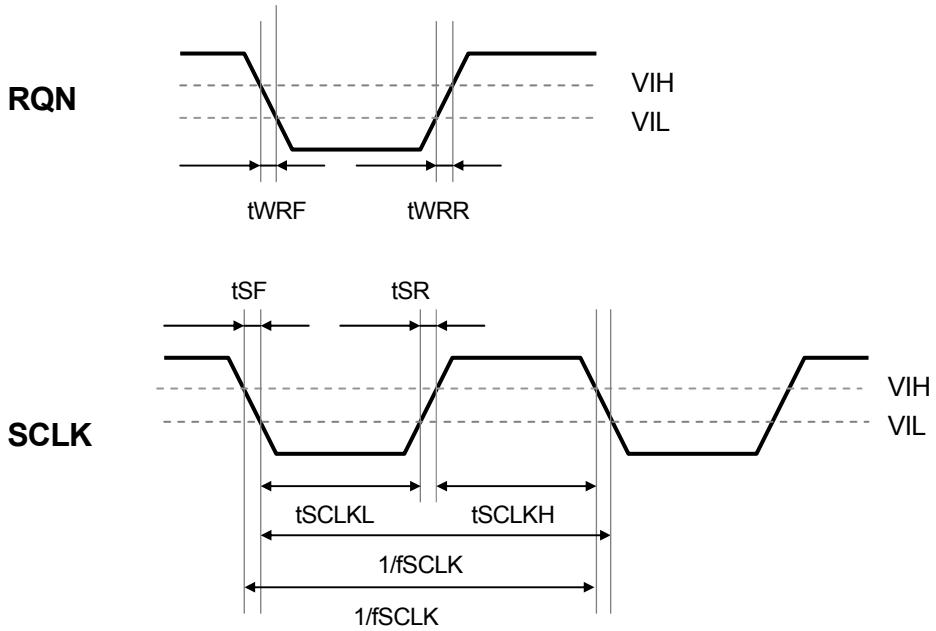


Figure 10. Microprocessor Interface

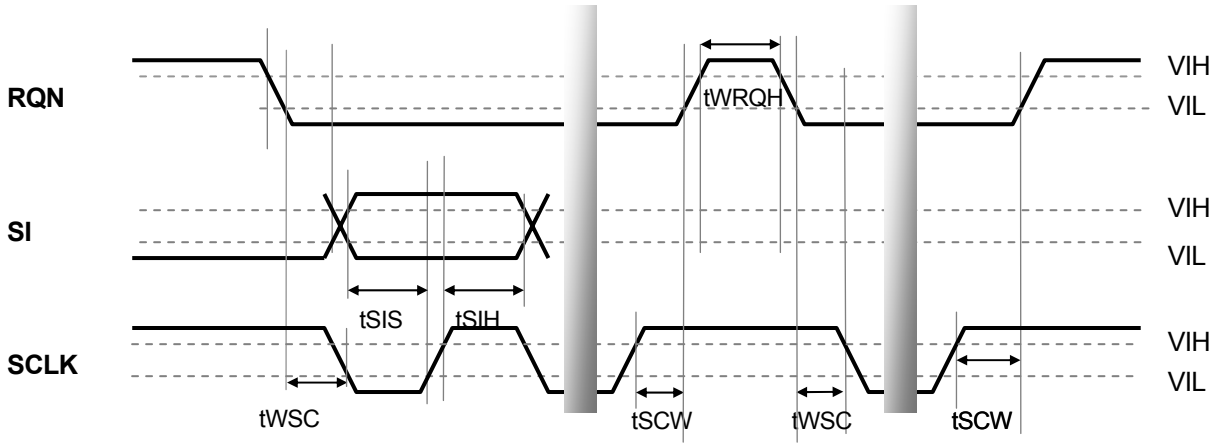


Figure 11. Microprocessor Interface (Microprocessor → AK7734)

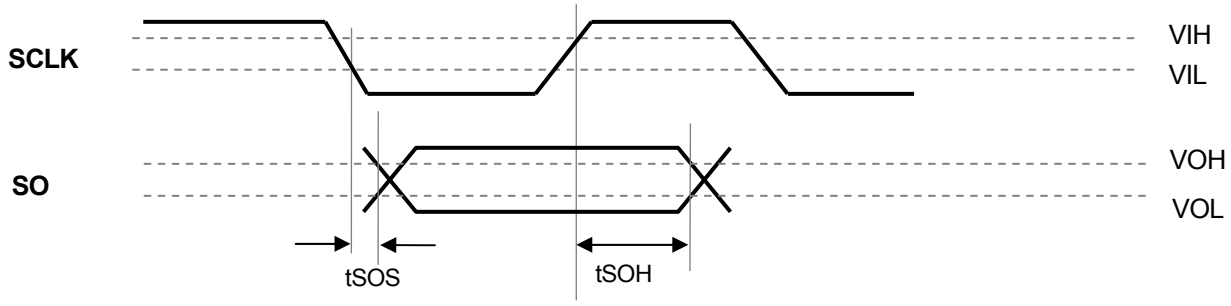


Figure 12. Microprocessor Interface (AK7734 → Microprocessor)

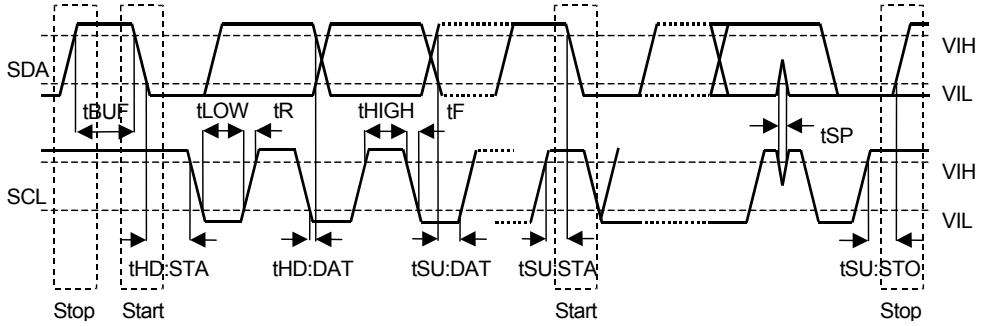
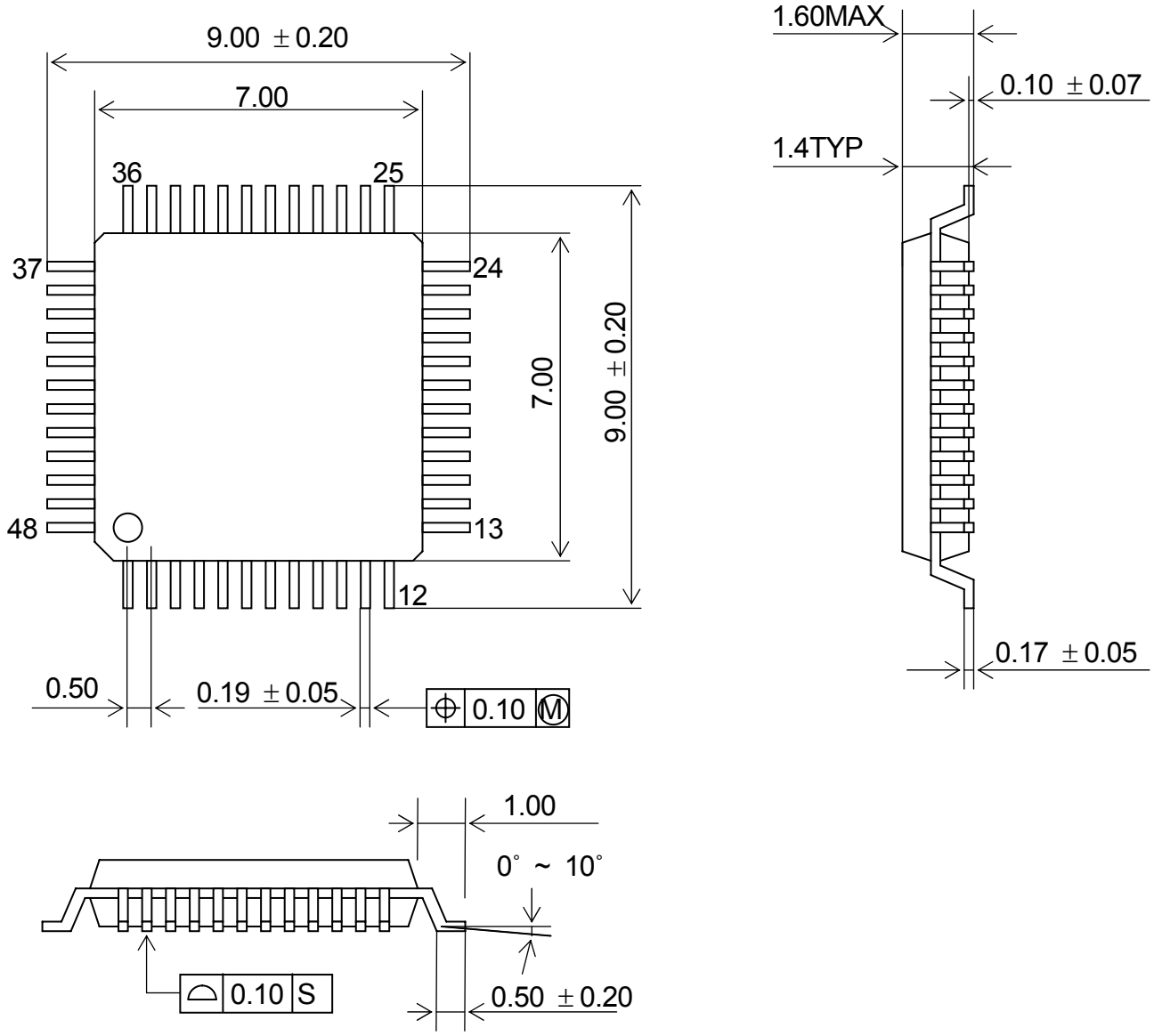


Figure 13. I^2C Bus Interface

PACKAGE

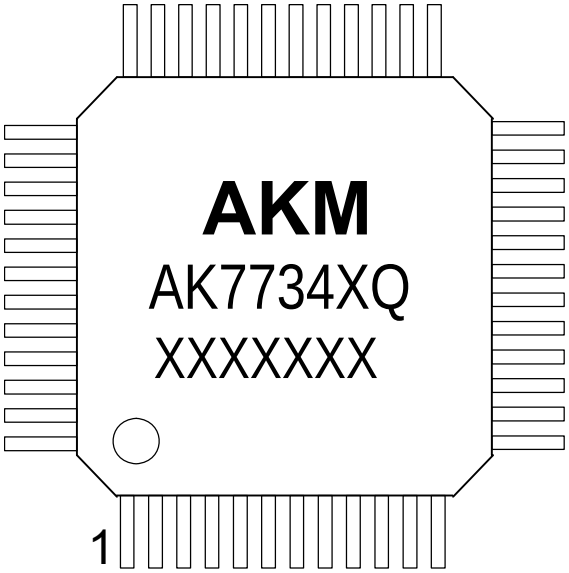
48pin LQFP (Unit: mm)



■ Materials and Lead Specification

Package:	Epoxy
Lead frame:	Copper
Lead-finish:	Soldering (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7digits)
3) Marking Code: AK7734XQ
4) Asahi Kasei Logo

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
09/03/24	00	First Edition		
09/11/16	01	Description Change	6, 7	Digital Ground 0V → Ground 0V Analog Ground 0V → Ground 0V
		Error Correction	13	DIGITAL FILTER CHARACTERISTICS Note 20: "n x 512kHz ±3.665kHz" → "n x 512kHz ±4.66kHz" Note 23: "n x 3.072MHz ±21.99kHz" → "n x 3.072MHz ±28kHz"
10/01/06	02			

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  Note2) A hazard related device or system is one designed or intended for life support or maintenance of s afety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to func tion or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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