AK7738A

Multi DSP with 5ch ADC + 4ch DAC + 8ch SRC

1. General Description

The AK7738A is a highly integrated digital signal processor, including a 24-bit stereo ADC with MIC gain amplifiers, a 24-bit stereo ADC with input selector, a monaural ADC, two 32-bit stereo DACs, 4 stereo sampling rate convertors supporting the sampling frequency up to 192kHz, two DSPs and a Sub DSP for Audio/HF process. Each two DSPs and a Sub DSP has 2560step/fs (when fs=48kHz) parallel processing power. The AK7738A is capable of processing sound and voice such as for hands-free function simultaneously because two DSPs are able to work on different but synchronized sampling frequencies. As the AK7738A is a RAM based DSP, it is freely programmable for user requirements, such as acoustic effects and proprietary high performance hands-free function. The AK7738A is available in a 64-pin LQFP package.

2. Features

□ DSP1/DSP2: (Memory areas are shared by DSP1 and DSP2)

- **Word length: 28-bit (Simple floating point supported)**
- **Instruction cycle: 8.1ns (2560fs at fs=48kHz)**
- **Multiplier: 24 x 24 → 48-bit (Double precision arithmetic available)**
- **Divider: 24 / 24 → 24-bit (Floating point normalization function)**
- **ALU: 52-bit arithmetic operation (with 4bits overflow margin)**
- **Program RAM: 8192 word x 36-bit**
- **Coefficient RAM: 6144 word x 24-bit**
- **Data RAM: 6144 word x 28-bit**
- **Delay RAM: 20480 word x 28-bit**
- **JX pins (Interrupt)**
- **Clock Mode Selector for DSP1, DSP2**
- **Independent Power Management Function for DSP1, DSP2**

□ Sub DSP

- **Word length: 28-bit (Simple floating point supported)**
- **Instruction cycle: 8.1ns (2560fs at fs=48kHz)**
- **Multiplier: 24 x 24 → 48-bit (Double precision arithmetic available)**
- **Divider: 24 / 24 → 24-bit (Floating point normalization function)**
- **ALU: 52-bit arithmetic operation (with 4bits overflow margin)**
- **Program RAM: 1024 word x 36-bit**
- **Coefficient RAM: 2048 word x 24-bit**
- **Data RAM: 4096 word x 28-bit**

□ ADC1: 24-bit Stereo ADC with MIC Gain Amplifiers

- **Sampling Frequency: fs=8kHz to 192kHz**
- **Channel Independent Analog Gain Amplifiers**
  (0 to 18dB(2dB Step), 18 to 36dB(3dB step))
- **Differential Input or Single-ended Input**
- **ADC Characteristics S/N: 102dB (fs=48kHz, Differential Input, MIC Gain=0dB,)**
- **Channel Independent Digital Volume Control (+24 to -103dB, 0.5dB Step, Mute)**
- **Analog DRC (Dynamic Range Control)**
- **Digital HPF for DC Offset Cancelling**
- **Low Noise MIC Power Output: 2ch**
- **5 types of Digital Filter for Sound Color Selection**

□ ADC2: 24-bit Stereo ADC with Input Selector
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Analog Input Selector: Differential Input x1 or Single-ended Input x2, Semi-Differential Input x1**
- **ADC Characteristics S/N: 102dB (fs=48kHz, Differential Input)**
- **Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **4 types of Digital Filter for Sound Color Selection**

□ ADCM: 24-bit Monaural ADC
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Differential Input or Single-ended Input**
- **ADC Characteristics S/N: 102dB (fs=48kHz, Differential Input)**
- **Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **4 types of Digital Filter for Sound Color Selection**

□ DAC: Advanced 32-bit DAC
- **2ch x2**
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Single-ended Output**
- **DAC Characteristics S/N: 108dB (fs=48kHz)**
- **Channel Independent Digital Volume Control (+12 to -115dB, 0.5dB Step, Mute)**
- **4 types of Digital Filter for Sound Color Selection**

□ SRC:
- **2ch x4**
- **FSI = 8kHz to 192kHz, FSO = 8kHz to 192kHz (FSO/FSI = 0.167 to 6.0)**

□ FSCONV: Monaural Simple SRC
- **1ch x2**
- **FSI = 44.1kHz to 48kHz, FSO = 8kHz to 16kHz (FSO/FSI = 0.167 to 0.363)**

□ DIT:
- **S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Compatible**
- **24-bit Stereo Output**

□ Digital Interface:
- **Digital Input Port: max 24ch when TDM mode**
- **Digital Output Port: max 28ch when TDM mode**
- **Independent LRCK/BICK Input port x 5 Lines**
- **Data Format: MSB 32,24-bit / LSB 24,20,16-bit / I^2S**
- **PCM Short / Long Frame Supported**
- **TDM Format Supported**

□ Digital Mixer Circuit

□ PLL Circuit

□ µP Interface: SPI(6MHz max), I^2C-bus (400kHz Fast Mode or 1MHz Fast Mode Plus)

□ Power Supply:
- **Analog AVDD: 3.0 to 3.6V (typ. 3.3V)**
- **Digital LVDD: 3.0 to 3.6V (typ. 3.3V) (3.3V → 1.2V regulator integrated)**
- **I/F VDD33: 3.0 to 3.6V (typ. 3.3V)**
  TVDD1: 1.7 to 3.6V (typ. 3.3V)
  TVDD2: 1.7 to 3.6V (typ. 3.3V)

□ Operating Temperature Range: -40°C to 85°C

□ Package: 64-pin LQFP (10mm x 10mm, 0.5mm pitch)

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

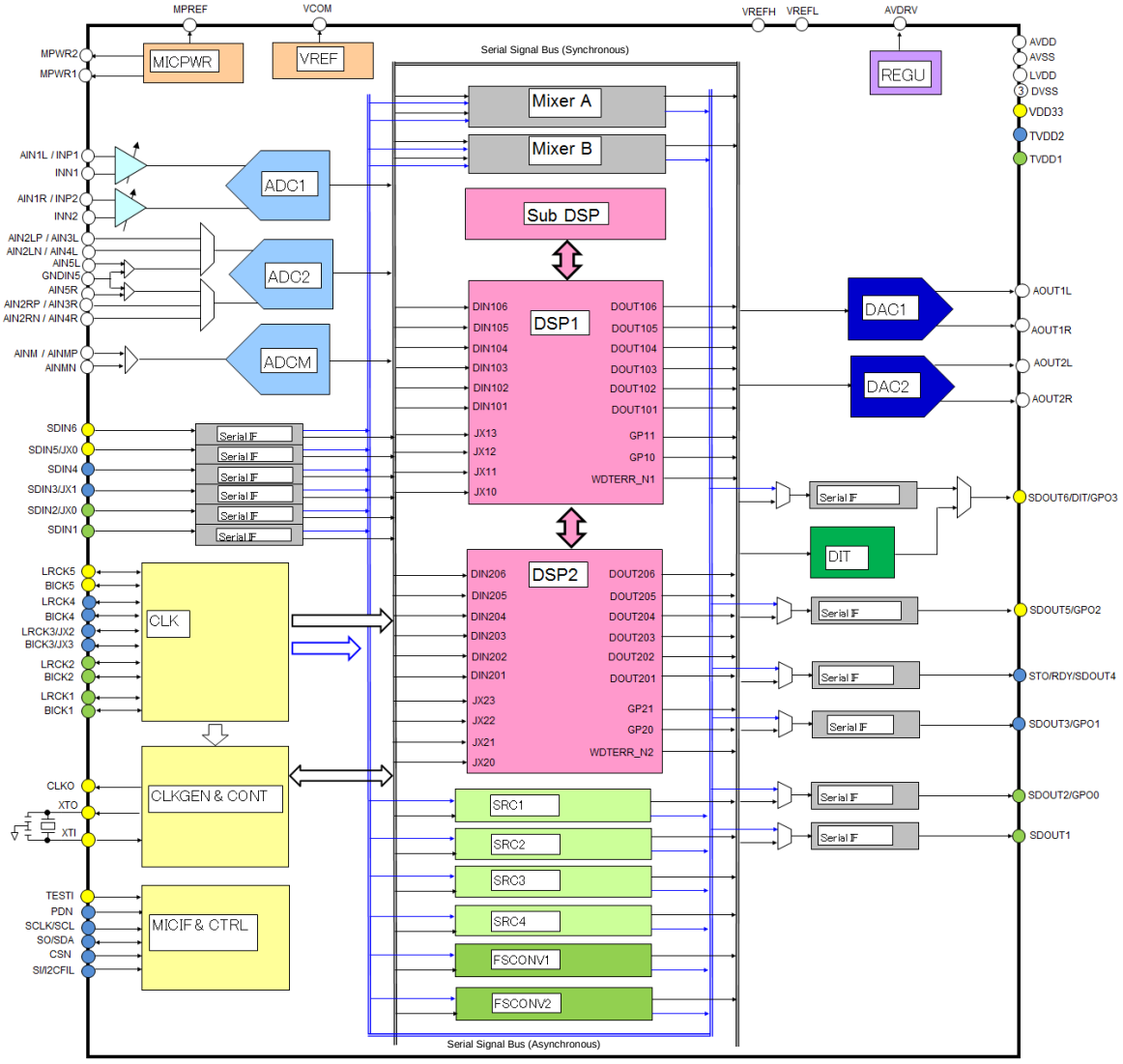


Figure 1. Block Diagram

■ DSP1 Block Diagram

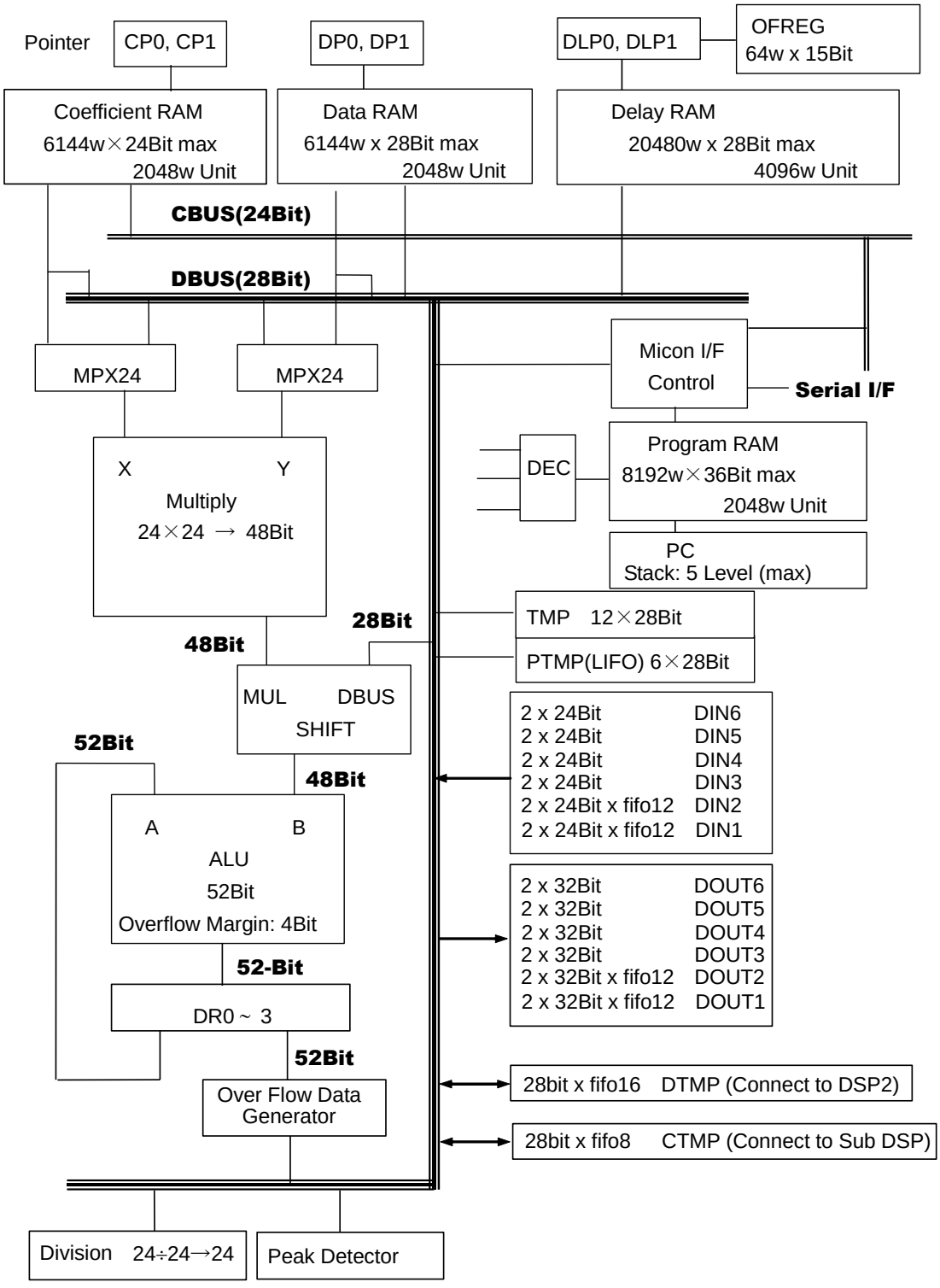


Figure 2. DSP1 Block Diagram (Note 1)

Note 1. Coefficient RAM, Data RAM, Delay RAM, Program RAM areas are shared by DSP1 and DSP2 and the sizes are configurable by control registers.

■ DSP2 Block Diagram

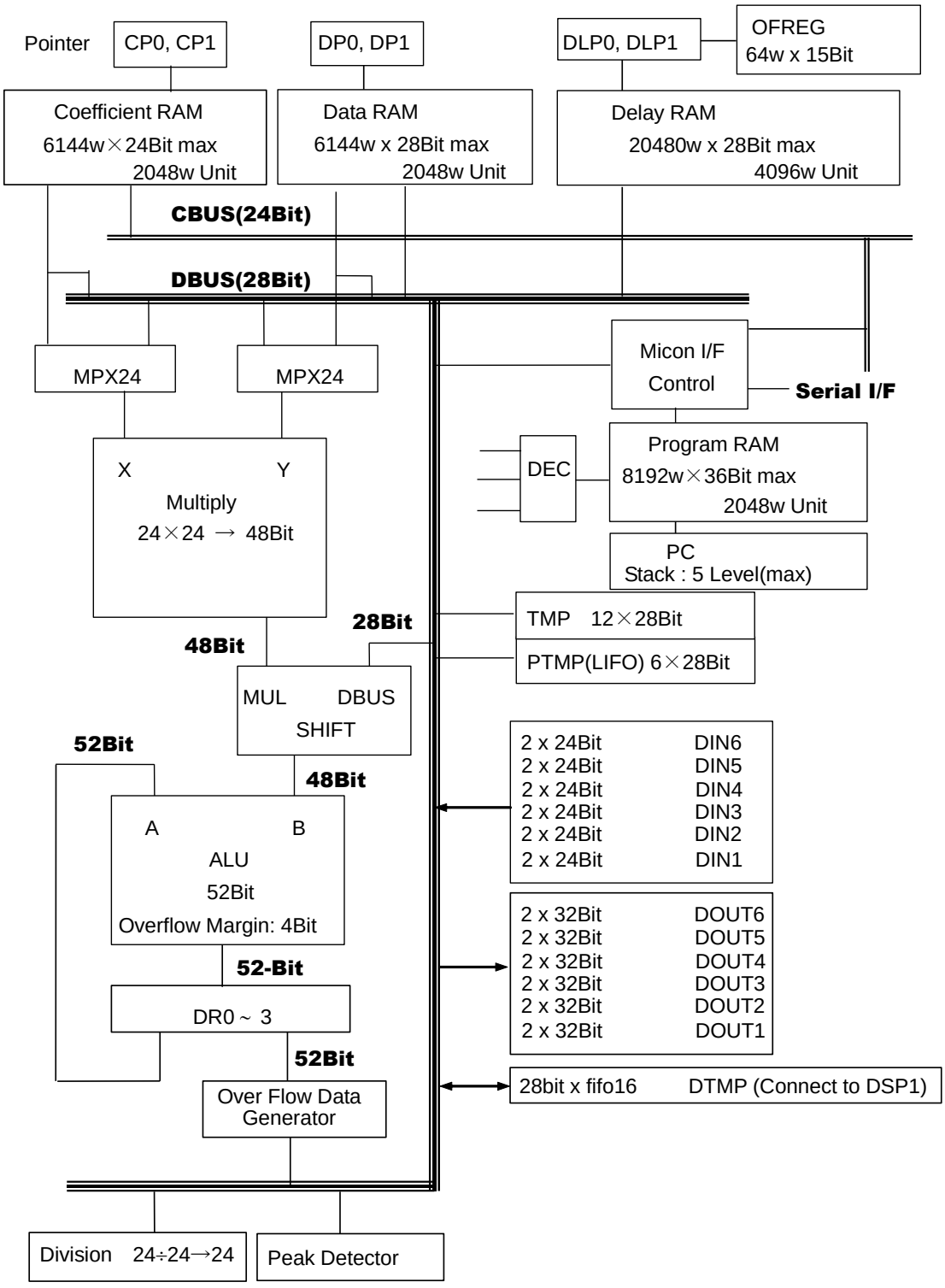


Figure 3. DSP2 Block Diagram (Note 1)

■ Sub DSP Block Diagram

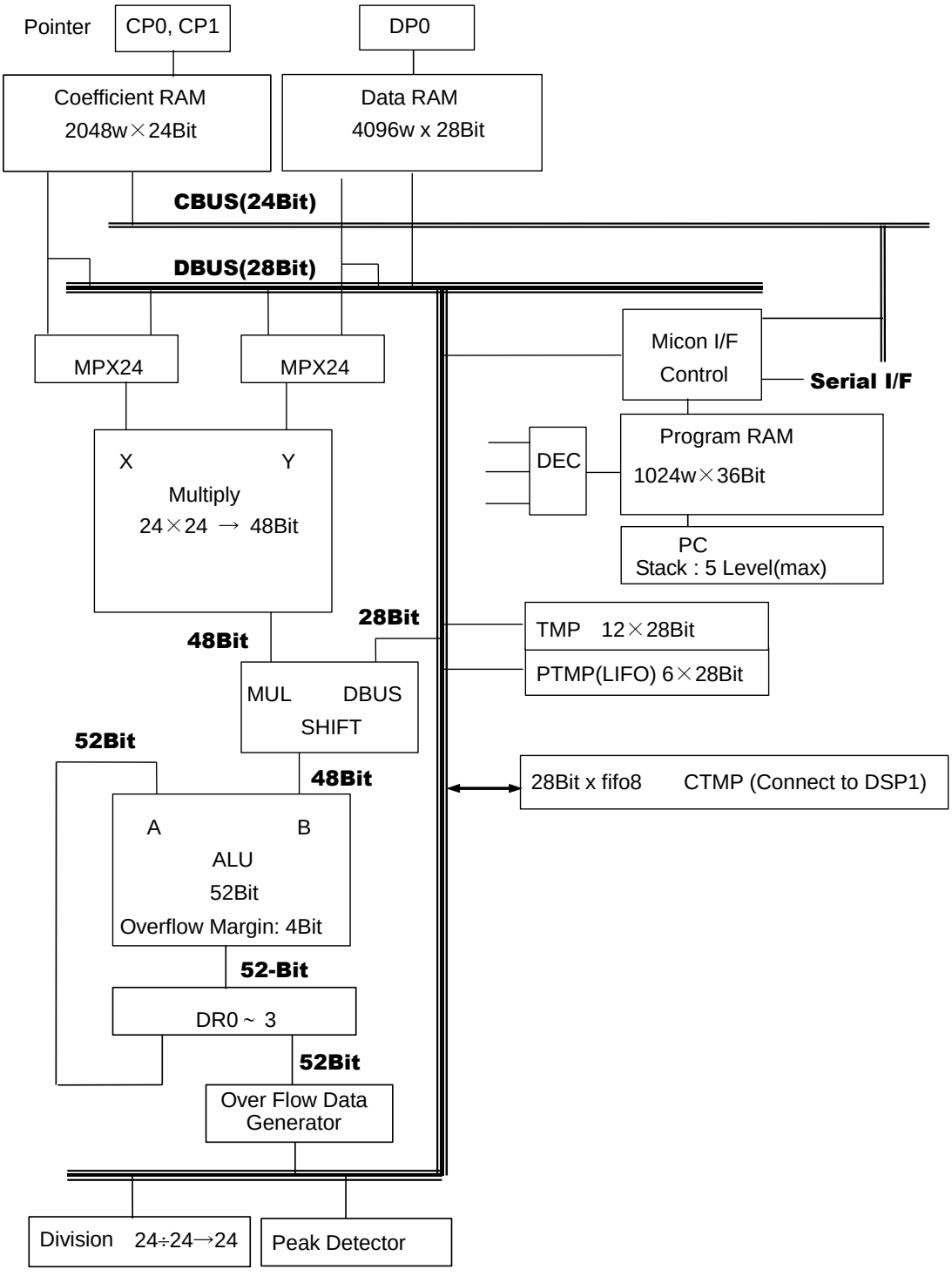


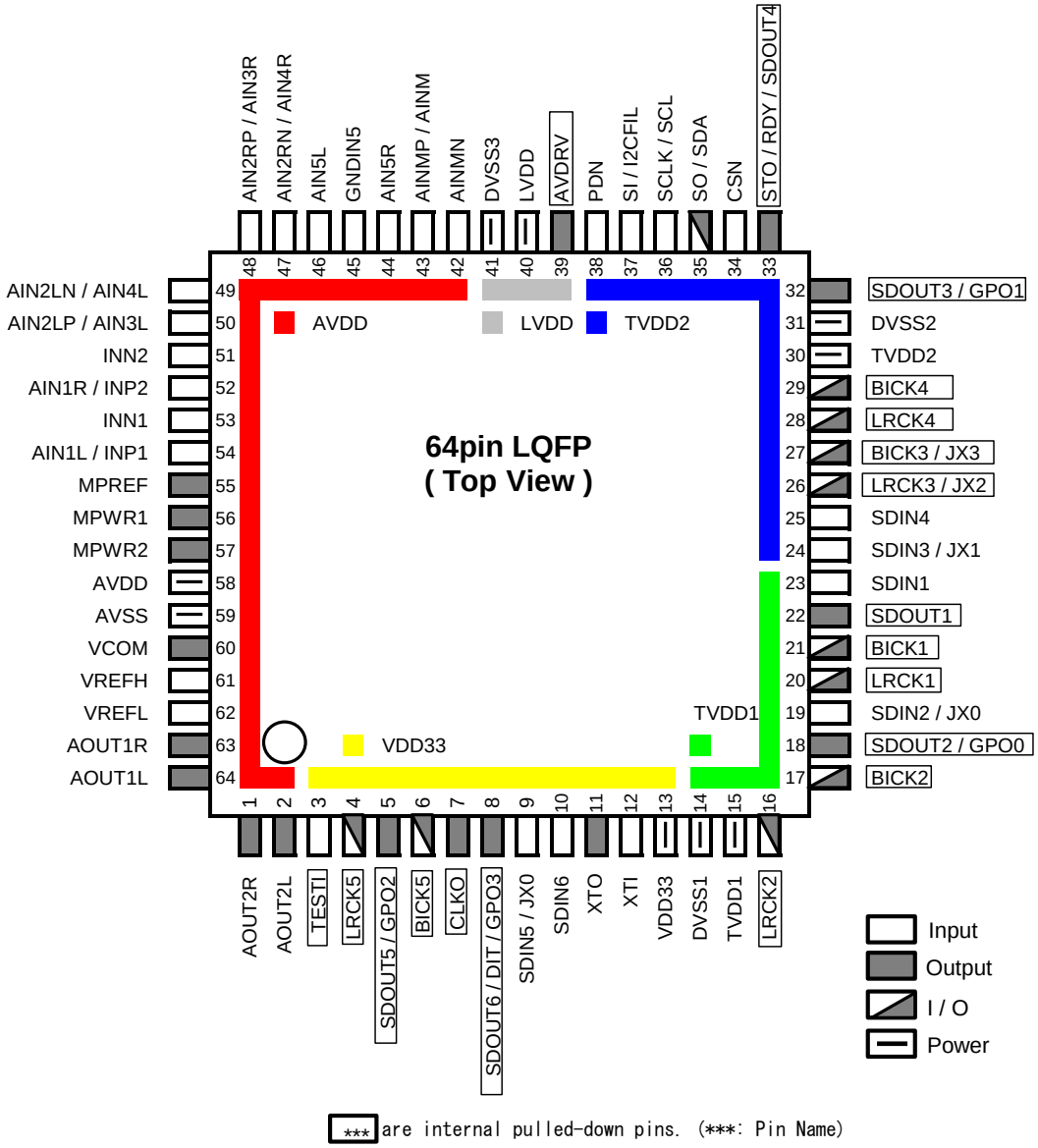
Figure 4. Sub DSP Block Diagram

5. Pin Configurations and Functions

■ Ordering Guide

AK7738AVQ:	-40 ~ +85°C	64-pin LQFP (0.5mm pitch)
AKD7738A:	Evaluation Board for AK7738A	

■ Pin Layout



■ Pin Functions

No.	Pin Name	I/O	Function
1	AOUT2R	O	DAC2 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
2	AOUT2L	O	DAC2 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
3	TESTI	I	Test Input Pin It must be tied “L”.
4	LRCK5	I/O	LR Channel Select Clock 5 Pin
5	SDOUT5	O	Serial Data Output 5 Pin
	GPO2	O	DSP Programmable Output 2 Pin (GPO0 Output of DSP2)
6	BICK5	I/O	Serial Bit Clock 5 Pin
7	CLKO	O	Master Clock Output Pin
8	SDOUT6	O	Serial Data Output 6 Pin
	DIT	O	Digital Transmit Channel Output Pin
	GPO3	O	DSP Programmable Output 3 Pin (GPO1 Output of DSP2)
9	SDIN5	I	Serial Data Input 5 Pin
	JX0	I	External Conditional Jump Input 0 Pin
10	SDIN6	I	Serial Data Input 6 Pin
11	XTO	O	Crystal Oscillator Output Pin When using a crystal oscillator, connect it between XTI and XTO. When not using a crystal oscillator, leave this pin open.
12	XTI	I	Crystal Oscillator Input Pin When using a crystal oscillator, connect it between XTI and XTO. When not using a crystal oscillator, connect this pin to an external clock or DVSS1.
13	VDD33	-	Digital I/F Power Supply Pin 3.0~3.6V (typ.3.3V)
14	DVSS1	-	Digital Ground 1 Pin 0V (Substrate potential)
15	TVDD1	-	Digital I/F Power Supply 1 Pin 1.7~3.6V (typ.3.3V)
16	LRCK2	I/O	LR Channel Select Clock 2 Pin
17	BICK2	I/O	Serial Bit Clock 2 Pin
18	SDOUT2	O	Serial Data Output 2 Pin
	GPO0	O	DSP Programmable Output 0 Pin (GPO0 Output of DSP1)
19	SDIN2	I	Serial Data Input 2 Pin
	JX0	I	External Conditional Jump Input 0 Pin
20	LRCK1	I/O	LR Channel Select Clock 1 Pin
21	BICK1	I/O	Serial Bit Clock 1 Pin
22	SDOUT1	O	Serial Data Output 1 Pin
23	SDIN1	I	Serial Data Input 1 Pin

No.	Pin Name	I/O	Function
24	SDIN3	I	Serial Data Input 3 Pin
	JX1	I	External Conditional Jump Input 1 Pin
25	SDIN4	I	Serial Data Input 4 Pin
26	LRCK3	I/O	LR Channel Select Clock 3 Pin
	JX2	I	External Conditional Jump Input 2 Pin
27	BICK3	I/O	Serial Bit Clock 3 Pin
	JX3	I	External Conditional Jump Input 3 Pin
28	LRCK4	I/O	LR Channel Select Clock 4 Pin
29	BICK4	I/O	Serial Bit Clock 4 Pin
30	TVDD2	-	Digital I/F Power Supply 2 Pin 1.7~3.6V (typ.3.3V)
31	DVSS2	-	Digital Ground 2 Pin 0V (Substrate potential)
32	SDOUT3	O	Serial Data Output 3 Pin
	GPO1	O	DSP Programmable Output 1 Pin (GPO1 Output of DSP1)
33	STO	O	Status Output Pin This pin outputs "L" during power-down state.
	RDY	O	RDY Signal Output Pin
	SDOUT4	O	Serial Data Output 4 Pin
34	CSN	I	SPI Mode SPI I/F Chip Select N Pin During power-down state or when μP I/F are not in use, leave this pin "H" level.
		I	I^2C Mode I^2C I/F Chip Address N Pin This pin must be pulled up or pulled down.
35	SO	O	Serial Data Output Pin for SPI I/F This pin outputs "Hi-Z" during power-down state.
	SDA	I/O	Serial Data In/Output Pin for I^2C I/F This pin outputs "Hi-Z" during power-down state.
36	SCLK	I	Serial Data Clock Input Pin for SPI I/F
	SCL	I	Serial Data Clock Input Pin for I^2C I/F
37	SI	I	Serial Data Input Pin for SPI I/F
	I2CFIL	I	I^2C I/F Mode Select Input Pin I2CFIL = "L": Fast Mode (400kHz) I2CFIL = "H": Fast Mode Plus (1MHz) (should be fixed to TVDD2)
38	PDN	I	Power-down N Pin Use this pin to power down the AK7738A. The PDN pin should be held "L" when power is supplied.
39	AVDRV	O	LDO Output Pin Connect a 2.2uF ceramic capacitor between this pin and DVSS3. Do not connect this pin to an external circuit.
40	LVDD	-	Digital Core Power Supply Pin 3.0~3.6V (typ.3.3V)
41	DVSS3	-	Digital Ground 3 Pin 0V (Substrate potential)

No.	Pin Name	I/O	Function
42	AINMN	I	ADCM Inverted Differential Input Pin
43	AINMP	I	ADCM Non-inverted Differential Input Pin
	AINM	I	ADCM Single-ended Input Pin
44	AIN5R	I	ADC2 Rch Pseudo Differential Input 5 Pin
45	GNDIN5	I	ADC2 Pseudo Differential Ground Input 5 Pin
46	AIN5L	I	ADC2 Lch Pseudo Differential Input 5 Pin
47	AIN2RN	I	ADC2 Rch Inverted Differential Input 2 Pin
	AIN4R	I	ADC2 Rch Single-ended Input 4 Pin
48	AIN2RP	I	ADC2 Rch Non-inverted Differential Input 2 Pin
	AIN3R	I	ADC2 Rch Single-ended Input 3 Pin
49	AIN2LN	I	ADC2 Lch Inverted Differential Input 2 Pin
	AIN4L	I	ADC2 Lch Single-ended Input 4 Pin
50	AIN2LP	I	ADC2 Lch Non-inverted Differential Input 2 Pin
	AIN3L	I	ADC2 Lch Single-ended Input 3 Pin
51	INN2	I	ADC1 Rch Inverted Differential Input 2 Pin
52	AIN1R	I	ADC1 Rch Single-ended Input 1 Pin
	INP2	I	ADC1 Rch Non-inverted Differential Input 2 Pin
53	INN1	I	ADC1 Lch Inverted Differential Input 1 Pin
54	AIN1L	I	ADC1 Lch Single-ended Input 1 Pin
	INP1	I	ADC1 Lch Non-inverted Differential Input 1 Pin
55	MPREF	O	Ripple Filter Pin for Microphone Power Supply Connect a 1uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit.
56	MPWR1	O	Power Supply Output 1 Pin for Microphone This pin outputs “Hi-Z” during power-down state.
57	MPWR2	O	Power Supply Output 2 Pin for Microphone This pin outputs “Hi-Z” during power-down state.
58	AVDD	-	Analog Power Supply Pin 3.0~3.6V (typ.3.3V)
59	AVSS	-	Analog Ground Pin 0V (Substrate potential)
60	VCOM	O	Analog Common Voltage Output Pin Connect a 2.2uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit. This pin outputs “L” during power-down state.
61	VREFH	I	Analog High-level Reference Voltage Input Pin Connect this pin to AVDD.
62	VREFL	I	Analog Low-level Reference Voltage Input Pin Connect this pin to AVSS.
63	AOUT1R	O	DAC1 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
64	AOUT1L	O	DAC1 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPREF, MPWR1, MPWR2, AIN1L/INP1, INN1, AIN1R/INP2, INN2, AIN2LP/AIN3L, AIN2LN/AIN4L, AIN2RP/AIN3R, AIN2RN/AIN4R, AIN5L, GNDIN5, AIN5R, AINMP/AINM, AINMN, AOUT1L, AOUT1R, AOUT2L, AOUT2R	Open
Digital	CLKO, XTO, SDOUT1, SDOUT2/GPO0, SDOUT3/GPO1, STO/RDY/SDOUT4, SDOUT5/GPO2, SDOUT6/DIT/GPO3	Open
	XTI , SDIN6, SDIN5/JX0, SDIN4, SDIN3/JX1, SDIN2/JX0, SDIN1, LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, LRCK5, BICK5, TESTI	Connect to DVSS1 ~ 3

Table 1. Handling of Unused Pins

Note 2. Although it is recommended that the LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, LRCK5 and BICK5 pins are connected to DVSS1-3 when not using, they can be open since they are pulled down internally.

■ Internal Pulled-down Pin Status

Internal pulled-down I/O pins have different statuses in power-down and power-down release statuses.

No	Pin Name	I/O	Power Down Status PDN pin = "L"	Power Down Release PDN pin = "H" (when I/O pin = Input)	Power Down Release PDN pin = "H" (when I/O pin = Output)
3	TESTI	I	Pulled-down (25kΩ)	Pulled-down (25kΩ)	Pulled-down (25kΩ)
4	LRCK5	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
5	SDOUT5/GPO2	O	Pulled-down (50kΩ)	Output	Output
6	BICK5	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
7	CLKO	O	Pulled-down (50kΩ)	Output	Output
8	SDOUT6/DIT/GPO3	O	Pulled-down (50kΩ)	Output	Output
16	LRCK2	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
17	BICK2	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
18	SDOUT2/GPO0	O	Pulled-down (50kΩ)	Output	Output
20	LRCK1	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
21	BICK1	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
22	SDOUT1	O	Pulled-down (50kΩ)	Output	Output
26	LRCK3/JX2	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
27	BICK3/JX3	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
28	LRCK4	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
29	BICK4	I/O	Pulled-down (50kΩ)	Pulled-down (46kΩ)	Output
32	SDOUT3/GPO1	O	Pulled-down (50kΩ)	Output	Output
33	STO/RDY/SDOUT4	O	Pulled-down (50kΩ)	Output	Output
39	AVDRV	O	Pulled-down (70Ω)	Output	Output

Table 2. Internal Pulled-down Pin Status

■ Power-down Status of Output Pins

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
60	VCOM	O	"L" Output	35	SO/SDA	I/O	"Hi-Z" Output
55	MPREF	O	"L" Output				
56	MPWR1	O	"Hi-Z" Output	22	SDOUT1	O	"L" Output (Pulled-down)
57	MPWR2	O	"Hi-Z" Output	18	SDOUT2/GPO0	O	"L" Output (Pulled-down)
64	AOUT1L	O	"Hi-Z" Output	32	SDOUT3/GPO1	O	"L" Output (Pulled-down)
63	AOUT1R	O	"Hi-Z" Output	33	STO/RDY/SDOUT4	O	"L" Output (Pulled-down)
2	AOUT2L	O	"Hi-Z" Output	5	SDOUT5/GPO2	O	"L" Output (Pulled-down)
1	AOUT2R	O	"Hi-Z" Output	8	SDOUT6/DIT/GPO3	O	"L" Output (Pulled-down)
20	LRCK1	I/O	Input	7	CLKO	O	"L" Output (Pulled-down)
21	BICK1	I/O	Input	11	XTO	O	"H" Output
16	LRCK2	I/O	Input	39	AVDRV	O	"L" Output (Pulled-down)
17	BICK2	I/O	Input				
26	LRCK3/JX2	I/O	Input				
27	BICK3/JX3	I/O	Input				
28	LRCK4	I/O	Input				
29	BICK4	I/O	Input				
4	LRCK5	I/O	Input				
6	BICK5	I/O	Input				

Table 3. Power-down Status of Output Pins

■ Relationship between Power Supplies and Digital Pins

Power Supply	Digital Pins
TVDD1	SDIN1, SDIN2/JX0, SDOUT1, SDOUT2/GPO0, LRCK1, BICK1, LRCK2, BICK2
TVDD2	SDIN3/JX1, SDIN4, SDOUT3/GPO1, STO/RDY/SDOUT4, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, PDN, SCLK/SCL, SO/SDA, CSN, SI/I2CFIL
VDD33	SDIN5/JX0, SDIN6, SDOUT5/GPO2, SDOUT6/DIT/GPO3, LRCK5, BICK5, CLKO, TESTI, XTO, XTI

Table 4. Relationship between Power Supplies and Digital Pins

6. Absolute Maximum Ratings

(AVSS=DVSS1=DVSS2=DVSS3=0V; Note 3)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core)	LVDD	-0.3	4.3	V
Digital2(I/F)	TVDD1	-0.3	4.3	V
Digital3(I/F)	TVDD2	-0.3	4.3	V
Digital4(I/F)	VDD33	-0.3	4.3	V
DVSS-AVSS (Note 3)	ΔGND	-0.3	0.3	V
Input Current (except power supply pins)	IIN	—	±10	mA
Analog Input Voltage (Note 4)	VINA	-0.3	(AVDD+0.3)≤4.3	V
Digital Input Voltage (Note 5)	VIND1	-0.3	(TVDD1+0.3)≤4.3	V
Digital Input Voltage (Note 6)	VIND2	-0.3	(TVDD2+0.3)≤4.3	V
Digital Input Voltage (Note 7)	VIND3	-0.3	(VDD33+0.3)≤4.3	V
Ambient Temperature (Power applied)	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 3. All voltages are with respect to ground. AVSS and DVSS1-3 must be connected to the same ground.
Note 4. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 5. The maximum digital input voltage of SDIN1, SDIN2/JX0, LRCK1, BICK1, LRCK2 and BICK2 pins is smaller value between (TVDD1+0.3)V and 4.3V.
Note 6. The maximum digital input voltage of SDIN3/JX1, SDIN4, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, PDN, SCLK/SCL, SO/SDA, CSN and SI/I2CFIL pins is smaller value between (TVDD2+0.3)V and 4.3V.
Note 7. The maximum digital input voltage of SDIN5/JX0, SDIN6, LRCK5, BICK5, TESTI and XTI pins is smaller value between (VDD33+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS1=DVSS2=DVSS3=0V; Note 3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core)	LVDD	3.0	3.3	3.6	V
Digital2(I/F)	TVDD1	1.7	3.3	3.6	V
Digital3(I/F)	TVDD2	1.7	3.3	3.6	V
Digital4(I/F)	VDD33	3.0	3.3	3.6	V

Note 8. The power-up sequence with AVDD, DVDD, TVDD1, TVDD2 and VDD33 is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
Note 9. Do not turn off the power supply of the AK7738A with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD2 or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP Gain

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP	Input Impedance		14	20	26	kΩ
	Gain	MGNL[3:0]bits=0h, MGNR[3:0]bits=0h	-1	0	1	dB
		MGNL[3:0]bits=1h, MGNR[3:0]bits=1h	1	2	3	
		MGNL[3:0]bits=2h, MGNR[3:0]bits=2h	3	4	5	
		MGNL[3:0]bits=3h, MGNR[3:0]bits=3h	5	6	7	
		MGNL[3:0]bits=4h, MGNR[3:0]bits=4h	7	8	9	
		MGNL[3:0]bits=5h, MGNR[3:0]bits=5h	9	10	11	
		MGNL[3:0]bits=6h, MGNR[3:0]bits=6h	11	12	13	
		MGNL[3:0]bits=7h, MGNR[3:0]bits=7h	13	14	15	
		MGNL[3:0]bits=8h, MGNR[3:0]bits=8h	15	16	17	
		MGNL[3:0]bits=9h, MGNR[3:0]bits=9h	17	18	19	
		MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah	20	21	22	
		MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh	23	24	25	
		MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch	26	27	28	
		MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh	29	30	31	
		MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh	32	33	34	
		MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh	35	36	37	

2. MIC Bias

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V;
Measurement Frequency =20Hz~20kHz)

	Parameter	Min.	Typ.	Max.	Unit
MIC Bias	Output Voltage	2.3	2.5	2.7	V
	Load Resistance	2			kΩ
	Load Capaitance			30	pF
	Output Noise (A-weighted)		-114	-108	dBV

3. MIC AMP + ADC1

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS=DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data; BICK=64fs, Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz, Differential Input, Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP + ADC1	Resolution				24	Bit
	Input Voltage (Note 13)	Differential Input (Note 11, Note 15)	±2.1	±2.3	±2.5	Vpp
		Differential Input (Note 12, Note 15)	±0.264	±0.290	±0.315	
		Single-ended Input (Note 11)	2.1	2.3	2.5	Vpp
		Single-ended Input (Note 12)	0.264	0.290	0.315	
	S/(N+D) (-1dBFS)	fs=48kHz (Note 11)	80	90		dB
		fs=48kHz (Note 12)		82		
		fs=96kHz (Note 11)		87		
		fs=96kHz (Note 12)		79		
		fs=192kHz (Note 11, Note 14)		87		
		fs=192kHz (Note 12, Note 14)		79		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) (Note 11)	94	102		dB
		fs=48kHz (A-weighted) (Note 12)		90		
		fs=96kHz (Note 11)		95		
		fs=96kHz (Note 12)		87		
		fs=192kHz (Note 11)		95		
		fs=192kHz (Note 12)		87		
	S/N	fs=48kHz (A-weighted) (Note 11)	94	102		dB
		fs=48kHz (A-weighted) (Note 12)		90		
		fs=96kHz (Note 11)		95		
		fs=96kHz (Note 12)		87		
		fs=192kHz (Note 11)		95		
		fs=192kHz (Note 12)		87		
	Inter-Channel Isolation (fin=1kHz) (Note 10)		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB

Note 10. Inter-channel isolation with -1dBFS signal input.
Note 11. MGNL/R[3:0] bits = 0h (0dB). Input full-scale voltage is propotional to AVDD (0.7 x AVDD).
Note 12. MGNL/R[3:0] bits = 9h (+18dB). Input full-scale voltage is propotional to AVDD (0.088 x AVDD).
Note 13. -0.7dBFS is output when fs=192kHz and ADC1 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.
Note 14. In the case of inputting -1.6dBFS when fs=192kHz and ADC1 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.
Note 15. When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

4. ADC2

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data, BICK = 64fs; Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz, Differential Input, Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
ADC2	Resolution				24	Bit
	Input Impedance		14	20	26	kΩ
	Input Voltage (Note 19)	Differential Input (Note 16)	±2.1	±2.3	±2.5	Vpp
		Single-ended Input (Note 17)	2.1	2.3	2.5	Vpp
		Pseudo Differential Input (Note 18)	2.1	2.3	2.5	Vpp
	S/(N+D) (-1dBFS)	fs=48kHz	80	90		dB
		fs=96kHz		87		
		fs=192kHz (Note 20)		87		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	94	102		dB
		fs=96kHz		95		
		fs=192kHz		95		
	S/N	fs=48kHz (A-weighted)	94	102		dB
		fs=96kHz		95		
		fs=192kHz		95		
	Inter-Channel Isolation (fin=1kHz) (Note 10)		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB

Note 16. AIN2LP, AIN2LN, AIN2RP and AIN2RN pins. When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

Note 17. AIN3L, AIN3R, AIN4L and AIN4R pins.

Note 18. AIN5L and AIN5R pins.

Note 19. -0.7dBFS is output when fs=192kHz and ADC2 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

Note 20. In the case of inputting -1.6dBFS when fs=192kHz and ADC2 digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

5. ADCM

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data, BICK = 64fs; Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz, Differential Input, Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
ADCM	Resolution				24	Bit
	Input Impedance		14	20	26	kΩ
	Input Voltage (Note 23)	Differential Input (Note 21)	±2.1	±2.3	±2.5	Vpp
		Single-ended Input (Note 22)	2.1	2.3	2.5	Vpp
	S/(N+D) (-1dBFS)	fs=48kHz	80	90		dB
		fs=96kHz		87		
		fs=192kHz (Note 24)		87		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	94	102		dB
		fs=96kHz		95		
		fs=192kHz		95		
	S/N	fs=48kHz (A-weighted)	94	102		dB
		fs=96kHz		95		
		fs=192kHz		95		

Note 21. AINMP and AINMN pins. When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

Note 22. AINM pin.

Note 23. -0.7dBFS is output when fs=192kHz and ADCM digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

Note 24. In the case of inputting -1.6dBFS when fs=192kHz and ADCM digital filter is set to Slow Roll-Off or Short Delay Slow Roll-Off filter.

6. DAC

(Ta=25°C; AVDD= LVDD =TVDD1=TVDD2= VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 32-bit Data, BICK = 64fs; Measurement Frequency=20Hz ~ 20kHz @ fs=48kHz; Measurement Frequency=20Hz ~ 40kHz @ fs=96kHz and fs=192kHz; Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
DAC1 DAC2	Resolution				32	Bit
	Output Voltage (Note 25)		2.55	2.83	3.11	Vpp
	S/(N+D) (0dBFS)	fs=48kHz	80	91		dB
		fs=96kHz		89		
		fs=192kHz		89		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	S/N	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	Inter-Channel Isolation (fin=1kHz) (Note 26)		90	110		dB
	Channel Gain Mismatch			0.0	0.7	dB
	Load Resistance (Note 27)		10			kΩ
	Load Capaitance				30	pF

Note 25. The output voltage when 0dBFS signal input. The output voltage is proportional to AVDD (AVDD x 0.86).

Note 26. Inter-channel isolation between each DAC of Lch and Rch with 0dBFS signal input. (AOUT1L and AOUT1R, and AOUT2L and AOUT2R)

Note 27. to AC load

7. SRC

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V;
Signal Frequency=1kHz; 24-bit Data; Measurement Frequency=20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution				24	Bit
	Input Sample Rate	FSI	8		192 (Note 28)	kHz
	Output Sample Rate	FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)					
	Audio Mode					
	FSO/FSI=192kHz/48kHz			-122		dB
	FSO/FSI=44.1kHz/48kHz			-125		dB
	FSO/FSI=48kHz/88.2kHz			-122		dB
	FSO/FSI=48kHz/96kHz			-133		dB
	FSO/FSI=44.1kHz/96kHz			-116		dB
	FSO/FSI=48kHz/192kHz			-133		dB
	FSO/FSI=8kHz/48kHz			-130		dB
	Voice Mode					
	FSO/FSI=24kHz/32kHz			-95		dB
	FSO/FSI=16kHz/24kHz			-98		dB
	FSO/FSI=24kHz/44.1kHz			-78		dB
	FSO/FSI=16kHz/44.1kHz			-69		dB
	FSO/FSI=8kHz/32kHz			-130		dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	Audio Mode					
	FSO/FSI=192kHz/48kHz			132		dB
	FSO/FSI=44.1kHz/48kHz			136		dB
	FSO/FSI=48kHz/88.2kHz			135		dB
	FSO/FSI=48kHz/96kHz			136		dB
	FSO/FSI=44.1kHz/96kHz			136		dB
	FSO/FSI=48kHz/192kHz			136		dB
	FSO/FSI=8kHz/48kHz			130		dB
	Voice Mode					
	FSO/FSI=24kHz/32kHz			132		dB
	FSO/FSI=16kHz/24kHz			135		dB
	FSO/FSI=24kHz/44.1kHz			132		dB
	FSO/FSI=16kHz/44.1kHz			128		dB
	FSO/FSI=8kHz/32kHz			130		dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted) FSO/FSI=44.1kHz/48kHz			137		dB
	Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

Note 28. Set FSI frequency of each operating SRC as the sum of the frequencies is below 384kHz. For example, if the frequency of FSI is 96kHz, four SRCs can operate at the same time, if the frequency of FSI is 192kHz, only two SRCs are allowed to operate at the same time.

8. FSCONV

(Ta=25°C; AVDD=LVDD=TVDD1=TVDD2=VDD33=3.3V; AVSS= DVSS1=DVSS2=DVSS3=0V; Signal Frequency=1kHz; 24-bit Data; Measurement Frequency=20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
FSCONV	Resolution				24	Bit
	Input Sample Rate	FSI	44.1		48	kHz
	Output Sample Rate	FSO	8		16	kHz
	THD+N (Input=1kHz, 0dBFS)					
	FSO/FSI=16kHz/48kHz			-114		dB
	FSO/FSI=16kHz/44.1kHz			-95		dB
	FSO/FSI=8kHz/48kHz			-115		dB
	FSO/FSI=8kHz/44.1kHz			-97		dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	FSO/FSI=16kHz/48kHz			114		dB
	FSO/FSI=16kHz/44.1kHz			114		dB
	FSO/FSI=8kHz/48kHz			114		dB
	FSO/FSI=8kHz/44.1kHz			114		dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted)					
	FSO/FSI=8kHz/48kHz			117		dB
	Ratio between Input and Output Sample Rate	FSO/FSI	0.167		0.363	-

■ Power Consumption

(Ta=25°C; AVDD=3.0~3.6V(typ=3.3V, max=3.6V); LVDD=3.0~3.6V(typ=3.3V, max=3.6V); TVDD1=1.7~3.6V(typ=3.3V, max=3.6V); TVDD2=1.7~3.6V (typ=3.3V, max=3.6V); VDD33=3.0~3.6V (typ=3.3V, max=3.6V); AVSS= DVSS1=DVSS2=DVSS3=0V; fs=192kHz; BICK=64fs; SDOUT1~6/LRCK1~5/BICK1~5=Output; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Up (PDN pin= "H") (Note 29)	AVDD		26	37	mA
	LVDD		70	140	mA
	TVDD1		1.6	2.4	mA
	TVDD2		1.6	2.4	mA
	VDD33		4	6	mA
Power-Down (PDN pin= "L")	AVDD		0.01		mA
	LVDD		0.01		mA
	TVDD1		0.01		mA
	TVDD2		0.01		mA
	VDD33		0.01		mA

Note 29. The current of LVDD changes depending on the system frequency and contents of DSP program.

9. Digital Filter Characteristics

1. ADC Block

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

1-1 Sharp Roll-Off Filter (ADSD bit = "0", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 30)	0dB ~ -0.06dB	PB	0		22.1	kHz
	-6.0dB	PB		24.4		kHz
Stopband (Note 30)		SB	27.8			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		19		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.0		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 30)	0dB ~ -0.06dB	PB	0		44.2	kHz
	-6.0dB	PB		48.7		kHz
Stopband (Note 30)		SB	55.6			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		19		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 30)	0dB ~ -0.04dB	PB	0		83.7	kHz
	-6.0dB	PB		100.1		kHz
Stopband (Note 30)		SB	122.9			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		15		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.9		Hz

1-2 Slow Roll-Off Filter (ADSD bit = "0", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 30)	0dB ~ -0.074dB	PB	0		12.5	kHz
	-6.0dB	PB		21.9		kHz
Stopband (Note 30)		SB	36.5			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		7		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.0		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 30)	0dB ~ -0.074dB	PB	0		25	kHz
	-6.0dB	PB		43.7		kHz
Stopband (Note 30)		SB	73			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		7		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 30)	0dB ~ -0.7dB	PB	0		49.9	kHz
	-6.0dB	PB		79.9		kHz
Stopband (Note 30)		SB	146			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		8		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.88		Hz

1-3 Short Delay Sharp Roll-Off Filter (ADSD bit = "1", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 30)	0dB ~ -0.06dB	PB	0		22.1	kHz
	-6.0dB	PB		24.4		kHz
Stopband (Note 30)		SB	27.8			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD			2.6	1/fs
Group Delay (Note 31)		GD		5		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.0		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 30)	0dB ~ -0.06dB	PB	0		44.2	kHz
	-6.0dB	PB		48.7		kHz
Stopband (Note 30)		SB	55.6			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			2.6	1/fs
Group Delay (Note 31)		GD		5		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 30)	0dB ~ -0.04dB	PB	0		83.7	kHz
	-6.0dB	PB		100.1		kHz
Stopband (Note 30)		SB	122.9			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			0.2	1/fs
Group Delay (Note 31)		GD		6		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.88		Hz

1-4 Short Delay Slow Roll-Off Filter (ADSD bit = "1", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 30)	0dB ~ -0.074dB	PB	0		12.5	kHz
	-6.0dB	PB		21.9		kHz
Stopband (Note 30)		SB	36.5			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD			2.6	1/fs
Group Delay (Note 31)		GD		5		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.0		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 30)	0dB ~ -0.074dB	PB	0		25	kHz
	-6.0dB	PB		43.7		kHz
Stopband (Note 30)		SB	73			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			2.6	1/fs
Group Delay (Note 31)		GD		5		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 30)	0dB ~ -0.7dB	PB	0		49.9	kHz
	-6.0dB	PB		77.7		kHz
Stopband (Note 30)		SB	145.9			kHz
Stopband Attenuation		SA	85			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD			0.5	1/fs
Group Delay (Note 31)		GD		6		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		3.88		Hz

1-5 Voice Filter (AD1HF bit = "1")

fs=16kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 30)	-0.5dB ~ 0.5dB	PB	0		6.3	kHz
	-6.0dB	PB		7.1		kHz
Stopband (Note 30)		SB	8.0			kHz
Stopband Attenuation		SA	60			dB
Group Delay Distortion : 0Hz~8kHz		ΔGD		0		1/fs
Group Delay (Note 31)		GD		20		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		0.3		Hz

Note 30. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter characteristics are not included.

Note 31. Delay time caused by the digital filter calculation. This time is measured from an analog signal input until 24-bit data of both channels are set into the output register.

2. DAC Block

(Ta= 25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

2-1 Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 32)	-0.08dB~+0.08dB	PB	0		22.2	kHz
	-6.0dB	PB		23.99		kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 32)		SB	26.2			kHz
Stopband Attenuation		SA	69.9			dB
Group Delay (Note 33)		GD		26.4		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 20kHz		FR	-0.20		0.10	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 32)	-0.08dB~+0.08dB	PB	0		44.4	kHz
	-6.0dB	PB		48.00		kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 32)		SB	52.5			kHz
Stopband Attenuation		SA	69.8			dB
Group Delay (Note 33)		GD		26.4		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 40kHz		FR	-0.50		0.10	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 32)	-0.08dB~+0.08dB	PB	0		88.8	kHz
	-6.0dB	PB		96.00		kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 32)		SB	104.9			kHz
Stopband Attenuation		SA	69.8			dB
Group Delay (Note 33)		GD		26.4		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 80kHz		FR	-2.00		-0.00	dB

2-2 Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 32)	-0.07dB~ +0.021dB	PB	0		9.0	kHz
	-3.0dB	PB		19.75		kHz
Passband Ripple		PR	-0.07		+0.021	dB
Stopband (Note 32)		SB	42.6			kHz
Stopband Attenuation (Note 34)		SA	72.6			dB
Group Delay (Note 33)		GD		26.4		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 20kHz		FR	-3.75		-2.75	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 32)	-0.07dB~+0.023dB	PB	0		18.1	kHz
	-3.0dB	PB		39.6		kHz
Passband Ripple		PR	-0.07		+0.023	dB
Stopband (Note 32)		SB	85.1			kHz
Stopband Attenuation (Note 34)		SA	72.6			dB
Group Delay (Note 33)		GD		26.4		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 40kHz		FR	-4.25		-2.75	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 32)	-0.07dB~+0.023dB	PB	0		36.1	kHz
	-3.0dB	PB		79.3		kHz
Passband Ripple		PR	-0.07		+0.023	dB
Stopband (Note 32)		SB	170.3			kHz
Stopband Attenuation (Note 34)		SA	72.6			dB
Group Delay (Note 33)		GD		26.4		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 80kHz		FR	-5.00		-3.00	dB

2-3 Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 32)	-0.07dB~+0.07dB	PB	0		22.0	kHz
	-6.0dB	PB		24.11		kHz
Passband Ripple		PR	-0.07		+0.07	dB
Stopband (Note 32)		SB	26.2			kHz
Stopband Attenuation		SA	56.6			dB
Group Delay (Note 33)		GD		5.9		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 20kHz		FR	-0.20		0.10	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 32)	-0.08dB~+0.08dB	PB	0		44.3	kHz
	-6.0dB	PB		48.25		kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 32)		SB	52.5			kHz
Stopband Attenuation		SA	56.4			dB
Group Delay (Note 33)		GD		5.9		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 40kHz		FR	-0.50		0.10	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 32)	-0.08dB~+0.08dB	PB	0		88.6	kHz
	-6.0dB	PB		96.50		kHz
Passband Ripple		PR	-0.08		+0.08	dB
Stopband (Note 32)		SB	104.9			kHz
Stopband Attenuation		SA	56.4			dB
Group Delay (Note 33)		GD		5.9		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 80kHz		FR	-2.00		-0.00	dB

2-4 Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 32)	-0.07dB~+0.05dB	PB	0		10.1	kHz
	-3.0dB	PB		20.24		kHz
Passband Ripple		PR	-0.07		+0.05	dB
Stopband (Note 32)		SB	43.0			kHz
Stopband Attenuation (Note 34)		SA	74.9			dB
Group Delay (Note 33)		GD		5.2		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 20kHz		FR	-3.50		-2.50	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 32)	-0.07dB~+0.05dB	PB	0		20.3	kHz
	-3.0dB	PB		40.50		kHz
Passband Ripple		PR	-0.07		+0.05	dB
Stopband (Note 32)		SB	86.0			kHz
Stopband Attenuation (Note 34)		SA	74.9			dB
Group Delay (Note 33)		GD		5.2		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 40kHz		FR	-4.00		-2.50	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 32)	-0.07dB~+0.05dB	PB	0		40.6	kHz
	-3.0dB	PB		81.00		kHz
Passband Ripple		PR	-0.07		+0.05	dB
Stopband (Note 32)		SB	172.0			kHz
Stopband Attenuation (Note 34)		SA	74.9			dB
Group Delay (Note 33)		GD		5.2		1/fs
Digital Filter + SCF						
Frequency Response : 0Hz ~ 80kHz		FR	-4.75		-2.75	dB

Note 32. The passband and stopband frequencies are proportional to fs (sampling rate).
Note 33. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/24/32-bit impulse data to the input registers to output of the analog peak signal.
Note 34. Band width of Stopband Attenuation ranges from SB to fs.

3. SRC Block

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

3-1 Audio Mode

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980≦FSO/FSI≦6.000	PB			0.4583FSI	kHz
	-0.01dB	0.900≦FSO/FSI＜0.990	PB			0.4167FSI	kHz
	-0.01dB	0.533≦FSO/FSI＜0.909	PB			0.2182FSI	kHz
	-0.01dB	0.490≦FSO/FSI＜0.539	PB			0.2177FSI	kHz
	-0.01dB	0.450≦FSO/FSI＜0.495	PB			0.1948FSI	kHz
	-0.01dB	0.225≦FSO/FSI＜0.455	PB			0.1312FSI	kHz
	-0.50dB	0.167≦FSO/FSI＜0.227	PB			0.0658FSI	kHz
Stopband		0.980≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
		0.900≦FSO/FSI＜0.990	SB	0.5021FSI			kHz
		0.533≦FSO/FSI＜0.909	SB	0.2974FSI			kHz
		0.490≦FSO/FSI＜0.539	SB	0.2812FSI			kHz
		0.450≦FSO/FSI＜0.495	SB	0.2604FSI			kHz
		0.225≦FSO/FSI＜0.455	SB	0.1802FSI			kHz
		0.167≦FSO/FSI＜0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225≦FSO/FSI≦6.000	PR			±0.01	dB
		0.167≦FSO/FSI＜0.227	PR			±0.50	dB
Stopband Attenuation		0.450≦FSO/FSI≦6.000	SA	95.2			dB
		0.167≦FSO/FSI＜0.455	SA	85.0			dB
Group Delay (Ts=1/fs) (Note 35)			GD		67 (55/FSI+12/FSO)		Ts

Note 35. This value is SRC block only. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

3-2 Voice Mode

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980≦FSO/FSI≦6.000	PB			0.4583FSI	kHz
	-0.01dB	0.900≦FSO/FSI＜0.990	PB			0.4167FSI	kHz
	-0.50dB	0.711≦FSO/FSI＜0.910	PB			0.3420FSI	kHz
	-0.50dB	0.653≦FSO/FSI＜0.718	PB			0.3007FSI	kHz
	-0.50dB	0.450≦FSO/FSI＜0.660	PB			0.2230FSI	kHz
	-0.50dB	0.327≦FSO/FSI＜0.455	PB			0.1417FSI	kHz
	-0.50dB	0.225≦FSO/FSI＜0.330	PB			0.1018FSI	kHz
	-0.50dB	0.167≦FSO/FSI＜0.227	PB			0.0658FSI	kHz
Stopband		0.980≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
		0.900≦FSO/FSI＜0.990	SB	0.5021FSI			kHz
		0.711≦FSO/FSI＜0.910	SB	0.3735FSI			kHz
		0.653≦FSO/FSI＜0.718	SB	0.3320FSI			kHz
		0.450≦FSO/FSI＜0.660	SB	0.2490FSI			kHz
		0.327≦FSO/FSI＜0.455	SB	0.1660FSI			kHz
		0.225≦FSO/FSI＜0.330	SB	0.1248FSI			kHz
		0.167≦FSO/FSI＜0.227	SB	0.0970FSI			kHz
Passband Ripple		0.900≦FSO/FSI≦6.000	PR			±0.01	dB
		0.167≦FSO/FSI≦0.910	PR			±0.50	dB
Stopband Attenuation		0.900≦FSO/FSI≦6.000	SA	95.2			dB
		0.653≦FSO/FSI＜0.909	SA	90.0			dB
		0.450≦FSO/FSI≦0.660	SA	70.0			dB
		0.167≦FSO/FSI＜0.455	SA	60.0			dB
Group Delay (Ts=1/fs) (Note 35)			GD		67 (55FSI+12FSO)		Ts

3-3 Echo Canceller Mode

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167≦FSO/FSI≦6.000	PB			0.4583FSI	kHz
Stopband		0.167≦FSO/FSI≦6.000	SB	0.5417FSI			kHz
Passband Ripple		0.167≦FSO/FSI≦6.000	PR			±0.01	dB
Stopband Attenuation		0.167≦FSO/FSI≦6.000	SA	95.2			dB
Group Delay (Ts=1/fs) (Note 35)			GD		67 (55/FSI+12/FSO)		Ts

4. FSCONV

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167 ≤ FSO/FSI ≤ 0.363	PB	0		0.1814FSI	kHz
Stopband		0.167 ≤ FSO/FSI ≤ 0.363	SB	0.8185FSI			kHz
Passband Ripple		0.167 ≤ FSO/FSI ≤ 0.363	PR			±0.005	dB
Stopband Attenuation		0.167 ≤ FSO/FSI ≤ 0.363	SA	94.0			dB
Group Delay (Ts=1/FSI) (Note 36)			GD		9		Ts

Note 36. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

10. DC Characteristics

■ DC Characteristics

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1	(Note 37)	VIH1	80%TVDD1			V
Low-Level Input Voltage 1	(Note 37)	VIL1			20%TVDD1	V
High-Level Input Voltage 2	(Note 38)	VIH2	80%TVDD2			V
Low-Level Input Voltage 2	(Note 38)	VIL2			20%TVDD2	V
High-Level Input Voltage 3	(Note 39)	VIH3	80%VDD33			V
Low-Level Input Voltage 3	(Note 39)	VIL3			20%VDD33	V
SCL, SDA High-Level Input Voltage		VIH4	70%TVDD2			V
SCL, SDA Low-Level Input Voltage		VIL4			30%TVDD2	V
High-Level Output Voltage Iout= -100µA	(Note 37)	VOH1	TVDD1-0.3			V
Low-Level Output Voltage Iout=100µA	(Note 37)	VOL1			0.3	V
High-Level Output Voltage Iout= -100µA	(Note 38)	VOH2	TVDD2-0.3			V
Low-Level Output Voltage Iout=100µA	(Note 38)	VOL2			0.3	V
High-Level Output Voltage Iout= -100µA	(Note 39)	VOH3	VDD33-0.3			V
Low-Level Output Voltage Iout=100µA	(Note 39)	VOL3			0.3	V
SCL, SDA Low Level Output Voltage	Fast Mode					
	TVDD2 ≥ 2.0V (Iout=3mA)	VOL4			0.4	V
	TVDD2< 2.0V (Iout=3mA)	VOL4			20%TVDD2	V
	Fast Mode Plus					
	TVDD2 ≥ 2.0V (Iout=20mA)	VOL4			0.4	V
	TVDD2 < 2.0V (Iout=3mA)	VOL4			20%TVDD2	V
Input Leak Current	(Note 40)	Iin			±10	µA
Input Leak Current, Pulled down pin Power Down	(Note 41)	Iid		66		µA
Input Leak Current, Pulled down pin Power Down Release	(Note 42)	Iid		72		µA
Input Leak Current, TESTI pin		lid		132		µA
Input Leak Current, XTI pin		lix		17		µA

Note 37. SDIN1, SDIN2/JX0, SDOUT1, SDOUT2/GPO0, LRCK1, BICK1, LRCK2 and BICK2 pins.

Note 38. SDIN3/JX1, SDIN4, SDOUT3/GPO1, STO/RDY/SDOUT4, LRCK3/JX2, BICK3/JX3, LRCK4, BICK4, PDN, SCLK/SCL, SO/SDA, CSN, and SI/I2CFIL pins. The SCL and SDA pins are not included.

Note 39. SDIN5/JX0, SDIN6, SDOUT5/GPO2, SDOUT6/DIT/GPO3, LRCK5, BICK5, CLKO, XTO, XTI and TESTI pins

Note 40. Except internal pulled-down pins and the XTI pin.

Note 41. LRCK5, BICK5, LRCK2, BICK2, LRCK1, BICK1, LRCK3/JX2, BICK3/JX3, LRCK4 and BICK4 pins are internal pulled-down pins (typ. 50 kΩ@3.3V) when the AK7738A is powered down (PDN pin = "L"). The TESTI pin is not included.

Note 42. LRCK5, BICK5, LRCK2, BICK2, LRCK1, BICK1, LRCK3/JX2, BICK3/JX3, LRCK4 and BICK4 pins are internal pulled-down pins (typ. 46 kΩ@3.3V) when power-down is released (PDN pin = "H"). The TESTI pin is not included.

11. Switching Characteristics

1. System Clock

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator					
Input Frequency	fXTI	11.2896		18.432	MHz
b) XTI Clock Input					
Duty Cycle		40	50	60	%
Input Frequency	fXTI	0.256		24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		24.576	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		192	kHz
BICK Input Timing					
Frequency (Note 43)	fBCLK	0.256		24.576	MHz
Pulse Width Low	tBCLKL	0.4/fBCLK			ns
Pulse Width High	tBCLKH	0.4/fBCLK			ns
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		192	kHz
Pulse Width High PCM Mode Except PCM Mode	 tLRCKH tLRCKH		 1/fBCLK 50		 ns %
BICK Output Timing					
Frequency (Note 43)	fBCLK	0.256		24.576	MHz
Duty	dBCLK		50		%

Note 43. Required to meet the following expression: fBCLK ≥ 2 x fs x (Input/Output Data Length).

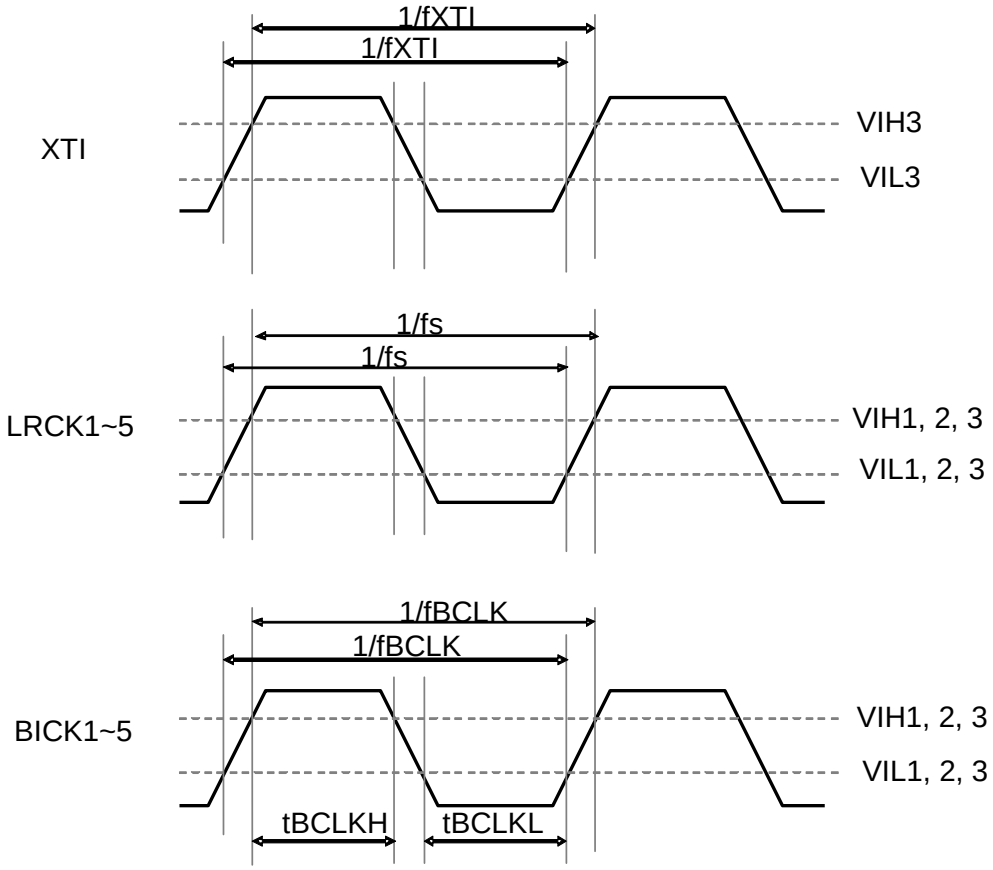


Figure 5. System Clock Timing

2. Power Down

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pluse Width (Note 44)	tRST	600			ns

Note 44. The PDN pin must be “L” when power up the AK7738A.

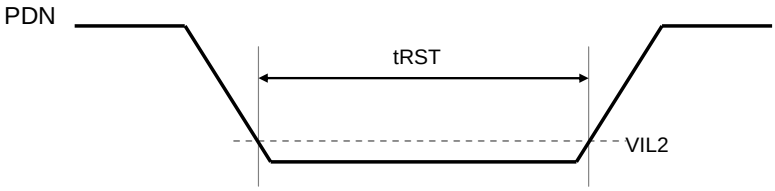


Figure 6. Reset Timing

3. Serial Data Interface (SDIN1 ~ SDIN6, SDOUT1 ~ SDOUT6)

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (Note 45)	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" (Note 45)	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from BICK"↓"to Serial Data Output (Note 46)	tBSOD1			20	ns
Delay Time from BICK "↑"to Serial Data Output (Note 45, Note 47)	tBSOD2	5		30	ns
Master Mode					
BICK frequency	fBCLK	-	32, 48, 64, 128, 256	-	fs
BICK Duty cycle			50		%
Delay Time from BICK "↓" to LRCK (Note 46)	tMBL	-10		10	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from BICK"↓"to Serial Data Output (Note 46, Note 47)	tBSOD			10	ns

Note 45. It is measured from BICK "↓" when the BICK polarity is inverted by setting BCKPx bit = "1".
Note 46. It is measured from BICK "↑" when the BICK polarity is inverted by setting BCKPx bit = "1".
Note 47. Set SDOPHx bit to "1" and the data should be output based on BICK "↑" when using TDM256 mode with 96kHz sampling frequency in slave mode. SDOPHx bit must be set to "0" in master mode.

3-1. Slave Mode

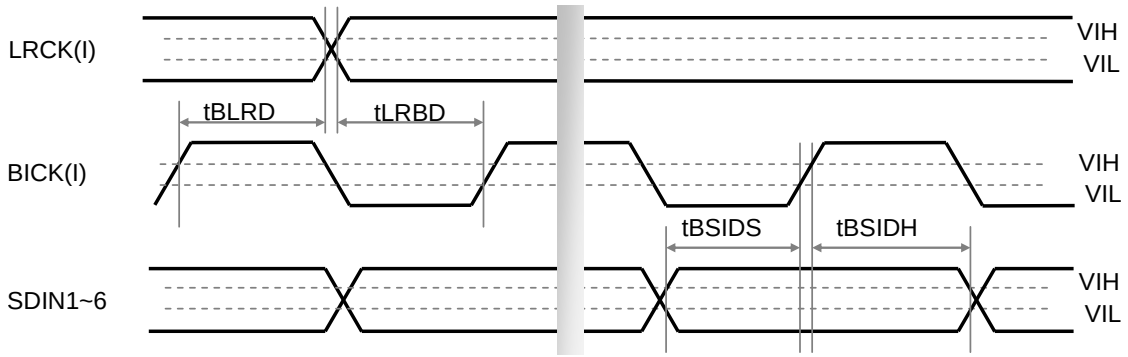


Figure 7. Serial Interface Input Timing in Slave Mode

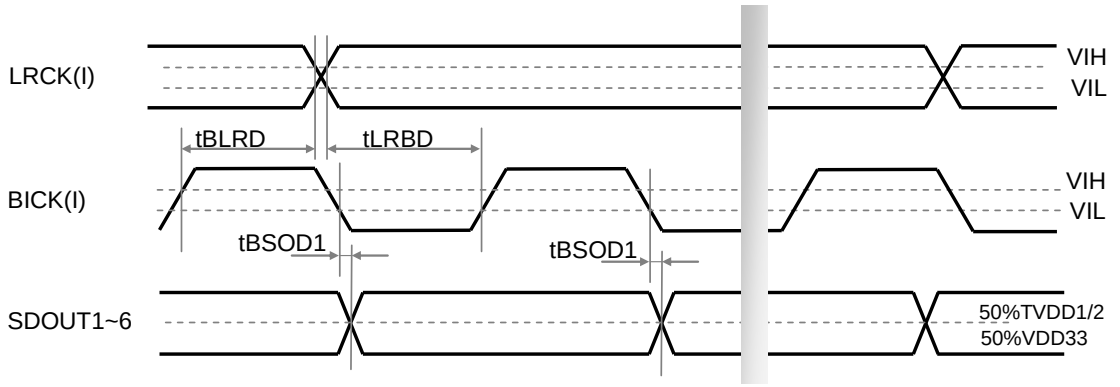


Figure 8. Serial Interface Output Timing in Slave Mode (SDOPHx bit = "0")

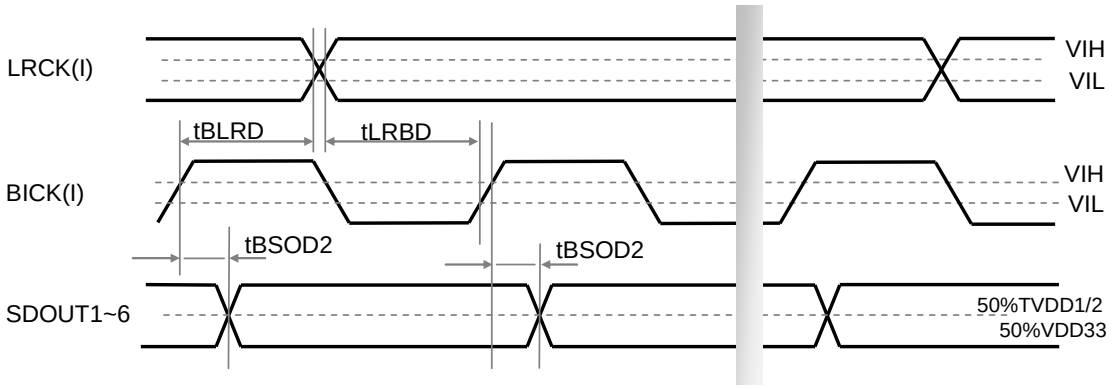


Figure 9. Serial Interface Output Timing in Slave Mode (SDOPHx bit = "1")

3-2. Master Mode

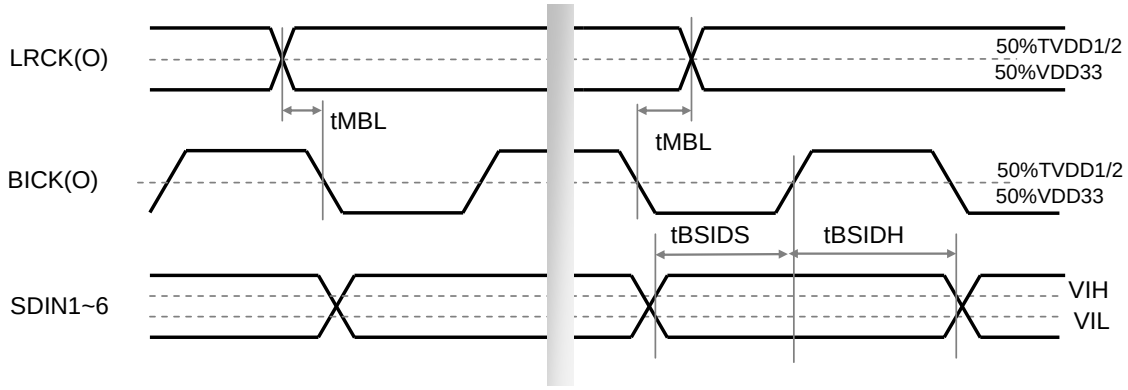


Figure 10. Serial Interface Input Timing in Master Mode

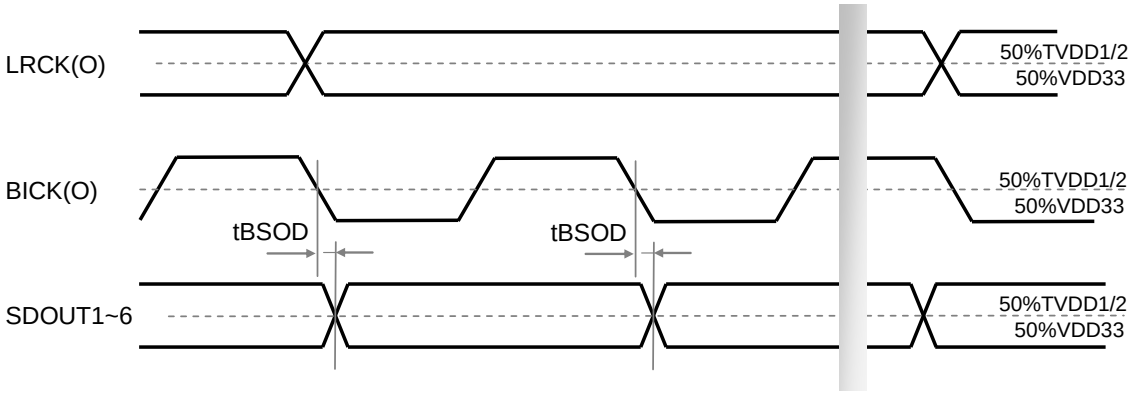


Figure 11. Serial Interface Output Timing in Master Mode (SDOPHx bit = “0”)

4. SPI Interface

4-1. Clock Reset (CKRESETN bit = "0")

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency (Note 50)	fSCLK			3	MHz
SCLK Low-level Width	tSCLKL	160			ns
SCLK High-level Width	tSCLKH	160			ns
Microcontroller → AK7738A					
CSN High-level Width	tWRQH	300			ns
From CSN "↑" to PDN "↑"	tRST	360			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	300			ns
From SCLK "↑" to CSN "↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7738A→ Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			120	ns
SO Output Hold Time from SCLK "↑" (Note 48)	tSOH	120			ns

Note 48. Except when writing the 24th bit (8 bits command + 16 bits address) of the command code. This will be the 8th bit (8 bits command) with "write preparation data read command (24H and 25H)".

4-2. PLL Lock (CKRESETN bit = "1" and PLL is locked)

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Timing (SPI mode)					
SCLK Frequency (Note 49) (Note 50)	fSCLK			6	MHz
SCLK Low Level Width	tSCLKL	72			ns
SCLK High Level Width	tSCLKH	72			ns
µP → AK7738A					
CSN High Level Width	tWRQH	150			ns
From CSN "↑"to PDN "↑"	tRST	180			ns
From PDN "↑"to CSN "↓"	tIRRQ	1			ms
From CSN "↓"to SCLK "↓"	tWSC	150			ns
From SCLK "↑"to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7738A→ µP					
Delay Time from SCLK "↓"to SO Output	tSOS			60	ns
SO Output Hold Time from SCLK "↑" (Note 48)	tSOH	60			ns

Note 49. It takes maximum 10ms to lock PLL after setting CKRESETN bit = "0"→ "1".

Note 50. Control registers can always be accessed by a maximum speed of 6MHz. Interfacing with the AK7738A except control registers should be made at a maximum speed of 3MHz when PLL is unlocked or at a maximum speed of 6MHz when PLL is locked. It is necessary to set DLRDY bit to "1" when interfacing with the AK7738A except control registers if PLL is unlocked.

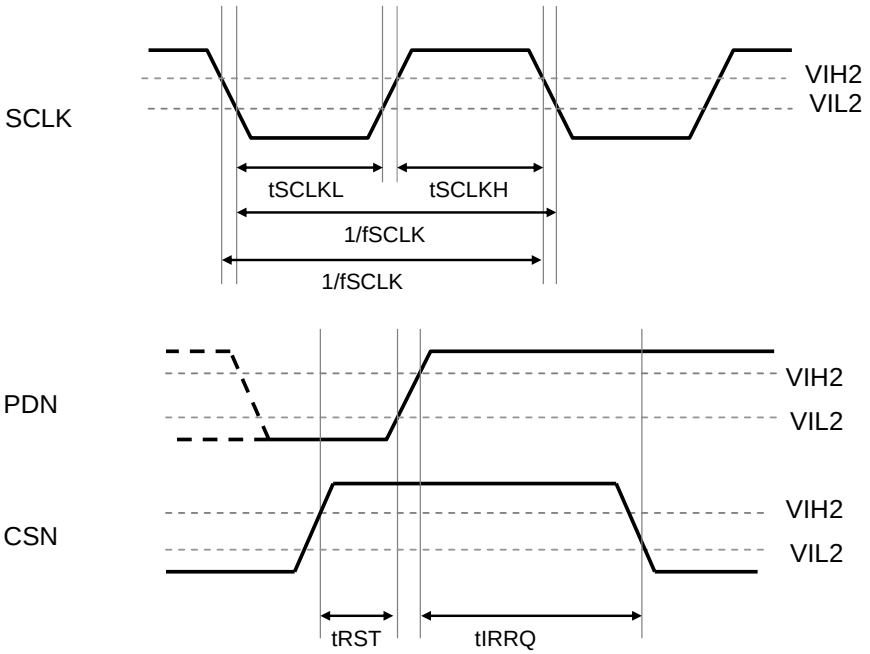


Figure 12. SPI Interface Timing 1

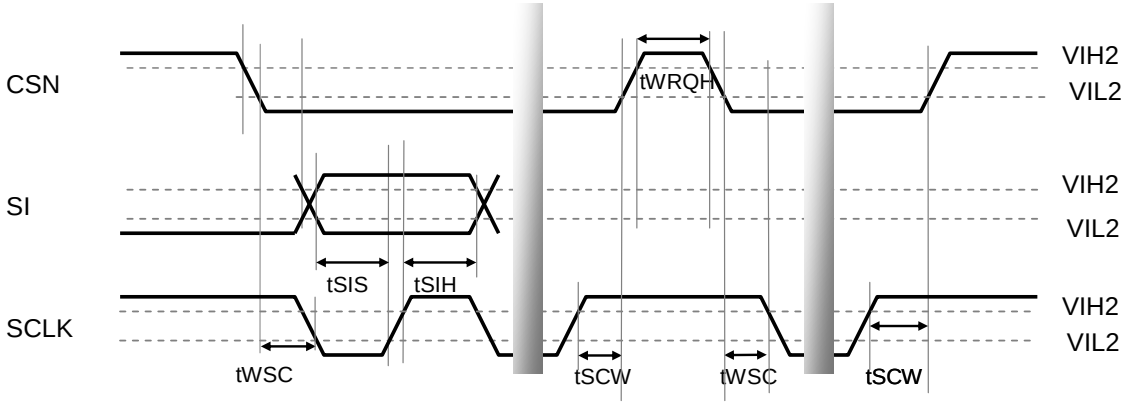


Figure 13. SPI Interface Timing 2 (Microcontroller → AK7738A)

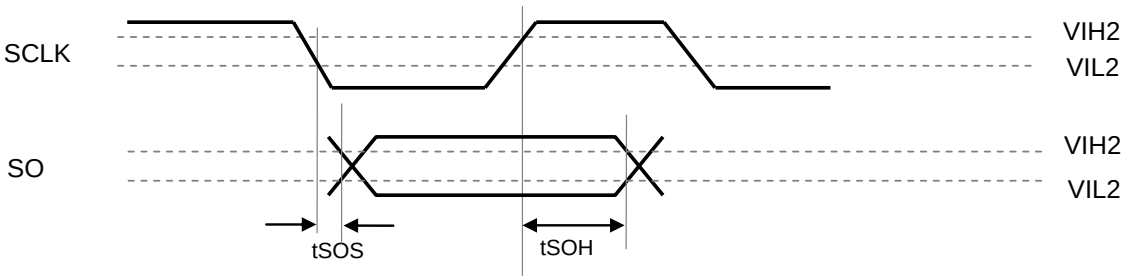


Figure 14. SPI Interface Timing 3 (AK7738A → Microcontroller)

5. I²C Interface

(Ta=25°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD1=1.7~3.6V; TVDD2=1.7~3.6V; VDD33=3.0~3.6V; AVSS=DVSS1=DVSS2=DVSS3=0V)

<I²C: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

<I²C: Fast Mode Plus>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	1	MHz
Bus Free Time Between Transmissions	tBUF	0.5	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.26	-	-	µs
Clock Low Time	tLOW	0.5	-	-	µs
Clock High Time	tHIGH	0.26	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.26	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.12	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	550	pF

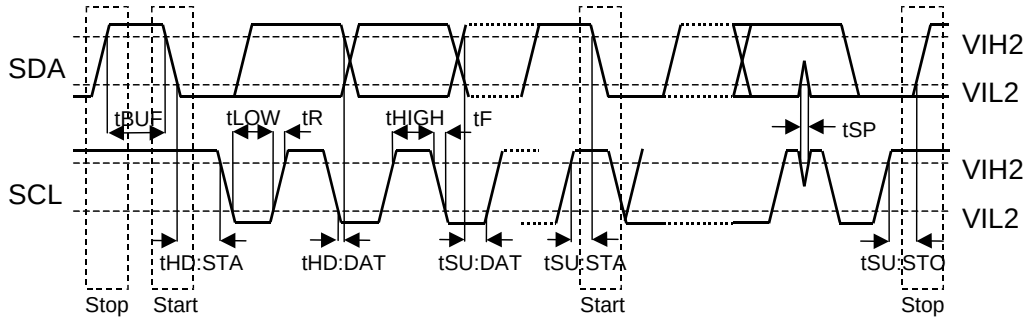


Figure 15. I²C-bus Interface Timing

12. Recommended External Circuits

■ Connection Diagram

1. I²C Interface

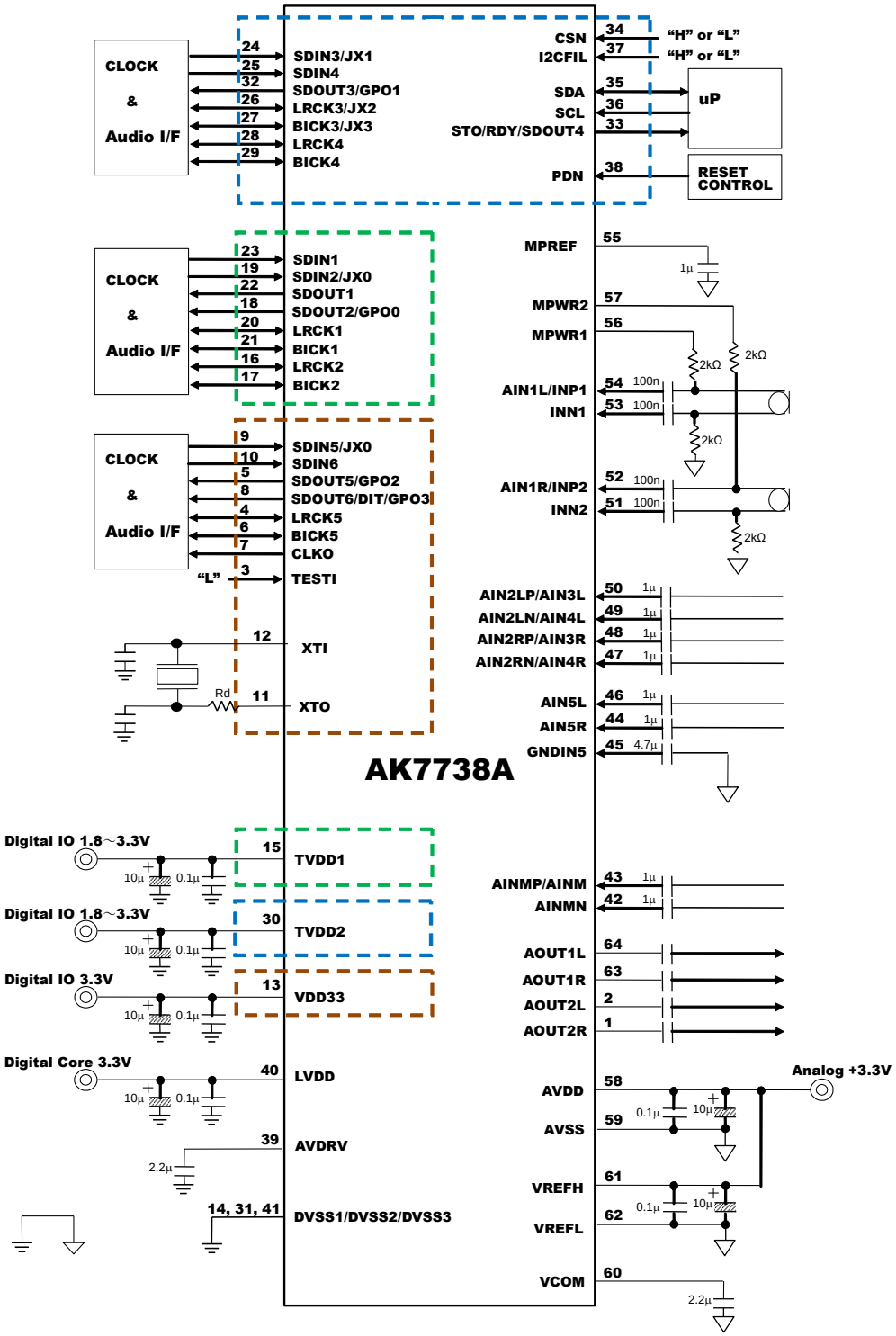


Figure 16. I²C Interface Connection Example

2. SPI Interface

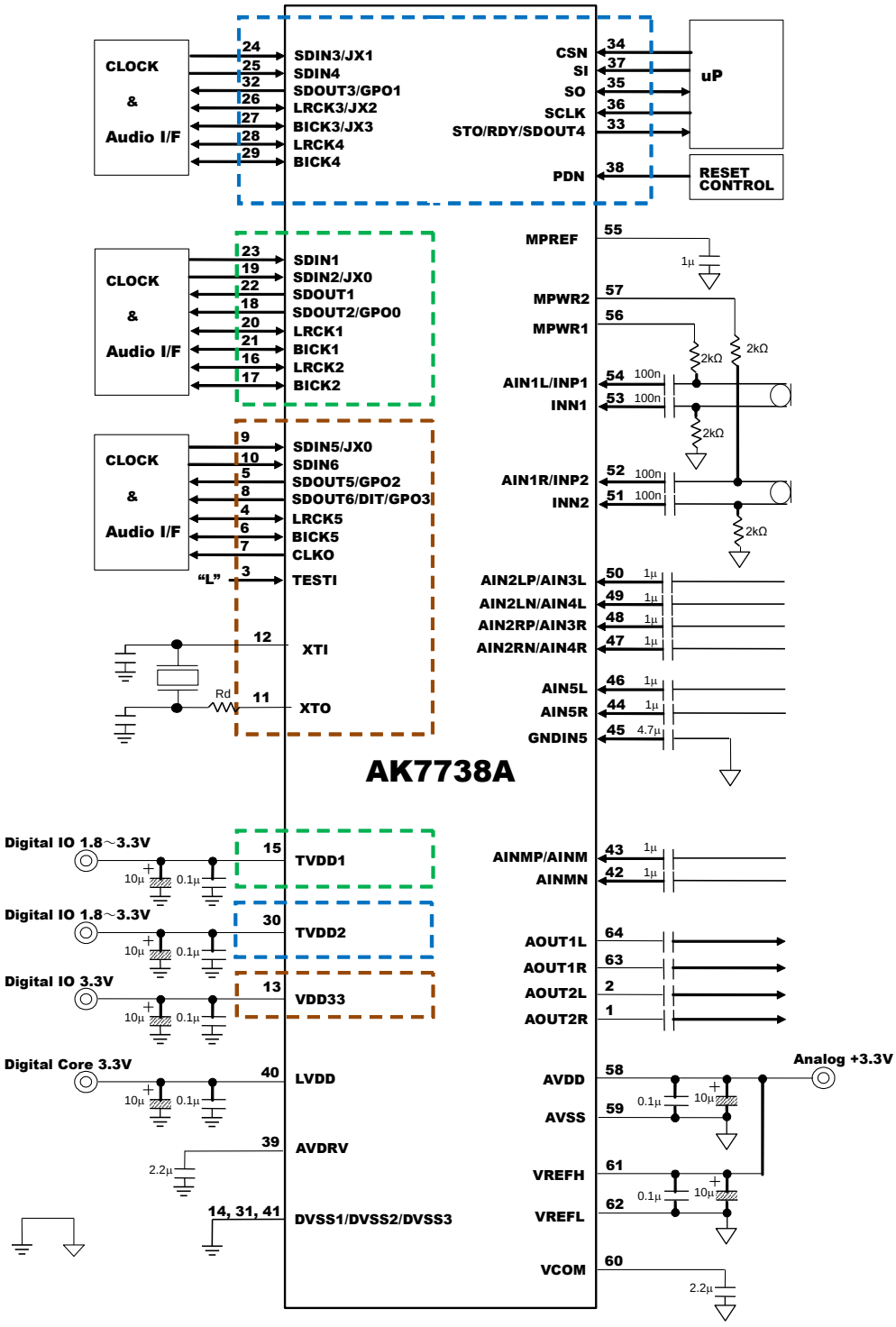


Figure 17. SPI Interface Connection Example

■ Peripheral Circuit

1. Ground

AVSS, DVSS1, DVSS2 and DVSS3 should be connected to the same ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as close as possible to the AK7738A.

2. Reference Voltage

The AVDD voltage controls analog signal range. VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2µF ceramic capacitor should be connected between the VCOM pin and AVSS.

Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK7738A.

3. Analog Input

The analog input signal is input to the analog modulator of the AK7738A. The maximum input voltage at differential input pins is FS = ±(AVDD - AVSS) x 2.3/3.3. The maximum input voltage at single-ended input pins is FS = (AVDD - AVSS) x 2.3/3.3. When AVDD = 3.3V and AVSS = 0.0V, the input voltage range at differential input pin is ±2.30Vpp and 2.30Vpp at single-ended input pin. The output code format is 2's complements. The internal HPF removes the DC offset.

After power-down is released, the internal operating point level AVDD/2 occurs on analog input pins of the AK7738A. Concerning the internal operating point formation circuit, each input pin has impedance of 20kΩ (typ @fs=48kHz). The pins that are connected to AC coupling capacitors require start-up time (time constant).

The AK7738A samples the analog inputs at 6.144MHz when fs=48kHz, 96kHz or 192kHz. The AK7738A includes an anti-aliasing filter (RC filter), and no external low-pass filter is needed in front of the ADC. However, an external low-pass filter should be connected before the ADC for the signal which has large out-of-band noise such as D/A converted signals.

The analog power supply to the AK7738A is +3.3V typical. Voltage of AVDD + 0.3V or larger, voltage of AVSS - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

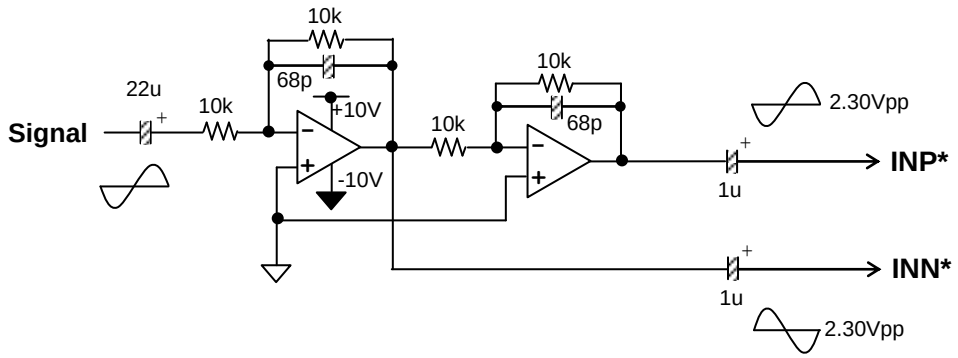


Figure 18. Input Buffer Circuit Example at fs=48kHz (Differential Input)

4. Analog Output

The analog output is single-ended and the output signal range is typically 0.857 x AVDD Vpp centered on VCOM. The digital input data format is two's compliment. Positive full-scale output corresponds to 7FFFFFFFH (@32bit) input code, Negative full scale is 80000000H (@32bit) and VCOM voltage ideally is 00000000H (@32bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

5. Connection to Digital Circuit

To minimize the noise from digital circuits, the digital output of the AK7738A must be connected to CMOS or low voltage logic ICs such as 74HC and 74AC for CMOS and 74LV, 74LV-A, 74ALVC and 74AVC for low voltage logic ICs.

6. Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

XTAL Oscillator	R1 (max)	C0 (max)	XTI, XTO pin Capacity
12.288MHz	120Ω	2.5pF	22pF
18.432MHz	80Ω	2.5pF	15pF

Table 5. Recommended Resistance and Capacitance with Crystal Oscillator

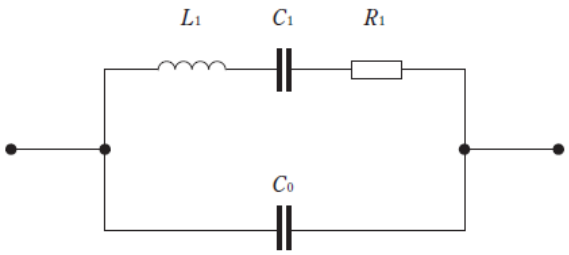
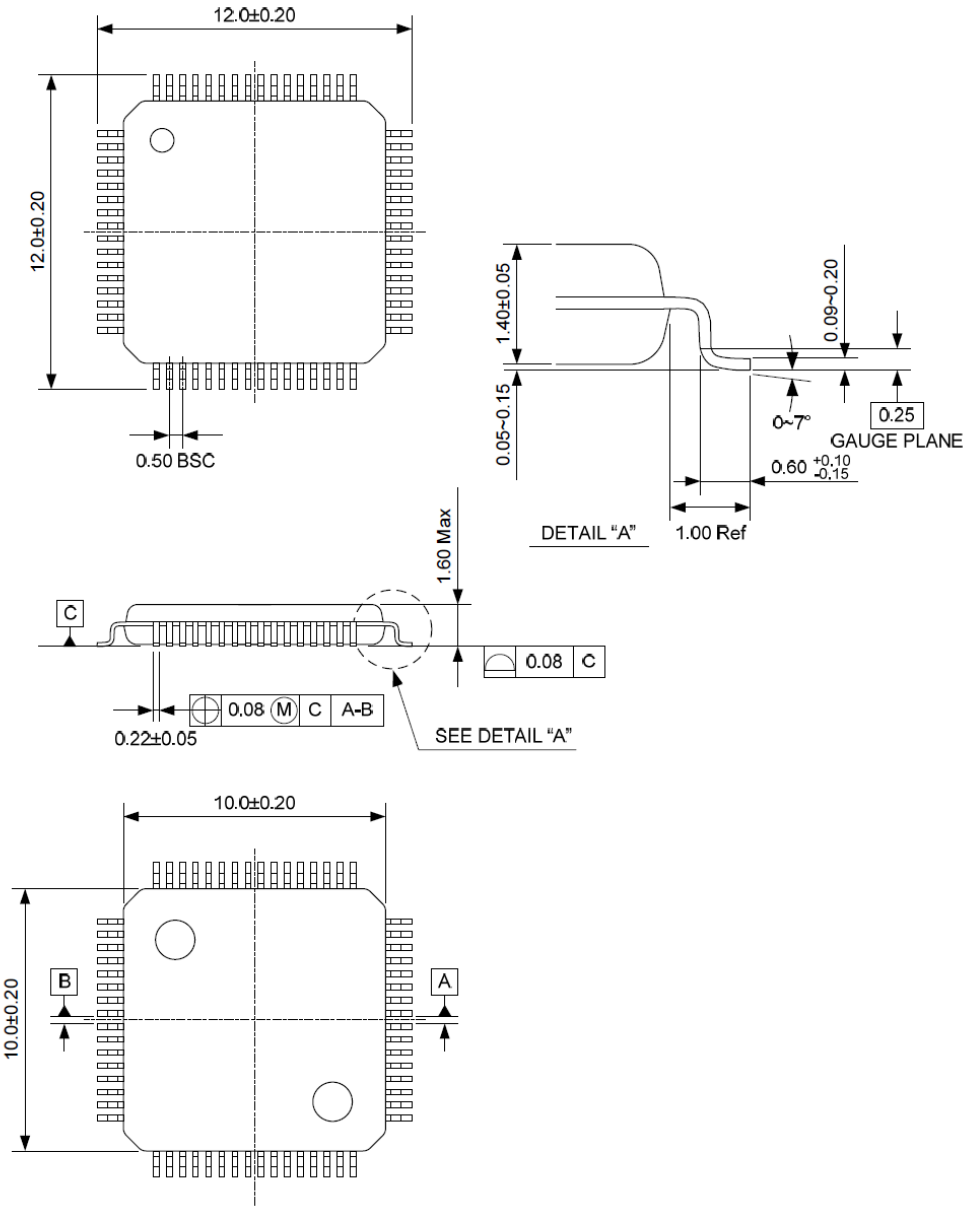


Figure 19. Electric Equivalent Circuit of Crystal Oscillator

13. Package

■ Outline Dimensions

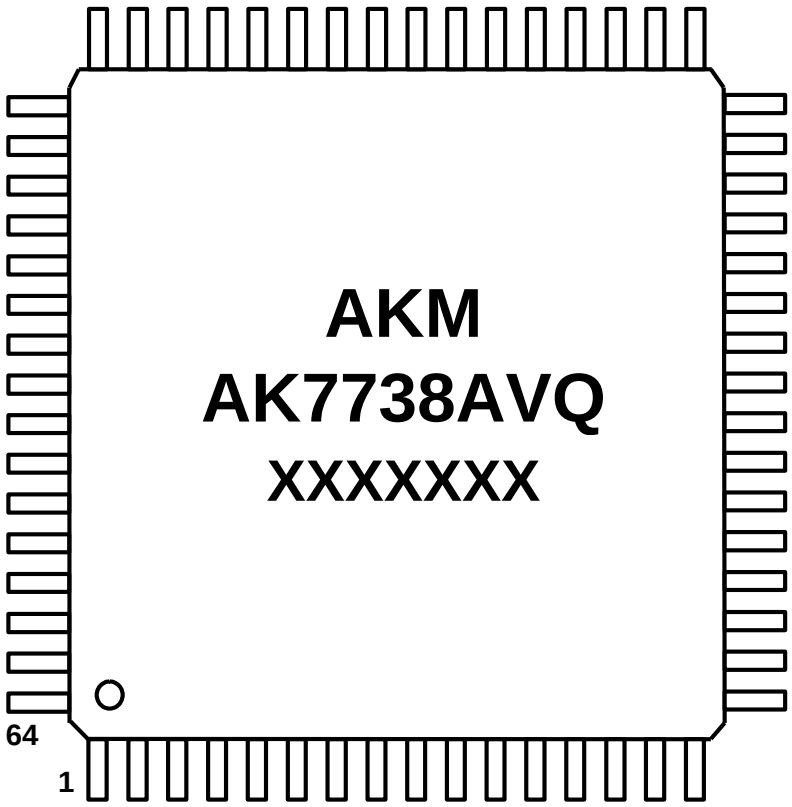
64-pin LQFP (Unit: mm)



■ Material and Lead Finish

Package: Epoxy
Lead frame: Copper
Lead-finish: Soldering (Pb free) plate

■ **Marking**



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7738AVQ
4) Asahi Kasei Logo

14. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
17/06/26	00	First Edition		

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