

AsahiKASEI
ASAHI KASEI EMD**AK7752****Audio/Hands Free DSP with Stereo CODEC****GENERAL DESCRIPTION**

The AK7752 is a digital signal processor with an integrated stereo CODEC. The digital signal processor (DSP) can execute a high-quality hands-free algorithm, using only internal memory. Fine tuning is available for improving voice quality of the hands-free function in actual user environments. The AK7752 includes delay RAM, an integrated PLL, four digital audio input and eight digital audio output ports. The AK7752 can perform pre and post processing for speech recognition, volume control adjustment and parametric equalization, executed by programs downloaded via the microprocessor interface.

FEATURES**[ADC Block]**

- Sampling rate: 8kHz ~ 48kHz
- 24-bit stereo
- S/(N+D): 86dB
- DR, S/N: 89dB (fs=8 kHz), 91dB (fs=48kHz)
- Integrated DC offset canceling High Pass Filter

[DAC Block]

- Sampling rate: 8kHz ~ 48kHz
- 18-bit stereo
- S/(N+D): 90dB (fs =8kHz), 88dB (fs=48kHz)
- DR, S/N: 95dB (fs =8kHz), 95dB (fs=48kHz)

[Input/Output Digital Interface]

- 4-channel Serial Data Input
- 8-channel Serial Output

[General]

- Integrated PLL
- EEPROM (AK6514C) Interface
- Microprocessor Interface: I²C BUS or AKM original mode
- Power Supply: Single 3.3V ±0.3V
- Operating Temperature Range: -40°C~85°C
- 64pin LQFP

BLOCK DIAGRAM

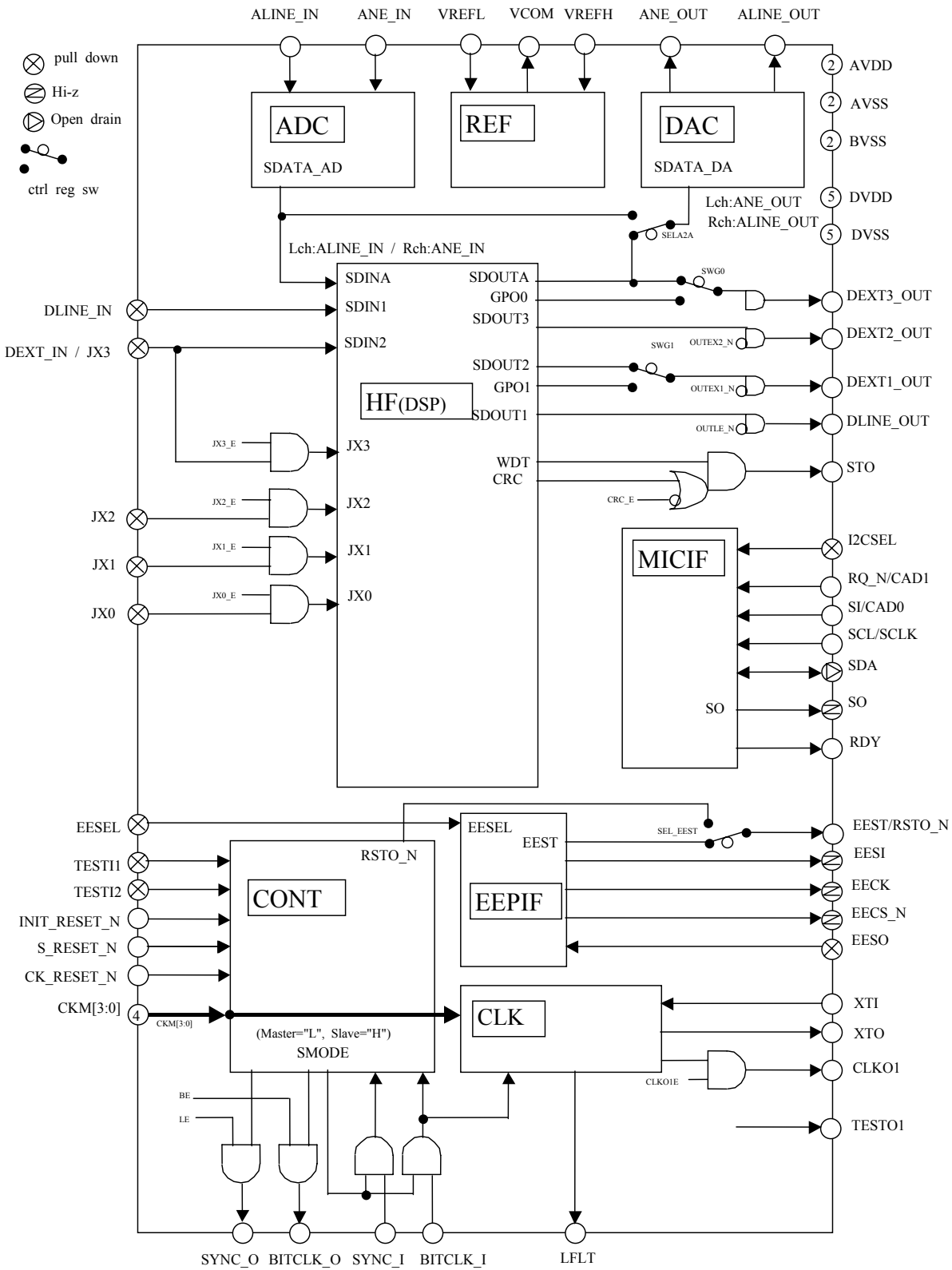


Figure 1. Block Diagram

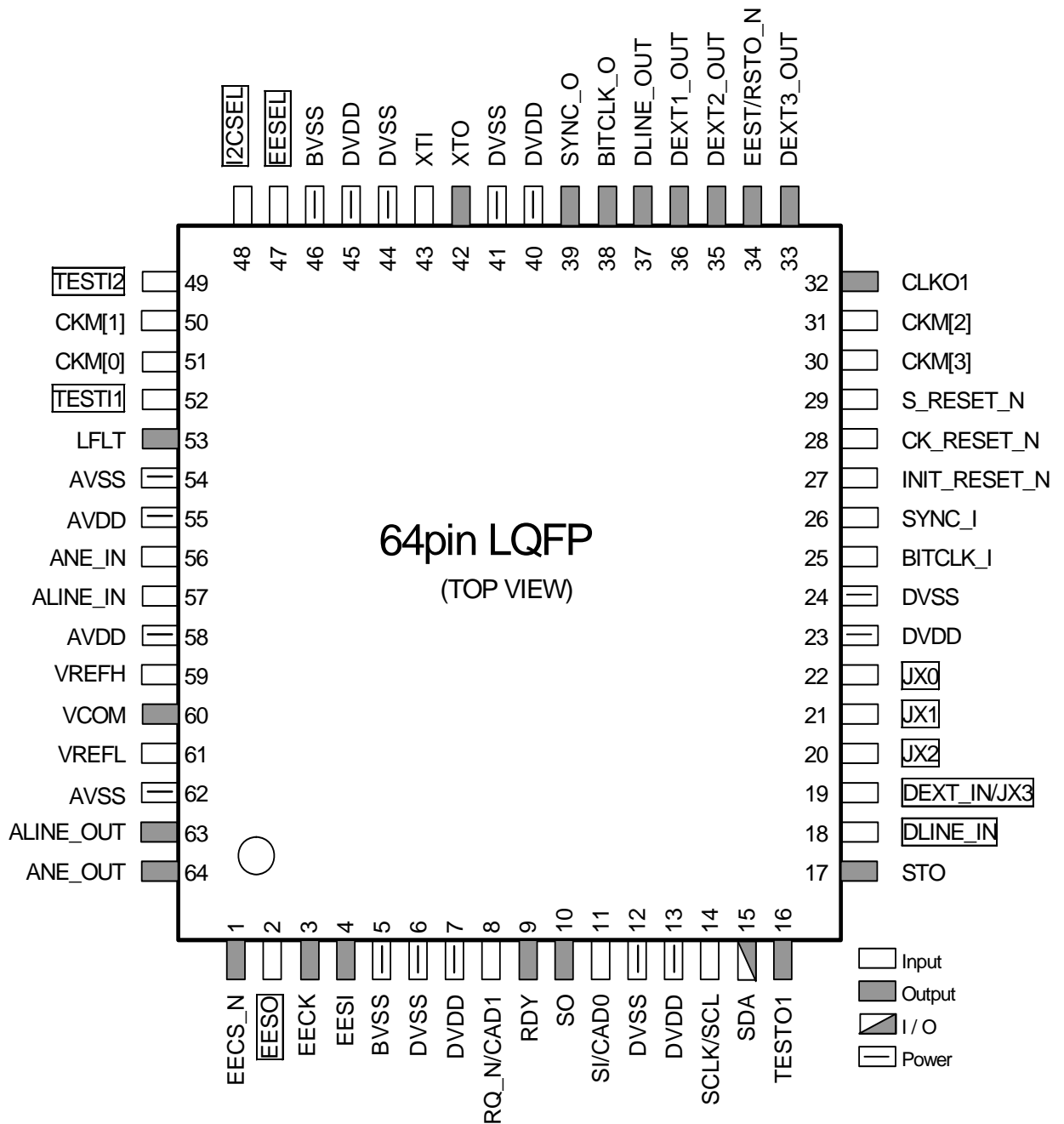
* Figure 1 shows a simplified diagram of the AK7752, which isn't the perfect same as the actual circuit diagram.

■ Ordering Guide

 AK7752VQ
 AKD7752

 -40 ~ +85°C 64pin LQFP
 Evaluation Board for AK7752

■ Pin Layout



Note) XXXX is internal pull-down pin. XXXX is the pin name.

PIN/FUNCTION

| No. | Pin Name | I/O | Function | Classification |
|-----|----------|-----|---|---------------------------|
| 1 | EECS_N | O | EEPROM Chip Select Pin Connect to the C_N pin of the AK6514C (EEPROM). The output is Hi-Z when EESEL pin= "L". | EEPIF |
| 2 | EESO | I | EEPROM Serial Data Receive Pin (Internal pull-down) Connect to the SO pin of the AK6514C (EEPROM). Connect to DVSS or leave open when a EEPROM is not use. | |
| 3 | EECK | O | EEPROM Serial Data Output Clock Pin Connect to the SCK pin of the AK6514C (EEPROM). The output is Hi-Z when EESEL pin = "L". | |
| 4 | EESI | O | EEPROM Serial Data Output Pin Connect to the SI pin of the AK6514C. The output is Hi-Z when EESEL pin= "L". | |
| 5 | BVSS | - | Silicon Substrate Potential 0V Connect to AVSS. | Analog Power Supply |
| 6 | DVSS | - | Ground Pin for Digital Section 0.0V | Digital |
| 7 | DVDD | - | Power Supply Pin for Digital Section (3.3V typical) | Power Supply |
| 8 | RQ_N | I | Microprocessor Interface Write Request Pin (I2CSEL pin = "L") When initial reset state and Microcomputer interface are not in use, leave RQ_N pin= "H". | Microprocessor Interface. |
| | CAD1 | I | I²C Bus Address Setting Pin 1 (I2CSEL pin = "H") | |
| 9 | RDY | O | Data Write Ready Output Pin for Microprocessor Interface | Microprocessor Interface |
| 10 | SO | O | Serial Data Output Pin for Microprocessor Interface When RQ_N pin = "H", SO pin= Hi-Z | |
| 11 | SI | I | Serial Data Input Pin for Microprocessor Interface (I2CSEL pin = "L") When SI is not used, tie the SI pin = "L". | |
| | CAD0 | I | I²CSEL= "H" I²C Bus Address Pin 0 | I ² C |
| 12 | DVSS | - | Ground Pin for Digital Section 0.0V | Digital |
| 13 | DVDD | - | Power Supply Pin for Digital Section (3.3V typical) | Power Supply |
| 14 | SCLK | I | Serial Data Clock Pin for Microprocessor Interface (I2CSEL pin = "L") When SCLK is not used, tie the SCLK pin = "H". | Microprocessor Interface |
| | SCL | I | I²C Bus Data Clock Pin (I2CSEL pin = "H") | |
| 15 | SDA | I/O | Test Pin (I2CSEL pin = "L") Leave open. SDA goes "L". | TEST |
| | SDA | I/O | I²C Bus Data Clock Pin (I2CSEL pin = "H") | I ² C |
| 16 | TESTO1 | O | Test Output Pin Leave open. Normally TESTO1 goes "L". | TEST |
| 17 | STO | O | Status Output Pin | Status |

| No. | Pin Name | I/O | Function | Classification |
|-----|-----------------|-----|--|---|
| 18 | DLINE_IN | I | HF Serial Data Input Pin (Internal pull-down) Compatible with MSB / LSB justified 24, 20 and 16 bits. Normally connected to Bluetooth line (receiving). | Digital Section Serial Input Data |
| 19 | DEXT_IN/ JX3 | I | HF Serial Data Input Pin (Internal pull-down) Compatible with MSB / LSB justified 24, 20 and 16 bits. This pin changes to a conditional jump pin (JX3) by setting control register (JX3_E) to "1". | Digital Section Serial Input Data / Conditional Input |
| 20 | JX2 | I | Conditional Jump Pin2 (Internal pull-down) A conditional jump pin (JX2) is available by setting control register (JX2_E) to "1". | Conditional Input |
| 21 | JX1 | I | Conditional Jump Pin1 (Internal pull-down) A conditional jump pin (JX1) is available by setting control register (JX1_E) to "1". | |
| 22 | JX0 | I | Conditional Jump Pin0 (Internal pull-down) A conditional jump pin (JX2) is available by setting control register (JX0_E) to "1". | |
| 23 | DVDD | - | Power Supply for Digital Section (3.3V typical) | Digital Power Supply |
| 24 | DVSS | - | Ground Pin for Digital Section 0V | |
| 25 | BITCLK_I | I | Serial Bit Clock Input Pin Normally connected to the Bluetooth Data Clock line (256kHz/512kHz). | System Clock |
| 26 | SYNC_I | I | SYNC Input Pin Normally connected to the Bluetooth Sync Clock line (8kHz). | |
| 27 | INIT_RESET_N | I | Reset Pin (for initialization) Use to initialize the AK7752. When changing CKM [3:0] and changing XTI or BITCLK_I input frequency, it is necessary to set this pin. | Reset |
| 28 | CK_RESET_N | I | Clock Reset Pin When changing CKM[3:0] and XTI or BITCLK_I input frequency without using INIT_RESET_N, it is necessary to set this pin. The control register CKRST has the same function. | |
| 29 | S_RESET_N | I | System Reset N Pin | |
| 30 | CKM[3] | I | Clock Mode Select Pin 3 | Mode Select |
| 31 | CKM[2] | I | Clock Mode Select Pin 2 | |
| 32 | CLKO1 | O | Clock Output Pin 1 The output frequency is selected by a control register. | Clock Output |

| No. | Pin Name | I/O | Function | Classification |
|-----|-----------------|-----|---|---|
| 33 | DEXT3_OUT | O | HF Serial Data Output Pin The data format is MSB justified. | TEST |
| 34 | EEST /RSTO_N | O | EES Output Pin / Internal Reset Monitor Pin Set by control resistor SEL_EEST. SEL_EEST bit=“0”: EEST pin SEL_EEST bit=“1”: RSTO_N Monitor internal reset process. RSTO_N pin =“L”: Reset mode, RSTO_N pin =“H”: Exit reset mode. | EEPIF/ Monitor |
| 35 | DEXT2_OUT | O | HF Serial Data Output Pin Compatible with MSB / LSB justified 24, 20 and 16 bits. | Digital Section Serial Input Data |
| 36 | DEXT1_OUT | O | HF Serial Data Input Pin Compatible with MSB / LSB justified 24, 20 and 16 bits. | |
| 37 | DLINE_OUT | O | HF Serial Data Output Pin Compatible with MSB / LSB justified 24, 20 and 16 bits. Normally connected to Bluetooth line (sending). | |
| 38 | BITCLK_O | O | Serial Bit Clock Output Pin Normally goes “L” by control register setting. Master Mode: Outputs 64fs or 32fs clock. Slave Mode: Outputs BITCLK_I clock. | System Clock |
| 39 | SYNC_O | O | SYNC Output Pin Normally goes “L” by control register setting. Master Mode: Outputs 64fs or 32fs clock. Slave Mode: Outputs SYNC_I clock. | |
| 40 | DVDD | - | Power Supply for Digital Section (3.3V typical) | Digital Power Supply |
| 41 | DVSS | - | Ground Pin for Digital Section 0V | |
| 42 | XTO | O | Crystal oscillator output pin When a crystal oscillator is used, connect it between XTI and XTO. When an external clock is used, leave this pin open. | System Clock |
| 43 | XTI | I | Crystal oscillator input pin Connect a crystal oscillator between this pin and the XTO pin, or input an external CMOS clock to the XTI pin. | |
| 44 | DVSS | - | Ground Pin for Digital Section 0V | Digital Power Supply |
| 45 | DVDD | - | Power Supply for Digital Section (3.3V typical) | |
| 46 | BVSS | - | Silicon Substrate Potential 0V Connect to AVSS. | Analog Power Supply |
| 47 | EESEL | I | Control Mode select pin (Internal pull-down) EESEL pin = “L” : Normal mode EESEL pin = “H”: In self-boot up mode using an AKM EEPROM, AK6514C | EEPIF |
| 48 | I2CSEL | I | I²C BUS Select Pin (Internal pull-down) I2CSEL pin = “L”: Normal serial interface I2CSEL pin = “H”: I2C Bus selected mode. SCL and SDA are active. I2CSEL should be connected to “L” (DVSS) or “H” (DVDD). | I ² C Select |
| 49 | TESTI2 | I | TEST pin (Internal pull-down) Connect to DVSS. | TEST |

| No. | Pin Name | I/O | Function | Classification |
|-----|-----------|-----|--|---------------------|
| 50 | CKM[1] | I | Clock Mode Select Pin 1 | Mode Select |
| 51 | CKM[0] | I | Clock Mode Select Pin 0 | |
| 52 | TEST1 | I | TEST pin (Internal pull-down) Connect to DVSS. | TEST |
| 53 | LFLT | O | PLL RC component connect pin Connect a series resistor and capacitor pair to this pin. | Analog Output |
| 54 | AVSS | - | Analog ground Pin 0V (Silicon substrate potential) | Analog Power Supply |
| 55 | AVDD | - | Power Supply Pin for Analog Section (3.3V typical) | |
| 56 | ANE_IN | I | ADC Analog Input Pin (ANE_IN) Normally connected to the microphone amplifier. | Analog Input |
| 57 | ALINE_IN | I | ADC Analog Input Pin (ALINE_IN) Normally the receiving analog phone voice signal is input. | |
| 58 | AVDD | - | Analog Power Supply Pin (3.3V typical) | Analog Power Supply |
| 59 | VREFH | I | Analog Reference Voltage Input Pin Connect this pin to AVDD. Connect capacitors of 0.1 uF and 10 uF between this pin and AVSS. | Analog Input |
| 60 | VCOM | O | Analog Common Voltage Output pin Connect capacitors of 0.1 uF and 10 uF between this pin and AVSS. No external circuits should be connected to this pin. | Analog Output |
| 61 | VREFL | I | Analog Reference Voltage Input pin Connect this pin to AVSS. | Analog Input |
| 62 | AVSS | - | Analog ground Pin 0V (Silicon substrate potential) | Analog Power Supply |
| 63 | ALINE_OUT | O | DAC Analog Output Pin (ALINE_OUT) Normally the sending analog phone voice signal is output. | Analog Output |
| 64 | ANE_OUT | O | DAC Analog Output Pin (ANE_OUT) Normally connected to the speaker amplifier. | |

Note 1. Do NOT leave digital input pins open except for pins that indicate “Internal pull down”, BITCLK_I and SYNC_I at master mode. (Internal pull down pins except TEST1 and TEST2 pins leave them open or connect them to DVSS. Connect TEST1 and TEST2 pins to DVSS).

Note 2. When analog input pins (ALINE_IN, ANE_IN) are not used, leave them open.

Note 3. Connect I2CSEL to “L” (DVSS) or “H” (DVDD).

Relationship between I2CSEL and SDA

| uP I/F | I2CSEL | INIT_RESET_N | SDA |
|---------------------------|--------|--------------|------------------|
| Normal Serial Interface | L | L | L |
| | L | H | L |
| I ² C Bus Mode | H | L | “Hi-Z” → pull-up |
| | H | H | function |

ABSOLUTE MAXIMUM RATINGS

(AVSS, BVSS, DVSS=0V: All voltages are with respect to ground)

| Parameter | Symbol | min | max | Units |
|--|--------------|------|----------|-------|
| Power Supply Voltage | | | | |
| Analog (AVDD) | VA | -0.3 | 4.6 | V |
| Digital (DVDD) | VD | -0.3 | 4.6 | V |
| AVSS(BVSS) – DVSS (Note 4) | Δ GND | | 0.3 | V |
| Input Current (except for power supply pin) | IIN | - | \pm 10 | mA |
| Analog Input Voltage | | | | |
| ALINE IN, ANE IN | VINA | -0.3 | VA+0.3 | V |
| Digital Input Voltage | VIND | -0.3 | VD+0.3 | V |
| Operating Ambient Temperature | Ta | -40 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 4. AVSS, BVSS and DVSS must be connected to the same ground plane..

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, BVSS, DVSS=0V: All voltages indicated are relative to the ground)

| Parameter | Symbol | min | typ | max | Units |
|--------------------------|--------|-----|-----|-----|-------|
| Power Supply Voltage | | | | | |
| AVDD | VA | 3.0 | 3.3 | 3.6 | V |
| DVDD | VD | 3.0 | 3.3 | 3.6 | V |
| Reference Voltage (VREF) | | | | | |
| VREFH (Note 5) | VRH | | VA | | V |
| VREFL (Note 6) | VRL | | 0.0 | | V |

Note 5. VREFH is normally connected to AVDD.

Note 6. VREFL is normally connected to AVSS

Note: The analog input voltage and output voltage are proportional to the VREFH-VREFL voltages.
When using the AK6514C, the same voltage as used for the digital section of the AK7752 is recommended.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

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|---------------------------------|
| ELECTRIC CHARACTERISTICS |
|---------------------------------|

(1) Analog Characteristics**1) fs=8kHz**

(Ta = 25°C; AVDD, DVDD = 3.3V; VREFH = AVDD, VREFL = AVSS;
 BITCLK = 64fs; Signal frequency 1kHz; Measurement frequency = 20Hz to 3.4 kHz; fs = 8kHz;
 CKM Mode 0 (CKM[3:0]=LLLL) Unless otherwise specified.)

| | Parameter | min | typ | max | Units | |
|--------------------|--|------|------|------|-------|--|
| ADC Section | Resolution | 24 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) (-1dBFS) | 76 | 86 | | dB | |
| | Dynamic Range (Note 7) | 81 | 89 | | dB | |
| | S/N | 81 | 89 | | dB | |
| | Inter-Channel Isolation (f=1kHz) (Note 8.) | 90 | 105 | | dB | |
| | DC accuracy | | | | | |
| | Channel Gain Mismatch | | 0.2 | 0.5 | dB | |
| | Analog Input | | | | | |
| | Input Voltage (Note 9) | 1.78 | 1.98 | 2.18 | Vp-p | |
| | Input Impedance | 40 | 60 | | kΩ | |
| DAC Section | Resolution | 18 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) (0dB) | 80 | 90 | | dB | |
| | Dynamic Range (Note 7) | 87 | 95 | | dB | |
| | S/N | 87 | 95 | | dB | |
| | Inter-Channel Isolation (f=1kHz) (Note 10) | 85 | 100 | | dB | |
| | DC accuracy | | | | | |
| | Channel Gain Mismatch | | 0.2 | 0.5 | dB | |
| | Analog Output | | | | | |
| | Output Voltage (Note 11) | 1.85 | 2.00 | 2.15 | Vp-p | |
| | Load Resistance | 10 | | | kΩ | |
| Load Capacitance | | | 50 | pF | | |

Note 7. S/(N+D) when -60dB signal is applied.

Note 8. Inter-channel isolation between ALINE_IN and ANE_IN at -1dB FS signal input.

Note 9. The full scale for analog input voltage is FS = (VREFH-VREFL) * 0.6.

Note 10. Between ANE_OUT and ALINE_OUT.

Note 11. Full scale output voltage when VREFH = AVDD, VREFL = AVSS.

2) $f_s=48\text{kHz}$

($T_a = 25^\circ\text{C}$; AVDD, DVDD = 3.3V; VREFH = AVDD, VREFL = AVSS;
 BITCLK = 64fs; Signal frequency 1kHz; Measurement frequency = 20Hz to 3.4kHz; $f_s = 48\text{kHz}$;
 CKM Mode 0 (CKM [3:0]=LLLL) Unless otherwise specified.)

| | Parameter | min | typ | max | Units | |
|--------------------|---|------|------|------|------------------|--|
| ADC Section | Resolution | 24 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) (-1dBFS) | 76 | 86 | | dB | |
| | Dynamic Range (A-weighted) (Note 12) | 83 | 91 | | dB | |
| | S/N (A-weighted) | 83 | 91 | | dB | |
| | Inter-Channel Isolation ($f=1\text{kHz}$) (Note 13) | 90 | 110 | | dB | |
| | DC accuracy | | | | | |
| | Channel Gain Mismatch | | 0.2 | 0.5 | dB | |
| | Analog Input | | | | | |
| | Input Voltage (Note 14) | 1.80 | 2.00 | 2.20 | V _{p-p} | |
| | Input Impedance | 35 | 50 | | k Ω | |
| DAC Section | Resolution | 18 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) (0 dB) | 78 | 88 | | dB | |
| | Dynamic Range (A-weighted) (Note 12) | 87 | 95 | | dB | |
| | S/N (A-weighted) | 87 | 95 | | dB | |
| | Inter-Channel Isolation ($f=1\text{kHz}$) (Note 15) | 85 | 100 | | dB | |
| | DC Accuracy | | | | | |
| | Channel Gain Mismatch | | 0.2 | 0.5 | dB | |
| | Analog input | | | | | |
| | Output Voltage (Note 16) | 1.85 | 2.00 | 2.15 | V _{p-p} | |
| | Load Resistance | 10 | | | k Ω | |
| Load Capacitance | | | 50 | pF | | |

Note 12. S/(N+D) when -60dB signal is applied.

Note 13. Inter-channel isolation between ALINE_IN and ANE_IN at -1 dB FS signal input.

Note 14. The full scale for analog input voltage is $FS=(VREFH-VREFL)\times 0.606$.

Note 15. Between ANE_OUT and ALINE_OUT.

Note 16. Full scale output voltage when VREFH=AVDD, VREFL=AVSS.

(2) DC Characteristics

(Ta=-40°C ~ 85°C; AVDD, DVDD=3.0 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|--|-----------------|---------|-----|--------|-------|
| High Level Input Voltage (Note 17) | V _{IH} | 80%VDD | | | V |
| Low Level Input Voltage (Note 17) | V _{IL} | | | 20%VDD | V |
| SCL, SDA High Level Input Voltage | V _{IH} | 70%VDD | | | V |
| SCL, SDA Low Level Input Voltage | V _{IL} | | | 30%VDD | V |
| High Level Output Voltage I _{out} =-100μA (Note 18) | V _{OH} | VDD-0.5 | | | V |
| Low Level Output Voltage I _{out} =100μA | V _{OL} | | | 0.5 | V |
| SDA Low Level Output Voltage I _{out} =3mA | V _{OL} | | | 0.4 | V |
| Input Leak Current (Note 19) | I _{in} | | | ±10 | μA |
| Input Leak Current (pull-down pin) (Note 20) | I _{id} | | 22 | | μA |
| Input Leak Current (XTI pin) | I _{ix} | | 26 | | μA |

Note 17. SCL and SDA pins are not included. (SI, SCLK pins are included)

Note 18. SDA pin is not included.

Note 19. Pull-down pins and XTI pin are not included.

Note 20. EESO, DLINE_IN, DEXT_IN / JX3, JX2, JX1, JX0, EESEL, I2CSEL, TESTI2 and TESTI1 (Typ150kΩ)

(3) Current Consumption

(Ta=25°C; AVDD, DVDD=3.0~3.6V (typ = 3.3V, max = 3.6V))

| Parameter | min | typ | max | Units |
|---------------------------------------|-----|-----|-----|-------|
| Power Supply Current (Note 21) | | | | |
| AVDD | | 10 | | mA |
| DVDD | | 90 | | mA |
| AVDD + DVDD | | 100 | 165 | mA |

Note 21. The current of DVDD changes depending on the system frequency and contents of the DSP program.

(4) Digital Filter Characteristics

1) ADC Section:

(Ta= 25°C; AVDD, DVDD=3.0 ~ 3.6V; fs = 8kHz; Note 22)

| Parameter | Symbol | min | typ | max | Units |
|---|--------|------|------|------|-------|
| Passband (±0.1dB) (Note 23) | PB | 0 | | 3.15 | kHz |
| (-1.0dB) | | | 3.63 | | kHz |
| (-3.0dB) | | | 3.83 | | kHz |
| Stopband | SB | 4.66 | | | kHz |
| Passband Ripple (Note 23) | PR | | | ±0.1 | dB |
| Stopband Attenuation (Note 24, Note 25) | SA | 65 | | | dB |
| Group Delay Distortion | GD | | | 0 | μs |
| Group Delay (Ts=1/fs) | GD | | 16.3 | | Ts |

Note 22. HPF response is not included.

Note 23. The passband is from DC to 3.15kHz when fs = 8kHz.

Note 24. The stopband is from 4.66kHz to 507.34kHz when fs = 8kHz.

Note 25. When fs = 8 kHz, the analog modulator samples the analog input at 512kHz

2) DAC Section:

(Ta=25°C; AVDD, DVDD=3.0~3.6V; fs=8kHz)

| Parameter | Symbol | min | typ | max | Units |
|------------------------------------|--------|------|------|-------|-------|
| Digital Filter | | | | | |
| Passband (±0.1dB) (Note 26) | PB | 0 | 4.0 | 3.5 | kHz |
| (-6.0dB) | | - | | - | kHz |
| Stopband (Note 26) | SB | 4.57 | | | kHz |
| Passband Ripple | PR | | | ±0.01 | dB |
| Stopband Attenuation | SA | 59 | | | dB |
| Group Delay (Ts=1/fs) (Note 27) | GD | - | 15 | | Ts |
| Digital Filter + SCF | | | | | |
| Amplitude Characteristics 0~3.5kHz | | | ±0.5 | | dB |

Note 26. The pass band and stop band frequencies are proportional to “fs” (system sampling rate), and represents PB=0.4292fs (@-0.06dB) and SB=0.571fs, respectively.

Note 27. The digital filter’s delay is calculated as the time from setting 18 Bit data into the input register until an analog signal is output.

(5) Switching Characteristics**1) System Clock**

(Ta=-40°C~85°C; AVDD, DVDD=3.0~3.6V)

| Parameter | Symbol | min | typ | max | Units |
|--------------------------------------|--------|------|-------------------|------|-------|
| XTI CKM Mode 0-6 | | | | | |
| a) with a Crystal Oscillator: | | | | | |
| Frequency (CKM Mode 0/2) | fXTI | - | 11.2896 12.288 | - | MHz |
| Frequency (CKM Mode 1/3) | fXTI | - | 24.576 | - | MHz |
| b) with an External Clock | | | | | |
| Duty Cycle | | 40 | 50 | 60 | % |
| Frequency (CKM Mode 0/2) | fXTI | 11.0 | | 12.4 | MHz |
| Frequency (CKM Mode 1/3) | fXTI | 22 | | 24.8 | MHz |
| Clock Rise Time | tCR | | | 6 | ns |
| Clock Fall Time | tCF | | | 6 | ns |
| SYNC_I Frequency (Note 28) | Fs | 7.35 | 8 | 48 | kHz |
| Clock rise time | tLR | | | 6 | ns |
| Clock fall time | tLF | | | 6 | ns |
| BITCLK_I Frequency | | | | | |
| High Level Width | tBCLKH | 120 | | | ns |
| Low Level Width | tBCLKL | 120 | | | ns |
| Clock Rise Time | tBR | | | 6 | ns |
| Clock Fall Time | tBF | | | 6 | ns |
| a) CKM Mode 2/3 (Note 29) | fBCLK | 32 | | 64 | fs |
| Duty Cycle | | 40 | 50 | 60 | % |
| Frequency (CKM Mode 2/3) | | 0.23 | | 3.2 | MHz |
| b) CKM Mode 4 (Note 30) | fBCLK | - | 32 | - | fs |
| Duty Cycle | | 40 | 50 | 60 | % |
| Frequency (CKM Mode 4) | fBCLK | 230 | 256 | 258 | kHz |
| c) CKM Mode 5/6 (Note 31) | fBCLK | - | 64 | - | fs |
| Duty Cycle | | 40 | 50 | 60 | % |
| Frequency (CKM Mode 5) | fBCLK | 460 | 512 | 516 | kHz |
| Frequency (CKM Mode 6) | fBCLK | 2.75 | 3.072 | 3.1 | MHz |

Note 28. SYNC_I frequency and sampling rate (fs) should be the same.

Note 29. When BITCLK_I is 32fs, I/O interface format has some limitation.

Note 30. When BITCLK_I is a source of master clock, it should be 32 times fs correctly.

Note 31. When BITCLK_I uses as a source of master clock, it should be 64 times fs correctly.

2) Reset

(Ta=-40°C~85°C; AVDD, DVDD=3.0~3.6V)

| Parameter | Symbol | min | typ | max | Units |
|------------------------|--------|-----|-----|-----|-------|
| INIT RESET N (Note 32) | tRST | 600 | | | ns |
| CK RESET N | tRST | 600 | | | ns |
| S RESET N | tRST | 600 | | | ns |

Note 32. The AK7752 can be powered up when INIT_RESET_N pin = "L". The power supply must be ON and the master clock must be input before the INIT_RESET_N pin transitions "H".

3) Audio interface

(Ta=-40°C~85°C; AVDD, DVDD=3.0~3.6V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|--------|-----|-----|-----|-------|
| Slave Mode (CKM Mode 2-4) | | | | | |
| Delay Time from BITCLK_I "↑" to SYNC_I (Note 33) | tBLRD | 60 | | | Ns |
| Delay Time from SYNC_I to BITCLK_I "↑" (Note 33) | tLRBD | 60 | | | Ns |
| Delay Time from SYNC_I, O to Serial Data Output | tLRD | | | 80 | ns |
| Delay Time from BITCLK_I, O to Serial Data Output | tBSOD | | | 80 | ns |
| Serial Data Output Latch Setup Time | tBSIDS | 80 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 80 | | | ns |
| Master Mode (CKM Mode 0-1) | | | | | |
| BITCLK_O Frequency (BIT32FS bit = "0") | fBCLK | | 64 | | fs |
| BITCLK_O Frequency (BIT32FS bit = "1") | | | 32 | | fs |
| BITCLK_O Duty Factor | | | 50 | | % |
| Delay Time from BITCLK_O "↑" to SYNC_O (Note 34) | tBLRD | 60 | | | ns |
| Delay Time from SYNC_O to BITCLK_O "↑" (Note 34) | tLRBD | 60 | | | ns |
| Delay Time from SYNC_O to Serial Data Output | tLRD | | | 80 | ns |
| Delay Time from BITCLK_O to Serial Data Output | tBSOD | | | 80 | ns |
| Serial Data Output Latch Setup Time | tBSIDS | 80 | | | Ns |
| Serial Data Input Latch Hold Time | tBSIDH | 80 | | | ns |

Note 33. BITCLK_I "↑" must not occur at the same time as SYNC_I edge.

Note 34. BITCLK_O "↑" must not occur at the same time as SYNC_O edge.

(When control register SEL_BCK bit = "0". The edge reverses when SEL_BCK bit = "1".)

4) Microprocessor Interface

(Ta=-40°C~85°C; AVDD, DVDD=3.0~3.6V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|-----|-----|-----|-------|
| Microprocessor Interface Signal | | | | | |
| RQ_N Fall Time | tWRF | | | 30 | ns |
| RQ_N Rise Time | tWRR | | | 30 | ns |
| SCLK Fall Time | tSF | | | 30 | ns |
| SCLK Rise Time | tSR | | | 30 | ns |
| SCLK Frequency | fSCLK | | | 2.1 | MHz |
| SCLK Low Level Width | tSCLKL | 200 | | | ns |
| SCLK High Level Width | tSCLKH | 200 | | | ns |
| Microprocessor to AK7752 | | | | | |
| Time from S_RESET_N “↓” to RQ_N “↓” | tREW | 500 | | | ns |
| Time from RQ_N “↑” to S_RESET_N “↑” | tWRE | 500 | | | ns |
| RQ_N High Level Width | tWRQH | 500 | | | ns |
| Time from RQ_N “↓” to SCLK “↓” | tWSC | 500 | | | ns |
| Time from SCLK “↑” to RQ_N “↑” | tSCW | 800 | | | ns |
| SI Latch Setup Time | tSIS | 200 | | | ns |
| SI Latch Hold Time | tSIH | 200 | | | ns |
| Delay Time from SCLK “↓” to SO Output | tSOS | | | 200 | ns |
| Hold Time from SCLK “↑” to SO Output | tSOH | 200 | | | ns |
| Time from RQ_N “↓” to SO Hi-Z Release (Iout=±360μA) | tRQHR | | | 600 | ns |
| RQ_N “↑” to SO Hi-Z set (Iout=±360μA) | tRQHS | | | 600 | ns |

5) I²C BUS Interface

(Ta=-40°C~85°C; AVDD, DVDD=3.0~3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---------|-----|-----|-----|-------|
| I²C Timing | | | | | |
| SCL Clock Frequency | fSCL | | | 400 | KHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | | μs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | | | μs |
| Clock Low Time | tLOW | 1.3 | | | μs |
| Clock High Time | tHIGH | 0.6 | | | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | | μs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | | 0.9 | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | | μs |
| Rise Time of Both SDA and SCL Lines | tR | | | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | | μs |
| Pulse Width of Spike Noise Suppressed By Input Filter | tSP | 0 | | 50 | ns |
| Capacitive Load on Bus | Cb | | | 400 | pF |

 Note 35. I²C is a registered trademark of Philips Semiconductors.

6) EEPROM Interface

(Ta=-40°C ~ 85°C; AVDD, DVDD=3.0 ~ 3.6V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|-----|-----|-----|-------|
| EEPROM→AK7752 | | | | | |
| EESO Latch Setup Time (ESEL pin = "H") | tEESOS | 160 | | | ns |
| EESO Latch Hold Time (ESEL pin = "H") | tEESOH | 160 | | | ns |
| Time from ESEL "↑" to EECS_N, EECK, EESI Hi-Z release (Iout=±360μA) | tESLHR | | | 600 | ns |
| Time from ESEL "↓" to EECS_N, EECK, EESI Hi-Z set (Iout=±360μA) | tESLHS | | | 600 | ns |

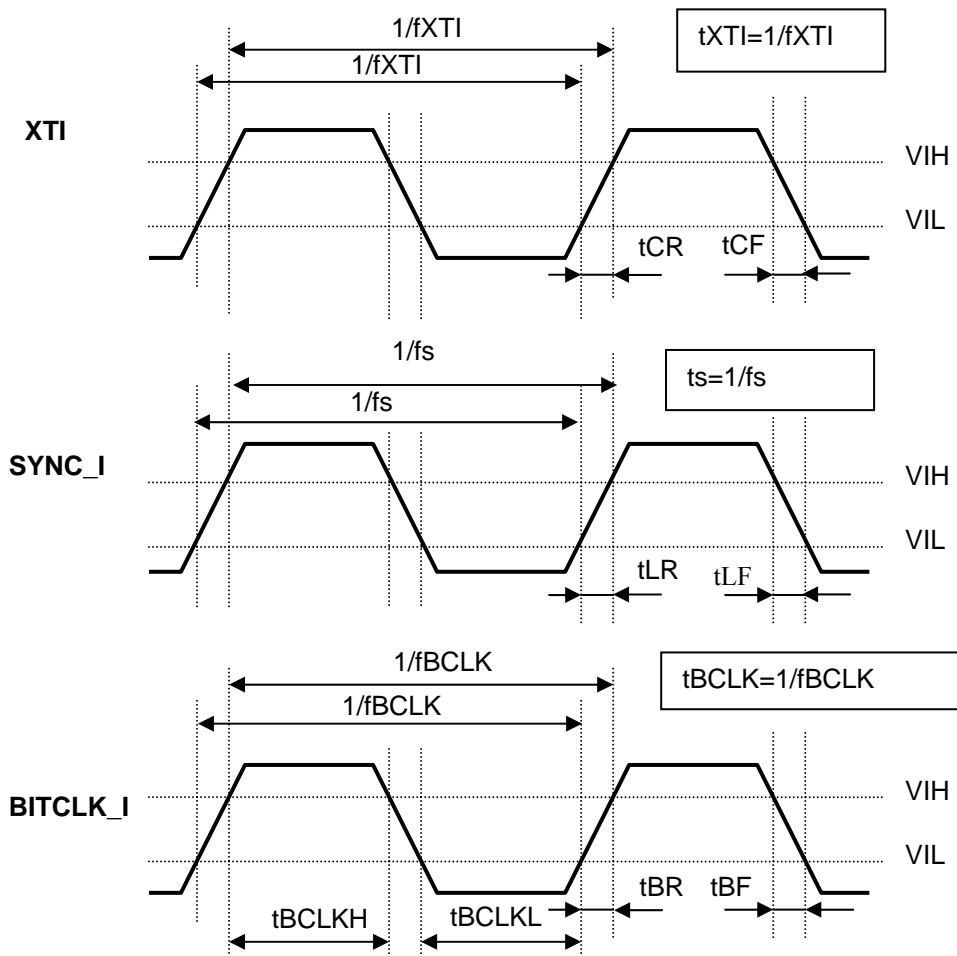
(6) Timing Diagram


Figure 2. System Clock

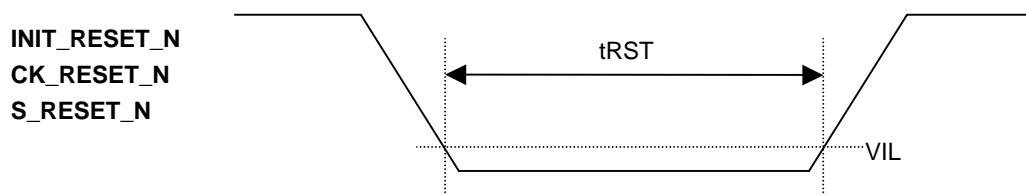


Figure 3. Reset

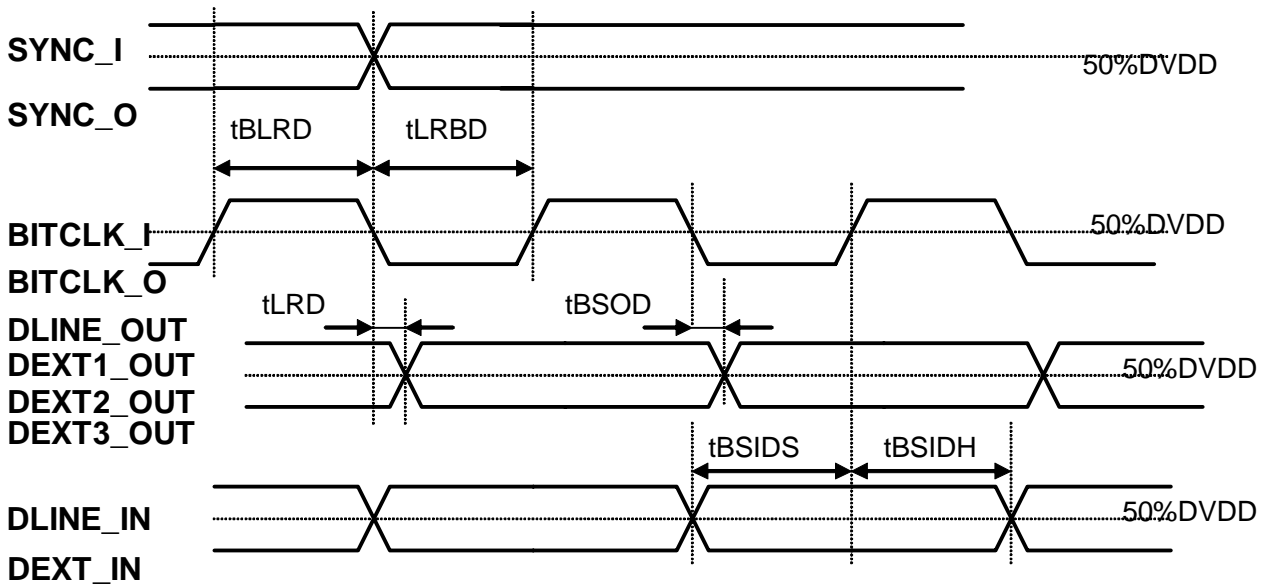


Figure 4. Audio Interface

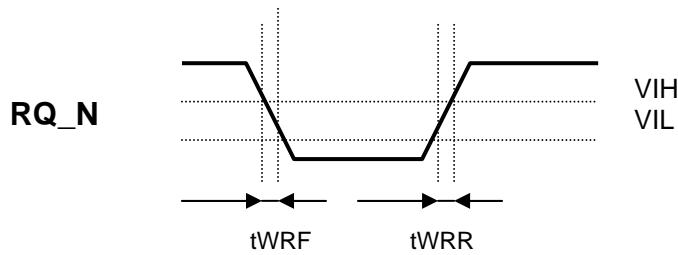


Figure 5. Microprocessor Interface Signal 1

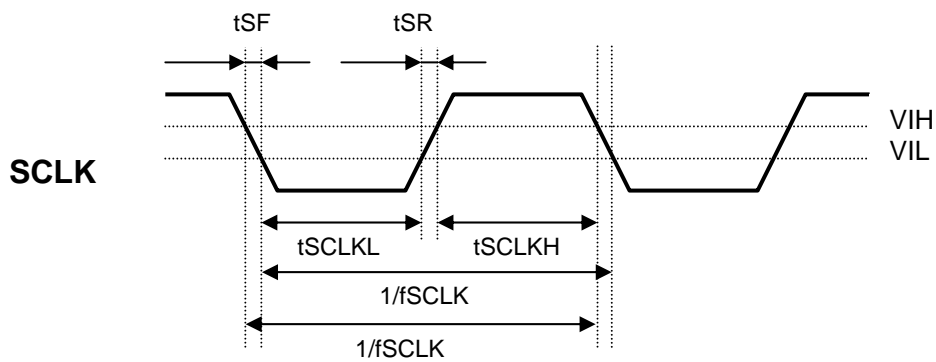


Figure 6. Microprocessor Interface Signal 2

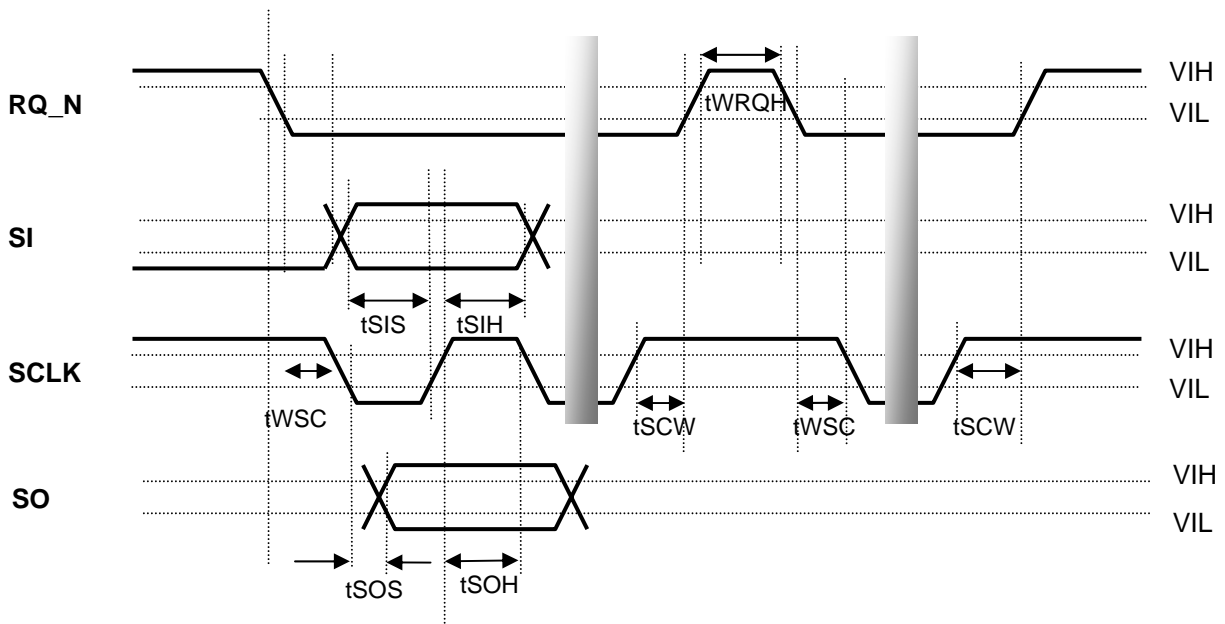


Figure 7. Microprocessor → AK7752

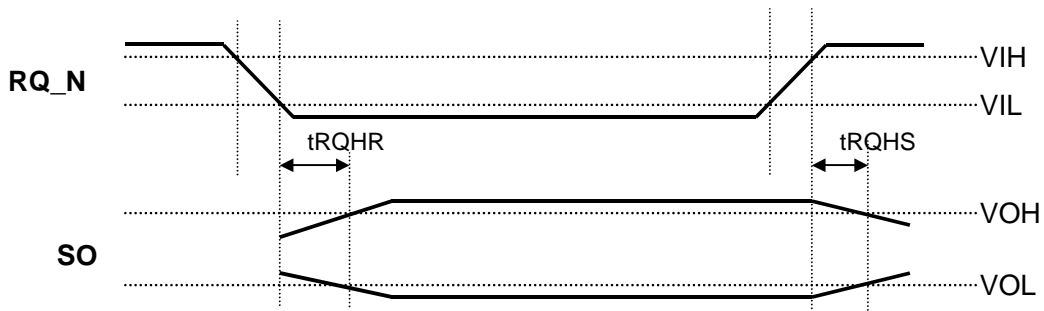


Figure 8. Microprocessor → AK7752

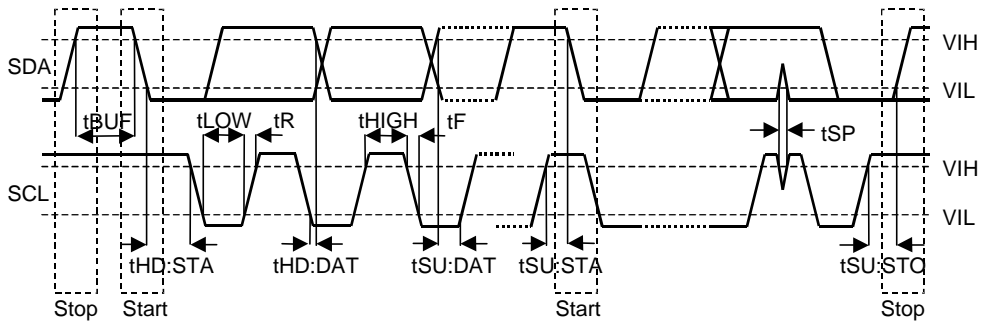


Figure 9. I²C Bus Interface

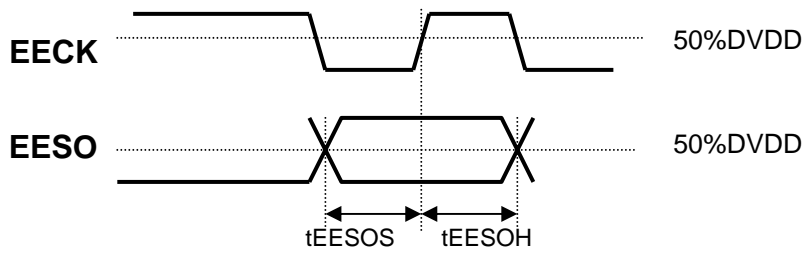


Figure 10. EEPROM Interface 1

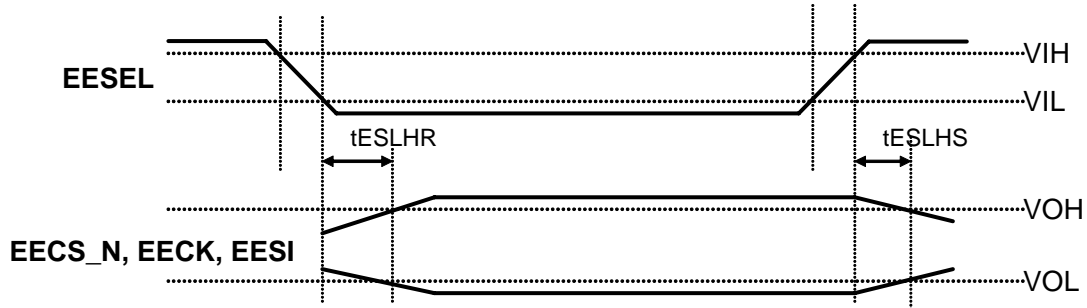
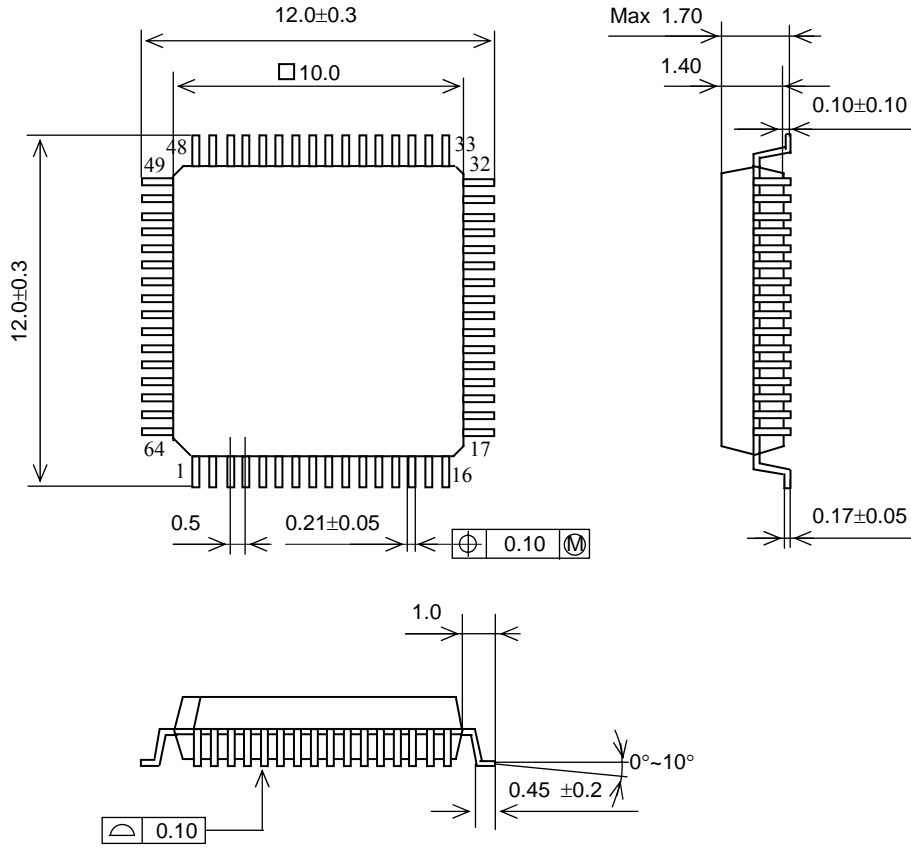


Figure 11. EEPROM Interface 2

PACKAGE

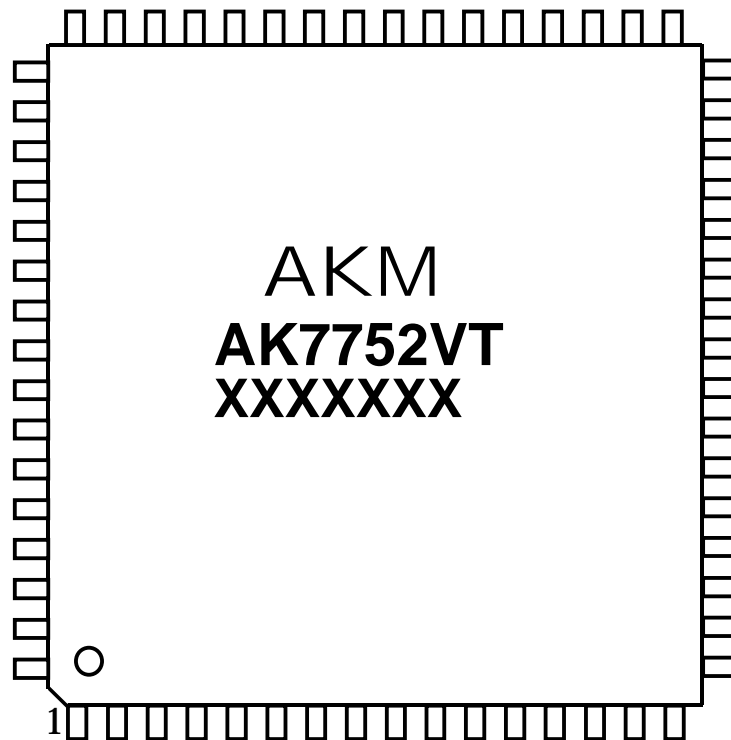
64pin LQFP (Unit: mm)



Material & Lead finish

| | |
|--------------|---------------------------|
| Package: | Epoxy |
| Lead-frame: | Copper |
| Lead-finish: | Soldering plate (Pb free) |

MARKING



- 1) Pin #1 indication
- 2) Date Code: XXXXXXXX (7 digits)
- 3) Marking Code: AK7752VT
- 4) Asahi Kasei Logo

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