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Product Brief

AK7759

DSP with Stereo CODEC

1. General Description

The AK7759 is a highly integrated digital signal processor, a stereo audio CODEC, a MIC gain amplifier, a line-out amplifier, digital audio I/F. The DSP has 3072step at fs = 48kHz parallel processing power. As the AK7759 is a RAM based DSP, it is programmable for user requirements such as high performance hands free function and acoustic effects. The AK7759 is available in a space saving small 36-pin QFN package.

2. Features

□ **DSP:**
- **Word Length: 28-bit (Floating Point)**
- **Instruction Cycle: Maximum 6.8ns (3072fs, fs=48kHz)**
- **Program RAM (PRAM): 5120 x 36-bit**
- **Coefficient RAM (CRAM): 4096 x 24-bit**
- **Offset Register (OFREG): 32 × 15-bit**
- **JX pins (Conditional Branch Control)**

□ **Digital Interface:**
- **Digital Signal Input Port (4ch) MSB justified 24-bit / LSB justified 24, 20, 16-bit and I^2S**
- **Digital Signal Input Port (6ch) MSB justified 24-bit / LSB justified 24, 20, 16-bit and I^2S**
- **Short / Long Frame**
- **TDM 256fs (8ch) Format**

□ **Analog Input:**
- **Full Differential / Single-ended, Pseudo Differential Inputs**
- **Channel Independent Microphone Analog Gain Amplifier (-6~27dB, 3dB Step)**

□ **Stereo 24-bit ADC:**
- **Sampling Frequency: fs = 8kHz ~ 48kHz**
- **ADC Characteristics S/(N+D): 80dB; DR, S/N: 90dB**
- **Channel Independent Digital Volume (24dB ~ -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **Digital LPF: Voice Filter / Sharp Roll-Off Filter**

□ **Stereo 24-bit DAC:**
- **Sampling Frequency: fs = 8kHz ~ 48kHz**
- **Digital Volume (12dB ~ -115dB, 0.5dB Step, Mute)**
- **Digital LPF: Sharp Roll-Off Filter**

□ **Line Output:**
- **Full Differential Output**
- **S/(N+D): 80dB; DR, S/N: 90dB**

□ **2ch Digital Microphone (DMIC) Interface:**
- **Digital LPF: Voice Filter / Sharp Roll-Off Filter**

□ **2 types Analog Direct Path:**
- **Full Differential / Single-ended Input/Output**

□ **Digital Mixer**

□ **PLL Circuit**

□ **DIT:**
- **S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Consumer Mode**
- **24bit 2ch Output**

□ µP Interface: SPI, I²CBUS(400kHz Fast-Mode, 1MHz Fast-Mode-Plus)
□ I²C bootloader
- EEPROM Mat Selectable
□ Power Supply:

Analog	AVDD: 3.0V ~ 3.6V (Typ. 3.3V)
Digital	LVDD: 3.0V ~ 3.6V (Typ. 3.3V)
I/F	TVDD: 1.7V ~ 3.6V (Typ. 3.3V)

□ Operationg Temperature Range: -40 ~ 105°C
□ Storage Temperature: -65 ~ 150°C
□ Package: 36-pin QFN (0.5mm pitch)

3. Table of Contents

4. Block Diagram

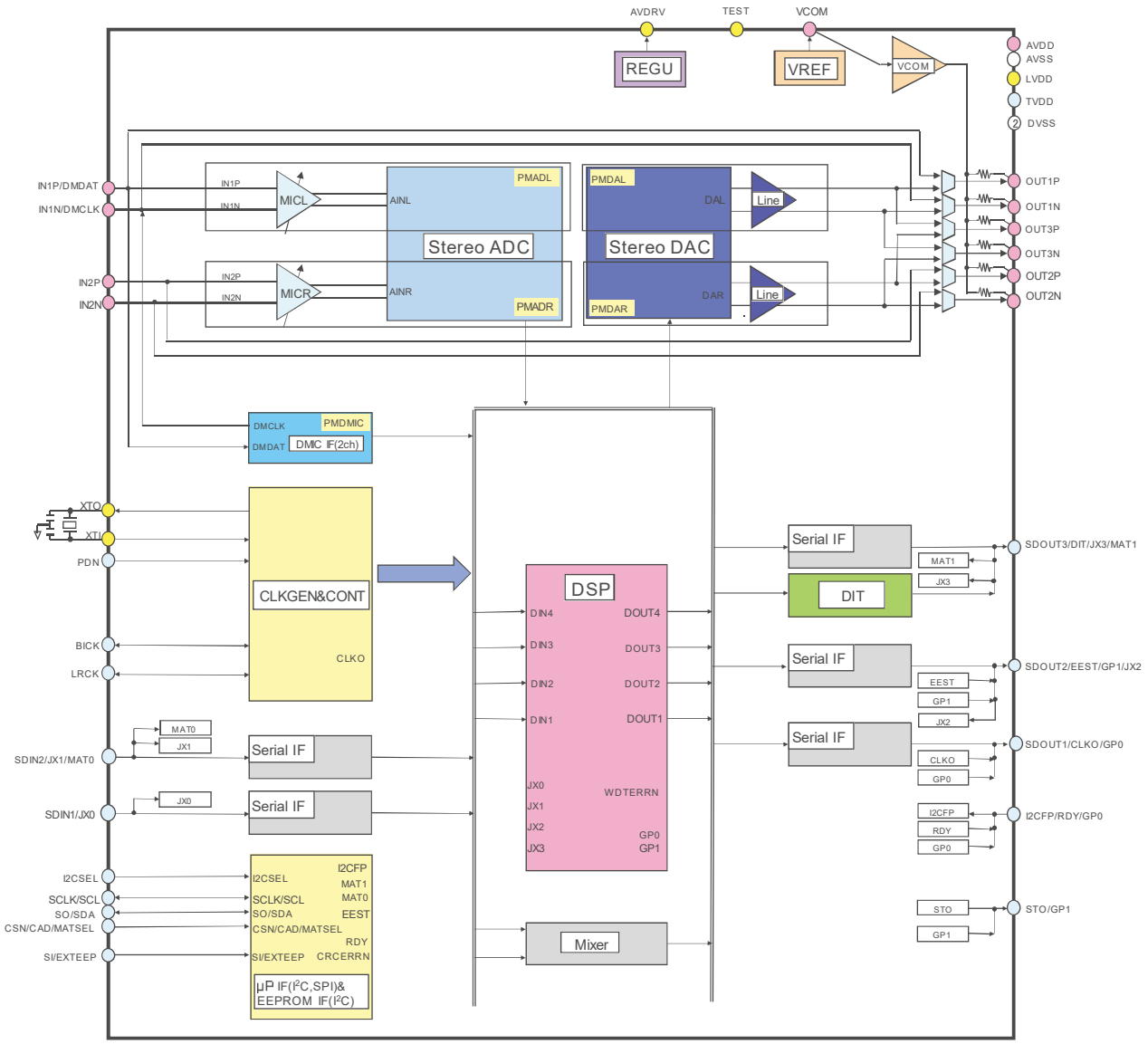


Figure 1. Whole Block Diagram

5. Pin Configurations and Functions

5.1. Pin Configurations

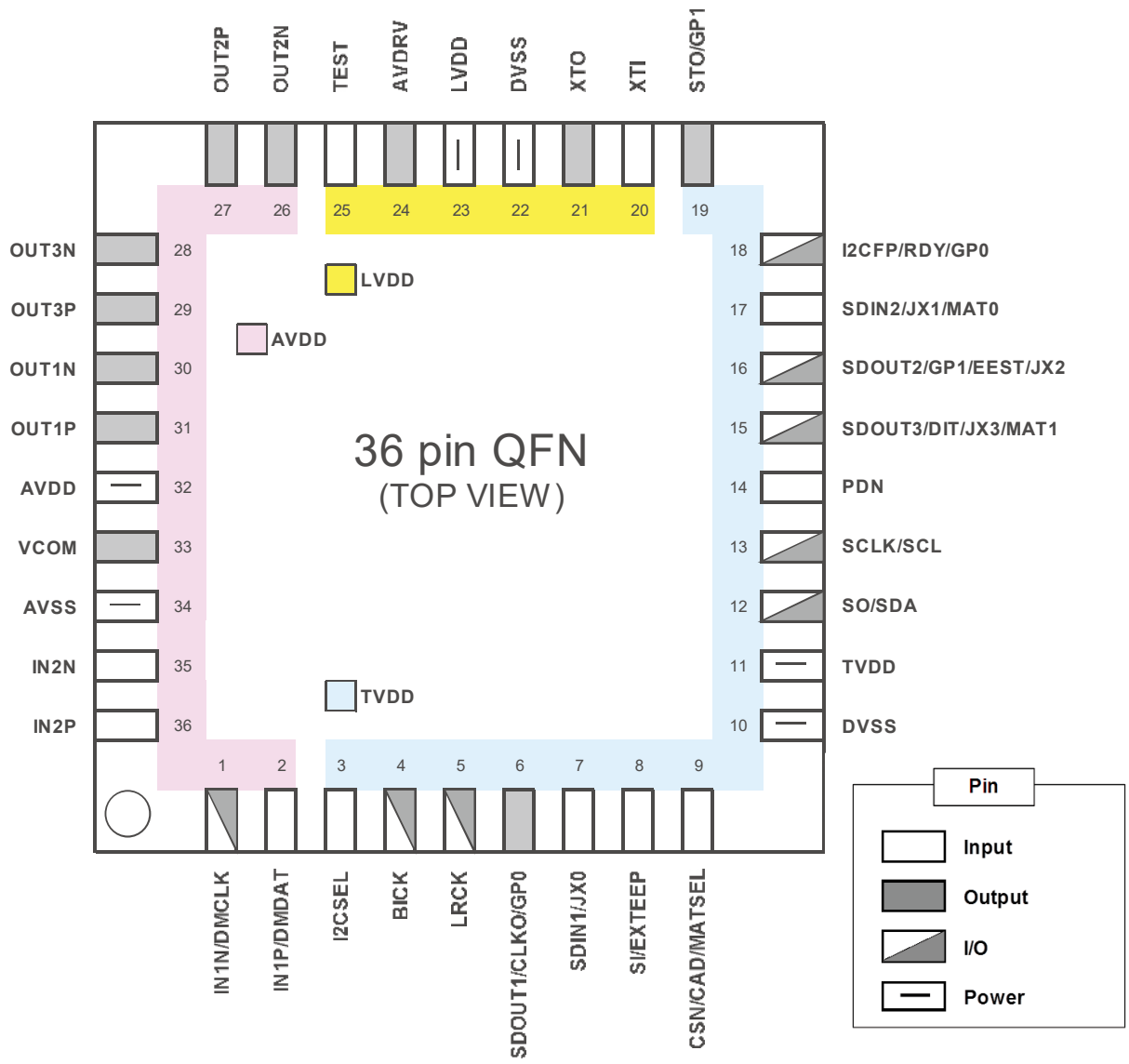


Figure 2. Pin Configurations

5.2. Pin Function

No.	Pin Name	I/O	Function	Power
1	IN1N	I	ADC Lch Differential Input N Pin (AINEL bit = "1" & ADDIFFLN bit = "0") ADC Lch Ground Input Pin (AINEL bit = "1" & ADDIFFLN bit = "1") Connect a 10μF ceramic capacitor between this pin and AVSS in single-ended input mode. Connect this pin to the ground via a 10μF ceramic capacitor in pseudo differential input mode. Do not connect a resistor more than 200Ω to the external capacitor in serial.	AVDD
	DMCLK	O	Digital Microphone Clock Output Pin (PMDMIC bit = "1" & PMADR bit = "1" & AINEL bit = "0")	
2	IN1P	I	ADC Lch Differential Input P Pin (AINEL bit = "1" & ADDIFFLN bit = "0") ADC Lch Single-ended / Pseudo Differential Input Pin (AINEL bit = "1" & ADDIFFLN bit = "1")	AVDD
	DMDAT	I	Digital Microphone Data Input Pin (PMDMIC bit = "1" & PMADR bit = "1" & AINEL bit = "0")	
3	I2CSEL	I	I2CBUS Selection Pin I2CSEL pin = "L": SPI Interface I2CSEL pin = "H": I²CBUS Interface I2CSEL should be fixed to "L (DVSS)" or "H (TVDD)".	TVDD
4	BICK	I/O	Serial Bit Clock Pin (Internal pull-down)	TVDD
5	LRCK	I/O	LR Channel Selection Pin (Internal pull-down)	TVDD
6	SDOUT1	O	Serial Data 1 Output Pin (SDOUT1E bit = "1" & SDOUT1SEL[1:0] bits = "00")	TVDD
	CLKO	O	Master Clock Output Pin (SDOUT1E bit = "1" & SDOUT1SEL[1:0] bits = "01")	
	GP0	O	General Purpose Output 0 Pin (SDOUT1E bit = "1" & SDOUT1SEL[1:0] bits = "10")	
7	SDIN1	I	Serial Data 1 Input Pin (SDIN1SEL bit = "0")	TVDD
	JX0	I	External Conditional Jump 0 Pin (SDIN1SEL bit = "1" & JX0E bit = "1")	
8	SI	I	Serial Data Input Pin for SPI Interface (I2CSEL pin = "L") Set this pin to "L" when not using the SPI Interface.	TVDD
	EXTEEP	I	EEPROM Download Control Pin (I2CSEL pin = "H")	
9	CSN	I	Chip Select N Pin for SPI Interface (I2CSEL pin = "L") Set this pin to "H" when the AK7759 is in power-down mode or when the microprocessor I/F is not used.	TVDD
	CAD	I	I²CBUS Address Pin (I2CSEL pin = "H")	
	MATSEL	I	EEPROM Download Mat Selection Pin (I2CSEL pin = EXTEEP pin = "H")	
10	DVSS	-	Digital Ground Pin 0V	-
11	TVDD	-	Digital IO Power Supply Pin 1.7~3.6V (Typ.3.3V)	-
12	SO	O	SO pin (I2CSEL pin = "L")	TVDD
	SDA	I/O	SDA pin I²CBUS Interface (I2CSEL pin = "H")	
13	SCLK	I	Serial Data Clock Pin for SPI Interface (I2CSEL pin = "L") The SCLK pin must be set to "H" when not inputting clock.	TVDD
	SCL	I/O	SCL pin I²CBUS Interface (I2CSEL pin = "H") This pin becomes an output pin when downloading EEPROM data (EXTEEP pin = "H").	
14	PDN	I	Power-down N Pin The AK7759 can be powered down by the PDN pin. Set this pin to "L" upon power-up the AK7759.	TVDD

No.	Pin Name	I/O	Function	Power
15	SDOUT3	O	Serial Data 3 Output Pin (SDOUT3E bit = "1" & SDOUT3SEL[1:0] bits = "00")	TVDD
	DIT	O	DIT Output Pin (SDOUT3E bit = "1" & SDOUT3SEL[1:0] bits = "01")	
	JX3	I	External Conditional Jump3 Pin (Internal pull-down) (SDOUT3E bit = "0" & JX3E bit = "1")	
	MAT1	I	Address 1 Pin for EEPROM Download Mat Selection (Internal pull-down) (I2CSEL pin = EXTEEP pin = MATSEL pin = "H")	
16	SDOUT2	O	Serial Data 2 Output Pin (SDOUT2E bit = "1" & SDOUT2SEL[1:0] bits = "00")	TVDD
	GP1	O	General Purpose Output 1 Pin (SDOUT2E bit = "1" & SDOUT2SEL[1:0] bits = "01")	
	EEST	O	EEPROM Interface Status Pin (when downloading EEPROM data) (SDOUT2E bit = "1" & SDOUT2SEL[1:0] bits = "10")	
	JX2	I	External Conditional Jump2 Pin (Internal pull-down) (SDOUT2E bit = "0" & JX2E bit = "1")	
17	SDIN2	I	Serial Data 2 Input Pin (Internal pull-down) (SDIN2SEL bit = "0")	TVDD
	JX1	I	External Conditional Jump 1 Pin (Internal pull-down) (SDIN2SEL bit = "1" & JX1E bit = "1")	
	MAT0	I	Address 0 Pin for EEPROM Download Mat Selection (Internal pull-down) (I2CSEL pin = EXTEEP pin = MATSEL pin = "H")	
18	I2CFP	I	I^2C High Speed Mode Plus Selection Pin (Internal pull-down) (I2CFP pin = "H" & RDYE bit = "0")	TVDD
	RDY	O	RDY Pin (RDYE bit = "1" & RDYSEL[1:0] bits = "00")	
	GP0	O	General Purpose Output 1 Pin (RDYE bit = "1" & RDYSEL[1:0] bits = "01")	
19	STO	O	Status Output Pin	TVDD
	GP1	O	General Purpose Output0 Pin	
20	XTI	I	Oscillation Circuit Input Pin When a crystal oscillator is used, connect it between XTI and XTO. When a crystal oscillator is not used, connect an external clock to this pin or leave it as open.	LVDD
21	XTO	O	Oscillation Circuit Output Pin When a crystal oscillator is used, connect it between XTI and XTO. When a crystal oscillator is not used, leave this pin as open.	LVDD
22	DVSS	-	Digital Ground Pin 0V	-
23	LVDD	-	Digital Core Power Supply Pin 3.0~3.6V (Typ.3.3V)	-
24	AVDRV	O	LDO Output Pin Connect a 2.2µF capacitor between this pin and DVSS. This pin must not be connected to an external circuit.	LVDD
25	TEST	I	TEST Input Pin (Internal Pull-down) This pin must be connected to DVSS.	LVDD
26	OUT2N	O	Differential Line Output2 N Pin	AVDD
27	OUT2P	O	Differential Line Output2 P Pin	AVDD
28	OUT3N	O	Differential Line Output3 N Pin	AVDD
29	OUT3P	O	Differential Line Output3 P Pin	AVDD
30	OUT1N	O	Differential Line Output1 N Pin	AVDD
31	OUT1P	O	Line Differential Output1 P Pin	AVDD
32	AVDD	-	Analog Power Pin 3.0~3.6V (Typ.3.3V)	-
33	VCOM	O	Analog Common Voltage Output Pin Connect a 2.2µF ceramic capacitor between this pin and AVSS. A low ESR ceramic capacitor is recommended. This pin must not be connected to an external circuit.	AVDD
34	AVSS	-	Analog Ground Pin 0V	-

No.	Pin Name	I/O	Function	Power
35	IN2N	I	ADC Rch Differential Input N Pin (AINER bit = "1" & ADDIFFRN bit = "1") ADC Rch Ground Input Pin (AINER bit = "1" & ADDIFFRN bit = "0") Connect a 10μF ceramic capacitor between this pin and AVSS in single-ended input mode. Connect this pin to the ground via a 10μF ceramic capacitor in pseudo differential input mode. Do not connect a resistor more than 200Ω to the external capacitor in serial.	AVDD
36	IN2P	I	ADC Rch Differential Input P Pin (AINER bit = "1" & ADDIFFRN bit = "1") ADC Rch Input Pin (AINER bit = "1" & ADDIFFRN bit = "0")	AVDD

Notes:
*1. The exposed pad on the bottom surface of the package must be open or connected to the ground.
*2. All digital input pins must not be allowed to float. If analog input are not used, leave them open.
*3. The description of "Internal Pull-down" above indicates the pin status just after power-down is released. (PDN pin = "H")
*4. GP0 pins (No. 6 and 18) and GP1 pins (No. 16 and 19) are exclusive.

5.3. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Table 1. Handling of Unused Pin

Classification	Pin Name	Setting
Analog	IN1N/DMCLK, IN1P/DMDAT, OUT2N, OUT2P, OUT3N, OUT3P, OUT1N, OUT1P, IN2N, IN2P,	Open
Digital	BICK, LRCK, SDOUT1/CLKO/GP0, SDOUT3/MAT1/JX3, SDOUT2/GP1/EEST/JX2, I2CFP/RDY/GP0, STO/GP1, XTI, XTO	Open
	SDIN1/JX0, SDIN2/JX1/MAT0, TEST	Connect to DVSS

Note:
*5. Although it is recommended to connect the LRCK and the BICK pins to DVSS when these pins are not used, there is no problem if they are left open.

5.4. Power-down and Power-down Release Pin Statuses

Table 2. Power-down and Power-down Release Pin Statuses

No.	Pin Name	I/O	PDN pin = "L"	PDN pin = "H" (default)
			Status	Status
1	IN1N	I	"Hi-Z"	"Hi-Z"
	DMCLK	O	"Hi-Z"	"Hi-Z"
2	IN1P	I	"Hi-Z"	"Hi-Z"
	DMDAT	I	"Hi-Z"	"Hi-Z"
3	I2CSEL	I	Input	Input
4	BICK	I/O	Pull Down (50kΩ)	Pull Down (46kΩ)
5	LRCK	I/O	Pull Down (50kΩ)	Pull Down (46kΩ)
6	SDOUT1	O	Pull Down (50kΩ)	"L"
	CLKO	O		
	GP0	O		
7	SDIN1	I	Pull Down (50kΩ)	Input
	JX0	I		
8	SI	I	Input	Input (I2CSEL pin = "L")
	EXTEEP	I		Input (I2CSEL pin = "H")
9	CSN	I	Input	Input (I2CSEL pin = "L")
	CAD	I		Input (I2CSEL pin = "H", EXTEEP pin = "L")
	MATSEL	I		Input (I2CSEL pin = "H", EXTEEP pin = "H")
12	SO	O	"Hi-Z"	"Hi-Z" (CSN= "H", I2CSEL pin = "L")
	SDA	I/O	"Hi-Z"	"Hi-Z"(I2CSEL pin = "H")

No.	Pin Name	I/O	PDN pin = "L"	PDN pin = "H"(@default)
			Status	Status
13	SCLK	I	"Hi-Z"	Input (I2CSEL pin = "L")
	SCL	I	"Hi-Z"	Input (I2CSEL pin = "H", EXTEEP pin = "L")
		O	"Hi-Z"	Output (I2CSEL pin= "H", EXTEEP pin = "H")
14	PDN	I	Input	Input
15	SDOUT3	O	Pull Down(50kΩ)	
	DIT	O		
	JX3	I		Pull Down(46kΩ)
	MAT1	I		Pull Down(46kΩ) (I2CSEL pin = "H", EXTEEP pin = "H")
16	SDOUT2	O	Pull Down(50kΩ)	
	GP1	O		
	EEST	O		
	JX2	I		Pull Down(46kΩ)
17	SDIN2	I	Pull Down(50kΩ)	Input
	JX1	I		
	MAT0	I		Input (I2CSEL pin = "H", EXTEEP pin = "H")
18	I2CFP	I	Pull Down(50kΩ)	Pull Down(46kΩ)
	RDY	O		
	GP0	O		
19	STO	O	Pull Down(50kΩ)	"H"
	GP1	O		
20	XTI	I	Feedback(193k)	Feedback(193k)
21	XTO	O	"H"	Inverted XTI Input
24	AVDRV	O	Pull Down(70Ω)	Output (Typ.1.2V)
25	TEST	I	Pull Down(25kΩ)	Pull Down(25kΩ)
26	OUT2N	O	"Hi-Z"	Output (AVDD/2)
27	OUT2P	O	"Hi-Z"	Output (AVDD/2)
28	OUT3N	O	"Hi-Z"	Output (AVDD/2)
29	OUT3P	O	"Hi-Z"	Output (AVDD/2)
30	OUT1N	O	"Hi-Z"	Output (AVDD/2)
31	OUT1P	O	"Hi-Z"	Output (AVDD/2)
33	VCOM	O	Pull Down(500Ω)	Output (AVDD/2)
35	IN2N	I	"Hi-Z"	"Hi-Z"
36	IN2P	I	"Hi-Z"	"Hi-Z"

6. Absolute Maximum Ratings

(AVSS=DVSS=0V:*6)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core:LVDD)	LVDD	-0.3	4.3	V
Digital2(I/F:TVDD)	TVDD	-0.3	4.3	V
Input Circuit (Except Power Supply Pin)	IIN	—	±10	mA
Analog Input Voltage (*7)	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage (*8)	VIND1	-0.3	(LVDD+0.3) or 4.3	V
Digital Input Voltage (*9)	VIND2	-0.3	(TVDD+0.3) or 4.3	V
Operating Temperature	Ta	-40	105	°C
Storage Temperature	Tstg	-65	150	°C

Notes:

*6. All voltages are with respect to ground. AVSS and DVSS must be connected to the same ground.

*7. The maximum analog input voltage is lower value between (AVDD + 0.3V) or 4.3V.

*8. The maximum digital input voltage of the XTI and TEST pins is lower value between (LVDD + 0.3V) or 4.3V.

*9. The maximum digital input voltage of the I2CSEL, BICK, LRCK, SDIN1/JX0, SI/EXTEEP, CSN/CAD/MATSEL, SDA, SCLK/SCL, JX3/MAT1, JX2, SDIN2/JX1/MAT0, and I2CFP pins is lower value between (TVDD + 0.3V) and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=0V:*6, PDN pin = "H")

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core:LVDD)	LVDD	3.0	3.3	3.6	V
Digital2(I/F:TVDD)	TVDD	1.7	3.3	3.6	V
Difference1	AVDD-LVDD	-0.1	0	0.1	V
Difference2	LVDD-TVDD	-0.1	-	-	V

Notes:

*10. The power-up sequence with AVDD, LVDD, and TVDD is not critical. The PDN pin should be held "L" when power is supplied. The PDN pin should be held "L" when power is supplied. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

*11. When using the I^2C interface (I2CSEL pin = "H"), do not turn off the power supply of the AK7759 with the power supply of the surrounding device turned on. Pull-up of SDA and SCL pins must not exceed TVDD2.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

8.1. Analog Characteristics

8.1.1. MIC Amp Gain

(Ta= 25°C; AVDD=LVDD=TVDD=3.3V; AVSS=DVSS=0V)

	Parameter		Min.	Typ.	Max.	Unit
MIC Amp Gain	MGNL[3:0]	MGNR[3:0]				
	0H	0H	-7.5	-6	-4.5	dB
	1H	1H	-4.5	-3	-1.5	dB
	2H(default)	2H(default)	-1.5	0	1.5	dB
	3H	3H	1.5	3	4.5	dB
	4H	4H	4.5	6	7.5	dB
	5H	5H	7.5	9	10.5	dB
	6H	6H	10.5	12	13.5	dB
	7H	7H	13.5	15	16.5	dB
	8H	8H	16.5	18	19.5	dB
	9H	9H	19.5	21	22.5	dB
	AH	AH	22.5	24	25.5	dB
	BH	BH	25.5	27	28.5	dB
	CH	CH				
	DH	DH				
	EH	EH				
	FH	FH				

Note:

*12. The AK7759 can accept analog inputs up to 3.0 Vp-p. The MIC amplifier gain should be set so as not to exceed the input full-scale voltage of the ADC and the analog signal must be input via a DC cut capacitor. The device may be damaged if an analog signal is input without cutting the DC component.

8.1.2. MIC Amp + ADC

(Ta= 25°C; AVDD=LVDD=TVDD=3.3V; AVSS=DVSS=0V; Signal Frequency 1kHz;
Sampling Rate fs=48kHz; Measurement Frequency = 20Hz ~ 20kHz, MGNL/R[3:0] bits = 2H (0dB))

	Parameter		Min.	Typ.	Max.	Unit
MIC Amp	Input Impedance					
	IN1P/IN1N, IN2P/IN2N	Full Differential Input (*13)	14	20		kΩ
	IN1P, IN2P	Pseudo Differential Input (*14)	16	24		kΩ
	IN1N, IN2N	Pseudo Differential Input (*14)	900	1300		kΩ
MIC Amp + ADC	Resolution				24	bit
	Dynamic Characteristics (Full Differential Input) (*13)					
	S/(N+D) (*15)	fs=48kHz	72	80		dB
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	82	90		dB
	S/N	fs=48kHz (A-weighted)	82	90		dB
	CMRR (*16)		60	80		dB
	Dynamic Characteristics (Single-ended Input, Pseudo Differential Input) (*14)					
	S/(N+D) (*15)	fs=48kHz	72	80		dB
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	82	90		dB
	S/N	fs=48kHz (A-weighted)	82	90		dB
	CMRR (Pseudo Differential Input) (*17)		55	75		dB
	Channel Isolation (*18)		90	105		dB
	DC Accuracy					
	Channel Gain Mismatch			0.0	0.3	dB
	Analog Input (Full Differential Input) (*13)					
	Input Full Scale Voltage (*19)	SDAD bit = "0"	±2.07	±2.28	±2.48	Vp-p
		SDAD bit = "1"	±2.0	±2.2	±2.4	Vp-p
	Analog Input (Single-ended, Pseudo Differential Input) (*14)					
	Input Full Scale Voltage (*19)	SDAD bit = "0"	2.07	2.28	2.48	Vp-p
		SDAD bit = "1"	2.0	2.2	2.4	Vp-p

Notes:
*13. ADDIFLN bit = ADDIFRN bit = "0"
*14. ADDIFLN bit = ADDIFRN bit = "1"
*15. -1.3 dBFS when SDAD bit = "0". -1 dBFS when SDAD bit = "1".
*16. It is a common mode rejection ratio when synchronized 1kHz, 100mVp-p signal is input to the IN1P/IN1N and IN2P/IN2N pins. The value with ± 100mVp-p signal is referenced.
*17. It is a common mode rejection ratio when synchronized 1kHz, 100mVp-p signal is input to the IN1P/IN1N and IN2P/IN2N pins. The value with 100mVp-p signal is referenced.
*18. Indicates inter-channel isolation between Lch and Rch when -1dBFS signal is input.
*19. Full scale input voltage is proportional to AVDD (AVDD x 0.67).
*20. S/(N+D) performance of the ADC degrades when ADC and DAC are operated simultaneously with a frequency other than 48kHz or 16kHz while DSMN bit = "0"(default). It can be prevented by setting DSMN bit = "1". S/(N+D) performance of the ADC will not degrade if ADC and DAC are not operated simultaneously.

8.1.3. DAC+Line-out Amp

(Ta= 25°C; AVDD=LVDD=TVDD=3.3V; AVSS=DVSS=0V; Signal Frequency 1kHz;
Sampling Rate fs=48kHz; Measurement Frequency = 20Hz~20kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC + Line-out Amp	Resolution				24	bit
	Differential Output (*21)					
	Output Voltage (*22)		±2.55	±2.83	±3.11	Vp-p
	S/(N+D) (0dBFS)	fs=48kHz	72	80		dB
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	82	90		dB
	S/N	fs=48kHz (A-weighted)	82	90		dB
	Inter-channel Isolation1 (*23) OUTxSEL[1:0] bit ≠ "00"(x=1,2,3)		90	110		dB
	Channel Gain Mismatch (*24)			0.0	0.5	dB
	Load Resistance (*25)		10			kΩ
	Load Capacitance				30	pF

Notes:
*21. When OUT1SEL[1:0] bits = "10" or OUT3SEL[1:0] bits = "01" and OUT2SEL[1:0] bits = "10" or OUT3SEL[1:0] bits = "10", object output pins are the OUT1P/OUT1N, OUT2P/OUT2N and OUT3P/OUT3N pins.
*22. Full scale output voltage. The output voltage is proportional to AVDD (AVDD x 0.86).
*23. Indicates DAC inter-channel isolation between Lch and Rch when 0dBFS signal is output from the DAC.
*24. Indicates DAC inter-channel gain mismatch between Lch and Rch when 0dBFS signal is output from the DAC.
*25. AC load.

8.1.4. Analog Direct Path

(Ta= 25°C; AVDD=LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=DVSS=0V; Signal Frequency 1kHz;
Measurement Frequency = 20Hz~20kHz)

	Parameter	Min.	Typ.	Max.	Unit
Analog Direct Path (*26)	Input Pin to Output Pin				
	Impedance between Pins			300	Ω
	Allowable Signal Impedance (*27)			3.0	Vp-p
	Load Resistance (*25)	10			kΩ
	Inter-channel Isolation (*28)	85	95		dB

Notes:
*26. OUT1SEL[1:0] bits = "01", OUT2SEL[1:0] bits = "01"
*27. AC input/output signal amplitude via an AC coupling capacitor.
*28. Channel isolation of Analog Direct Paths (IN1P-OUT1P, IN1N-OUT1N, IN2P–OUT2P, IN2N-OUT2N).

8.2. DC Characteristics

(Ta= -40~105°C, AVDD= LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage		VIH	75%LVDD 75%TVDD			V
Low Level Input Voltage		VIL			25%LVDD 25%TVDD	V
SCL, SDA High Level Input Voltage		VIH2	70%TVDD			V
SCL, SDA Low Level Input Voltage		VIL2			30%TVDD	V
DMDAT High Level Input Voltage (*29)		VIH3	65%AVDD			V
DMDAT Low Level Input Voltage (*29)		VIL3			35%AVDD	V
High Level Output Iout= -100μA (*30)		VOH	TVDD-0.3			V
Low Level Output Iout=100μA (*31)		VOL			0.3	V
SCL, SDA Low Level Output Voltage	Fast Mode					
	TVDD ≥ 2.0V (Iout = 3mA)	VOL2			0.4	V
	TVDD < 2.0V (Iout = 3mA)	VOL2			20%TVDD	V
	Fast Mode Plus					
	TVDD ≥ 2.0V (Iout = 20mA)	VOL2			0.4	V
	TVDD < 2.0V (Iout = 3mA)	VOL2			20%TVDD	V
DMCLK High Level Output Voltage Iout = -80μA (*29)		VOH3	AVDD-0.4			V
DMCLK Low Level Output Voltage Iout = 80μA (*29)		VOL3			0.4	V
Input Leak Current (*32)		Iin			±10	μA
Input Leak Current at Pulled-down Pins Power-down (PDN pin = "L") (*33)		Iid		66		μA
Input Leak Current at Pulled-down Pins Power-down Release (PDN pin = "H") (*34)		Iid		77		μA
Input Leak Current at the XTI pin		Iix		17		μA

Notes:
*29. PMDMIC bit = "1" & PMADR bit = "1" & AINEL bit = "0"
*30. Except XTO pin
*31. Except SDA and XTO pins.
*32. Internal Pulled-down pins, except the XTI pin
*33. BICK, LRCK, SDOUT1/CLKO/GP0, SDOUT3/DIT/JX3/MAT1, SDOUT2/GP1/EEST/JX2, SDIN2/JX1/MAT0, I2CFP/RDY/GP0, STO/GP1 pin (Typ. 50 kΩ@3.3V)
*34. BICK, LRCK, SDOUT3/DIT/JX3/MAT1, SDOUT2/GP1/EEST/JX2, SDIN2/JX1/MAT0, I2CFP/RDY/GP0 pin (Typ. 46kΩ@3.3V)

8.3. Power Consumptions

(Ta=25°C; AVDD=LVDD=3.0~3.6V (Typ =3.3V, Max.=3.6V); TVDD=1.7~3.6V (Typ.=3.3V, Max.=3.6V); AVSS=DVSS=0V; fs=48kHz; Master Mode; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power consumptions in operation (*35)	AVDD		16.0	22.4	mA
	LVDD		24.0	52.0	mA
	TVDD		3.6	6.6	mA
Power consumptions in power-down (PDN pin = "L")	AVDD		1.5		μA
	LVDD		1.5		μA
	TVDD		1.0		μA

Note
*35. LVDD power consumption will be changed depending on DSP programs.

8.4. Digital Filter Characteristics

8.4.1. ADC

8.4.1.1. Voice Filter (SDAD bit = "0", SDDMIC bit = "0")

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, fs=16kHz (*36))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Voice Filter						
Passband (*37)	0dB ~ -0.47dB	PB	0		6.3	kHz
	-3.0dB	PB		6.9		kHz
Passband Ripple (*37)		PR	-0.47		0	dB
Stopband (*38)		SB	8			kHz
Stopband Attenuation (*38, *39)		SA	59.5			dB
Group Delay Distortion: 0Hz ~ 8kHz		△GD		0		μs
Group Delay		GD		14.1		1/fs
ADC Digital Filter (HPF)						
Frequency Response	-3.0dB	FR		29.8		Hz

Notes:
*36. The passband and stopband frequencies scale with "fs" (system sampling rate). The characteristic of the high pass filter is not included.
*37. The passband is from DC to 6.3kHz when fs=16kHz.
*38. The stopband is 8kHz to 1.016MHz when fs=16kHz.
*39. When fs = 16kHz, the analog modulator samples the input signal at 1.024MHz. There is no attenuation of an input signal in band (n x 1.024MHz ±6.3kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

8.4.1.2. Sharp Roll Off Filter (SDAD bit = "1", SDDMIC bit = "1")

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, fs=16kHz (*40))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Sharp Roll Off Filter						
Passband (*41)	0.14dB ~ -0.12dB	PB	0		6.9	kHz
	-3.0dB	PB		7.6		kHz
Passband Ripple (*41)		PR	-0.14		0.14	dB
Stopband (*42)		SB	9.5			kHz
Stopband Attenuation (*42, *43)		SA	65			dB
Group Delay Distortion: 0Hz ~ 8kHz		△GD		0		μs
Group Delay		GD		12.5		1/fs
ADC Digital Filter (HPF)						
Frequency Response	-3.0dB	FR		9.9		Hz

Notes:
*40. The passband and stopband frequencies scale with "fs" (system sampling rate). The characteristic of the high pass filter is not included.
*41. The passband is from DC to 6.3kHz when fs=16kHz.
*42. The stopband is 9.3kHz to 1.015MHz when fs=16kHz.
*43. When fs = 16kHz, the analog modulator samples the input signal at 1.024MHz. There is no attenuation of an input signal in band (n x 1.024MHz ±7.3kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

8.4.2. DAC

(Ta=-40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, fs=16kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Sharp Roll Off Filter						
Passband (*44)	±0.05dB	PB	0		7.2	kHz
	-6.0dB			8		kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband (*44)		SB	8.7			kHz
Stopband Attenuation: 0~ 8kHz (*45)		SA	64			dB
Group Delay (*46)		GD		24		1/fs
Digital Filter + Analog Filter						
Amplitude Characteristics 20Hz ~ 8kHz				±0.5		dB

Notes:
*44. The passband and stopband frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4535 × fs(@ ± 0.05dB) and SB=0.5465 × fs, respectively.
*45. The output level with 1kHz 0dB sine wave input is referred as 0dB.
*46. The digital filter delay is calculated as the time from setting 16/20/24 bit data into the input register until an analog signal is output.

8.5. Switching Characteristics

8.5.1. System Clock

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, CL=20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
with Crystal Oscillator (*47)						
Input Frequency (REFMODE[4:0] bits = "01111")		fXTI		11.2896 12.288		MHz
Input Frequency (REFMODE[4:0] bits = "10000")		fXTI		16.9344 18.432		MHz
with External Clock						
Duty Cycle			40	50	60	%
Input Frequency (REFMODE[4:0] bits = "01111")		fXTI	11.0	11.2896 12.288	12.4	MHz
Input Frequency (REFMODE[4:0] bits = "10000")		fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK Frequency (*48)		fs	7.8		49	kHz
BICK Frequency (*49)						
Normal Interface	High Level Width	tBCLKH	128			ns
	Low Level Width	tBCLKL	128			ns
	Frequency	fBCLK	0.23	3.072	3.1	MHz
TDM Interface	High Level Width	tBCLKH	32			ns
	Low Level Width	tBCLKL	32			ns
	Frequency	fBCLK	1.8	12.288	12.3	MHz

Notes:

*47. The crystal oscillator must have Typ. ±100ppm frequency accuracy.

*48. LRCK frequency and sampling rate (fs) should be the same.

*49. When BICK is the source of the master clock, it should be synchronized to LRCK and have stable frequency.

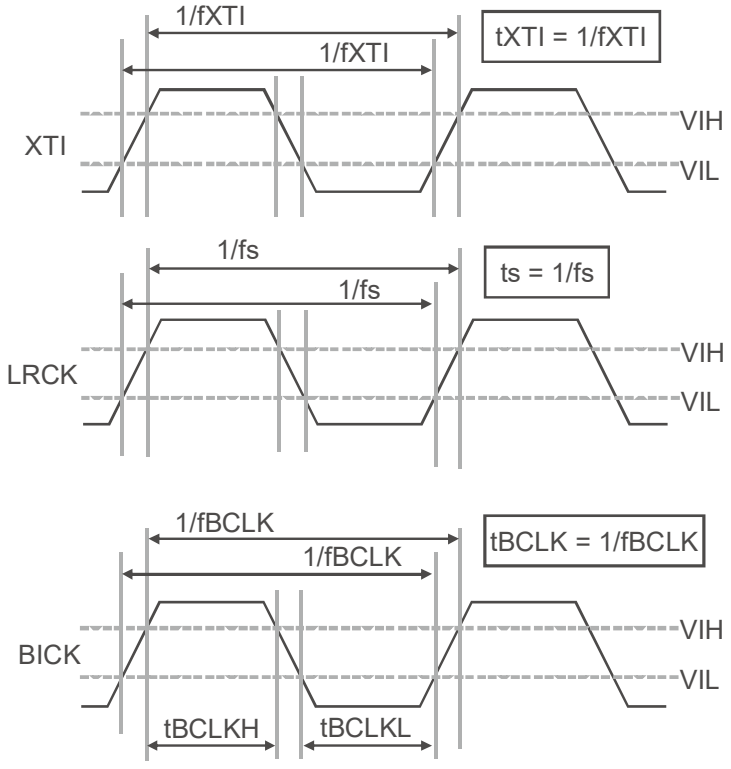


Figure 3. System Clock Timing

8.5.2. Power-down

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (*50)	tRST	600			ns

Note:
*50. The PDN pin must be "L" when power up the AK7759.

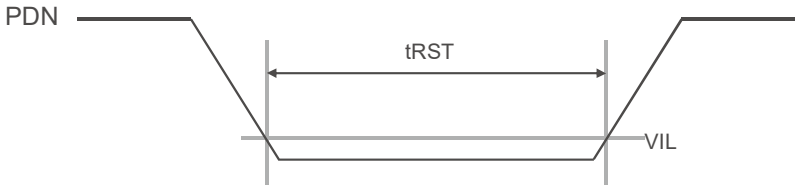


Figure 4. Reset Timing

8.5.3. Serial Data Interface (SDIN1/2, SDOUT1/2/3)

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (*51)	tBLRD	20			ns
Delay Time from LRCK to BICK "↑" (*51)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from LRCK to Serial Data Output (*52)	tLRD			30	ns
Delay Time from BICK "↓" to Serial Data Output (*53)	tBSOD			30	ns
Master Mode					
BICK Frequency	fBCLK		32,48,64, 128, 256		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK (*53)	tMBL	-12		12	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	20			ns
Delay Time from LRCK to Serial Data Output (*52)	tLRD			20	ns
Delay Time from BICK "↓" to Serial Data Output (*53)	tBSOD			20	ns

Notes:
*51. BICK edge must not occur at the same time as LRCK edge. If the BICK polarity was inverted, the counting edge of BICK will be "↓".
*52. Except I^2S.
*53. When the polarity of BICK is inverted, delay time is counted from BICK "↑".

8.5.3.1. Slave Mode

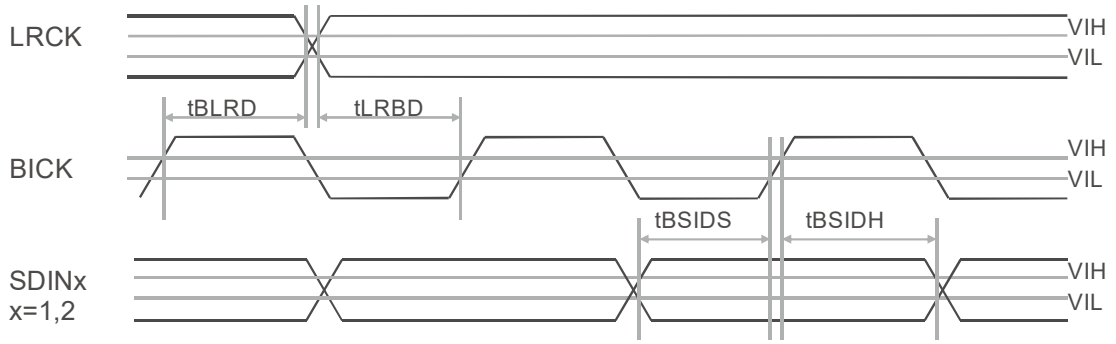


Figure 5. Serial Interface Input Timing in Slave Mode

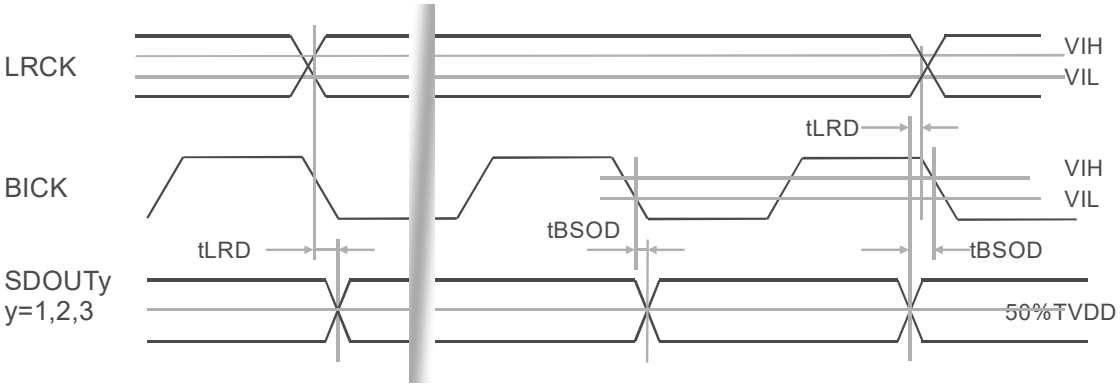


Figure 6. Serial Interface Output Timing in Slave Mode

8.5.3.2. Master Mode

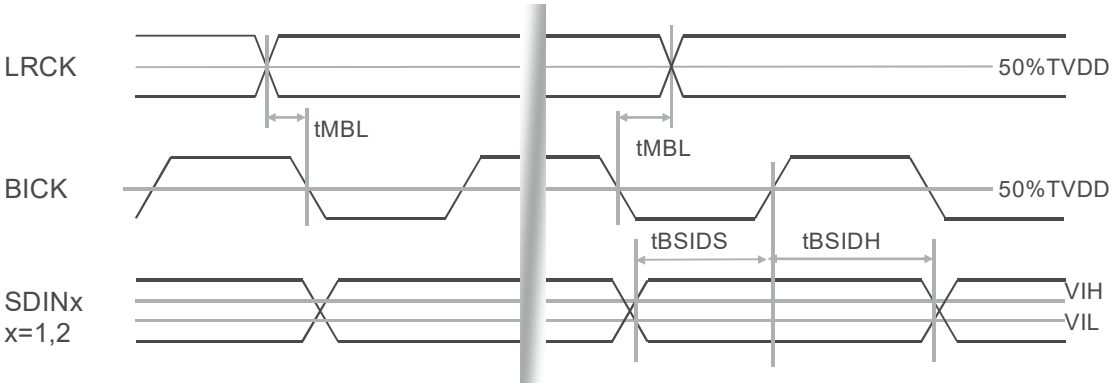


Figure 7. Serial Interface Input Timing in Master Mode

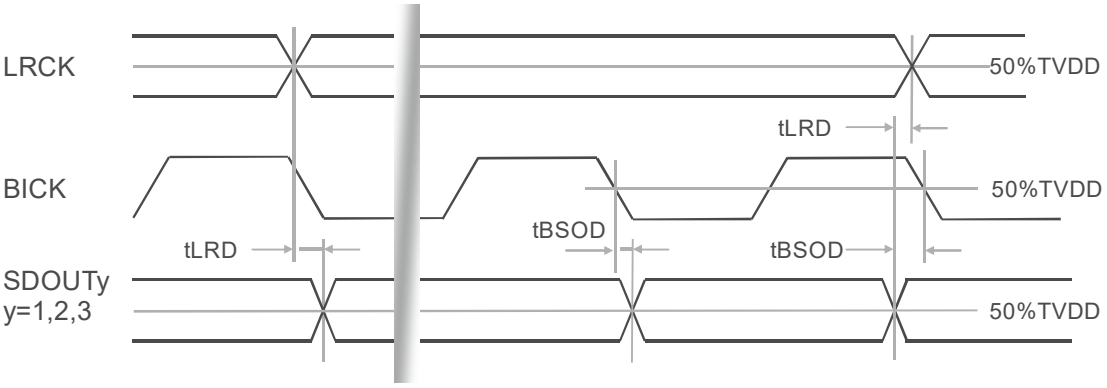


Figure 8. Serial Interface Output Timing in Master Mode

8.5.4. SPI Interface

8.5.4.1. Clock Reset (CKRESTN bit = "0")

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Microcontroller Interface Signal					
SCLK Frequency (*54)	fSCLK			3.5	MHz
SCLK Low Level Width	tSCLKL	120			ns
SCLK High Level Width	tSCLKH	120			ns
Microcontroller → AK7759					
CSN High Level Width	tWRQH	300			ns
Time from CSN "↑" to PDN "↑"	tRST	360			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from CSN"↓" to SCLK"↓"	tWSC	360			ns
Time from SCLK"↑" to CSN"↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	40			ns
SI Latch Hold Time	tSIH	40			ns
AK7759 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			40	ns

Note:
*54. SCLK frequency becomes 7 MHz when accessing control registers.

8.5.4.2. PLL Lock (CKRESTN bit = "1")

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Microcontroller Interface Signal					
SCLK Frequency (*55)	fSCLK			7	MHz
SCLK Low Level Width	tSCLKL	60			ns
SCLK High Level Width	tSCLKH	60			ns
Microcontroller → AK7759					
CSN High Level Width	tWRQH	150			ns
Time from CSN "↑" to PDN "↑"	tRST	180			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from CSN"↓" to SCLK"↓"	tWSC	150			ns
Time from SCLK"↑" to CSN"↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	20			ns
SI Latch Hold Time	tSIH	20			ns
AK7759 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			40	ns

Note:
*55. It takes 10ms at maximum until PLL is locked, after setting CKRESTN bit to "1" from "0".

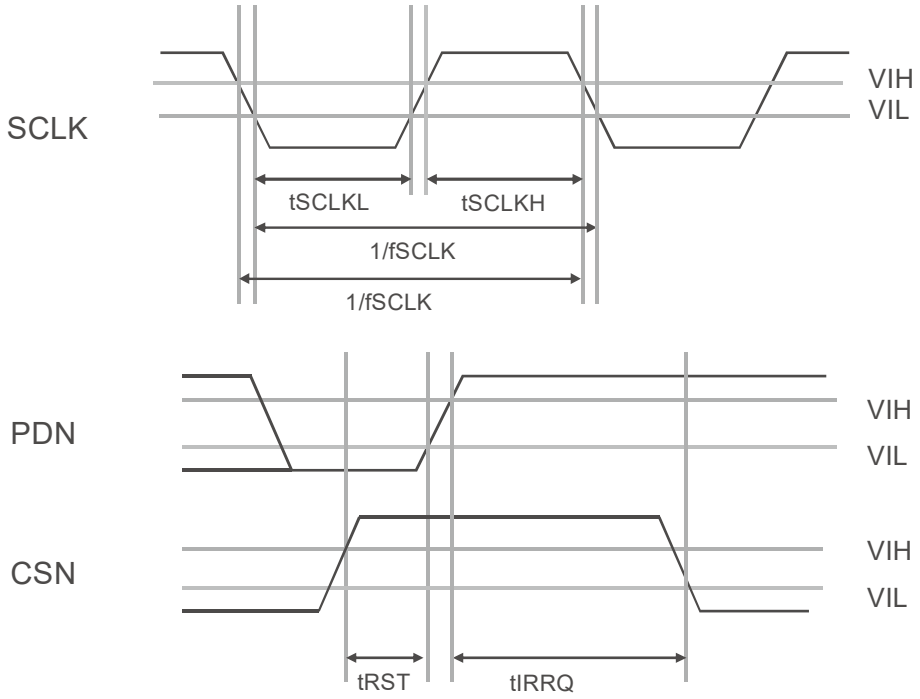


Figure 9. SPI Interface Timing 1

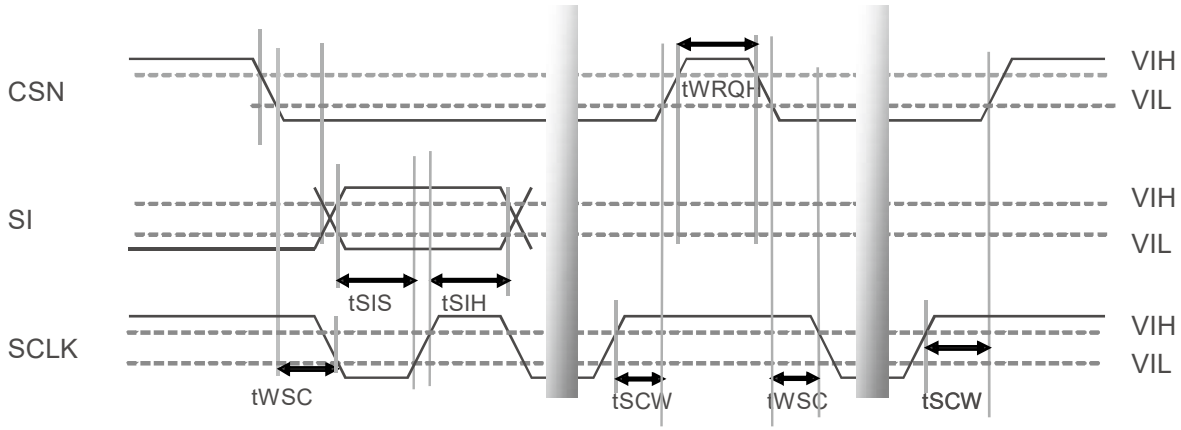


Figure 10. SPI Interface Timing 2 (Microcontroller → AK7759)

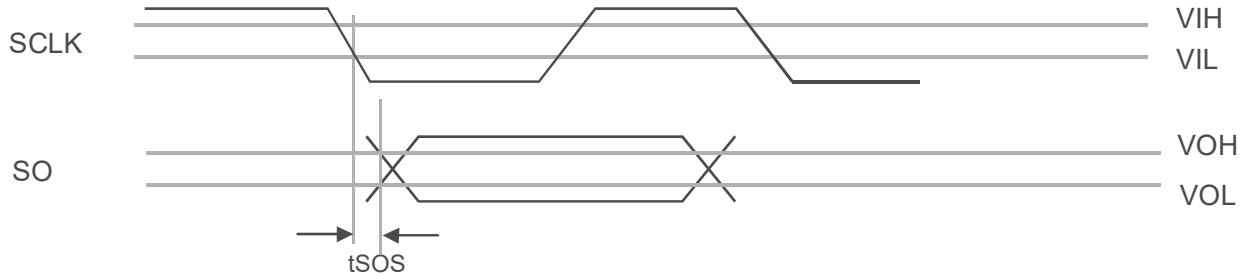


Figure 11. SPI Interface Timing 3 (AK7759 → Microcontroller)

8.5.5. I²C BUS Interface

(Ta= -40~105°C; AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V)
<I²C: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0			µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

<I²C: Fast Mode Plus>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL			1	MHz
Bus Free Time Between Transmissions	tBUF	0.5			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.26			µs
Clock Low Time	tLOW	0.5			µs
Clock High Time	tHIGH	0.26			µs
Setup Time for Repeated Start Condition	tSU:STA	0.26			µs
SDA Hold Time from SCL Falling	tHD:DAT	0			µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05			µs
Rise Time of Both SDA and SCL Lines	tR			0.12	µs
Fall Time of Both SDA and SCL Lines	tF			0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26			µs
Pulse Width of Spike Noise Suppressed By Input Filter (*56)	tSP	0		50	ns
Capacitive load on bus	Cb			550	pF

Note:
*56. In the interval of tHIGH, spike noise of Max. 50ns can be removed after 0.16µs.

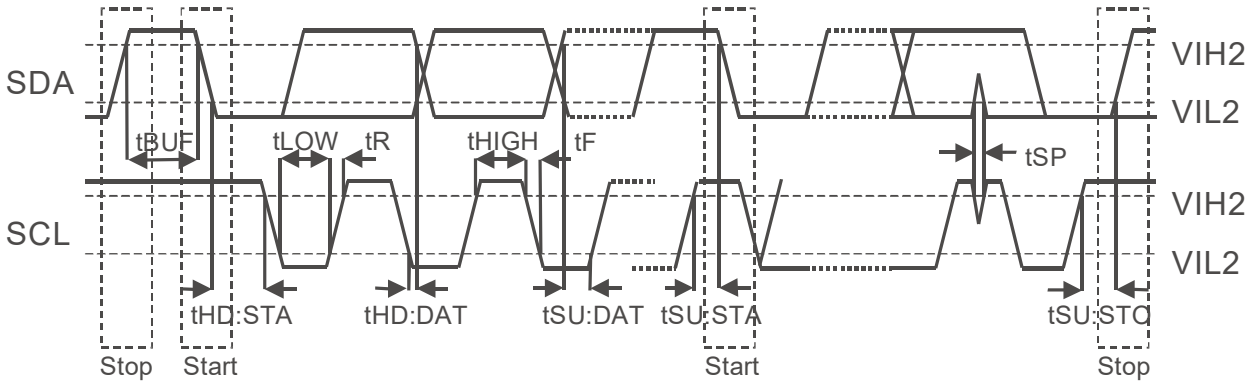


Figure 12. I²C BUS Interface Timing

8.5.6. Digital Microphone Interface

(Ta= -40°C~105°C, AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V, CL=100pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DMDAT					
Serial Data Input Latch Setup Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK					
Clock Frequency (*57)	fDMCK	0.5	64fs	3.1	MHz
Duty Cycle	dDMCK	40	50	60	%
Rise Time	tDMCKR			10	ns
Fall Time	tDMCKF			10	ns

Note:
*57. Clock frequency is determined by the sampling rate (fs) selected by clock sync domain of DMIC (SDCODEC[1:0] bits).

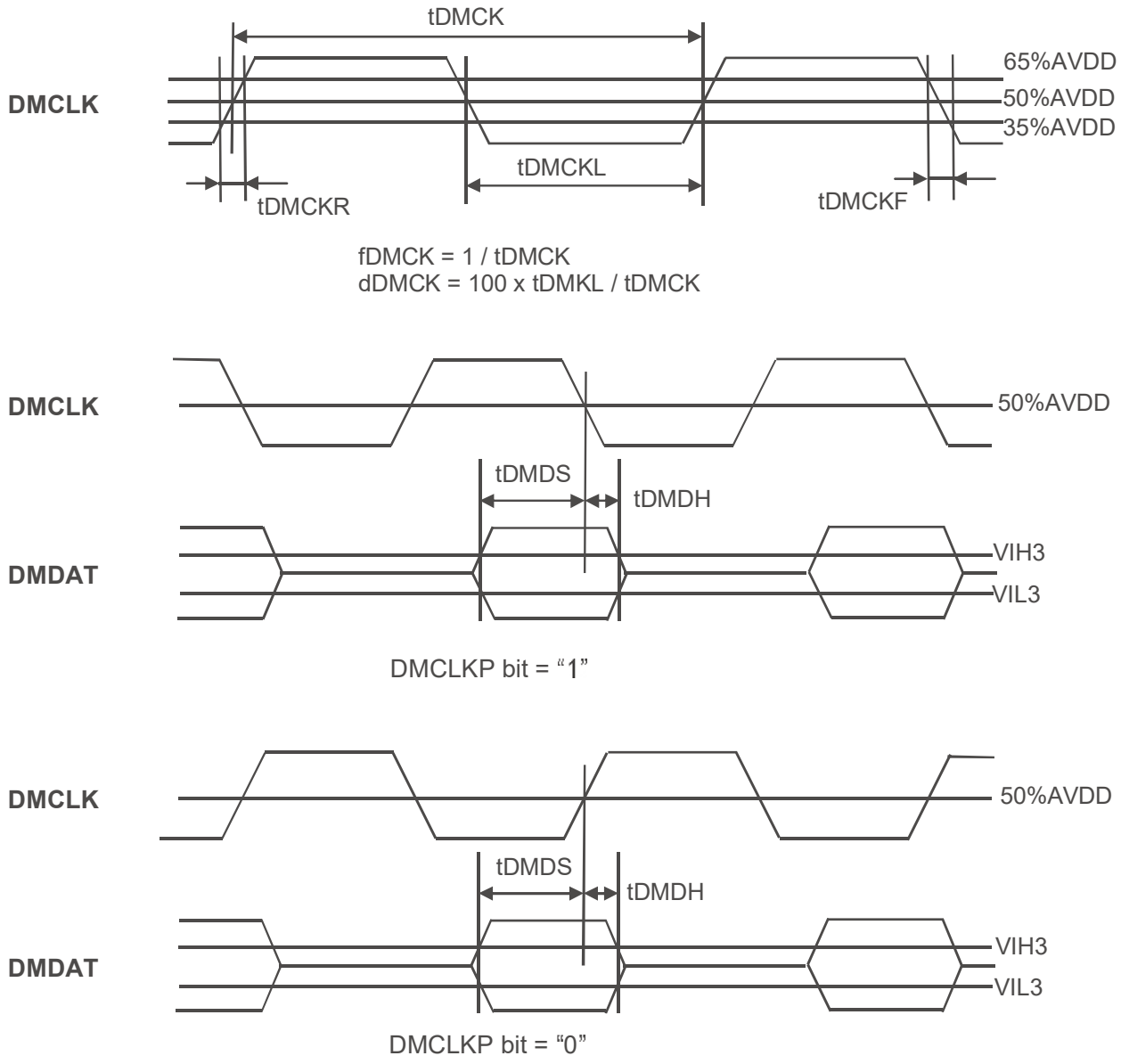


Figure 13. Digital Microphone Interface Timing Wave Form

8.5.7. EEPROM Interface

(Ta= -40~105°C, AVDD=LVDD=3.0~3.6V, TVDD=1.7~3.6V, AVSS=DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
EXTEEP H Pulse Width (*58)		tBTH	1.0			ms
EXTEEP L Pulse Width		tBTS	0.6			µs
MAT Selection Download Starting Pulse Width (*59)	MATNFN bit = "0"	tMT1	700			µs
	MATNFN bit = "1"	tMT2	0.6			µs
MAT Selection Re-download Starting Time (*60)	MATNFN bit = "0"	tRBT1		tDNFBT + 0.68		ms
	MATNFN bit = "1"	tRBT2		tDNFBT		ms
MAT Simultaneous Switching (*60)		tDLT			tDNFBT - 0.6	ms

Notes:

*58. The EXTEEP pin must be held "H" until data downloading from EEPROM is finished.

*59. Set the MARSEL pin = "H" when selecting the MAT.
The first data download from EEPROM should be executed by setting the EXTEEP pin = "L" → "H" while the PDN pin = "H" or by setting the PDN pin = "L" → "H" while the EXTEEP pin = "H". The second and succeeding data downloads can be executed by setting the MAT0/MAT1 pin.
It is necessary to keep pin statuses for 700µs when starting data download if MATNFN bit = "0" (noise filter ON). The AK7759 re-downloads data if the MAT0/MAT1 pin status of when finishing data download is different form the pin status when starting the download.

*60. Response time of the MAT switching (tDNFBT) can be changed by DNFBOOT[1:0] bits.
Re-download starting time of MAT selection is controlled by MATNFN bit. It can be represented as "tRBT1 = tDNFBT + 0.68ms" when MATNFN bit = "0" (noise filter ON) and "tRBT2 = tDNFBT" when MATNFN bit = "1" (noise filter OFF). Error time of MAT simultaneous switching (tDLT) is represented as "tDLT = tDNFBT – 0.6ms".

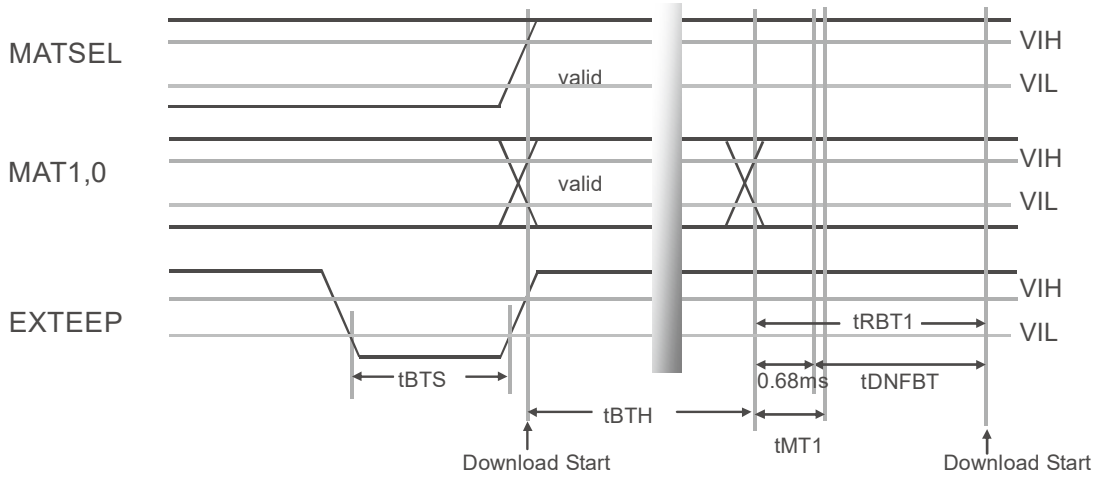
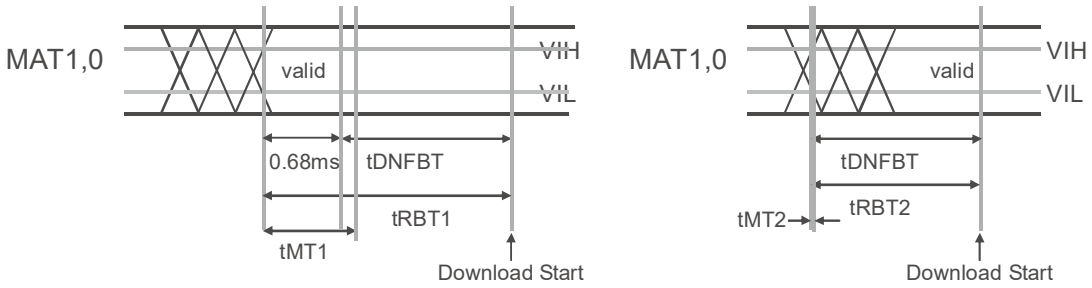


Figure 14. MAT Setting Timing (MATNFN bit = "0")



a. MATNFN bit = "0" b. MATNFN bit = "1"

Figure 15. MAT Selection Re-downloading Start Time (EXTEEP pin = MATSEL pin = "H")

Note:

*61. When MATNFN bit = "0" (noise filter ON), the AK7759 starts data download in "tDNFBT + 0.68ms" by holding the MAT0/MAT1 pin status for 0.7ms or more after changing the pin status. The AK7759 starts downloading in "tDNFBT" after changing the pin status of the MAT0/MAT1 pin when MATNFN bit = "1" (noise filter OFF).

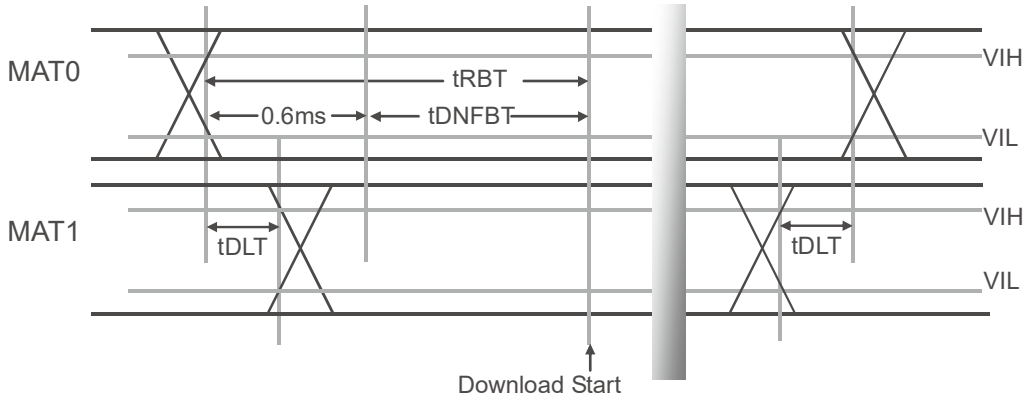


Figure 16. MAT Simultaneous Switching Error

Note:

*62. Input data of the MAT0/1 pins should be settled in "tDLT = tDNFBT - 0.6ms = 0.4ms" when "tDNFBT = 1ms" (DNFBOOT[1:0] bit = "00", I2CFP pin = "H"). If not, the AK7759 detects MATERR and executes re-downloading in the status when finish downloading.

9. Recommended External Circuits

9.1. Connection Diagram

9.1.1. I2CSEL pin = “L”

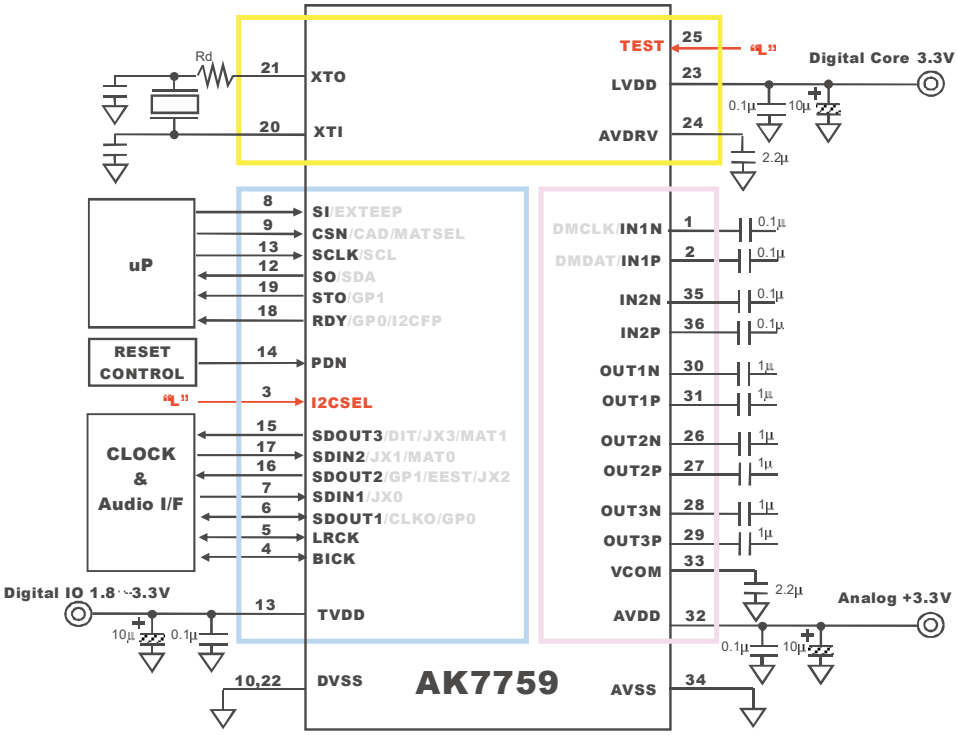


Figure 17. Serial Interface Connection Example

9.1.2. I2CSEL pin = “H”, EXTEEP pin = “L”

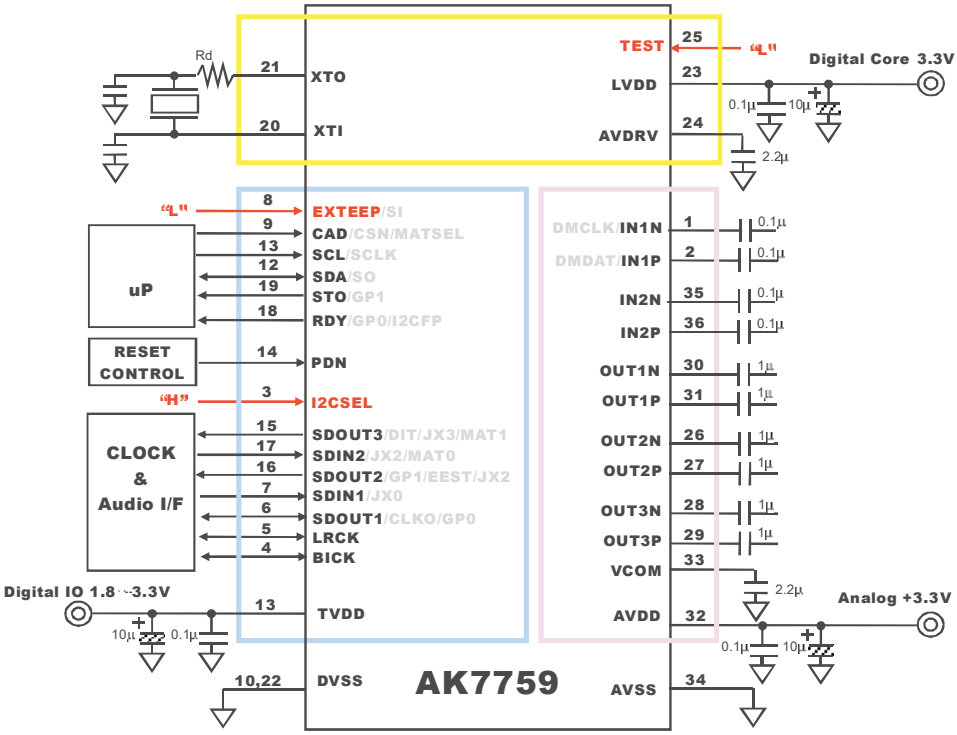


Figure 18. I²C Interface Connection Example

9.1.3. I2CSEL pin = “H”, EXTEEP pin = “H”, MATSEL pin = “L”

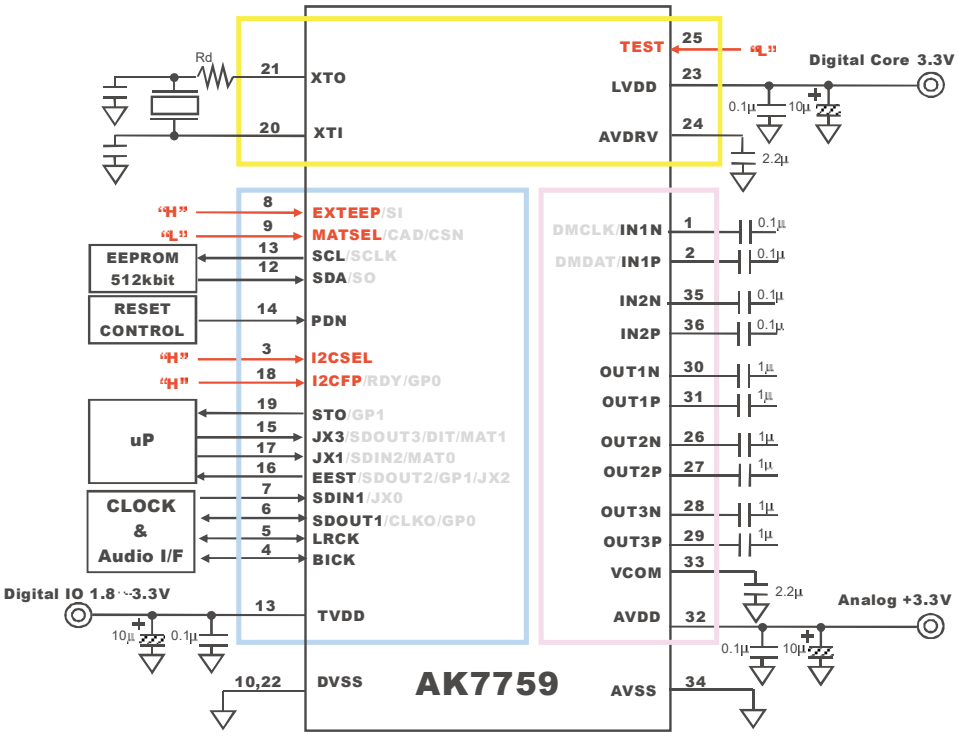


Figure 19. I²C Interface Connection with External EEPROM

9.1.4. I2CSEL pin = “H”, EXTEEP pin = “H”, MATSEL pin = “H”

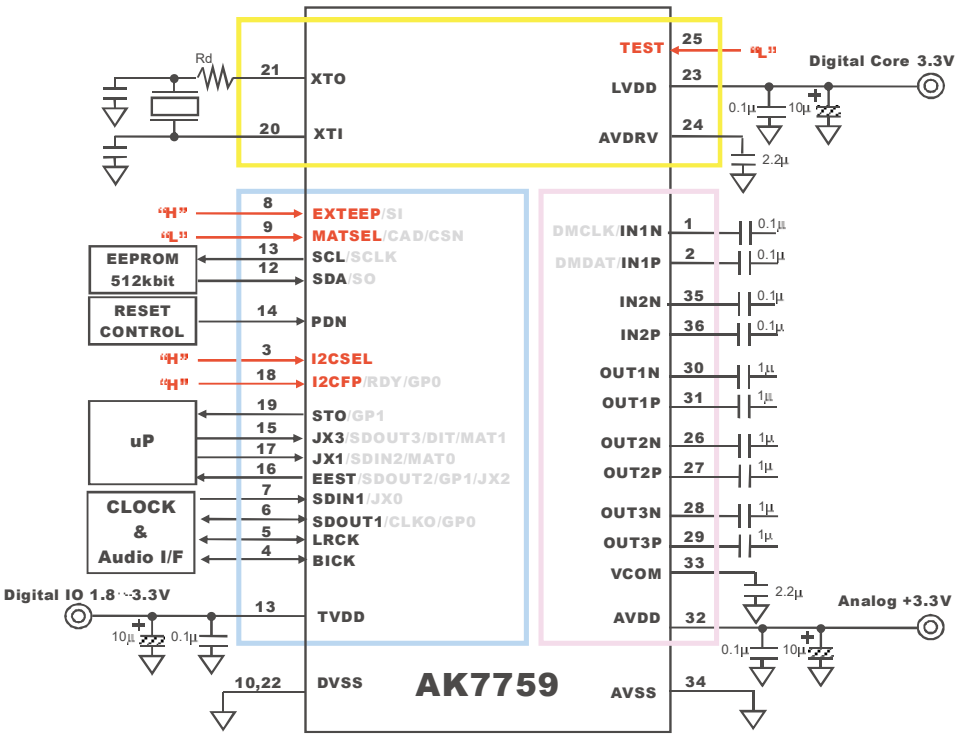


Figure 20. I²C Interface Connection with External EEPROM (Mat Select ON)

9.2. Peripheral Circuit

9.2.1. Ground

AVSS and DVSS must be connected to the same analog ground plane. Decoupling capacitors, particularly small capacity ceramic capacitors, should be connected as close as possible to the AK7759.

9.2.2. Reference Voltage

The AVDD voltage controls analog signal range. VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2μF ceramic capacitor connected between the VCOM and AVSS pins eliminates the effects of high frequency noise. The ceramic capacitor should be connected as close as possible to the VCOM pin.
The VCOM pin must not be connected to external circuits. Digital signal lines, especially clock signal line should be kept away as far as possible from the VCOM pin in order to avoid unwanted coupling into the AK7759.

9.2.3. Analog Input

Analog input signals are applied to the modulator through the input pin of each channel. Input voltage is ±FS = ±AVDD x 0.67 Vp-p for differential pin and FS = AVDD x 0.67 Vp-p for single-ended pin. When AVDD = 3.3V and AVSS=0.0V, the differential input range is ±2.2Vp-p (Typ.) and it is 2.2Vp-p (typ) for single-ended input. The digital output code format is 2's complements. DC offset can be cancelled by an internal HPF.

The AK7759 samples the analog inputs in 3.072MHz at fs = 48kHz. The digital filter removes noise in the range from 30 kHz to 3.042 MHz. The AK7759 includes an anti-aliasing filter (RC filter) to attenuate a noise around the range from 3.042 MHz to 3.072 MHz witch is not removed by the HPF. An external Low Pass Filter is not necessary since most of audio signals do not have large noise in the band around 3.072MHz. However, it is recommended to connect a Low Pass Filter before the ADC when a signal with large out-of-band noises is input.

The analog source voltage to the AK7759 is +3.3V (Typ.). Voltage of AVDD + 0.3V or more, voltage of AVSS – 0.3V or less, and current of 10mA or more must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. If the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are in absolute maximum rating level or more.

9.2.4. Analog Output

The analog line-outputs are single-ended. The output signal range is 0.86 × AVDD Vp-p (Typ.) centered around VCOM voltage. The input code format is in 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal voltage at 000000H is VCOM. The VCOM voltage is AVDD/2 (Typ.). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

9.2.5. Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

Table 3. Recommended Resistance and Capacitance with Cristal Oscillator
•LVDD = 3.0 ~ 3.6V

Oscillation Frequency [MHz]	R1(Max.)	C0(Max.)	XTI, XTO Pin Connection Capacity (CL)
11.2896 12.288	120Ω	2.5pF	22pF
16.9344 18.432	80Ω	2.5pF	15pF

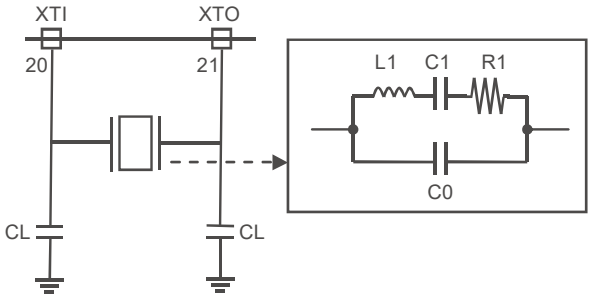
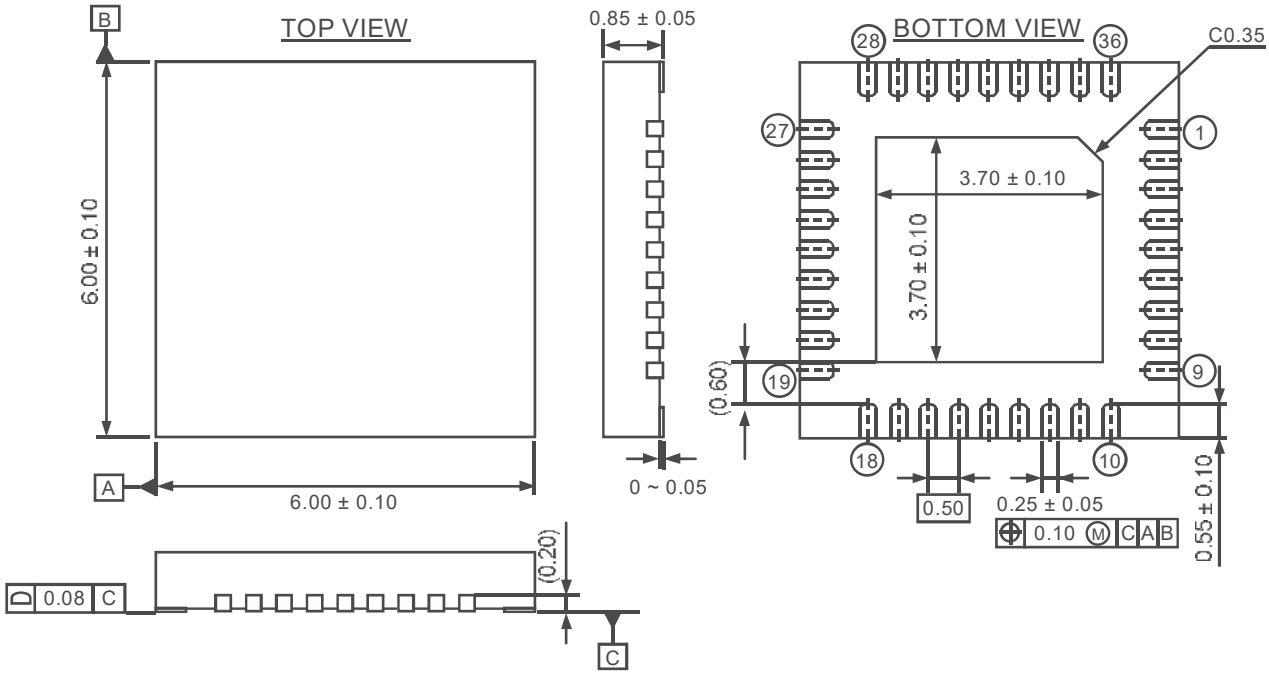


Figure 21. Electric Equivalent Circuit of Crystal Oscillator

10. Package

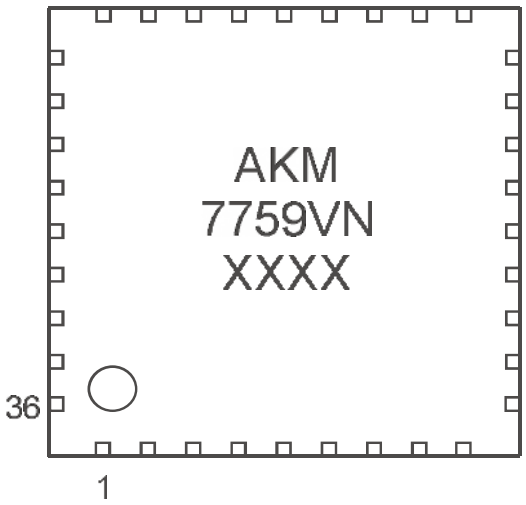
10.1. Outline Dimensions



10.2. Material and Finish

Package: Epoxy
Lead Frame: Copper
Pin surface treatment: Soldering (Pb free) plate

10.3. Marking



1) Pin #1 indication
2) Date Code: XXXX(4 digits)
3) Marking Code: 7759VN
4) Asahi Kasei Logo

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