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AK7780

24bit 5ch ADC & SRC + Audio DSP

GENERAL DESCRIPTION

The AK7780 is a highly integrated audio processor, including a 28-bit floating point DSP, two 24-bit stereo ADC's and one mono ADC. The stereo ADC's feature high performance, achieving 96dB dynamic range, they include 8:1 input selectors. The ADC supports sampling frequencies from 7.35 kHz to 96 kHz. The AK7780 also includes a stereo sample rate converter (SRC), so it can be used as a master device when it receives digital audio inputs. The DSP includes 168kbits of SRAM for audio delay data that is suitable for creating simulated surround fields. The programmable DSP block is realized with 2560step/fs DSP. It supports sampling frequencies from 7.35kHz to 96 kHz. The AK7780 is used to implement complete sound field control, such as echo, 3D, parametric equalization, and other sound enhancements. It is packaged in a 100-lead LQFP package.

FEATURES

[DSP]

Main

- Word length: 28-bit (Data RAM F24.4 limited range floating point)
- Instruction cycle time: 8.1 ns (2560step/fs fs=48kHz; 1280step/fs fs=96kHz)
- Multiplier: 24 x 16 → 40-bit (Double precision available)
- Divider: 24 / 24 → 24-bit
- ALU: 44-bit arithmetic operation (overflow margin: 4-bits)
F24.4 arithmetic and logic operation
- Shift+Register: Flexible setting
- Program RAM: 2048 x 36-bit
- Coefficient RAM: 2048 x 16-bit
- Data RAM: 2048 x 28-bit (F24.4[sign bit + 23-bit mantissa + 4-bit exponent])
- Offset RAM: 64 x 13-bit
- Internal Delay RAM: 168kbits
(6144 x 28 bit / 2048 x 28 bit + 8192 x 14 bit / 3072 x 28 bit + 6144 x 14 bit
/ 4096 x 28 bit + 4096 x 14 bit) 4 pattern setting
28bit = F24.4 [24 bit sign & mantissa: 4 bit exponent]
14bit = F10.4 [10 bit sign & mantissa: 4 bit exponent]
- Sampling frequency: 7.35kHz ~ 96kHz
- Serial interface port for microcontroller or I²C BUS control
- Master Clock: 2560fs (generated by PLL from 32fs, 64fs, 256fs and 384fs)
- Master/Slave operation
- Serial signal input port (10ch): MSB justified 24-bit / LSB justified 16/20/24-bit and I²S
- Serial signal output port(12ch): MSB justified 24-bit / LSB justified 24,16-bit and I²S
(SDOUT1,SDOUT2 and SDOUT3)

[ADC]

4 channels (2 stereo pairs)

- 24-bit 64X over-sampling delta-sigma (fs = 7.35kHz ~ 96kHz)
- DR, S/N: 96dBA (fs = 48kHz, fully-differential input)
- S/(N+D): 92dB (fs = 48kHz)
- Digital HPF (fc = 1Hz)

[ADC]**Mono single channel**

- 24-bit 64X over-sampling delta sigma ($f_s = 7.35\text{kHz} \sim 96\text{kHz}$)
- DR, S/N: 95dBA ($f_s = 48\text{kHz}$)
- Includes digital attenuator

[SRC]**Stereo pair**

- Input frequency 7.35kHz ~ 96kHz → Output frequency 44.1kHz ~ 96kHz

[Other]

- Power supply: +3.3V \pm 0.3V, +1.7V~+2.0V(typ +1.8V)
- Operating temperature range: -40°C~85°C
- Package: 100pin LQFP(0.5mm pitch)

BLOCK DIAGRAM

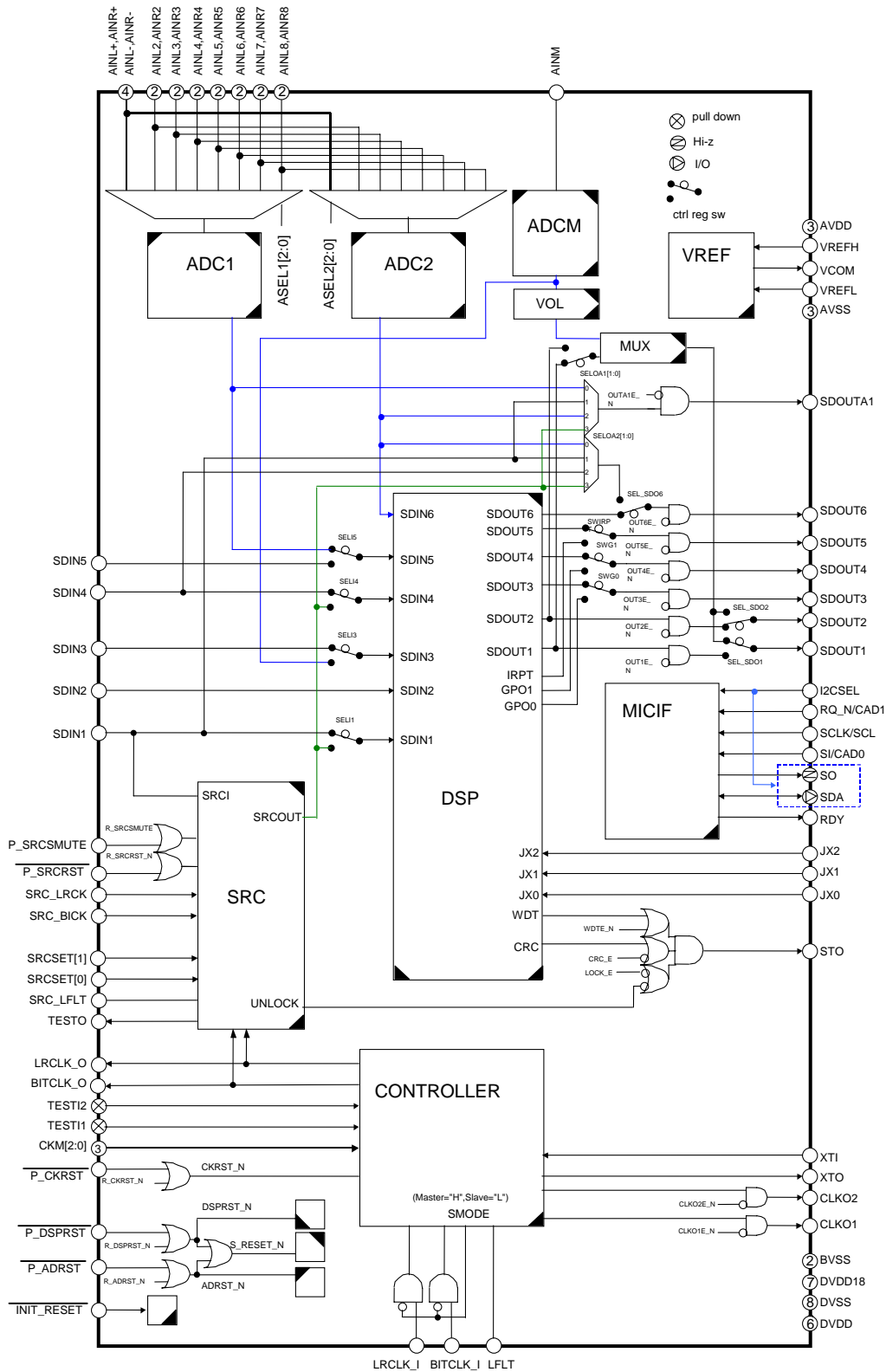


Figure 1. Whole Block Diagram

* Figure 1 shows a simplified diagram of the AK7780, which isn't the perfect same as the actual circuit diagram. Each describes the relationship of reset control and target reset blocks.

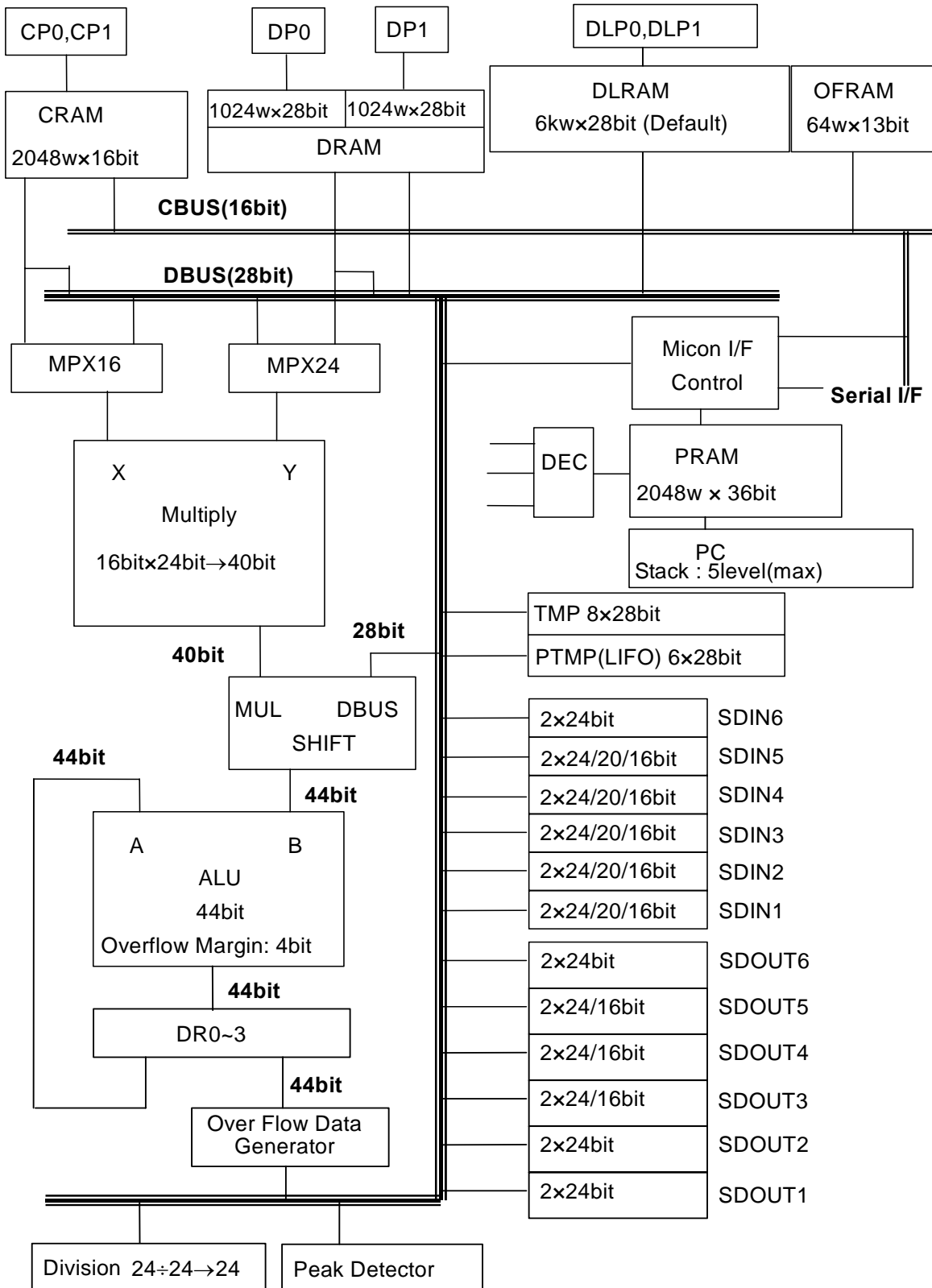


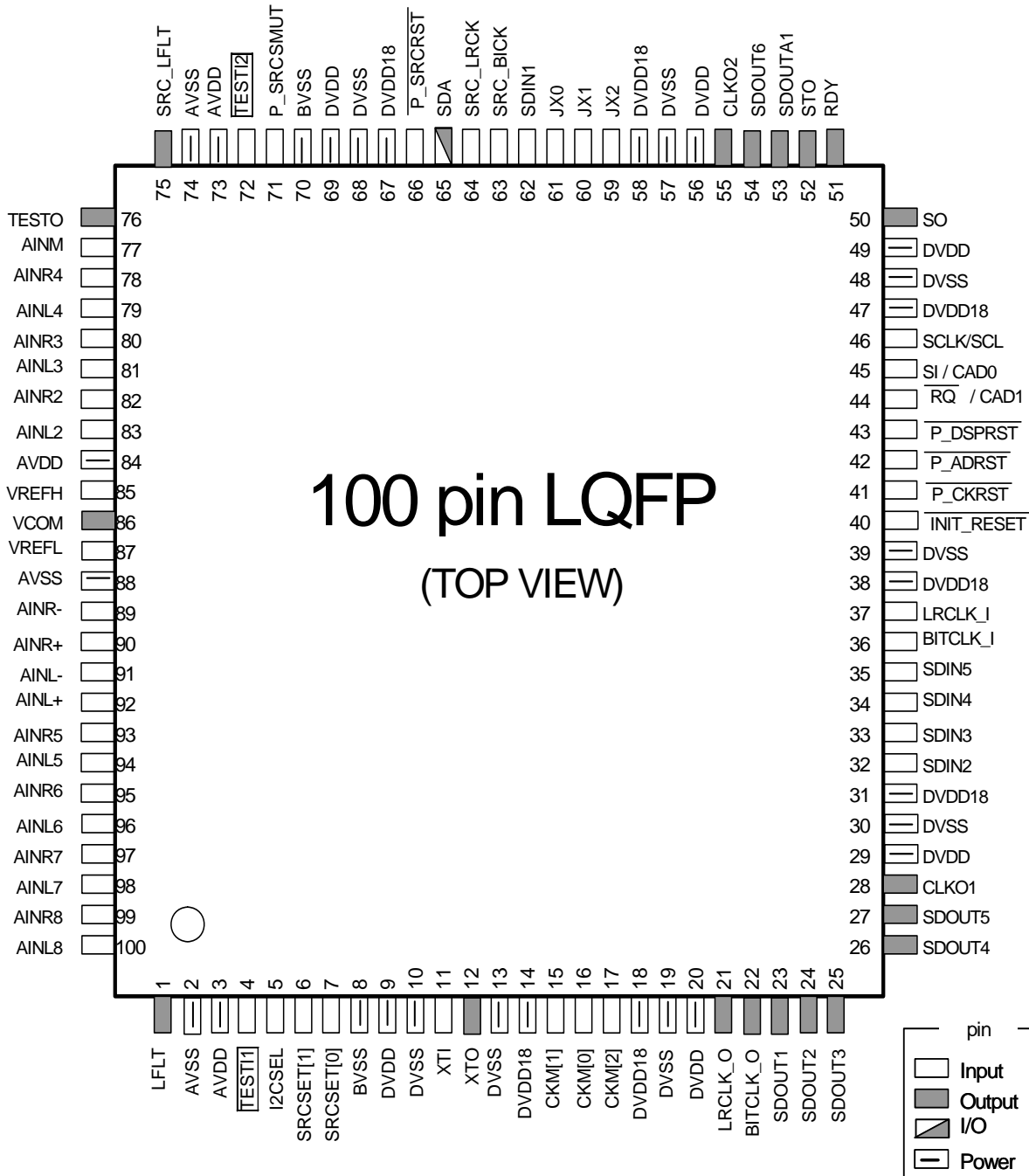
Figure 2. DSP Block Diagram

■ Ordering Guide

AK7780VQ
AKD7780

-40 ~ +85°C 100pin LQFP(0.5mm pitch)
Evaluation Board for AK7780

■ Pin layout



PIN FUNCTION

| No | Pin Name | I/O | Function | Classification |
|----|------------|-----|---|-------------------------|
| 1 | LFLT | O | Filter connection pin for AK7780 core PLL When using the PLL function, connect with R (1.5kΩ) and C (47nF) in series and connected to analog ground (AVSS) see. 9. System design (1) | Analog Output |
| 2 | AVSS | - | Analog ground 0V | Analog Power Supply |
| 3 | AVDD | - | Power supply pin for analog section 3.3V (typ) | |
| 4 | TEST11 | I | TEST pin (Internal pull-down) * Connect to DVSS | TEST |
| 5 | I2CSEL | I | I²CBUS select pin * I2CSEL= "L": Normal serial interface * I2CSEL= "H": I ² CBus selected mode. SCL and SDA are active. I2CSEL must be set to "L (DVSS)" or "H (DVDD)". | I ² C Select |
| 6 | SRCSET [1] | I | SRC select pin 1 | SRC |
| 7 | SRCSET [0] | I | SRC select pin 0 | |
| 8 | BVSS | - | Silicon substrate potential 0V Connect to AVSS. | Analog Power Supply |
| 9 | DVDD | - | Power supply pin for digital section 3.3V (typ) | Digital Power Supply |
| 10 | DVSS | - | Ground pin for digital section 0V | |
| 11 | XTI | I | Master clock input pin Connect a crystal between this pin and the XTO pin, or input an external CMOS clock signal to the XTI pin. | System Clock |
| 12 | XTO | O | Crystal oscillator output pin When using a crystal, connect it between XTI and XTO. When using an external clock, keep this pin open. | |
| 13 | DVSS | - | Ground pin for digital section 0V | Digital Power Supply |
| 14 | DVDD18 | - | Power supply pin for digital section 1.8V (typ) | |
| 15 | CKM [1] | I | Clock mode select pin 1 | Mode select |
| 16 | CKM [0] | I | Clock mode select pin 0 | |
| 17 | CKM [2] | I | Clock mode select pin 2 | |
| 18 | DVDD18 | - | Power supply pin for digital section 1.8V (typ) | Digital Power Supply |
| 19 | DVSS | - | Ground pin for digital section 0V | |
| 20 | DVDD | - | Power supply pin for digital section 3.3V (typ) | |

| No | Pin Name | I/O | Function | Classification |
|----|----------|-----|--|---------------------------------------|
| 21 | LRCLK_O | O | LR channel select clock output pin Master mode: Outputs fs clock. Slave mode: Outputs LRCLK_I clock. | System Clock |
| 22 | BITCLK_O | O | Serial bit clock output pin Master mode: Outputs 64fs clock. Slave mode: Outputs BITCLK_I clock | |
| 23 | SDOUT1 | O | DSP Serial data output pin * Compatible with MSB justified 24 bits / I ² S. | Digital section Serial output data |
| 24 | SDOUT2 | O | DSP Serial data output pin * Compatible with MSB justified 24 bits / I ² S. | |
| 25 | SDOUT3 | O | DSP Serial data output pin * Compatible with MSB justified 24 bits / LSB justified 24 and 16 bits/ I ² S. | |
| 26 | SDOUT4 | O | DSP Serial data output pin * Compatible with MSB justified 24 bits / LSB justified 24 and 16 bits/ I ² S. | |
| 27 | SDOUT5 | O | DSP Serial data output pin * Compatible with MSB justified 24 bits / LSB justified 24 and 16 bits/ I ² S. | |
| 28 | CLKO1 | O | Clock output pin 1 Select the output frequency through a control register. | Clock output |
| 29 | DVDD | - | Power supply pin for digital section 3.3V(typ) | Digital Power Supply |
| 30 | DVSS | - | Ground pin for digital section 0.0V | |
| 31 | DVDD18 | - | Power supply pin for digital section 1.8V(typ) | |
| 32 | SDIN2 | I | DSP serial data input pin Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits / I ² S. * If not used, connect to DVSS | Digital section Serial input data |
| 33 | SDIN3 | I | DSP serial data input pin Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits / I ² S. * If not used, connect to DVSS | |
| 34 | SDIN4 | I | DSP serial data input pin Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits / I ² S. * If not used, connect to DVSS | |
| 35 | SDIN5 | I | DSP serial data input pin Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits / I ² S. * If not used, connect to DVSS | |

| No | Pin Name | I/O | Function | Classification |
|----|---------------------------------|-----|---|--------------------------|
| 36 | BITCLK_I | I | Serial bit clock input pin | System Clock |
| 37 | LRCLK_I | I | LR channel select clock input pin. | |
| 38 | DVDD18 | - | Power supply pin for digital section 1.8V(typ) | Digital power supply |
| 39 | DVSS | - | Ground pin for digital section 0.0V | |
| 40 | $\overline{\text{INIT_RESET}}$ | I | Reset pin (for initialization) Use for initialization. When changing CKM[2:0], XTI or BITCLK_I input frequency, this reset pin must be used. | Reset |
| 41 | $\overline{\text{P_CKRST}}$ | I | Clock reset pin When changing CKM[2:0] and XTI or BITCLK_I input frequency without using INIT_RESET, pin control is necessary. The control register R_CKRST_N can also rest the clock. | |
| 42 | $\overline{\text{P_ADRST}}$ | I | ADC Reset pin The control register R_ADRST_N can also reset the ADC. $\overline{\text{P_ADRST}} = \text{“L”}$ and $\overline{\text{P_DSPRST}} = \text{“L”}$ state causes a system reset (S_RESET). | |
| 43 | $\overline{\text{P_DSPRST}}$ | I | DSP Reset pin The control register R_DSPRST_N can also rest the DSP. $\overline{\text{P_ADRST}} = \text{“L”}$ and $\overline{\text{P_DSPRST}} = \text{“L”}$ state causes a system reset (S_RESET). | |
| 44 | $\overline{\text{RQ}}$ | I | I2CSEL= “L” Microcomputer interface write request pin. After initial reset, if the microcomputer interface is not used, $\overline{\text{RQ}} = \text{“H”}$ | Microcomputer Interface. |
| | CAD1 | I | I2CSEL=“H” I²C Bus address setting pin 1 | I ² C |
| 45 | SI | I | Microcomputer interface serial data input and serial data output control pin. When SI is not used, leave SI = “L”. | Microcomputer Interface. |
| | CAD0 | I | I2CSEL= “H” I²C Bus address pin 0 | I ² C |
| 46 | SCLK | I | I2CSEL= “L” Microcomputer interface serial data clock pin. When SCLK is not used, leave SCLK= “H” | Microcomputer Interface. |
| | SCL | I | I2CSEL= “H” I²C bus data clock pin | I ² C |
| 47 | DVDD18 | - | Power supply pin for digital section 1.8V(typ) | Digital power supply |
| 48 | DVSS | - | Ground pin for digital section 0.0V | |
| 49 | DVDD | - | Power supply pin for digital section 3.3V(typ) | |
| 50 | SO | O | Serial data output pin for microcomputer interfaces. When $\overline{\text{RQ}} = \text{“H”}$, SO = Hi-Z | Microcomputer Interface. |

| No | Pin Name | I/O | Function | Classification |
|----|-------------|-----|--|--------------------------------------|
| 51 | RDY | O | Data write ready output pin for microcomputer interface. | Microcomputer Interface. |
| 52 | STO | O | Status output pin Normal state output "H". When WDT, CRC error or SRC UNLOCK occurs, then output "L". See 3.(1) Whole block diagram. | Status |
| 53 | SDOUTA1 | O | DSP or ADC Serial data output pin * Compatible with MSB justified 24 bits / I ² S. | Digital section |
| 54 | SDOUT6 | O | DSP or ADC Serial data output pin * Compatible with MSB justified 24 bits / I ² S. | Serial output data |
| 55 | CLKO2 | O | Clock output pin 2 Select the output frequency through a control register. | Clock output |
| 56 | DVDD | - | Power supply pin for digital section 3.3V(typ) | Digital power supply |
| 57 | DVSS | - | Ground pin for digital section 0.0V | |
| 58 | DVDD18 | - | Power supply pin for digital section 1.8V(typ) | |
| 59 | JX2 | I | External condition jump pin * When not used, connect to DVSS | Conditional input |
| 60 | JX1 | I | External condition jump pin * When not used, connect to DVSS | |
| 61 | JX0 | I | External condition jump pin * When not used, connect to DVSS | |
| 62 | SDIN1 | I | DSP/SRC Serial input pin Input pin for SRC. When not used, connect to DVSS. | Digital section Serial input data |
| 63 | SRC_BICK | I | SRC Serial bit clock input pin. | SRC |
| 64 | SRC_LRCK | I | SRC LR channel select clock input pin. | |
| 65 | SDA | I | I²CSEL= "L" SDA Outputs "L" level. | I ² C |
| | | I/O | I²CSEL= "H" I²C bus interface data pin | |
| 66 | P_SRCRST | I | SRC Reset pin The control register R_SRCRST_N can also rest the SRC. | RESET |
| 67 | DVDD18 | - | Power supply pin for digital section 1.8V(typ) | Digital power supply |
| 68 | DVSS | - | Ground pin for digital section 0.0V | |
| 69 | DVDD | - | Power supply pin for digital section 3.3V(typ) | |
| 70 | BVSS | - | Silicon substrate potential 0V Connect to AVSS. | Analog power supply |
| 71 | P_SRC SMUTE | I | SRC Soft mute pin The control register R_SRCSMUTE can also execute a soft mute on the SRC. | SRC |
| 72 | TESTI2 | I | TEST pin (Internal pull-down) * Connect to DVSS. | TEST |
| 73 | AVDD | - | Power supply pin for analog section 3.3V (typ) | Analog power supply |
| 74 | AVSS | - | Analog ground 0V | |
| 75 | SRC_LFLT | O | RC Filter connection pin for SRC. See p.86 10-2-5-2: SRC PLL loop filter setting. | Analog output |

| No | Pin Name | I/O | Function | Classification |
|-----|----------|-----|--|---------------------|
| 76 | TESTO | O | TEST OUT pin Hi-Z Output pin. Leave it open. | TEST |
| 77 | AINM | I | ADCM single ended analog input | Analog input |
| 78 | AINR4 | I | ADC1 or ADC2 Rch single ended analog input 4 | |
| 79 | AINL4 | I | ADC1 or ADC2 Lch single ended analog input 4 | |
| 80 | AINR3 | I | ADC1 or ADC2 Rch single ended analog input 3 | |
| 81 | AINL3 | I | ADC1 or ADC2 Lch single ended analog input 3 | |
| 82 | AINR2 | I | ADC1 or ADC2 Rch single ended analog input 2 | |
| 83 | AINL2 | I | ADC1 or ADC2 Lch single ended analog input 2 | |
| 84 | AVDD | - | Power supply pin for analog section 3.3V (typ) | Analog Power Supply |
| 85 | VREFH | I | Analog reference voltage input pin. Connect to AVDD, and connect 0.1μF and 10μF bypass capacitors between this pin and AVSS. | Analog input |
| 86 | VCOM | O | Common voltage Connect to 0.1μF and 10μF capacitors between this pin and AVSS. Do not connect to external circuitry. | Analog output |
| 87 | VREFL | I | Analog reference voltage input pin for low-level. Connect to AVSS. | Analog input |
| 88 | AVSS | - | Analog ground 0V | Analog Power Supply |
| 89 | AINR- | I | ADC1 or ADC2 Rch inverted input pin | Analog input |
| 90 | AINR+ | I | ADC1 or ADC2 Rch non- inverted input pin | |
| 91 | AINL- | I | ADC1 or ADC2 Lch inverted input pin | |
| 92 | AINL+ | I | ADC1 or ADC2 Lch non- inverted input pin | |
| 93 | AINR5 | I | ADC1 or ADC2 Rch single ended analog input 5 | |
| 94 | AINL5 | I | ADC1 or ADC2 Lch single ended analog input 5 | |
| 95 | AINR6 | I | ADC1 or ADC2 Rch single ended analog input 6 | |
| 96 | AINL6 | I | ADC1 or ADC2 Lch single ended analog input 6 | |
| 97 | AINR7 | I | ADC1 or ADC2 Rch single ended analog input 7 | |
| 98 | AINL7 | I | ADC1 or ADC2 Lch single ended analog input 7 | |
| 99 | AINR8 | I | ADC1 or ADC2 Rch single ended analog input 8 | |
| 100 | AINL8 | I | ADC1 or ADC2 Lch single ended analog input 8 | |

Note 1. Digital input pins must not be allowed to float

Note 2. If analog input pins (AINR-, AINR+, AINL-, AINL+, AINL2-8, AINR2-8, AINM) are not used, leave them open.

Note 3. I2CSEL should be set to "L" (DVSS) or "H" (DVDD).

Relationship with I2CSEL and SDA.

| | I2CSEL | $\overline{\text{INIT_RESET}}$ | SDA |
|----------------------------------|--------|---------------------------------|---------------------------|
| Normal Microcontroller Interface | L | L | L |
| | L | H | L |
| I ² C bus compatible | H | L | "Hi-Z" → pull-up function |
| | H | H | function |

ABSOLUTE MAXIMUM RATINGS

(AVSS = BVSS = DVSS = 0V: All indicated voltages are with respect to ground.)

| Item | Symbol | min | max | Unit |
|---|---------------|------|----------|------|
| Power supply voltage | | | | |
| Analog(AVDD) | VA | -0.3 | 4.3 | V |
| Digital(DVDD) | VD | -0.3 | 4.3 | V |
| Digital(DVDD18) | VD18 | -0.3 | 2.5 | V |
| AVSS(BVSS) – DVSS (Note 4) | Δ GNND | | 0.3 | V |
| Input current (except for power supply pin) | IIN | - | \pm 10 | mA |
| Analog input voltage | | | | |
| AINL+, AINL-, AINR+, AINR-, AINL2-8, AINR2-8, AINM VREFH, VREFL | VINA | -0.3 | VA+0.3 | V |
| Digital input voltage | VIND | -0.3 | VD+0.3 | V |
| Operating ambient temperature | Ta | -40 | 85 | °C |
| Storage temperature | Tstg | -65 | 150 | °C |

Note 4. AVSS (BVSS) should be at the same level as DVSS.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these critical conditions.

RECOMMENDED OPERATING CONDITIONS

(AVSS = BVSS = DVSS = 0V: All indicated voltages are with respect to ground.)

| Items | Symbol | min | typ | max | Unit |
|--------------------------|--------|-----|-----|-----|------|
| Power supply voltage | | | | | |
| AVDD | VA | 3.0 | 3.3 | 3.6 | V |
| DVDD | VD | 3.0 | 3.3 | 3.6 | V |
| DVDD18 | VD18 | 1.7 | 1.8 | 2.0 | V |
| Reference voltage (VREF) | | | | | |
| VREFH (Note 5) | VRH | | VA | | V |
| VREFL (Note 6) | VRL | | 0.0 | | V |

Note 5. VREFH normally connects to AVDD.

Note 6. VREFL normally connects to AVSS

Note: The analog input voltage and output voltage are proportional to the VREFH-VREFL voltages.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTRIC CHARACTERISTICS

(1) Analog Characteristics

1) ADC Characteristics

(Unless otherwise specified, Ta = 25°C; AVDD = DVDD = 3.3V, DVDD18=1.8V; VREFH = AVDD, VREFL = AVSS; BITCLK = 64 fs; signal frequency = 1kHz; Measurement bandwidth = 20Hz to 20kHz @ 48kHz, 20Hz ~ 40kHz @ 96kHz; ADC specified with differential inputs (ADC1, ADC2); CKM Mode 1(CKM[2:0]= “000”), SRC RESET)

| | Parameter | min | typ | max | Unit | |
|--|--|--|-------|-------|-------|------|
| Stereo ADC | Resolution | 24 | | | Bits | |
| | Dynamic characteristics | | | | | |
| | S/(N+D) | fs = 48kHz (-1dBFS) (Note 7) | 82 | 92 | | dB |
| | | fs = 96kHz (-1dBFS) | | 90 | | dB |
| | Dynamic range | fs = 48kHz (A filter) (Note 7, Note 8) | 88 | 96 | | dB |
| | | fs = 96kHz | | 93 | | dB |
| | S/N | fs = 48kHz (A filter) (Note 7) | 88 | 96 | | dB |
| | | fs = 96kHz | | 93 | | dB |
| | Inter-channel isolation (f=1kHz) (Note 9) | 90 | 115 | | dB | |
| | DC accuracy | | | | | |
| | Channel gain mismatch | | | 0.1 | 0.3 | dB |
| | Analog input | | | | | |
| | Input voltage (Differential input) (Note 10) | | ±1.85 | ±2.00 | ±2.15 | Vp-p |
| Input voltage (Single-ended input) (Note 11) | | 1.85 | 2.00 | 2.15 | Vp-p | |
| Input impedance (Note 12) | | 22 | 33 | | kΩ | |
| Monaural ADC part | Resolution | 24 | | | Bits | |
| | Dynamic characteristics | | | | | |
| | S/(N+D) | fs = 48kHz (-1dBFS) | 78 | 88 | | dB |
| | | fs = 96kHz (-1dBFS) | | 87 | | dB |
| | Dynamic range | fs = 48kHz (A filter) (Note 8) | 87 | 95 | | dB |
| | | fs = 96kHz | | 92 | | dB |
| | S/N | fs = 48kHz (A filter) | 87 | 95 | | dB |
| | | fs = 96kHz | | 92 | | dB |
| | Analog input | | | | | |
| | Input voltage (Note 13) | | 1.85 | 2.00 | 2.15 | Vp-p |
| Input impedance (Note 14) | | 22 | 33 | | kΩ | |

Note 7. This value is not guaranteed for single-ended inputs.

Note 8. Indicates S/(N+D) when -60 dBFS signal is applied.

Note 9. Indicates isolation between L and R when -1dBFS signal is applied.

Note 10. Target input pins are AINL+, AINL-, AINR+ and AINR-.

Differential full scale is $(\pm FS = (VREFH - VREFL) \times (2.0/3.3))$

Note 11. Target input pins are AINL2~L8, AINR2~R8.,

Single-ended full scale is $(FS = (VREFH - VREFL) \times (2.0/3.3))$

Note 12. Target input pins are AINL+, AINL-, AINR+, AINR-, AINL2-L8, AINR2-R8.

Note 13. Target input pin is AINM, The full scale of this pin is $(FS = (VREFH - VREFL) \times (2.0/3.3))$

Note 14. Target input pin is AINM.

2) SRC Characteristics

($T_a=25^{\circ}\text{C}$; $AVDD = 3.3\text{V}$; $DVDD=3.3\text{V}$; $DVDD18=1.8\text{V}$; data = 24-bits; measurement bandwidth = $20\text{Hz} \sim \text{FSO}/2$; unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Units |
|--|---------|------|------|------|-------|
| Resolution | | | | 24 | Bits |
| Input Sample Rate | FSI | 7.35 | | 96 | kHz |
| Output Sample Rate | FSO | 44.1 | | 96 | kHz |
| THD+N (Input= 1kHz, 0dBFS) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | -113 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | -112 | | dB |
| FSO/FSI=48kHz/44.1kHz | | | -113 | | dB |
| FSO/FSI=48kHz/96kHz | | | -113 | | dB |
| FSO/FSI=48kHz/8kHz | | | -112 | -103 | dB |
| Dynamic Range (Input= 1kHz, -60dBFS) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | 114 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | 114 | | dB |
| FSO/FSI=48kHz/44.1kHz | | | 114 | | dB |
| FSO/FSI=48kHz/96kHz | | | 114 | | dB |
| FSO/FSI=48kHz/8kHz | | 110 | 114 | | dB |
| Dynamic Range (Input= 1kHz, -60dBFS, A-weighted) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | 116 | | dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.45 | | 6 | - |

(2) DC Characteristics

(Ta = -40°C ~ 85°C; AVDD = DVDD = 3.0~3.6V; DVDD18 = 1.7~2.0V)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|----------|-----|---------|------|
| High level input voltage (Note 15) | VIH | 80%DVDD | | | V |
| Low level input voltage (Note 15) | VIL | | | 20%DVDD | V |
| SCL,SDA High level input voltage | VIH | 70%DVDD | | | V |
| SCL,SDA Low level input voltage | VIL | | | 30%DVDD | V |
| High level output voltage Iout=-100μA | VOH | DVDD-0.5 | | | V |
| Low level output voltage Iout=100μA (Note 16) | VOL | | | 0.5 | V |
| SDA Low level output voltage Iout=3mA | VOL | | | 0.4 | V |
| Input leak current (Note 17) | Iin | | | ±10 | μA |
| Input leak current (pull-down) (Note 18) | Iid | | 22 | | μA |
| Input leak current (XTI pin) | Iix | | 26 | | μA |

Note 15. SCL (I2CSEL=1) and SDA pins are not included. (SCLK pin is included when I2CSEL=0)

Note 16. SDA pin is not included.

Note 17. The pull-down pins and XTI pin are not included.

Note 18. The pull-down pins (Typ150kΩ) are: TESTI1, TESTI2

(3) Current Consumption

(Ta=25°C; AVDD=DVDD=3.0~3.6V(typ=3.3V,max=3.6V); DVDD18=1.7~2.0V(typ=1.8V, max=2.0V))

| Power supply | | | | | |
|---|--|-----|-----|-----|------|
| Parameter | | min | typ | max | Unit |
| Power supply current (Note 19) | | | | | |
| 1) a) AVDD | | | 52 | 70 | mA |
| b) DVDD | | | 8 | 15 | mA |
| c) DVDD18 | | | 110 | 165 | mA |
| 2) INIT_RESET = "L" (reference) (Note 20) | | | 1 | | mA |

Note 19. Varies slightly according to the system frequency and contents of the DSP program.

Note 20. This is a reference value when using a crystal oscillator.

Since most of the supply current at the initial reset state is in the oscillator section, the value may vary slightly according to the crystal type and the external circuit. This is a "reference value" only.

(4) Digital Filter Characteristics

1) ADC Section: ADC1, ADC2

($T_a = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$; $AVDD = DVDD = 3.0\text{V} \sim 3.6\text{V}$; $DVDD18 = 1.7\text{V} \sim 2.0\text{V}$; $f_s = 48\text{kHz}$; [Note 21](#))

| Parameter | Symbol | min | typ | max | Unit |
|---|-------------------|------|------------|-------------|---------------|
| Pass band ($\pm 0.005\text{dB}$) (Note 22) (-0.02dB) (-6.0dB) | PB | 0 | | 21.5 | kHz |
| | | | | 21.768 | kHz |
| | | | | 24.00 | kHz |
| Stop band | SB | 26.5 | | | kHz |
| Pass band ripple (Note 22) | PR | | | ± 0.005 | dB |
| Stop band attenuation (Note 23 , Note 24) | SA | 80 | | | dB |
| Group delay distortion | ΔGD | | | 0 | μs |
| Group delay ($T_s = 1/f_s$) | GD | | 29 | | T_s |
| Digital filter + SFC | | | | | |
| Amplitude characteristics (20Hz~20.0kHz) | | | ± 0.01 | | dB |

Note 21. Each parameter is related to the sampling frequency (f_s). HPF response is not included.

Note 22. The pass band is from DC to 21.5kHz at $f_s = 48\text{kHz}$.

Note 23. The stop band is from 26.5kHz to 3.0455MHz at $f_s = 48\text{kHz}$.

Note 24. When $f_s = 48\text{kHz}$, the analog modulator samples the analog input at 3.072MHz. The input signal is not attenuated by the digital filter in multiple bands ($n \times 3.072\text{MHz} \pm 21.99\text{kHz}$; $n=0, 1, 2, 3, \dots$) of the sampling frequency.

2) ADC Section ADCM

($T_a = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$; $AVDD = DVDD = 3.0\text{V} \sim 3.6\text{V}$; $DVDD18 = 1.7\text{V} \sim 2.0\text{V}$; $f_s = 48\text{kHz}$; [Note 25](#))

| Parameter | Symbol | min | typ | max | Unit |
|---|-------------------|------|-----------|-------------|---------------|
| Pass band ($\pm 0.005\text{dB}$) (Note 26) (-0.02dB) (-6.0dB) | PB | 0 | | 21.5 | kHz |
| | | | | 21.768 | kHz |
| | | | | 24.00 | kHz |
| Stop band | SB | 26.5 | | | kHz |
| Pass band ripple (Note 26) | PR | | | ± 0.005 | dB |
| Stop band attenuation (Note 27 , Note 28) | SA | 80 | | | dB |
| Group delay distortion | ΔGD | | | 0 | μs |
| Group delay ($T_s = 1/f_s$) (Note 29) | GD | | 29 | | T_s |
| Digital filter + SFC | | | | | |
| Amplitude characteristics (20Hz~20.0kHz) | | | ± 0.1 | | dB |

Note 25. Each parameter is related to the sampling frequency (f_s). HPF response is not included.

Note 26. The pass band is from DC to 21.5kHz at $f_s = 48\text{kHz}$.

Note 27. The stop band is from 26.5kHz to 3.0455MHz at $f_s = 48\text{kHz}$.

Note 28. When $f_s = 48\text{kHz}$, the analog modulator samples the analog input at 3.072MHz. The input signal is not attenuated by the digital filter in the multiple bands ($n \times 3.072\text{MHz} \pm 21.99\text{kHz}$; $n=0, 1, 2, 3, \dots$) of the sampling frequency.

Note 29. VOL+ MUX path adds one additional T_s .

3) SRC

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V; DVDD18 = 1.7~2.0V)

| Parameter | Range | Symbol | min | typ | max | Unit |
|------------------------------------|---------------------------------|--------|-----------|-----|-----------|------|
| Pass band -0.01dB | $0.980 \leq FSO/FSI \leq 6.000$ | PB | 0 | | 0.4583FSI | kHz |
| | $0.900 \leq FSO/FSI < 0.990$ | PB | 0 | | 0.4167FSI | kHz |
| | $0.533 \leq FSO/FSI < 0.909$ | PB | 0 | | 0.2182FSI | kHz |
| | $0.490 \leq FSO/FSI < 0.539$ | PB | 0 | | 0.2177FSI | kHz |
| | $0.450 \leq FSO/FSI < 0.495$ | PB | 0 | | 0.1948FSI | kHz |
| Stop band | $0.980 \leq FSO/FSI \leq 6.000$ | SB | 0.5417FSI | | | kHz |
| | $0.900 \leq FSO/FSI < 0.990$ | SB | 0.5021FSI | | | kHz |
| | $0.533 \leq FSO/FSI < 0.909$ | SB | 0.2974FSI | | | kHz |
| | $0.490 \leq FSO/FSI < 0.539$ | SB | 0.2812FSI | | | kHz |
| | $0.450 \leq FSO/FSI < 0.495$ | SB | 0.2604FSI | | | kHz |
| Pass band ripple | | PR | | | ±0.01 | dB |
| Stop band attenuation | | SA | 95.2 | | | dB |
| Group delay (Ts=1/fs) (Note 30) | | GD | | 56 | | Ts |

Note 30. Measured from the rising edge of SRC_LRCK on the input to the rising edge of LRCLK_O on the output, with there is no phase difference between input and output.

(5) Switching Characteristics

[#h means hexadecimal code. (#=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)]

1) System Clock

(Ta = -40~85°C; AVDD=DVDD=3.0V~3.6V; DVDD18 = 1.7V~2.0V)

| Parameter | Symbol | min | typ | max | Unit |
|--------------------------------------|--------|------|-------------------|------|------|
| XTI CKM[2:0] 0h,1h,2h,3h | | | | | |
| a) with a crystal oscillator: | | | | | |
| CKM[2:0]=0h,2h | fXTI | - | 11.2896 12.288 | - | MHz |
| CKM[2:0]=1h,3h | fXTI | - | 16.9344 18.432 | - | MHz |
| b) with an external clock | | | | | |
| Duty cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=0h,2h | fXTI | 11.0 | | 12.4 | MHz |
| CKM[2:0]=1h,3h | fXTI | 16.5 | | 18.6 | MHz |
| Clock rise time | tCR | | | 6 | ns |
| Clock fall time | tCF | | | 6 | ns |
| LRCLK_I frequency (Note 31) | fs | 7.35 | 48 | 96 | kHz |
| Clock rise time | tLR | | | 6 | ns |
| Clock fall time | tLF | | | 6 | ns |
| BITCLK_I frequency | | | | | |
| High level width | tBCLKH | 64 | | | ns |
| Low level width | tBCLKL | 64 | | | ns |
| Clock rise time | tBR | | | 6 | ns |
| Clock fall time | tBF | | | 6 | ns |
| a) CKM[2:0]=2h,3h | | | | | |
| | fBCLK | - | 64 | - | fs |
| Duty cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=2h,3h | | 0.23 | | 6.2 | MHz |
| b) CKM[2:0]=4h,5h (Note 32) | | | | | |
| | fBCLK | - | 64 | - | fs |
| Duty cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=4h | fBCLK | 2.75 | | 3.1 | MHz |
| CKM[2:0]=5h | fBCLK | 5.5 | | 6.2 | MHz |

Note 31. LRCLK and sampling rate (fs) should match.

Note 32. When BITCLK_I uses as a resource of master clock, it should be 64 clocks correctly divided within 1fs.

(Ta = -40°C ~85°C; AVDD=DVDD=3.0~3.6V, DVDD18 = 1.7~2.0V)

| Parameter | Symbol | min | typ | max | Unit |
|-------------------------------------|-----------------|------|-----|-----|------|
| SRC_LRCK frequency (Note 33) | fs | 7.35 | 48 | 96 | kHz |
| Clock rise time | tLR | | | 6 | ns |
| Clock fall time | tLF | | | 6 | ns |
| SRC_BICK frequency | | | | | |
| High level width | tBCLKH | 60 | | | ns |
| Low level width | tBCLKL | 60 | | | ns |
| Clock rise time | tBR | | | 6 | ns |
| Clock fall time | tBF | | | 6 | ns |
| | (Note 34) fBCLK | 32 | | 128 | fs |
| Duty factor | | 40 | 50 | 60 | % |
| | | 0.23 | | 6.2 | MHz |

Note 33. SRC_LRCK and sampling rate (fs) should match.

Note 34. 128fs is up to fs = 48kHz.

2) Reset

(Ta=-40°C ~85°C; AVDD=DVDD=3.0~3.6V; DVDD18 = 1.7~2.0V)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| $\overline{\text{INIT_RESET}}$ (Note 35) | tRST | 600 | | | ns |
| $\overline{\text{P_CKRST}}$ | tRST | 600 | | | ns |
| $\overline{\text{P_ADRST}}$ | tRST | 600 | | | ns |
| $\overline{\text{P_DSRST}}$ | tRST | 600 | | | ns |
| $\overline{\text{P_SRCRST}}$ | tRST | 600 | | | ns |

Note 35. "L" is acceptable when power is turned on, but a stable master clock must present before transitioning to "H".

3) Audio interface

3-1) SDIN1~SDIN5,SDOUT1~SDOUT6,SDOUTA1 (Up to fs = 96kHz)

AKM Normal and I²S Compatible Format

(Ta = -40°C~85°C; AVDD=DVDD=3.0~3.6V, DVDD18 = 1.7~2.0V, CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| Slave mode CKM[2:0]=2h, 3h, 4h, 5h | | | | | |
| Delay time from BITCLK_I "↑" to LRCLK_I (Note 36) | tBLRD | 20 | | | ns |
| Delay time from LRCLK_I to BITCLK_I "↑" (Note 36) | tLRBD | 20 | | | ns |
| Delay time from LRCLK_I, LRCLK_O to serial data output | tLRD | | | 40 | ns |
| Delay time from BITCLK_I, BITCLK_O to serial data output | tBSOD | | | 40 | ns |
| Serial data input latch setup time | tBSIDS | 40 | | | ns |
| Serial data input latch hold time | tBSIDH | 40 | | | ns |
| Master mode CKM[2:0]=0h, 1h | | | | | |
| BITCLK_O frequency | fBCLK | | 64 | | fs |
| BITCLK_O duty cycle | | | 50 | | % |
| Delay time from BITCLK_O "↓" to LRCLK_O | tBLRD | -20 | | 40 | ns |
| Delay time from LRCLK_O to serial data output | tLRD | | | 40 | ns |
| Delay time from BITCLK_O to serial data output | tBSOD | | | 40 | ns |
| Serial data input latch setup time | tBSIDS | 40 | | | ns |
| Serial data input latch hold time | tBSIDH | 40 | | | ns |

Note 36. LRCLK_I edge and BITCLK_I "↑" edge cannot be synchronous.

3-2) SDIN1(SRCI Input) (Up to fs = 96kHz)

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V, DVDD18 = 1.7~2.0V)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| Slave mode | | | | | |
| Delay time from SRC_BICK "↑" to SRC_LRCK (Note 37) | tBLRD | 20 | | | ns |
| Delay time from SRC_LRCK to SRC_BICK "↑" (Note 37) | tLRBD | 20 | | | ns |
| Serial data input latch setup time | tBSIDS | 40 | | | ns |
| Serial data input latch hold time | tBSIDH | 40 | | | ns |

Note 37. SRC_BICK edge and SRC_LRCK edge cannot be synchronous.

3) Microcontroller Interface

($T_a = -40 \sim 85^\circ\text{C}$; $AVDD=DVDD=3.0\text{V} \sim 3.6\text{V}$, $DVDD18 = 1.7 \sim 2.0\text{V}$, $CL = 20\text{pF}$)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| Microcomputer interface signal | | | | | |
| $\overline{\text{RQ}}$ Fall time | tWRF | | | 30 | ns |
| $\overline{\text{RQ}}$ Rise time | tWRR | | | 30 | ns |
| SCLK fall time | tSF | | | 30 | ns |
| SCLK rise time | tSR | | | 30 | ns |
| SCLK frequency | fSCLK | | | 2.1 | MHz |
| SCLK low level width | tSCLKL | 200 | | | ns |
| SCLK High level width | tSCLKH | 200 | | | ns |
| Microcomputer to AK7780 | | | | | |
| Time from $\overline{\text{P_DSPRST}}$, $\overline{\text{P_ADRST}}$ “ \downarrow ” to $\overline{\text{RQ}}$ “ \downarrow ” | tREW | 500 | | | ns |
| Time from $\overline{\text{RQ}}$ “ \uparrow ” to $\overline{\text{P_DSPRST}}$, $\overline{\text{P_ADRST}}$ “ \uparrow ” | tWRE | 500 | | | ns |
| $\overline{\text{RQ}}$ high level width | tWRQH | 500 | | | ns |
| Time from $\overline{\text{RQ}}$ “ \downarrow ” to SCLK “ \downarrow ” | tWSC | 500 | | | ns |
| Time from SCLK “ \uparrow ” to $\overline{\text{RQ}}$ “ \uparrow ” | tSCW | 800 | | | ns |
| SI latch setup time | tSIS | 200 | | | ns |
| SI latch hold time | tSIH | 200 | | | ns |
| AK7780 to Microcomputer | | | | | |
| Delay time from SCLK “ \downarrow ” to SO output | tSOS | | | 300 | ns |
| Hold time from SCLK “ \uparrow ” to SO output (Note 38) | tSOH | 200 | | | ns |
| Time from $\overline{\text{RQ}}$ “ \downarrow ” to SO Hi-Z ($I_{\text{out}} = \pm 360\mu\text{A}$) release | tRQHR | | | 600 | ns |
| $\overline{\text{RQ}}$ “ \uparrow ” to SO Hi-Z set ($I_{\text{out}} = \pm 360\mu\text{A}$) | tRQHS | | | 600 | ns |

Note 38. Except last 1bit of the command code.

4) I2C BUS Interface

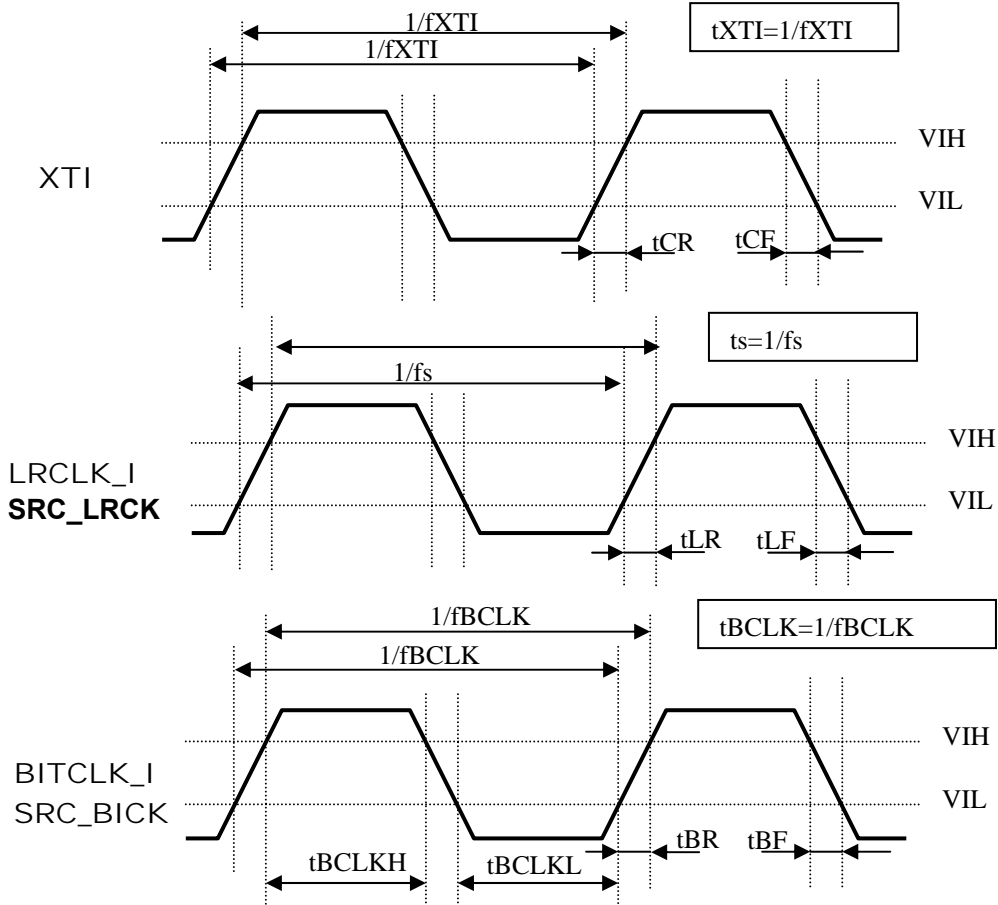
(Ta = -40°C~85°C; AVDD=DVDD=3.0~3.6V, DVDD18 = 1.7~2.0V)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|---------|-----|-----|-----|------|
| I²C Timing | | | | | |
| SCL clock frequency | fSCL | | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | | μs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | | | μs |
| Clock Low Time | tLOW | 1.3 | | | μs |
| Clock High Time | tHIGH | 0.6 | | | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | | μs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | | 0.9 | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | | μs |
| Rise Time of Both SDA and SCL Lines | tR | | | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | | μs |
| Pulse Width of Spike Noise Suppressed By Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | | | 400 | pF |

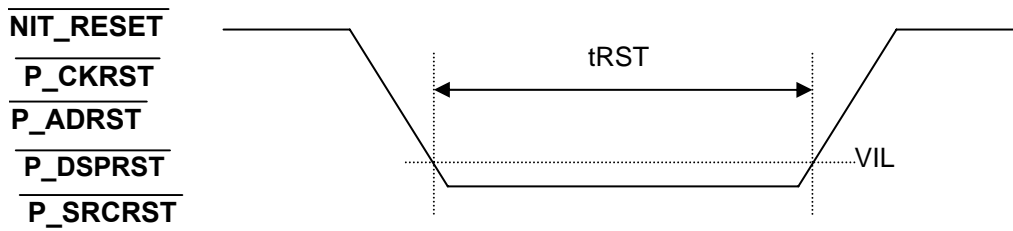
Note 39. I²C is a registered trademark of Philips Semiconductors.

(6) Timing Diagram

1) System clock

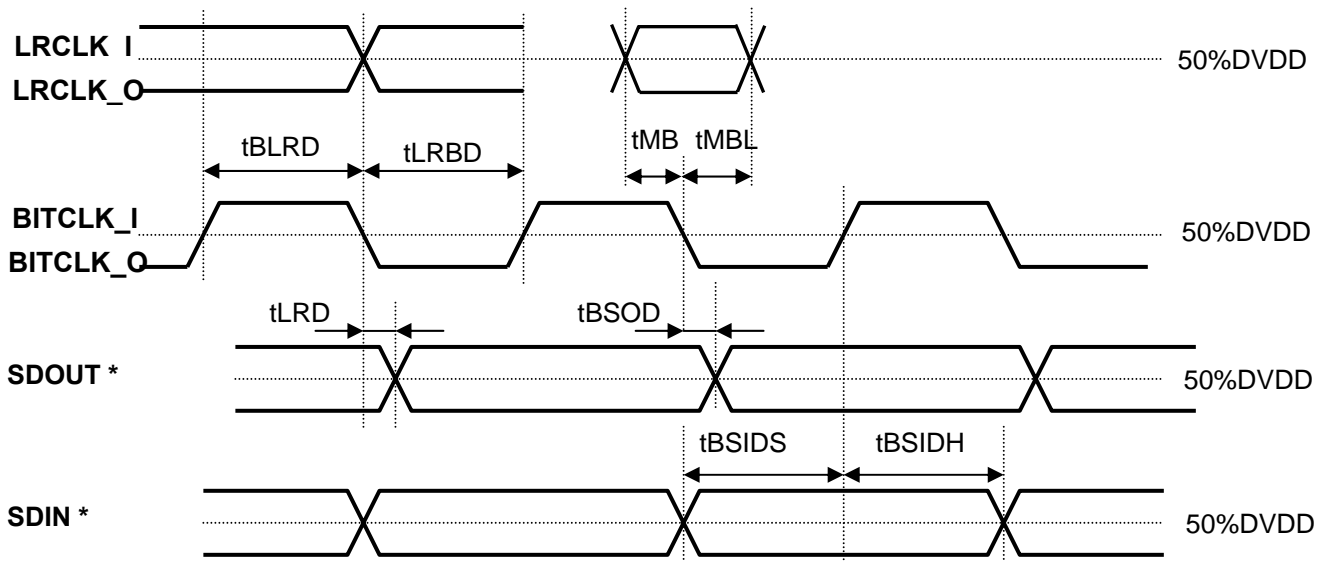


2) RESET



3) Audio Interface

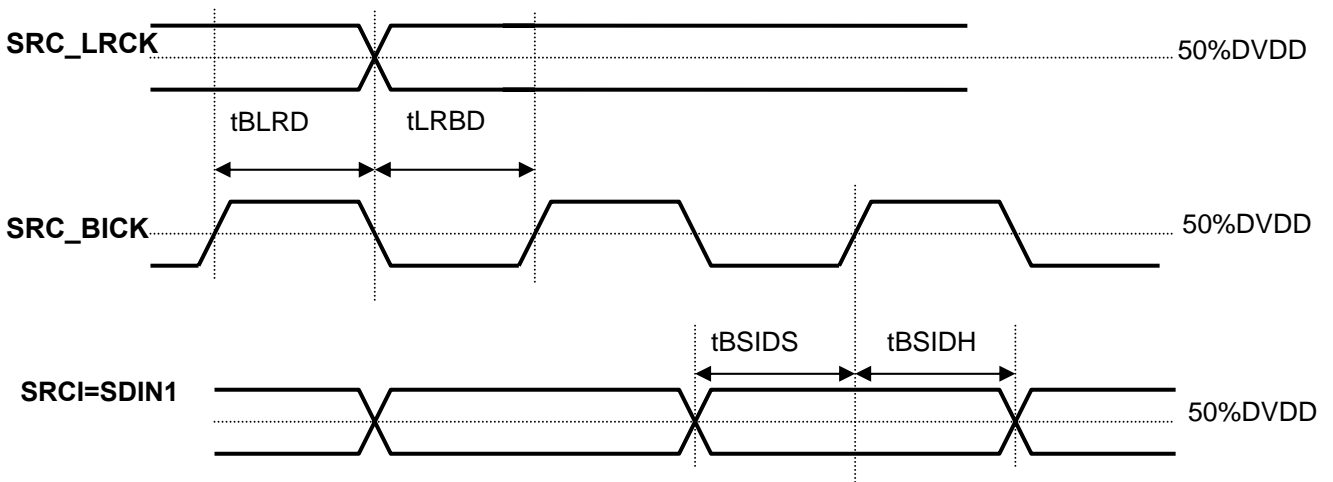
① Normal and I²S compatible format



SDIN * =SDIN1, SDIN2, SDIN3, SDIN4, SDIN5

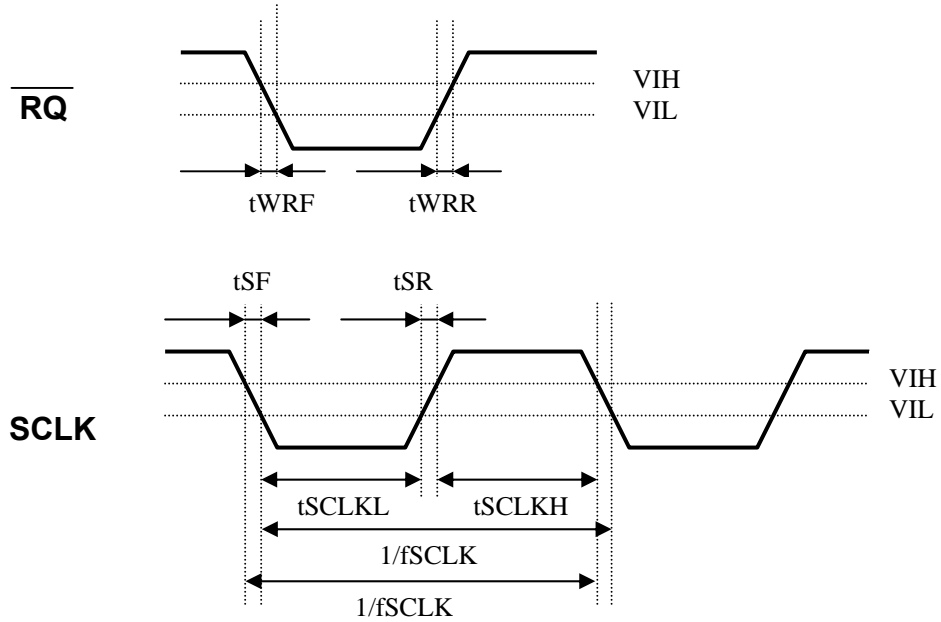
SDOUT * =SDOUT1, SDOUT2, SDOUT3, SDOUT4, SDOUT5, SDOUT6, SDOUTA1

② SRC

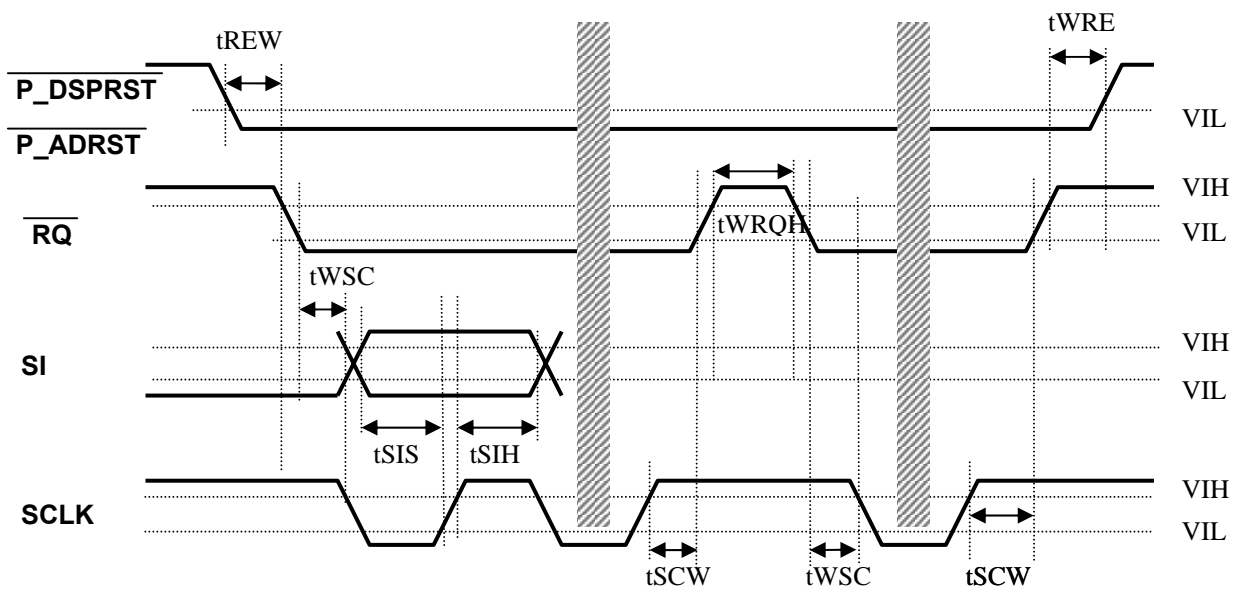


4) Microcontroller Interface

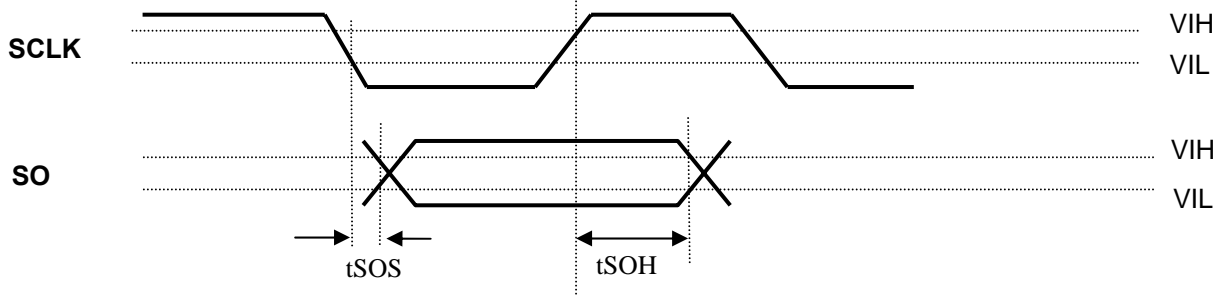
◆ Microcontroller interface



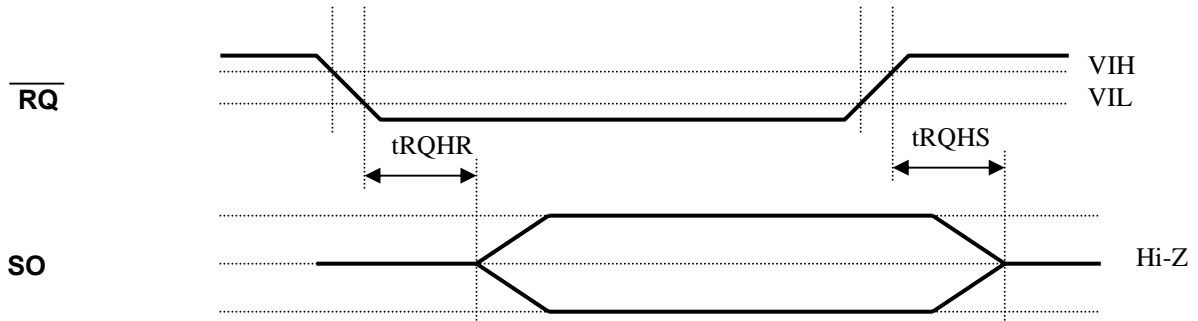
◆ Microcontrollerr → AK7780



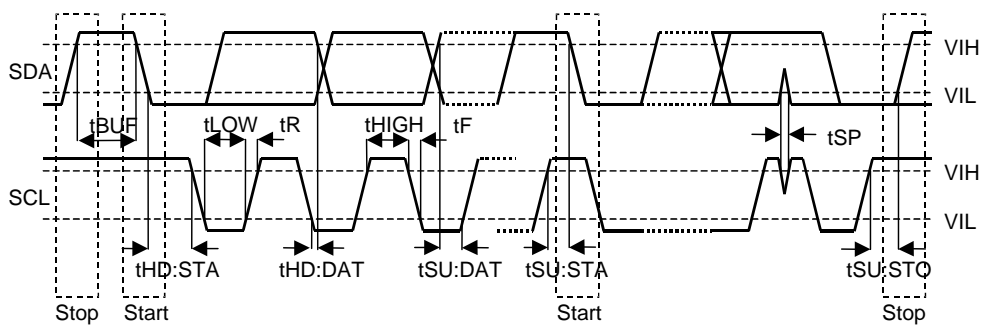
◆ AK7780 → Microcontroller



Note: Timing during the RUN state is identical, except that $\overline{P_DSPRST}$ and $\overline{P_ADRST}$ are “H”.

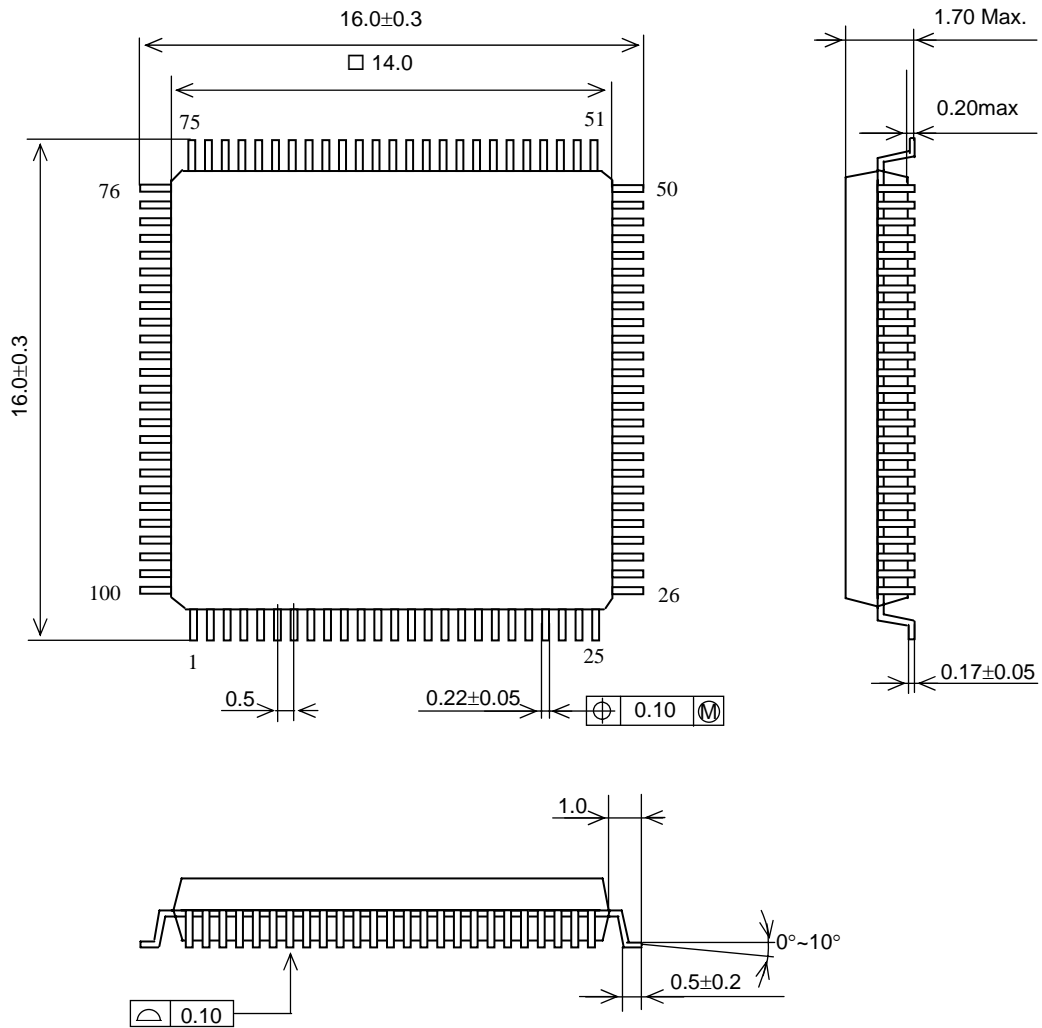


5) I²C Bus Interface



PACKAGE

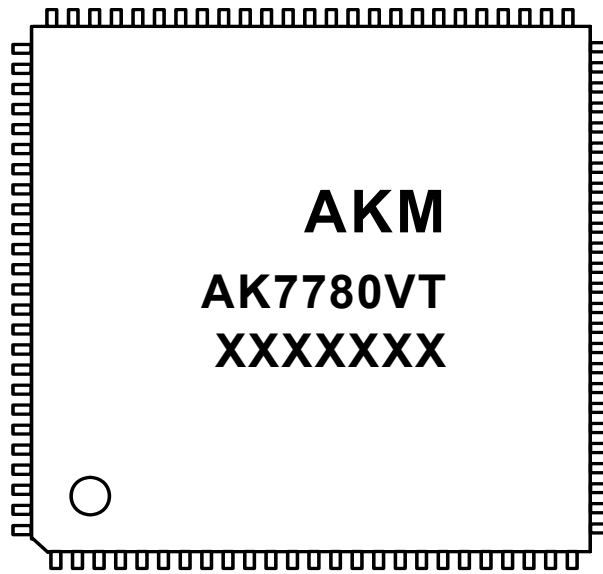
- 100 pin LQFP (Unit: mm)



■ **Material & Lead finish**

Package: Epoxy
 Lead-frame: Cu
 Lead-finish: Solder (Pb free) plate

MARKING



- 1) Pin #1 indication
- 2) Date Code: XXXXXXX(7digits)
- 3) Marking Code: AK7780VT
- 4) Asahi Kasei Logo

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