

[Stereo ADC, Common for ADC1 and ADC2]

- 24-bit 2ch x 2
- S/(N+D): 90dB (fs=48kHz)
- D-range: 96dBA (fs=48kHz)
- S/N: 96dBA (fs=48kHz)
- 8ch bidirectional analog input selector
- High-pass filter (HPF) for DC offset cancellation
- fs=7.35kHz ~ 96kHz

[Mono ADC]

- 24bit 1ch
- S/(N+D) 88dB (fs=48kHz)
- D-range 95dBA (fs=48kHz)
- S/N 95dBA (fs=48kHz)
- High-pass filter (HPF) for DC offset cancellation
- fs=7.35kHz ~ 96kHz
- Digital volume control

[DSP1/DSP2 In/Output Digital Interface]

- Serial Data Input: 14ch (including ADC block)
- Serial Data Output: 16ch (each DSP outputs are 14ch)
- Microcomputer Interface: 1ch In/Out or I²C-bus

[SRC, Common for SRC1 and SRC2]

- 2ch x 2
- fs=7.35kHz ~ 96kHz

[General]

- PLL
- 3.3V±0.3V, 1.8V ±0.1V
- Operational Temperature: -40°C ~ 85°C
- 100pin LQFP

■ Block Diagram

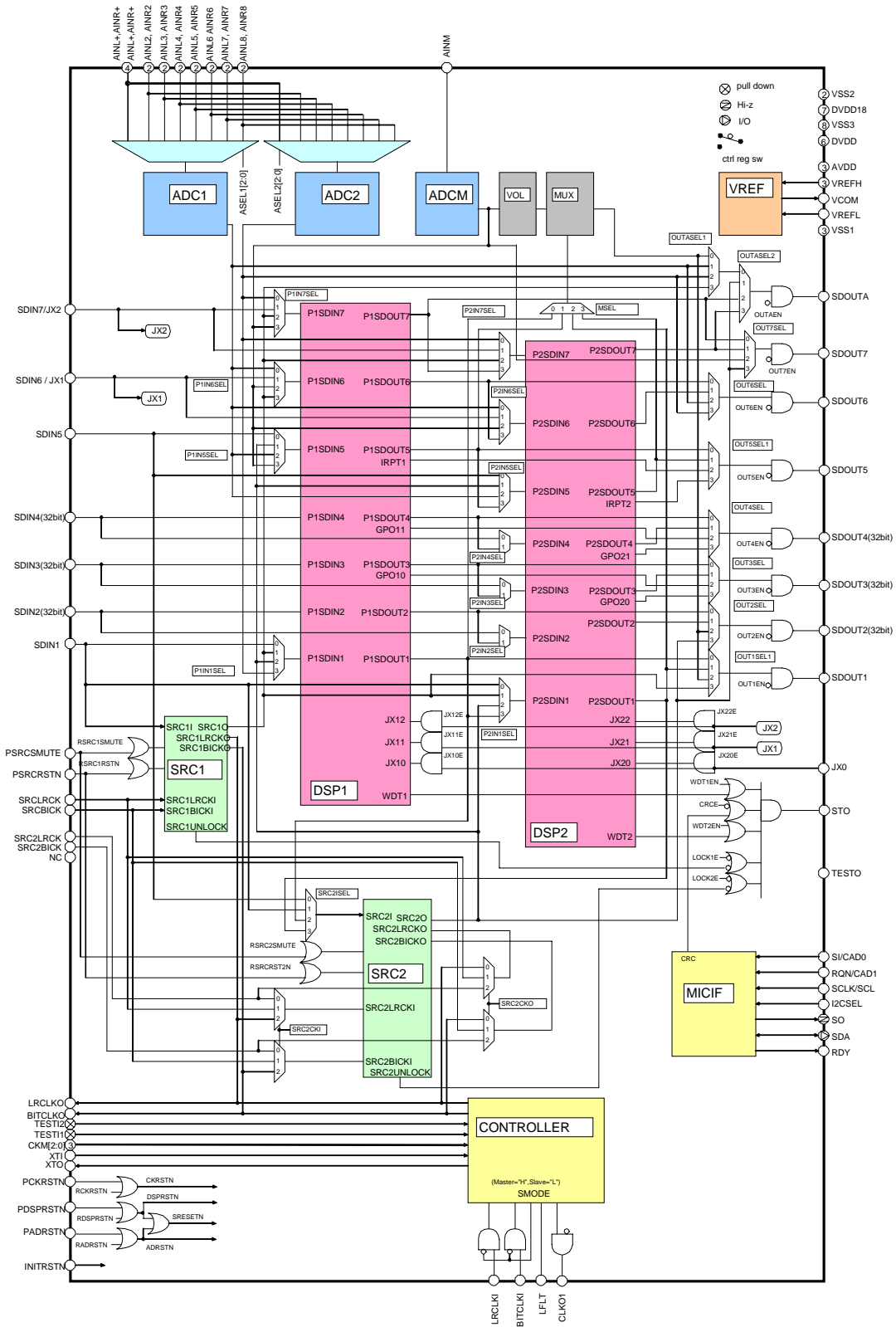
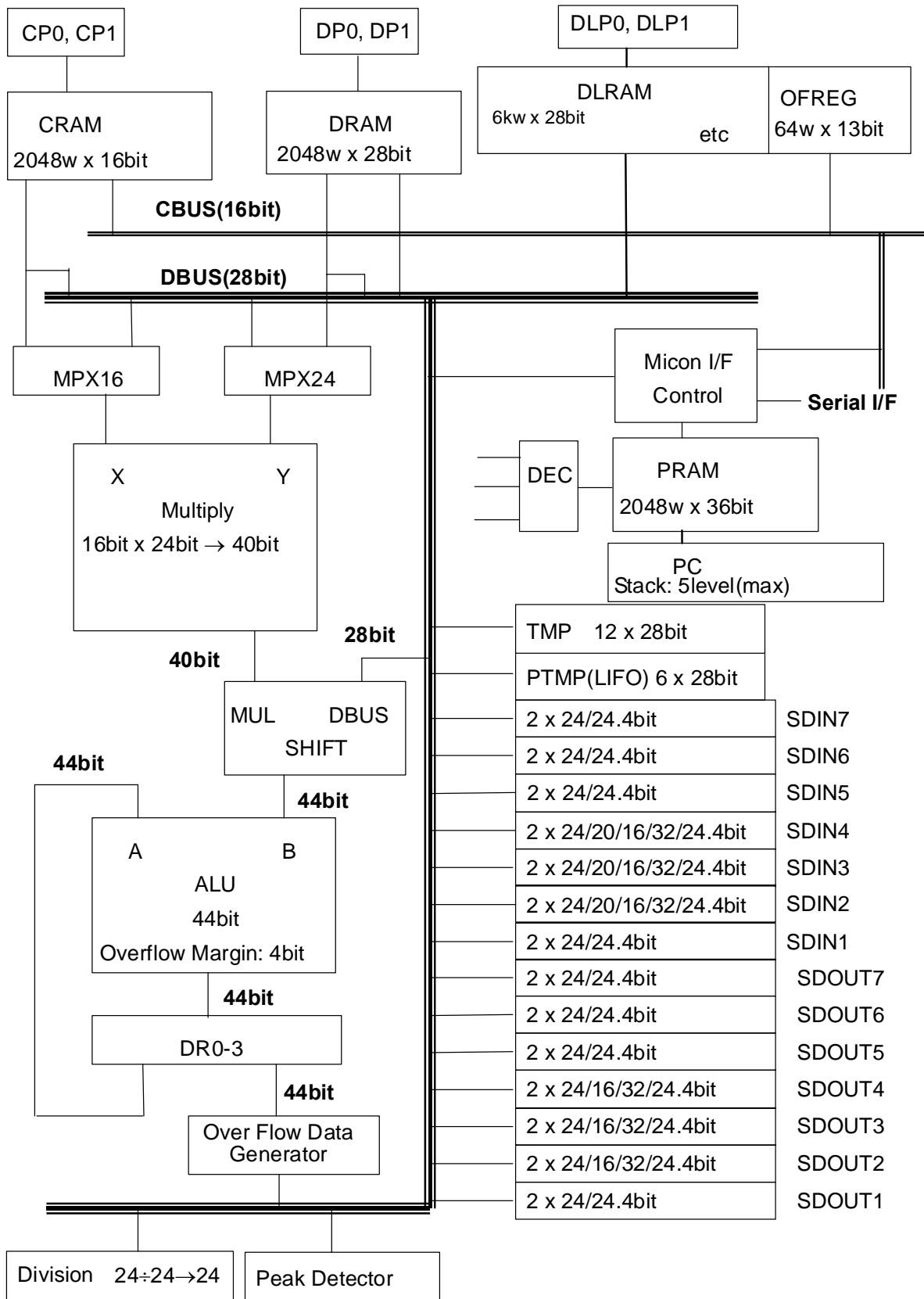


Figure 1. Block Diagram

■ DSP Block Diagram (Common for DSP1 and DSP2)



■ Ordering Guide

AK7782VQ
AKD7782

-40 ~ +85°C 100pin LQFP (0.5mm pitch)
Evaluation Board for AK7782

■ Pin Layout

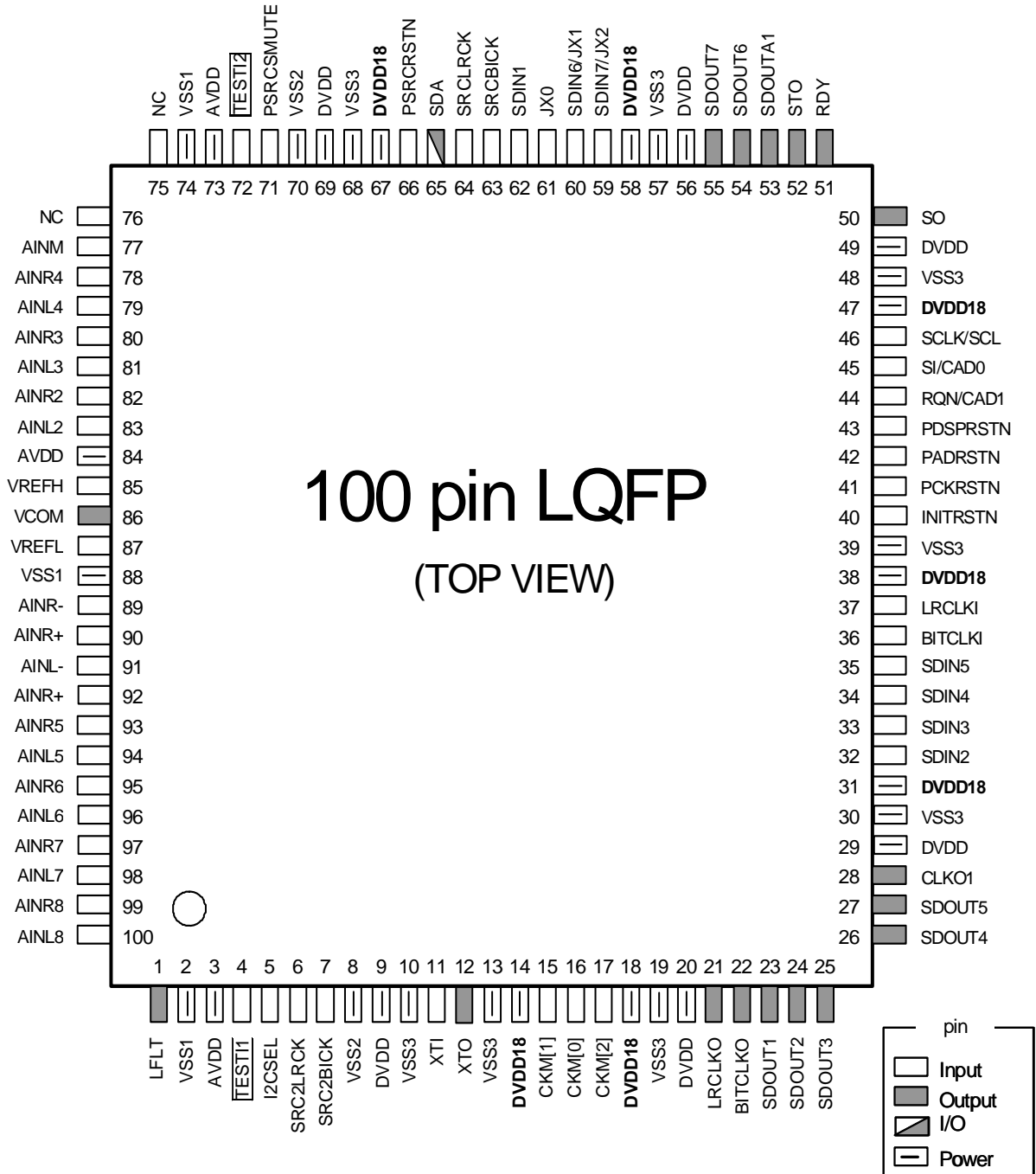


Figure 2. Pin Layout

| PIN/FUNCTION | | | | |
|--------------|----------|-----|---|-------------------------|
| No. | Pin Name | I/O | Function | Classification |
| 1 | LFLT | O | Filter Connection Pin for AK7782 Core PLL When using the PLL function, connect with R (1.5kΩ) and C (47nF) in series and connected to analog ground (VSS1) | Analog Output |
| 2 | VSS1 | - | Ground Pin 0V (silicon board potential) | Power Supply |
| 3 | AVDD | - | Power Supply Pin for Analog Block 3.3V (typ) | |
| 4 | TEST11 | I | Test Pin (Internal pull-down) Connect to VSS3 | Test |
| 5 | I2CSEL | I | I ² C-bus Select Pin “L”: Normal Microcomputer Interface “H”: I ² C-bus selected mode. SCL and SDA are active. I2CSEL must be fixed to “L” (VSS3) or “H” (DVDD). | I ² C Select |
| 6 | SRC2LRCK | I | LR Clock Input Pin for SRC2 | SRC2 |
| 7 | SRC2BICK | I | BIT Clock Input Pin for SRC2 | |
| 8 | VSS2 | - | Ground Pin (silicon board potential) Connect to VSS1 | Power Supply |
| 9 | DVDD | - | Power Supply Pin for Digital Block 3.3V (typ) | Digital Power Supply |
| 10 | VSS3 | - | Ground Pin 0V | Power Supply |
| 11 | XTI | I | Crystal Oscillator Input Pin Connect a crystal oscillator between the XTI pin and XTO pin or input an external clock into the XTI pin when not using a crystal oscillator. | System Clock |
| 12 | XTO | O | Crystal Oscillator Output Pin Connect a crystal oscillator between the XTI pin and XTO pin or leave open when using an external clock source. | |
| 13 | VSS3 | - | Ground Pin 0V | Power Supply |
| 14 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | Mode Select |
| 15 | CKM [1] | I | Clock Mode Select Pin | |
| 16 | CKM [0] | I | Clock Mode Select Pin | |
| 17 | CKM [2] | I | Clock Mode Select Pin | |
| 18 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | Digital Power Supply |
| 19 | VSS3 | - | Ground Pin 0V | Power Supply |
| 20 | DVDD | - | Power Supply Pin for Digital Block 3.3V (typ) | |

| No. | Pin Name | I/O | Function | Classification |
|-----|----------|-----|---|-------------------------------------|
| 21 | LRCLKO | O | LR Channel Select Pin Master mode: Outputs 1fs clock. Slave mode: Outputs LRCLKI clock. | System Clock |
| 22 | BITCLKO | O | Serial bit Clock Output Pin Master mode: Outputs 64fs clock. Slave mode: Outputs BITCLKI clock | |
| 23 | SDOUT1 | O | DSP Serial Data Output Pin Outputs "L" during initial reset. The output data is selected by CONT7 D3, D2. | Digital Block Serial Data Output |
| 24 | SDOUT2 | O | DSP Serial Data Output Pin Outputs "L" during initial reset. The output data is selected by CONT7 D5, D4. | |
| 25 | SDOUT3 | O | DSP Serial Data Output Pin Outputs "L" during initial reset. The output data is selected by CONT7 D7, D6. | |
| 26 | SDOUT4 | O | DSP Serial Data Output Pin Outputs "L" during initial reset. The output data is selected by CONT6 D1, D0. | |
| 27 | SDOUT5 | O | DSP Serial Data Output Pin Outputs "L" during initial reset. The output data is selected by CONT6 D3, D2. | |
| 28 | CLKO1 | O | Clock Output Pin 1 Output frequency can be set by control registers. Outputs "L" during initial reset. | Clock Output |
| 29 | DVDD | - | Power Supply Pin for Digital Block 3.3V (typ) | Digital Power Supply |
| 30 | VSS3 | - | Ground Pin 0V | Power Supply |
| 31 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | |
| 32 | SDIN2 | I | DSP Serial Data Input Pin Supports floating point input F24.4: MSB 32-bit and 24-bit / LSB 24-bit, 20-bit and 16-bit. Connect to VSS3 when this pin is not used. | Digital Block Serial Data Input |
| 33 | SDIN3 | I | DSP Serial Data Input Pin Supports floating point input F24.4: MSB 32-bit and 24-bit / LSB 24-bit, 20-bit and 16-bit. Connect to VSS3 when this pin is not used. | |
| 34 | SDIN4 | I | DSP Serial Data Input Pin Supports floating point input F24.4: MSB 32-bit and 24-bit / LSB 24-bit, 20-bit and 16-bit. Connect to VSS3 when this pin is not used. | |
| 35 | SDIN5 | I | DSP Serial Data Input Pin Supports floating point input F24.4: MSB 24-bit / LSB 24-bit, 20-bit and 16-bit. Connect to VSS3 when this pin is not used. | Digital Block Serial Data Input |

| No. | Pin Name | I/O | Function | Classification |
|-----|----------|-----|---|----------------------|
| 36 | BITCLKI | I | Serial bit Clock input Pin | System Clock |
| 37 | LRCLKI | I | LR channel select Input Pin | |
| 38 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | Digital Power Supply |
| 39 | VSS3 | - | Ground Pin 0V | Power Supply |
| 40 | INTRSTN | I | Initial Reset N Pin (for device initialization) The AK7782 is initialized by the INTRSTN pin = "L". This pin must be "L" upon power-up the AK7782. CKM[2:0] Pin settings can be change when the INTRSTN pin = "L". | Reset |
| 41 | PCKRSTN | I | Clock Reset N Pin The internal clock is reset by the PCKRSTN pin = "L". Setting of CKM[2:0] can be changed by the PCKRSTN pin = "L", even if the INTRSTN pin is "H". | |
| 42 | PADRSTN | I | ADC Reset N Pin ADC1, ADC2 and ADCM are reset by the PADRSTN pin = "L". Control register RADRSTN bit= "0" can also reset these blocks. The AK7782 is in system reset state when PADRSTN and PDSRSTN pins = "L". | |
| 43 | PDSRSTN | I | DSP Reset N Pin DSP1 and DSP2 are reset by the PDSRSTN= "L". Control Register RDSRE bit = "0" can also reset these blocks . The AK7782 is in system reset state when PADRSTN and PDSRSTN pins = "L". | |
| 44 | RQN | I | Microcomputer Interface Request N Pin (I2CSEL= "L") Set this pin to "H" during initial reset or when not interfacing to a microcomputer. | Microcomputer I/F |
| | CAD1 | I | I ² C-bus Address Pin 1 (I2CSEL= "H") | I ² C |
| 45 | SI | I | Serial Data Input Pin for Microcomputer Interface (I2CSEL= "L") Set this pin to "L" when not used. | Microcomputer I/F |
| | CAD0 | I | I ² C-bus address Pin 0 (I2CSEL= "H") | I ² C |
| 46 | SCLK | I | Serial Data Clock Pin for Microcomputer Interface (I2CSEL= "L") Set this pin to "H" when there is no clock input. | Microcomputer I/F |
| | SCL | I | SCL I ² C-bus Interface Pin (I2CSEL= "H") | I ² C |
| 47 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | Digital Power Supply |
| 48 | VSS3 | - | Ground Pin 0V | Power Supply |
| 49 | DVDD | - | Power Supply Pin for Digital Block 3.3V (typ) | Digital Power Supply |
| 50 | SO | O | Serial Data Output Pin for Microcomputer Interface Outputs "Hi-z" when the RQN pin = "H". Outputs "Hi-z" during initial reset. | Microcomputer I/F |

| No. | Pin Name | I/O | Function | Classification |
|-----|------------|-----|---|-------------------------------------|
| 51 | RDY | O | Data write ready Pin for Microcomputer Interface | Microcomputer I/F |
| 52 | STO | O | Status Output Pin “H”: Normal operation “L”: WDT, CRC error or SRCUNLOCK status (Figure 1) Outputs “H” during initial reset. | Status |
| 53 | SDOUTA1 | O | Serial Data Output Pin Supports MSB 24-bit. Outputs “L” during initial reset. | Digital Block Serial Data Output |
| 54 | SDOUT6 | O | Serial Data Output Pin Supports MSB 24-bit. Outputs “L” during initial reset. | |
| 55 | SDOUT7 | O | Serial Data Output Pin Supports MSB 24-bit. Outputs “L” during initial reset. | |
| 56 | DVDD | - | Power Supply Pin for Digital Block 3.3V (typ) | Digital Power Supply |
| 57 | VSS3 | - | Ground Pin 0V | Power Supply |
| 58 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | Digital Power Supply |
| 59 | SDIN7 | I | DSP Serial Data Input Pin Connect to VSS3 when this pin is not used. This pin supports 24-bit MSB justified, floating point F24.4. | Digital Block Serial Data Input |
| | JX2 | I | Conditional Jump Pin Connect to VSS3 when this pin is not used. | Condition |
| 60 | SDIN6 | I | DSP Serial Data Input Pin Connect to VSS3 when this pin is not used. This pin supports 24-bit MSB justified, floating point F24.4. | Digital Block Serial Data Input |
| | JX1 | I | Conditional Jump Pin Connect to VSS3 when this pin is not used. | Condition |
| 61 | JX0 | I | Conditional Jump Pin Connect to VSS3 when this pin is not used. | Condition |
| 62 | SDIN1 | I | DSP/SRC Serial Data Input Pin Connect to VSS3 when this pin is not used. This pin supports 24-bit MSB justified, floating point F24.4. | Digital Block Serial Data Input |
| 63 | SRCBICK | I | SRC Serial bit Clock Input Pin | SRC1 |
| 64 | SRCLRCK | I | SRC LR channel Select Input Pin | |
| 65 | SDA | O | I2CSEL Pin = “L” Outputs “L”. | I ² C |
| | | I/O | I2CSEL Pin = “H” SDA I ² C-bus Interface | |
| 66 | PSRCRSTN | I | SRC Reset N Pin SRC1 and SRC2 blocks are reset by the PSRCRSTN pin = “L”. Control register RSRCCRSTN bit = “0” can also reset these blocks. | Reset |
| 67 | DVDD18 | - | Power Supply Pin for Digital Block 1.8V (typ) | Digital Power Supply |
| 68 | VSS3 | - | Ground Pin 0V | Power Supply |
| 69 | DVDD | - | Power Supply Pin for Digital Block 3.3V (typ) | Digital Power Supply |
| 70 | VSS2 | - | Ground Pin 0V (silicon board potential) Connect to VSS1. | Power Supply |
| 71 | PSRC SMUTE | I | SRC Soft Mute Pin SRC1 and SRC2 blocks are soft muted by the PSRCSMUTE pin = “H”. Control register RSRCSMUTE bit = “1” can also soft mutes these blocks. | SRC |

| No. | Pin Name | I/O | Function | Classification |
|-----|----------|-----|--|---------------------|
| 72 | TESTI2 | I | Test Pin (Internal pull-down) Connect to VSS3. | Test |
| 73 | AVDD | - | Power Supply Pin for Analog Block 3.3V (typ) | Analog Power Supply |
| 74 | VSS1 | - | Ground Pin 0V (silicon board potential) | Power Supply |
| 75 | NC | - | NC Pin Connect to VSS1. | NC |
| 76 | NC | - | NC Pin Connect to VSS1. | NC |
| 77 | AINM | I | ADCM Mono Single-ended Input Pin | Analog Input |
| 78 | AINR4 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 79 | AINL4 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |
| 80 | AINR3 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 81 | AINL3 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |
| 82 | AINR2 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 83 | AINL2 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |
| 84 | AVDD | - | Power Supply Pin for analog Block 3.3V (typ) | Analog Power Supply |
| 85 | VREFH | I | Reference voltage Input Pin for analog Block Connect this pin to AVDD, and connect a 0.1 μ F and 10 μ F capacitors between this pin and VSS1. | Analog Input |
| 86 | VCOM | O | Common voltage Output Pin for analog Block Connect a 0.1 μ F and 10 μ F capacitors between this pin and VSS1. Do not connect to external circuits. | Analog Output |
| 87 | VREFL | I | Reference voltage input Pin for analog Block Normally, this pin is connected to VSS1. | Analog Input |
| 88 | VSS1 | - | Ground Pin 0V (silicon board potential) | Power Supply |
| 89 | AINR- | I | Rch Differential Input Pin for ADC1 or ADC2 | Analog Input |
| 90 | AINR+ | I | Rch Differential Input Pin for ADC1 or ADC2 | |
| 91 | AINL- | I | Lch Differential Input Pin for ADC1 or ADC2 | |
| 92 | AINL+ | I | Lch Differential Input Pin for ADC1 or ADC2 | |
| 93 | AINR5 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 94 | AINL5 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |
| 95 | AINR6 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 96 | AINL6 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |
| 97 | AINR7 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 98 | AINL7 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |
| 99 | AINR8 | I | Rch Single-ended Input Pin for ADC1 or ADC2 | |
| 100 | AINL8 | I | Lch Single-ended Input Pin for ADC1 or ADC2 | |

Note 1. All digital input pins must not be allowed to float.

Note 2. If analog input pins (AINR-, AINR+, AINL-, AINL+, AINL2~8, AINR2~8, AINM) are not used, leave them open.

Note 3. The I2CSEL pin should be fixed to "L" (VSS3) or "H" (DVDD).

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

| | Pin Name | Setting |
|---------|--|-----------------|
| Analog | AINL+, AINL-, AINR+, AINR-, AINL2, AINR2, AINL3, AINR3, AINL4, AINR4, AINL5, AINR5, AINL6, AINR6, AINL7, AINR7, AINL8, AINR8, AINM | Leave Open |
| Digital | XTO, LRCLKO, BITCLKO, SDOUT1, SDOUT2, SDOUT3, SDOUT4, SDOUT5, CLK01, SO, RDY, STO, SDOTUA1, SDOUT6, SDOUT7, SDA (I2CSEL="L") | Leave Open |
| | TESTI1, SRC2LRCK, SRC2BICK, XTI, SDIN2, SDIN3, SDIN4, SDIN5, PCKRSTN, PADRSTN, SDIN7/JX2, SDIN6/JX1, JX0, SDIN1, SRCBICK, SRCLRCK, PSRCRSTN, PSRCSMUTE, TESTI2 | Connect to VSS3 |

Relationship between the I2CSEL pin and the SDA

| | I2CSEL | INTRSTN | SDA |
|--------------------------------|--------|---------|------------------|
| Normal Microcomputer Interface | L | L | L |
| | L | H | L |
| I ² C-bus | H | L | "Hi-Z" → pull-up |
| | H | H | function |

| |
|---------------------------------|
| ABSOLUTE MAXIMUM RATINGS |
|---------------------------------|

(VSS1=VSS2=VSS3=0V; Note 4)

| Parameter | Symbol | min | max | Unit |
|---|--------|------|---------------------|------|
| Power Supply Voltage | | | | |
| Analog (AVDD) | VA | -0.3 | 4.3 | V |
| Digital (DVDD) | VD | -0.3 | 4.3 | V |
| Digital (DVDD18) | VD18 | -0.3 | 2.5 | V |
| VSS1(VSS2) – VSS3 (Note 5) | ΔGND | -0.3 | +0.3 | V |
| Input Current (except for power supply pin) | IIN | – | ±10 | mA |
| Analog Input Voltage | | | | |
| AINL+, AINL-, AINR+, AINR-, AINL2~8, AINR2~8, AINM VREFH, VREFL | VINA | -0.3 | $(VA+0.3) \leq 4.3$ | V |
| Digital Input Voltage | VIND | -0.3 | $(VD+0.3) \leq 4.3$ | V |
| Operational Ambient Temperature | Ta | -40 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 4. All voltages with respect to ground.

Note 5. VSS1, VSS2 and VSS3 must be connected to the same ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

| |
|--|
| RECOMMENDED OPERATION CONDITION |
|--|

(VSS1=VSS2=VSS3=0V; Note 4)

| Parameter | Symbol | min | typ | max | Unit |
|--------------------------|--------|------|-----|------|------|
| Power Supply Voltage | | | | | |
| AVDD | VA | 3.0 | 3.3 | 3.6 | V |
| DVDD | VD | 3.0 | 3.3 | 3.6 | V |
| DVDD18 | VD18 | 1.7 | 1.8 | 1.9 | V |
| AVDD-DVDD | ΔVDD | -0.3 | 0 | +0.3 | V |
| Reference Voltage (VREF) | | | | | |
| VREFH (Note 6) | VRH | | VA | | V |
| VREFL (Note 7) | VRL | | 0.0 | | V |

Note 4. All voltages with respect to ground.

Note 6. The VREFH pin is normally connected to AVDD.

Note 7. The VREFL pin is normally connected to VSS1.

Note 8. The analog input voltage is proportional to the (VREFH-VREFL) voltage.

Note 9. The power-up sequence between AVDD, DVDD and DVDD18 is not critical. The INTRSTN pin should be held “L” when power is supplied. The INTRSTN pin is allowed to be “H” after all power supplies are applied and settled.

Note 10. Do not turn off the power supply of the AK7782 when the power supplies of the surrounding device are turned on in I²C-bus mode (I2CSEL pin = “H”). Pull-up resistors at SDA and SCL pins must be connected to the DVDD voltage or less. (A diode exists for DVDD in the SDA and SCL pins.)

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

| |
|-------------------------------|
| ANALOG CHARACTERISTICS |
|-------------------------------|

(1) Analog Characteristics**1-1) ADC**

(Ta=25°C; AVDD=DVDD=3.3V; DVDD18=1.8V, VREFH=AVDD, VREFL=VSS1, BITCLK=64fs; Signal frequency 1kHz; Measurement frequency=20Hz~20kHz@48kHz, 20Hz~40kHz@96kHz; ADC full differential input (ADC1, ADC2); CKM Mode 0 (CKM[2:0]=000), during SRC reset, unless otherwise specified.)

| | Parameter | min | typ | max | Unit | |
|------------------------------------|--|--|-------|-------|------|----|
| Stereo ADC | Resolution | 24 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) | fs = 48kHz (-1dBFS) Note 11 | 82 | 90 | | dB |
| | | fs = 96kHz (-1dBFS) | | 87 | | dB |
| | Dynamic Range | fs = 48kHz (A-filter) Note 11, Note 12 | 88 | 96 | | dB |
| | | fs = 96kHz | | 93 | | dB |
| | | S/N | 88 | 96 | | dB |
| | | fs = 48kHz (A-filter) Note 11 | | 93 | | dB |
| | | fs = 96kHz | | | | dB |
| | Inter-channel Isolation (f=1kHz) Note 13 | 90 | 115 | | dB | |
| | DC Accuracy | | | | | |
| | Channel Gain Mismatch | | | 0.0 | 0.3 | dB |
| | Analog Input | | | | | |
| Input Voltage (Differential Input) | Note 14 | ±1.85 | ±2.00 | ±2.15 | Vp-p | |
| Input Voltage (Single-ended Input) | Note 15 | 1.85 | 2.00 | 2.15 | Vp-p | |
| Input Impedance | Note 16 | 22 | 33 | | kΩ | |
| Mono ADC | Resolution | 24 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) | fs = 48kHz (-1dBFS) | 78 | 88 | | dB |
| | | fs = 96kHz (-1dBFS) | | 87 | | dB |
| | Dynamic Range | fs = 48kHz (A-filter) Note 12 | 87 | 95 | | dB |
| | | fs = 96kHz | | 92 | | dB |
| | | S/N | 87 | 95 | | dB |
| | | fs = 48kHz (A-filter) | | 92 | | dB |
| | | fs = 96kHz | | | | dB |
| | Analog Input | | | | | |
| Input Voltage | Note 17 | 1.85 | 2.00 | 2.15 | Vp-p | |
| Input Impedance | Note 18 | 22 | 33 | | kΩ | |

Note 11. Values are not guaranteed with single-ended inputs.

Note 12. S/(N+D) when -60dB signal is applied.

Note 13. Inter-channel isolation between L-channel and R-channel at -1dBFS signal input.

Note 14. AINL+, AINL-, AINR+, and AINR- pins.

The full scale for differential input voltage is ($\pm FS = \pm (VREFH - VREFL) \times (2.0/3.3)$).

Note 15. AINL2~L8, and AINR2~R8 pins.

The full scale of single-ended input voltage ($FS = (VREFH - VREFL) \times (2.0/3.3)$).

Note 16. AINL+, AINL-, AINR+, AINR-, AINL2~L8, and AINR2~R8 pins.

Note 17. AINM pin. The full scale of input voltage is ($FS = (VREFH - VREFL) \times (2.0/3.3)$).

Note 18. AINM pin.

1-2) SRC

(Ta=25°C; AVDD = 3.3V; DVDD=3.3V; DVDD18=1.8V; data = 24bit; measurement bandwidth = 20Hz~ FSO/2, unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Unit |
|--|---------|-------|------|------|------|
| Resolution | | | | 24 | Bits |
| Input Sample Rate | FSI | 7.35 | | 96 | kHz |
| Output Sample Rate | FSO | 7.35 | | 96 | kHz |
| THD+N (Input= 1kHz, 0dBFS) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | -112 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | -112 | | dB |
| FSO/FSI=48kHz/44.1kHz | | | -112 | | dB |
| FSO/FSI=48kHz/96kHz | | | -112 | | dB |
| FSO/FSI=48kHz/8kHz | | | -111 | -103 | dB |
| FSO/FSI=8kHz/48kHz | | | -112 | | dB |
| FSO/FSI=8kHz/44.1kHz | | | -100 | | dB |
| Dynamic Range (Input= 1kHz, -60dBFS) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | 113 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | 113 | | dB |
| FSO/FSI=48kHz/44.1kHz | | | 113 | | dB |
| FSO/FSI=48kHz/96kHz | | | 113 | | dB |
| FSO/FSI=48kHz/8kHz | | 109 | 112 | | dB |
| FSO/FSI=8kHz/48kHz | | | 113 | | dB |
| FSO/FSI=8kHz/44.1kHz | | | 113 | | dB |
| Dynamic Range (Input= 1kHz, -60dBFS, A-weighted) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | 115 | | dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.167 | | 6 | |

| |
|---------------------------|
| DC CHARACTERISTICS |
|---------------------------|

(Ta=-40°C~85°C, AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|----------|-----|---------|------|
| High Level Input Voltage Note 19) | VIH | 80%DVDD | | | V |
| Low Level Input Voltage Note 19) | VIL | | | 20%DVDD | V |
| SCL, SDA High Level Input Voltage | VIH | 70%DVDD | | | V |
| SCL, SDA Low Level Input Voltage | VIL | | | 30%DVDD | V |
| High Level Output Voltage Iout=-100μA | VOH | DVDD-0.5 | | | V |
| Low Level Output Voltage Iout=100μA Note 20) | VOL | | | 0.5 | V |
| SDA Low Level Output Voltage Iout=3mA | VOL | | | 0.4 | V |
| Input Leak Current Note 21) | Iin | | | ±10 | μA |
| Input Leak Current (pull-down pin) Note 22) | Iid | | 22 | | μA |
| Input Leak Current (XTI pin) | Iix | | 26 | | μA |

Note 19. Except for the SDA pin and the SCL pin (when I2CSEL="1"). The SCLK pin is included when I2CSEL="0".

Note 20. Except for the SDA pin.

Note 21. Except for the XTI pin and pull-down pins.

Note 22. Pull-down pins (typ. 150kΩ) are the TESTI1 and TESTI2 pins.

| |
|--------------------------|
| POWER CONSUMPTION |
|--------------------------|

(Ta=25°C, AVDD=DVDD=3.0~3.6V(typ=3.3V, max=3.6V), DVDD18=1.7~1.9V(typ=1.8V, max=1.9V))

| Parameter | min | typ | max | Unit |
|--|-----|-----|-----|------|
| Power Supply Current (Note 23) | | | | |
| 1) a) AVDD | | 52 | 70 | mA |
| b) DVDD | | 8 | 15 | mA |
| c) DVDD18 | | 140 | 210 | mA |

Note 23. The current of DVDD18 changes depending on the system frequency and contents of the DSP program.

| |
|---------------------------------------|
| DIGITAL FILTER CHARACTERISTICS |
|---------------------------------------|

1) ADC1, ADC2

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V; fs=48kHz (Note 24))

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-------|--------|--------|------|
| Passband (±0.005dB) (Note 25) | PB | 0 | | 21.5 | kHz |
| (-0.02dB) | | | 21.768 | | kHz |
| (-6.0dB) | | | 23.99 | | kHz |
| Stopband | SB | 26.54 | | | kHz |
| Passband Ripple (Note 25) | PR | | | ±0.005 | dB |
| Stopband Attenuation (Note 26, Note 27) | SA | 80 | | | dB |
| Group Delay Distortion | ΔGD | | | 0 | μs |
| Group Delay (Ts=1/fs) | GD | | 29 | | Ts |
| Digital Delay Filter + Analog Filter | | | | | |
| Amplitude Characteristics 20Hz~20.0kHz | | | ±0.01 | | dB |

Note 24. Frequency of each amplitude characteristic is in proportion to fs (sampling rate). The characteristic of the high pass filter is not included.

Note 25. The passband is from DC to 21.5kHz when fs=48kHz.

Note 26. The stopband is from 26.5kHz to 3.0455MHz when fs = 48kHz.

Note 27. When fs = 48 kHz, the analog modulator samples the analog input at 3.072MHz. There is no attenuation of an input signal in band of integer times (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency by the digital filter.

2) ADCM

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V fs=48kHz; (Note 24))

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-------|--------|--------|------|
| Passband (±0.005dB) (Note 25) | PB | 0 | | 21.5 | kHz |
| (-0.02dB) | | | 21.768 | | kHz |
| (-6.0dB) | | | 23.99 | | kHz |
| Stopband | SB | 26.54 | | | kHz |
| Passband Ripple (Note 25) | PR | | | ±0.005 | dB |
| Stopband Attenuation (Note 26, Note 27) | SA | 80 | | | dB |
| Group Delay Distortion | ΔGD | | | 0 | μs |
| Group Delay (Ts=1/fs) (Note 28) | GD | | 29 | | Ts |
| Digital Delay Filter + Analog Filter | | | | | |
| Amplitude Characteristics 20Hz~20.0kHz | | | ±0.1 | | dB |

Note 24. Frequency of each amplitude characteristic is in proportion to fs (sampling rate). The characteristic of the high pass filter is not included.

Note 25. The passband is from DC to 21.5kHz when fs=48kHz.

Note 26. The stopband is from 26.5kHz to 3.0455MHz when fs = 48kHz.

Note 27. When fs = 48 kHz, the analog modulator samples the analog input at 3.072MHz. There is no attenuation of an input signal in band of integer times (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency by the digital filter.

Note 28. 1Ts additional delay occurs in VOL + MUX path.

3) SRC (Common for SRC1 and SRC2)

(Ta=-40°C ~85°C; AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V)

| Parameter | | Symbol | min | typ | max | Unit |
|-------------------------------------|--|--|-----------|-----------|-----------|------|
| Passband -0.01dB | $0.980 \leq \text{FSO/FSI} \leq 6.000$ | PB | 0 | | 0.4583FSI | kHz |
| | $0.900 \leq \text{FSO/FSI} < 0.990$ | PB | 0 | | 0.4167FSI | kHz |
| | $0.533 \leq \text{FSO/FSI} < 0.909$ | PB | 0 | | 0.2182FSI | kHz |
| | $0.490 \leq \text{FSO/FSI} < 0.539$ | PB | 0 | | 0.2177FSI | kHz |
| | $0.450 \leq \text{FSO/FSI} < 0.495$ | PB | 0 | | 0.1948FSI | kHz |
| | $0.225 \leq \text{FSO/FSI} < 0.455$ | PB | 0 | | 0.0917FSI | kHz |
| | $0.167 \leq \text{FSO/FSI} < 0.227$ | PB | 0 | | 0.0917FSI | kHz |
| | Stopband | $0.980 \leq \text{FSO/FSI} \leq 6.000$ | SB | 0.5417FSI | | |
| $0.900 \leq \text{FSO/FSI} < 0.990$ | | SB | 0.5021FSI | | | kHz |
| $0.533 \leq \text{FSO/FSI} < 0.909$ | | SB | 0.2974FSI | | | kHz |
| $0.490 \leq \text{FSO/FSI} < 0.539$ | | SB | 0.2812FSI | | | kHz |
| $0.450 \leq \text{FSO/FSI} < 0.495$ | | SB | 0.2604FSI | | | kHz |
| $0.225 \leq \text{FSO/FSI} < 0.455$ | | SB | 0.1573FSI | | | kHz |
| $0.167 \leq \text{FSO/FSI} < 0.227$ | | SB | 0.1354FSI | | | kHz |
| Passband Ripple | $0.225 \leq \text{FSO/FSI} \leq 6.000$ | PR | | | ±0.01 | dB |
| | $0.167 \leq \text{FSO/FSI} < 0.227$ | PR | | | ±0.0612 | dB |
| Stopband Attenuation | $0.450 \leq \text{FSO/FSI} \leq 6.000$ | SA | 95.2 | | | dB |
| | $0.167 \leq \text{FSO/FSI} < 0.455$ | SA | 92.3 | | | dB |
| Group Delay (Ts=1/fs) (Note 29) | | GD | | 56 | | Ts |

Note 29. SRC delay time is calculated from the rising edge of SRCLRCK just after data input to the rising edge of LRCLKO just after data output, when there is no phase difference between SRCLRCK and LRCLKO.

| |
|----------------------------------|
| SWITCHING CHARACTERISTICS |
|----------------------------------|

[#h indicates hexadecimal numbers. (#=0, 1, 2 ~ 9, A, B, C, D, E, F)]

1) System Clock

(Ta=-40°C~85°C, AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V)

| Parameter | Symbol | min | typ | max | Unit |
|-------------------------------------|--------|------|-------------------|------|------|
| XTI CKM[2:0] 0h, 1h, 2h, 3h | | | | | |
| a) with a Crystal Oscillator | | | | | |
| CKM[2:0]=0h, 2h | fXTI | | 11.2896 12.288 | | MHz |
| CKM[2:0]=1h, 3h | fXTI | | 16.9344 18.432 | | MHz |
| b) with an External Clock | | | | | |
| Duty Cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=0h, 2h | fXTI | 11.0 | | 12.4 | MHz |
| CKM[2:0]=1h, 3h | fXTI | 16.5 | | 18.6 | MHz |
| LRCLKI Frequency (Note 30) | fs | 7.35 | 48 | 96 | kHz |
| BITCLKI Frequency | | | | | |
| High Level Width | tBCLKH | 64 | | | ns |
| Low Level Width | tBCLKL | 64 | | | ns |
| a) CKM[2:0]=2h, 3h | fBCLK | | 64 | | fs |
| Duty Cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=2h, 3h | | 0.23 | | 6.2 | MHz |
| b) CKM[2:0]=4h, 5h (Note 31) | fBCLK | | 64 | | fs |
| Duty Cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=4h | fBCLK | 2.75 | | 3.1 | MHz |
| CKM[2:0]=5h | fBCLK | 5.5 | | 6.2 | MHz |

Note 30. LRCLK frequency and sampling rate (fs) should be the same.

Note 31. BITCLKI is a source of master clock. It should be 64 times fs correctly.

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V)

| Parameter | Symbol | min | typ | max | Unit |
|------------------------------------|--------|------|-----|-----|------|
| SRCLRCK Frequency (Note 30) | fs | 7.35 | 48 | 96 | kHz |
| SRCBICK Frequency | | | | | |
| High Level Width | tBCLKH | 64 | | | ns |
| Low Level Width | tBCLKL | 64 | | | ns |
| (Note 32) | fBCLK | 32 | | 128 | fs |
| Duty Cycle | | 40 | 50 | 60 | % |
| | | 0.23 | | 6.2 | MHz |

Note 30. LRCLK frequency and sampling rate (fs) should be the same.

Note 32. The maximum value 128fs is achieved when fs ≤ 48kHz.

2) Reset

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V)

| Parameter | Symbol | min | typ | max | Unit |
|-------------------|--------|-----|-----|-----|------|
| INTRSTN (Note 33) | tRST | 600 | | | ns |
| PCKRSTN | tRST | 600 | | | ns |
| PADRSTN | tRST | 600 | | | ns |
| PDSRSTN | tRST | 600 | | | ns |
| PSRCRSTN | tRST | 600 | | | ns |

Note 33. The INTRSTN pin must be “L” when power-up the AK7782.

3) Audio Interface

3-1) SDIN1~ SDIN7, SDOUT1~ SDOUT7 and SDOUTA1 (supports up to fs=96kHz)

MSB, LSB justified and I²S Compatible Format

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V, CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| Slave Mode CKM[2:0]=2h, 3h, 4h, 5h | | | | | |
| Delay Time from BITCLKI “↑” to LRCLKI (Note 34) | tBLRD | 20 | | | ns |
| Delay Time from LRCLKI to BITCLKI “↑” (Note 34) | tLRBD | 20 | | | ns |
| Delay Time from LRCLKI/O to Serial Data Output | tLRD | | | 40 | ns |
| Delay Time from BITCLKI/O to Serial Data Output | tBSOD | | | 40 | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 40 | | | ns |
| Master Mode CKM[2:0]=0h, 1h | | | | | |
| BITCLKO Frequency | fBCLK | | 64 | | fs |
| BITCLKO Duty Cycle | | | 50 | | % |
| Delay Time from BITCLKI “↓” to LRCLKO | tMBL | -20 | | 40 | ns |
| Delay Time from LRCLKO to Serial Data Output | tLRD | | | 40 | ns |
| Delay Time from BITCLKO to Serial Data Output | tBSOD | | | 40 | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 40 | | | ns |

Note 34. BITCLKI edge must not occur at the same time as LRCLKI edge.

3-2) SDIN1 and SDIN5 (SRC1I and SRC2I Inputs) (supports up to fs=96kHz)

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| Slave Mode | | | | | |
| Delay Time from SRCBICK1 “↑” to SRCLRCK1 (Note 35) | tBLRD | 20 | | | ns |
| Delay Time from SRCLRCK1 to SRCBICK1 “↑” (Note 35) | tLRBD | 20 | | | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 40 | | | ns |

Note 35. SRCBICK1 edge must not occur at the same time as SRCLRCK1 edge.

4) Microprocessor Interface

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V; DVDD18=1.7~1.9V, CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| Microprocessor Interface Signal | | | | | |
| SCLK Frequency | fSCLK | | | 2.1 | MHz |
| SCLK Low Level Width | tSCLKL | 200 | | | ns |
| SCLK High Level Width | tSCLKH | 200 | | | ns |
| Microprocessor → AK7782 | | | | | |
| Time from PDSRSTN, PADRSTN“↓” to RQN“↓” | tREW | 500 | | | ns |
| Time from RQN“↑” to PDSRSTN, PADRSTN“↑” | tWRE | 500 | | | ns |
| RQN High Level Width | tWRQH | 500 | | | ns |
| Time from RQN“↓” to SCLK“↓” | tWSC | 500 | | | ns |
| Time from SCLK“↑” to RQN“↑” | tSCW | 800 | | | ns |
| SI Latch Setup Time | tSIS | 200 | | | ns |
| SI Latch Hold Time | tSIH | 200 | | | ns |
| AK7782 ← Microprocessor | | | | | |
| Delay Time from SCLK “↓” to SO Output | tSOS | | | 200 | ns |
| Delay Time from SCLK “↑” to SO Output | tSOH | 200 | | | ns |
| Time from RQN “↓” to SO Hi-Z Release (Iout=±360μA) | tRQHR | | | 600 | ns |
| Time from RQN “↑” to SO Hi-Z set (Iout=±360μA) | tRQHS | | | 600 | ns |

5) I²C-BUS Interface

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V, DVDD18=1.7~1.9V)

| Parameter | Symbol | min | typ | max | Unit |
|--|---------|-----|-----|-----|------|
| I²C Timing | | | | | |
| SCL clock frequency | fSCL | | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | | μs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | | | μs |
| Clock Low Time | tLOW | 1.3 | | | μs |
| Clock High Time | tHIGH | 0.6 | | | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | | μs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | | 0.9 | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | | μs |
| Rise Time of Both SDA and SCL Lines | tR | | | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | | μs |
| Pulse Width of Spike Noise Suppressed By Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | | | 400 | pF |

Note 36. I²C-bus is a trademark of NXP B.V.

■ Timing Diagram

1) System Clock

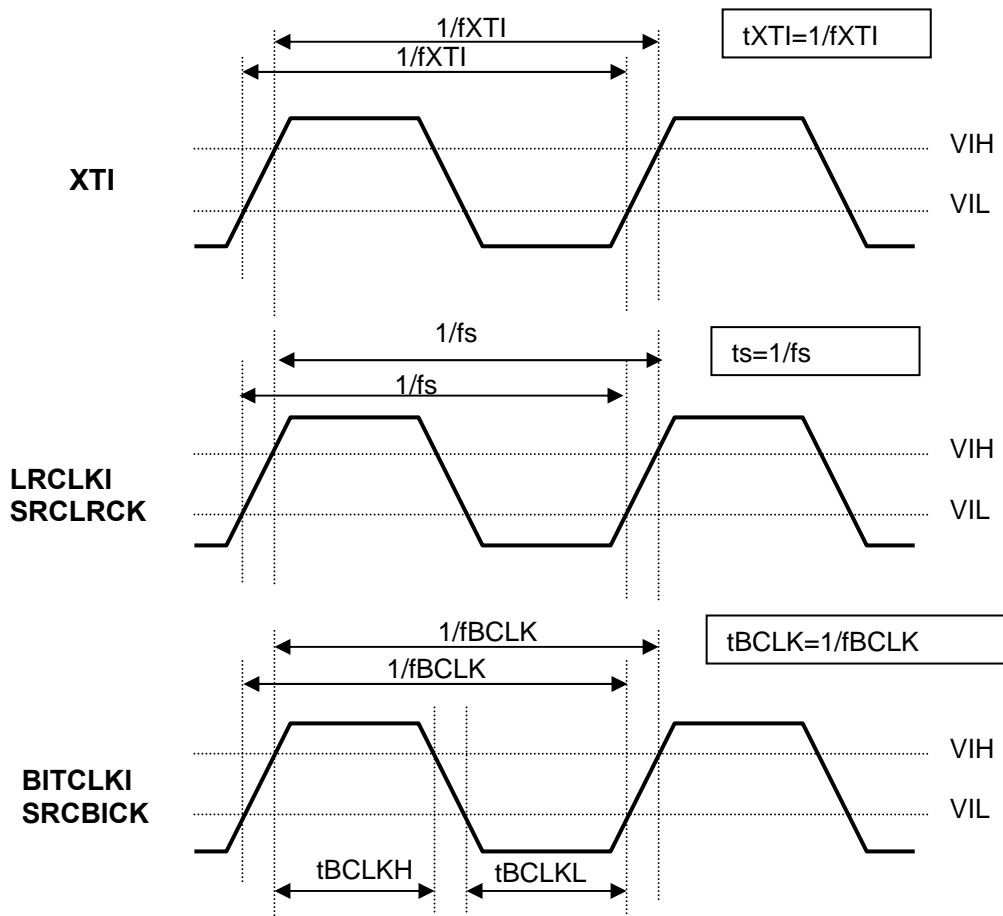


Figure 3. System Clock

2) Reset

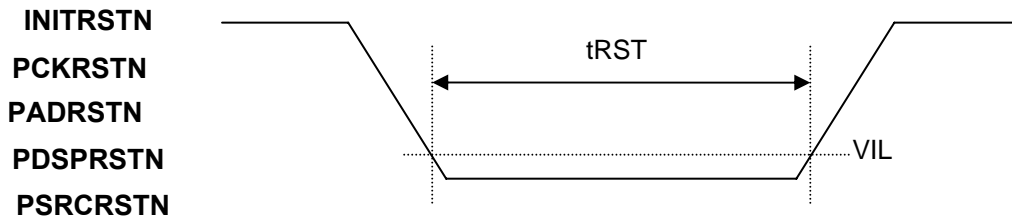
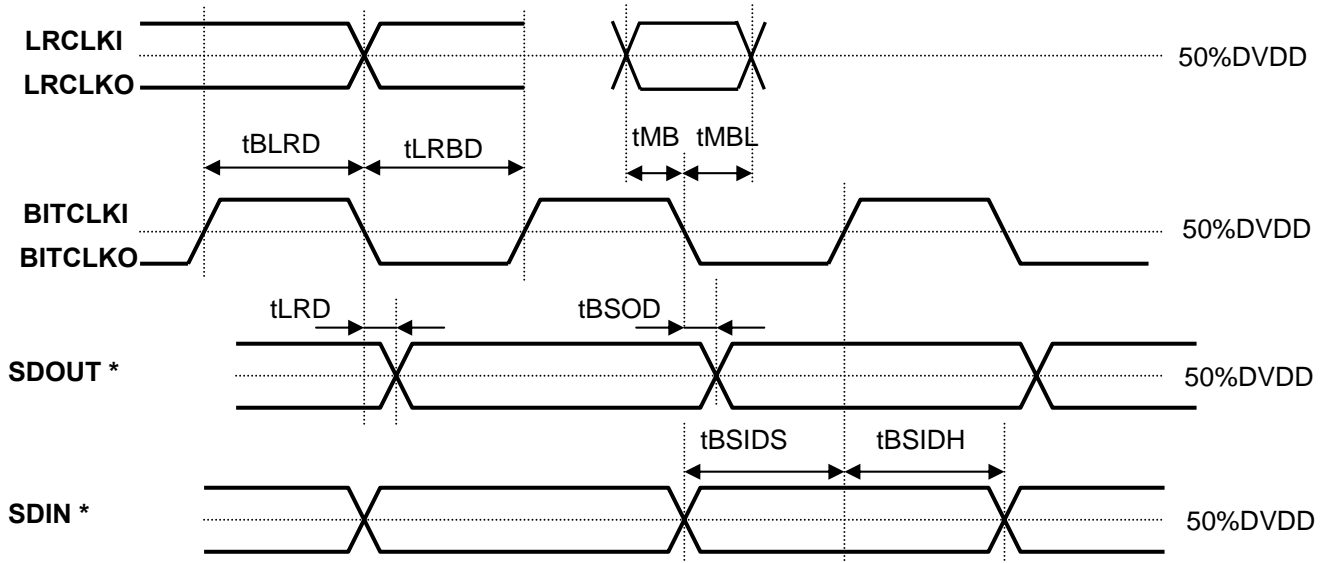


Figure 4. Reset

3) Audio Interface



SDIN * =SDIN1, SDIN2, SDIN3, SDIN4, SDIN5, SDIN6, SDIN7

SDOUT * =SDOUT1, SDOUT2, SDOUT3, SDOUT4, SDOUT5, SDOUT6, SDOUT7, SDOUTA1

Figure 5. Standard / I²C Compatible Format

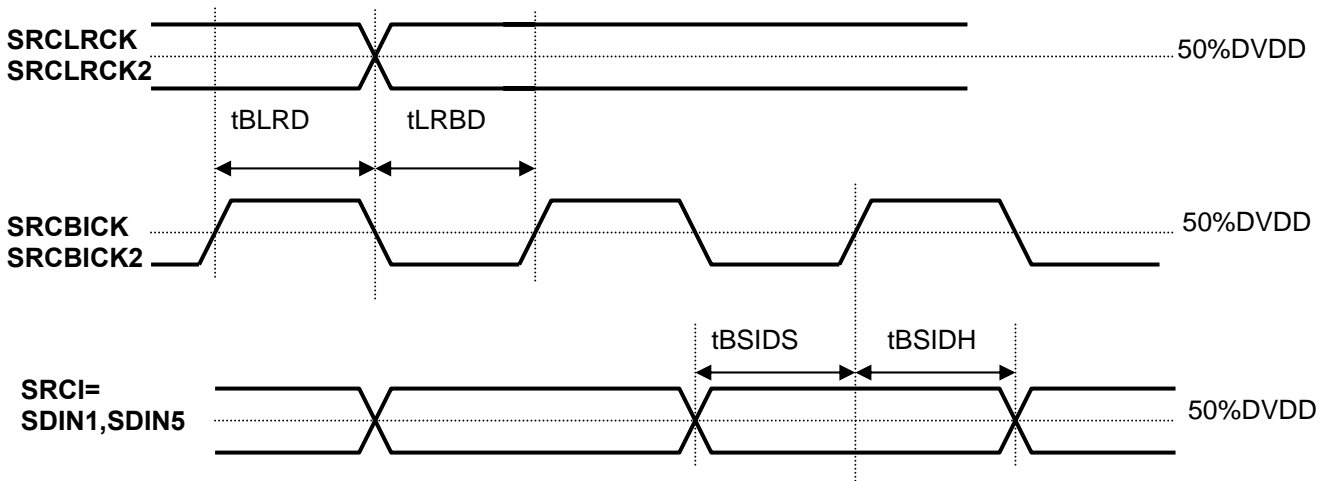


Figure 6. SRC

4) Microprocessor Interface

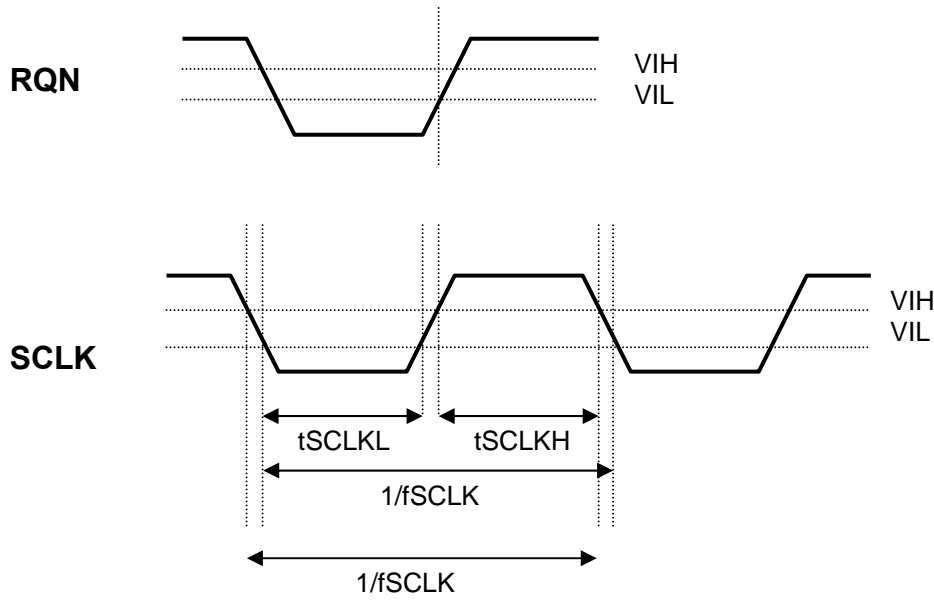


Figure 7. Microprocessor Interface Signal

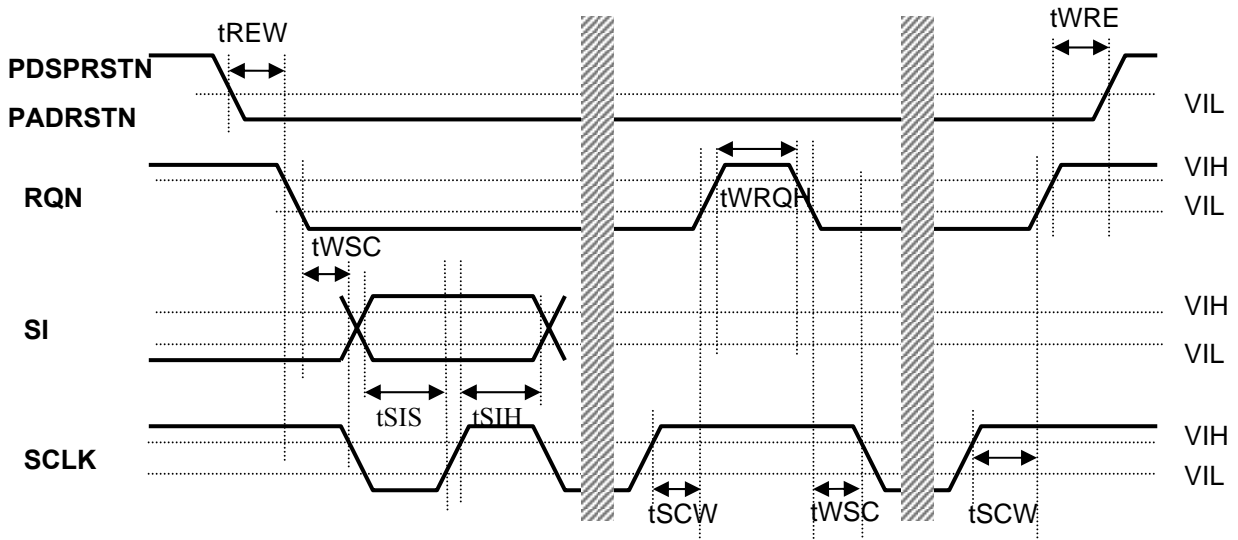


Figure 8. Microprocessor → AK7782

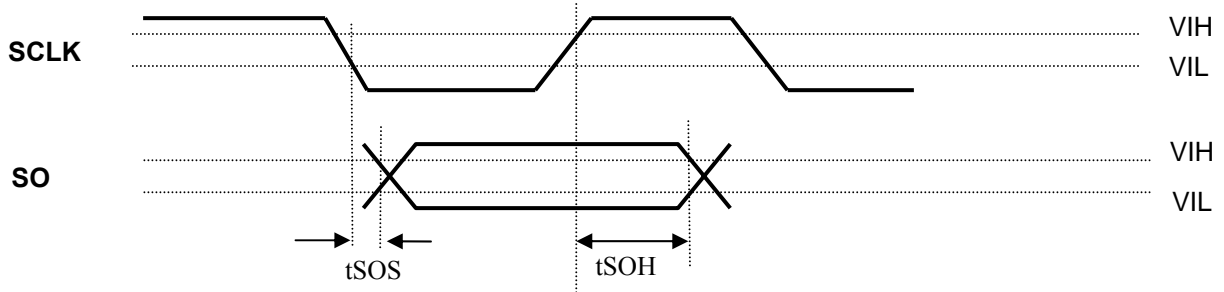


Figure 9. AK7782 → Microprocessor

Note 37. The timing diagram during RUN state is identical except PDSRSTN and PASRSTN are “H”.

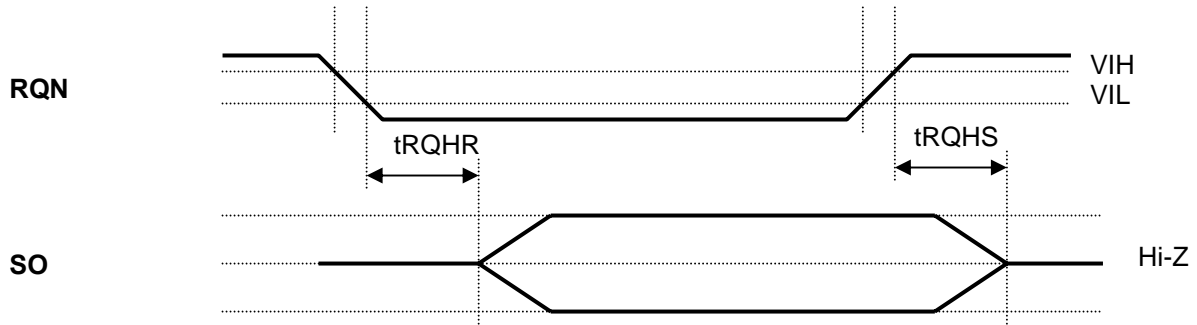


Figure 10. SO Output Timing

5) I²C-bus Interface

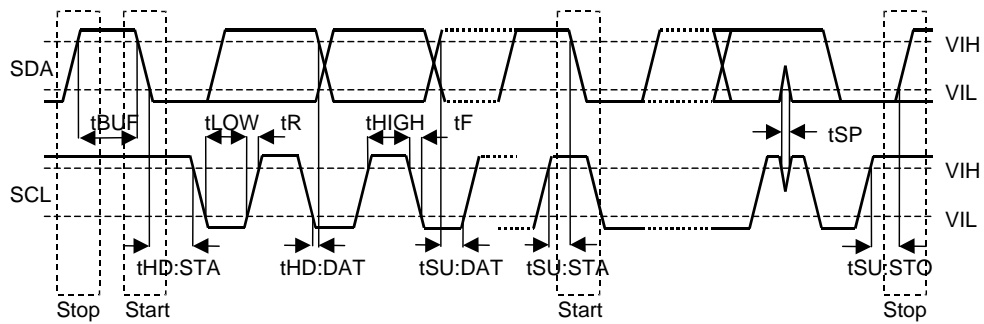
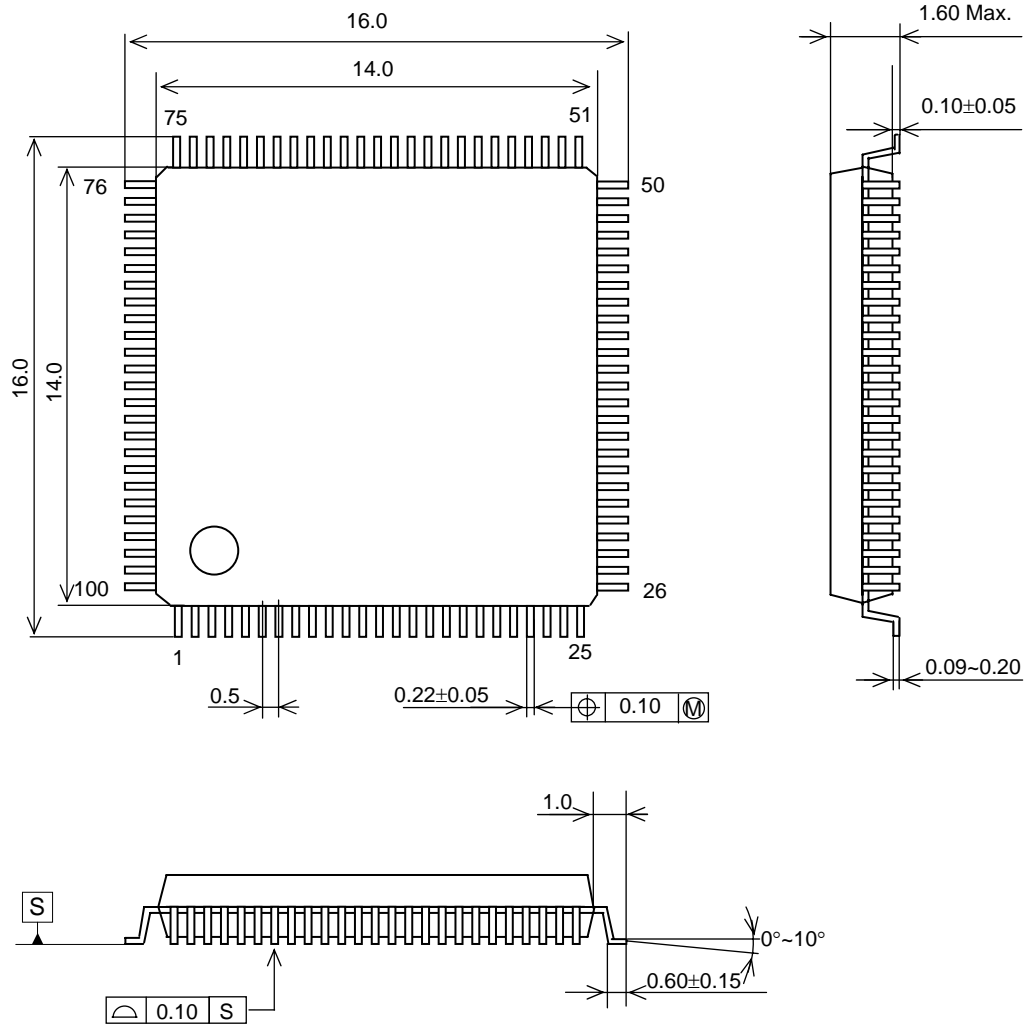


Figure 11. I²C-bus Interface

PACKAGE

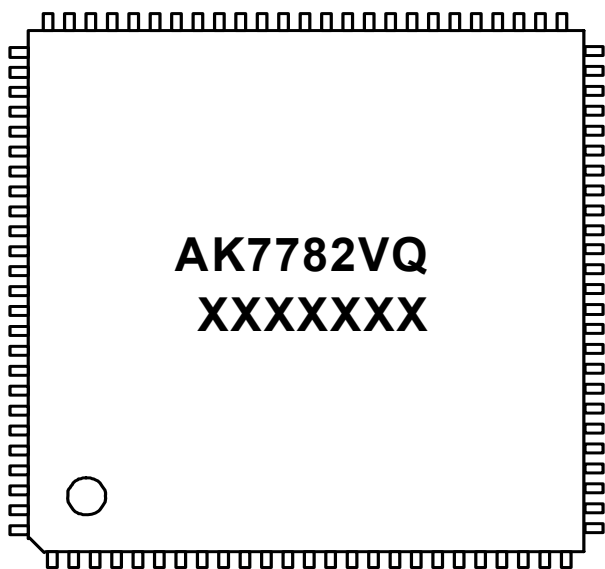
100-pin LQFP (Unit: mm)



■ Package & Lead frame material

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate

MARKING



- 1) Pin #1 indication
- 2) Date Code: XXXXXXXX(7 digits)
- 3) Marking Code: AK7782VQ

REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|---------------|------|----------|
| 11/11/02 | 00 | First Edition | | |

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.
- Descriptions of external circuits, application circuits, software and other related information contained in this document are provided only to illustrate the operation and application examples of the semiconductor products. You are fully responsible for the incorporation of these external circuits, application circuits, software and other related information in the design of your equipments. AKM assumes no responsibility for any losses incurred by you or third parties arising from the use of these information herein. AKM assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of such information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components^{Note1)} in any safety, life support, or other hazard related device or system^{Note2)}, and AKM assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKM. As used here:
Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.

Thank you for your access to AKM product information.
More detail product information is available, please contact our
sales office or authorized distributors.