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# AK7846

## Stereo Audio Class-D Amp with Power Booster for Piezo Speakers

## GENERAL DESCRIPTION

THE AK7846 is Stereo Class-D amplifier for driving Piezo-Electric Speakers. Built-in Boost DCDC converter generates adequate high voltage for driving Piezo Speakers from Li-Ion battery.
AKM state-of-the-art filter-less solution eliminates LC-filters, which are normally required at Class-D outputs. That contributes to total space saving. Class-D operation ensures higher power efficiency, and couple with Piezo Speaker that is low-power- consumption and low-profile figure. The AK7846 is very applicable for cellular phones with piezo speakers.

## FEATURES

☐ **Class-D Amplifier :**
- Piezo-Electric Speaker Driver
- Single-ended analog Input
- BTL output
- Output voltage = 8Vrms @VDD1=13V
- Filter-less solution
- Stereo mode
- Pop noise suppressor
- Output short protection

☐ **Boost DCDC Converter :**
- Input voltage (Battery) = 2.7V ~ 4.5V → Boosted voltage will be 13V
- Over-current protection
- Over-voltage protection

☐ **Control function :**
- Pre-gain amplifier −6dB ~ +15dB, 3dB step * Adjustable by Pin (PG0, PG1 and PG2) control
- Built-in Second order lowpass filter at Input.
- Cutoff Frequency (4kHz,8kHz,16kHz) * Adjustable by Pin (PG0, PG1 and PG2) control
- Power-on/off control
- Over-temperature protection

☐ **Operational voltage : VBAT=2.7V ~ 4.5V、DVDDI=1.65V ~ 4.5V**

☐ **Operational temperature : –30°C ~ 85°C**

☐ **Package : 31pin WL-CSP (3.0mm × 3.0mm, 0.5mm pitch)**

## BLOCK DIAGRAM

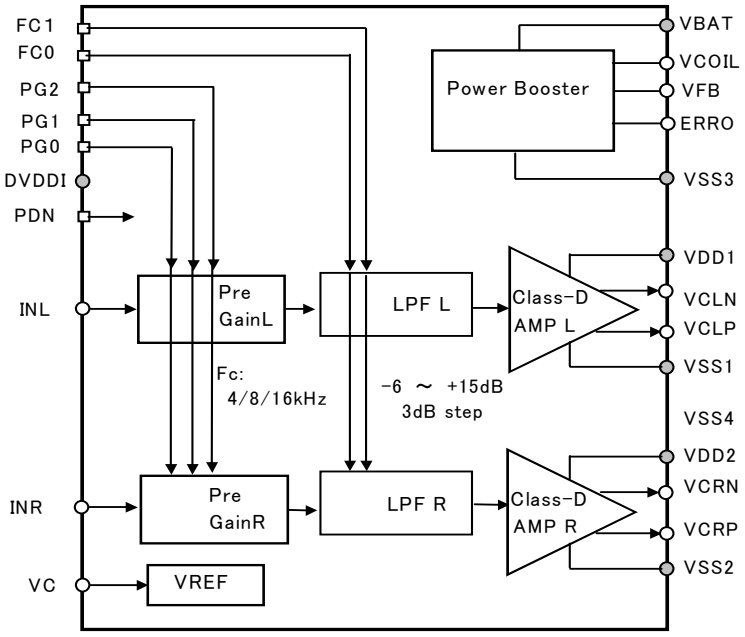
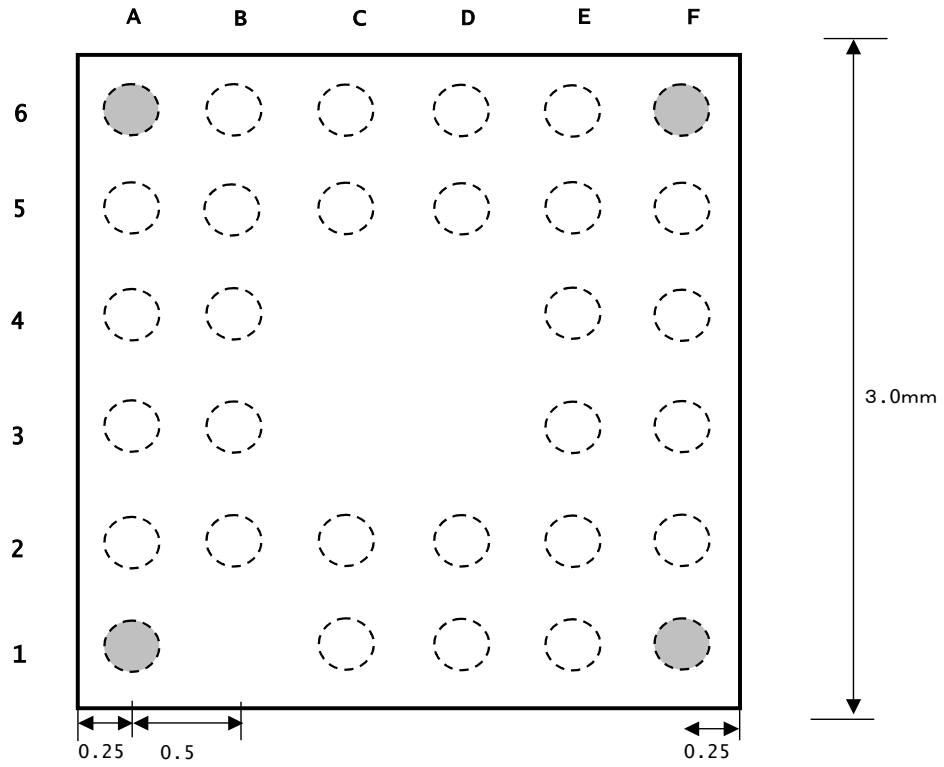



Figure 1. BLOCK DIAGRAM

## PIN ASSIGNMENT




| - | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 6 | NC | VDD2 | VFB | NC | VDD1 | NC |
| 5 | VCRP | VCRN | NC | NC | VCLN | VCLP |
| 4 | ERRO | VSS2 | — | — | VSS1 | INL |
| 3 | PG2 | VSS4 | — | — | VBAT | INR |
| 2 | VCOIL | VSS3 | PG1 | FC1 | FC0 | VC |
| 1 | NC | <Index> | PG0 | DVDDI | PDN | NC |

Figure 2. Pin Assighnment

## Pin / FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| A1 | NC | — | No Connection pin. Connect to ground. |
| A2 | VCOIL | — | Inductor pin for Boost DCDC. |
| A3 | PG2 | I | Pre Gain setting pin2 (available when I2CEN="L") |
| A4 | ERRO | | Phase compensation capacitor connection pin for Boost DCDC.<br>Connect a 0.1μF capacitor between VC pin and ground. |
| A5 | VCRP | O | Right channel Class D amp plus output (+) |
| A6 | NC | | No Connection pin. Connect to ground. |
| B1 | — | — | <Index> |
| B2 | VSS3 | — | Power Booster ground pin : VSS3=0V |
| B3 | VSS4 | | Internal analog circuit ground pin : VSS4=0V |
| B4 | VSS2 | I | Right channel Class D amp ground pin : VSS2=0V |
| B5 | VCRN | O | Right channel Class D amp minus output (-) |
| B6 | VDD2 | | Right channel Class D amp power supply : VDD2=13V(typ.) |
| C1 | PG0 | I | Pre Gain setting pin0 |
| C2 | PG1 | I | Pre Gain setting pin1 |
| C3 | — | — | — |
| C4 | — | — | — |
| C5 | NC | | No Connection pin. Connect to ground. |
| C6 | VFB | | Boosted voltege feedback pin. |
| D1 | DVDDI | | Digital interface power : DVDDI=1.65V～4.5V |
| D2 | FC1 | I | SCF cutoff frequency setting pin1 |
| D3 | — | — | — |
| D4 | — | — | — |
| D5 | NC | | No Connection pin. Connect to ground. |
| D6 | NC | | No Connection pin. Connect to ground. |
| E1 | PDN | I | Power down contorol : schmitt trigger input<br>"High" : poewer up、"Low" : power down |
| E2 | FC0 | I | SCF cutoff frequency setting pin2 |
| E3 | VBAT | — | Battery voltage input : VBAT=2.7V～4.5V |
| E4 | VSS1 | — | Left channel Class D amp ground pin : VSS1=0V |
| E5 | VCLN | O | Left channel Class D amp minus output (-) |
| E6 | VDD1 | | Left channel Class D amp power supply : VDD1=13V(typ.) |
| F1 | NC | | No Connection pin. Connect to ground. |
| F2 | VC | | Voltage reference output. Connect a 0.01μF capacitor between VC pin and ground. |
| F3 | INR | I | Right channel analog signal input |
| F4 | INL | I | Left channel analog signal input |
| F5 | VCLP | O | Left channel Class D amp plus output (+) |
| F6 | NC | | No Connection pin. Connect to ground. |

Note 1. Digital input pins (PDN, PG2, PG1, PG0, FC1, FC0) must not be open.

### ■ Unused Pins

Unused pins should be configured as below.

| Category | Pin Name | Configuration |
|---|---|---|
| NoConnection | NC | VSS |

## ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V;Note 3)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: (Note.4) | Battery | VBAT | –0.3 | 6.5 | V |
| | Digital I/F | DVDDI | –0.3 | 6.5 | V |
| | Class-D Amp | VDD1,2 | –0.3 | 15 | V |
| Input Current, Any Pin Except Supplies | | IIN | -10 | +10 | mA |
| Analog Input Voltage (Note 4) (Note 6) | | VINA | –0.3 | VBAT+0.3 | V |
| Digital Input Voltage (Note 5) (Note 6) | | VIND | –0.3 | DVDDI+0.3 | V |
| Ambient Temperature (powered applied) | | Ta | –30 | 85 | °C |
| Storage Temperature | | Tstg | –65 | 150 | °C |

Note 2. All voltages are with respect to ground.

Note 3. VSS1, VSS2, VSS3, VSS4 pin must be connected to the same analog ground plane.

Note 4. INL,INR pin

Note 5. PDN, PG2, PG1, PG0, FC1, FC0 pin

Note 6. Maximum value must not exceed 6.5V even if VBAT or DVDDI is more than 6.2V.

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 2)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies | Battery (Note 7) | VBAT | 2.7 | 3.6 | 4.5 | V |
| | VDD (Note 8) | VDDx | 12 | 13 | 14 | V |
| | DigitalI/F(Note 7) | DVDDI | 1.65 | 2.8 | 4.5 | V |

Note 2. All voltages are with respect to ground.

Note 7. Should sustain "VBAT≧ DVDDI" condition

Note 8. Supply with boosted voltage (typ. 13V) by the Power Booster.

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

## DC CHARACTERISTICS

(Ta=25°C; VBAT=2.7 ~ 4.5V,DVDDI = 1.65～4.5V,VSS1=VSS2=VSS3=VSS4=0V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage1 (Note 9) | VIH1 | 70%DVDDI | - | - | V |
| Low-Level Input Voltage1 (Note 9) | VIL1 | - | - | 30%DVDDI | V |
| High-Level Input Voltage2 (Note 10) | VIH2 | 80%DVDDI | - | - | V |
| Low-Level Input Voltage2 (Note 10) | VIL2 | - | - | 20%DVDDI | V |
| Input Leakage Current | | | | ±10 | μA |

Note 9. Applied to PG0, PG1, PG2.

Note 10. Applied to PDN, FC1, FC2 (Summit trigger input).

## ANALOG CHARACTERISTICS

(Unless otherwise noted, Ta＝25℃、VBAT=3.6V、DVDDI=2.8V、VSS1,2,3,4＝0V, Input Signal Frequency =1kHz , Measurement Band Width =20～20kHz ,PreGain=0dB , Fc= 16kHz Class-D ampu Output Load Impedance $Z_L$=**150nF**)

| Parameter | Condition | min | typ | max | Units |
|---|---|---|---|---|---|
| Idd | No input signal.<br>With output Load | | T.B.D | | mA |
| ShutdownCurrent | PDN pin = "Low" | | 1.0 | 10 | μA |
| Input Impedance | INL | 25 | 50 | 75 | kΩ |
| | INR | 25 | 50 | 75 | kΩ |
| PreGain<br>Control Range | | -6 | | +15 | dB |
| PreGain<br>Step Size<br>(Note 11) | PG2="Low",PG1=" Low",PG0=" Low" | -7 | -6 | -5 | dB |
| | PG2="Low",PG1=" Low",PG0=" High" | -4 | -3 | -2 | dB |
| | PG2="Low",PG1=" High",PG0=" Low" | -1 | 0 | +1 | dB |
| | PG2="Low",PG1=" High",PG0=" High" | +2 | +3 | +4 | dB |
| | PG2=" High",PG1=" Low",PG0=" Low" | +5 | +6 | +7 | dB |
| | PG2=" High",PG1=" Low",PG0=" High" | +8 | +9 | +10 | dB |
| | PG2=" High",PG1=" High",PG0=" Low" | +11 | +12 | +13 | dB |
| | PG2=" High",PG1=" High",PG0=" High" | +14 | +15 | +16 | dB |
| Output Voltage | VCL(R)P/VCL(R)N<br>Input Signal=0.7Vrms | 7.2 | 8.0 | 8.8 | Vrms |
| Output<br>Offset Voltage | VCL(R)P/VCL(R)N<br>No input signal | - | - | T.B.D. | mV |
| THD+N | VCL(R)P/VCL(R)N (Note 12)<br>Input Signal=0.7Vrms | - | - | -30 | dB |
| SNR | VCL(R)P/VCL(R)N (Note 12)<br>Input Signal=0.7Vrms<br>using an A wating filter. | 70 | 80 | - | dB |
| PSRR<br>(Note 13) | VCL(R)P/VCL(R)N (Note 12)<br>Vripple=200mVpp@1kHz sinwave | | 50 | | |
| Cross Talk | INL：NoInput 、INR=2Vpp<br>Lch：OutputPin monitoring. | | 70 | | dB |
| | INR：NoInput 、INL=2Vpp<br>Rch：OutputPin monitoring. | | 70 | | dB |
| Switching<br>Frequency | Class-D Amp | 225 | 250 | 275 | kHz |
| | PowerBooster | 900 | 1000 | 1100 | |
| Startup Time<br>(Note 14) | C3=0.01uF, C5=C6= 0.1uF(Note 15)<br>VBAT=2.7V | | 28 | | ms |

Note 11. Setting accuracy of each setting is within ±1dB. Monotony is guaranteed.

Note 12 . Measure signals between VCL(R)N and VC L(R)P through Low-Pass-Filter (fc=20kHz).

Note 13. 200mVpp@1kHz superimposed signal at VBAT pin, and measured output.

Note 14. Time period from "PDN" turns "High" to stability operation.

Note 15. Refer to section "TYPICAL APPLICATION CIRCUIT".

## OPERATION OVERVIEW

### ■ Power Control

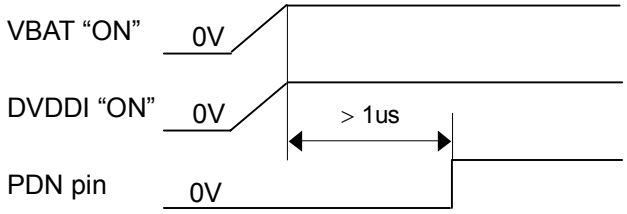
The AK7848 enters SHUT-DOWN MODE by setting PDN pin to Logic "Low" level.

**Power-Up Control**

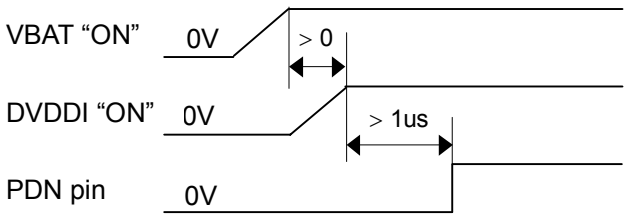
Power supply (VBAT pin, DVDDI pin) sequence must be either (1) or (2) as follows.

(1) VBAT and DVDDI are simultaneously turned on.
(2) First, VBAT pin is turned on. Next, DVDDI is turned on.

- Simultaneous turn-on of DVDDI pin and PDN pin is prohibited. At least 1 us delay is needed before the transision ("L"→"H") of PDN pin.




Power-Up Sequence (1)




Power –Up Sequence (2)

**CAUTION**: The performance of the device will not be guaranteed after the sequence below.
(3) First, DVDDI pin = "H", Next VBAT = "H"

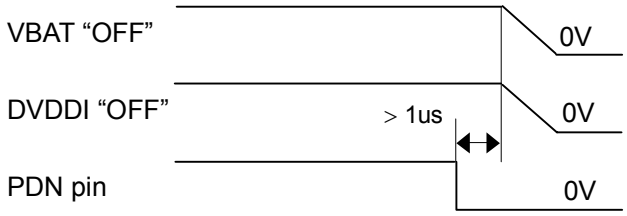
## Power-Down Control

Power supply (VBAT, DVDDI) sequences must be either (4) or (5) as follows.

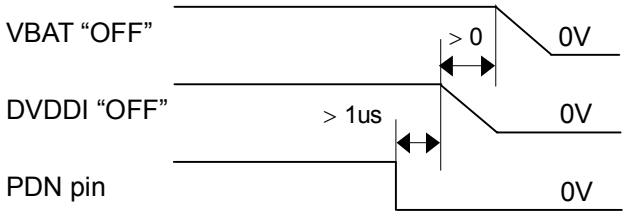
(4) VBAT and DVDDI are simultaneously turned-off.
(5) First DVDDI is turned-off, Next, VBAT is turned-on.

* Simultaneous turn-off of PDN pin and DVDDI pin is prohibited. At least 1 us delay is needed before the transision ("L"→"H") of DVDDI pin.

- In case PDN pin is "High" and VBAT/DVDDI supply is suddenly cut off due to unexpected event, pop noise may be detected, however, LSI will not be harmed even under such a case.




Power-Down Sequence (4)




Power –Down Sequence (5)

**CAUTION**: The performance of the device will not be guaranteed after the sequence below.
(5) First VBAT is turned-off, Next, DVDDI is turned-off.

## ■ Analog inputs

AC-coupling capacitor is required at analog inputs. Recommended capacitance is 0.1μF. This AC-coupling capacitance configures High-Pass-Filter, and used to configuration of POP NOISE SUPPRESSOR as well. Therefore, any variation of this capacitance affects both HPF cut-off frequency and POP NOISE SUPPRESSOR operation.
Additional input filter is applicable. When using filter at analog input, place it before AC-coupling capacitors.

Note 16. Cut off frequency (fc) of the High-pass filter, used as decoupling before input, is caluculated by an equation, $1 / (2 \times \pi \times R \times C)$. For example, when Input impedance of INN and INP pins are 50kΩ(typ.) and AC coupling capacitors are 0.1μF, then the cut off frequency will be 31.8Hz.

## ■ Pre AMP

THE AK7846 has internal Pre-Amplifier, which supports from −6dB to +15dB(3dB/step) gain range.
Pre-Amplifier gain is adjusted by PG0,PG1 and PG2 like as shown below.

| PG2 | PG1 | PG0 | Pre Gain Setting Value |
|---|---|---|---|
| “Low” | “Low” | “Low” | −6dB |
| “Low” | “Low” | “High” | -3dB |
| “Low” | “High” | “Low” | 0dB |
| “Low” | “High” | “High” | +3dB |
| “High” | “Low” | “Low” | +6dB |
| “High” | “Low” | “High” | +9dB |
| “High” | “High” | “Low” | +12dB |
| “High” | “High” | “High” | +15dB |

Table. 1 Pre Gain Setting

## ■ Class-D AMP

Class-D architecture features higher efficiency and low power consumption operation.
AKM filter-less solution offers Class-AB performance with Class-D efficiency and minimal board space.

## ■ Pop Noise Suppressor

The AK7846 features extensive pop noise suppression circuitry.

## ■ Power Booster

Built-in BOOST DCDC CONVERTER generates adequate high voltage for Piezo-Speaker. Input voltage range corresponds with Li-Ion battery voltage range (2.7V ~ 4.5V), and output voltage is 13V. Normally, output connected to and supply VDD1 and VDD2 for Class-D operation.

## ■ Lowpass Filter

The AK7846 has a built-in Lowpass Filter at the input side. Cutoff frequency can be adjusted by FC0 and FC1 as follows. FC0 and FC1 must be connected to either ground (VSS4) or DVDDI.

| FC1 | FC0 | CurOff Frequency |
|---|---|---|
| “Low” | “Low” | 16kHz |
| “Low” | “High” | 8kHz |
| “High” | “Low” | 4kHz |
| “High” | “High” | 4kHz |

Table. 2 Adjustable Cutoff Frequency of Lowpass filter

## ■ Protection

The AK7846 supports following protection circuits for protecting against any damages.

### Output Short-Circuit Protection

In case of detecting VCL(R)P and VCL(R)N short, the AK7846 clamps peak current of Class-D output circuit without shutting down the outputs.

### Over-Temperature Protection

The AK7846 is designed to shutdown at +150°C of inside temperature so that it can be protected from heat damage. Note that the AK7846 DOES NOT support resume function from Over-Temperature Protection. Once it is activated, the AK7846 does not back in normal operation unless "PDN" is toggled ("L" → "H").

### Over-Current Protection

Class-D amplifiers' current-limiting protection clamps the output current without shutting down the outputs.

### Over-Voltage Protection

Boost DCDC Converter has the voltage-limiting function to avoid destrying itself.

## Performance characteristics

※ The following various characteristics are typical characteristic data in the typical condition. It is not the one necessarily to secure the characteristic of the description.

(TBD)

## LEVEL DIAGRAM

The gain of AK7846 are determined by Pre-Amplifier, LPF and Class-D Amp, Total gain will be +21dB while Pre-Amplifier is default setting (PG=0). LPF gain and Class-D Amp gain are not changeable.
Figure 3 shows level diagram of two example, PG=0dB and PG=+15dB.

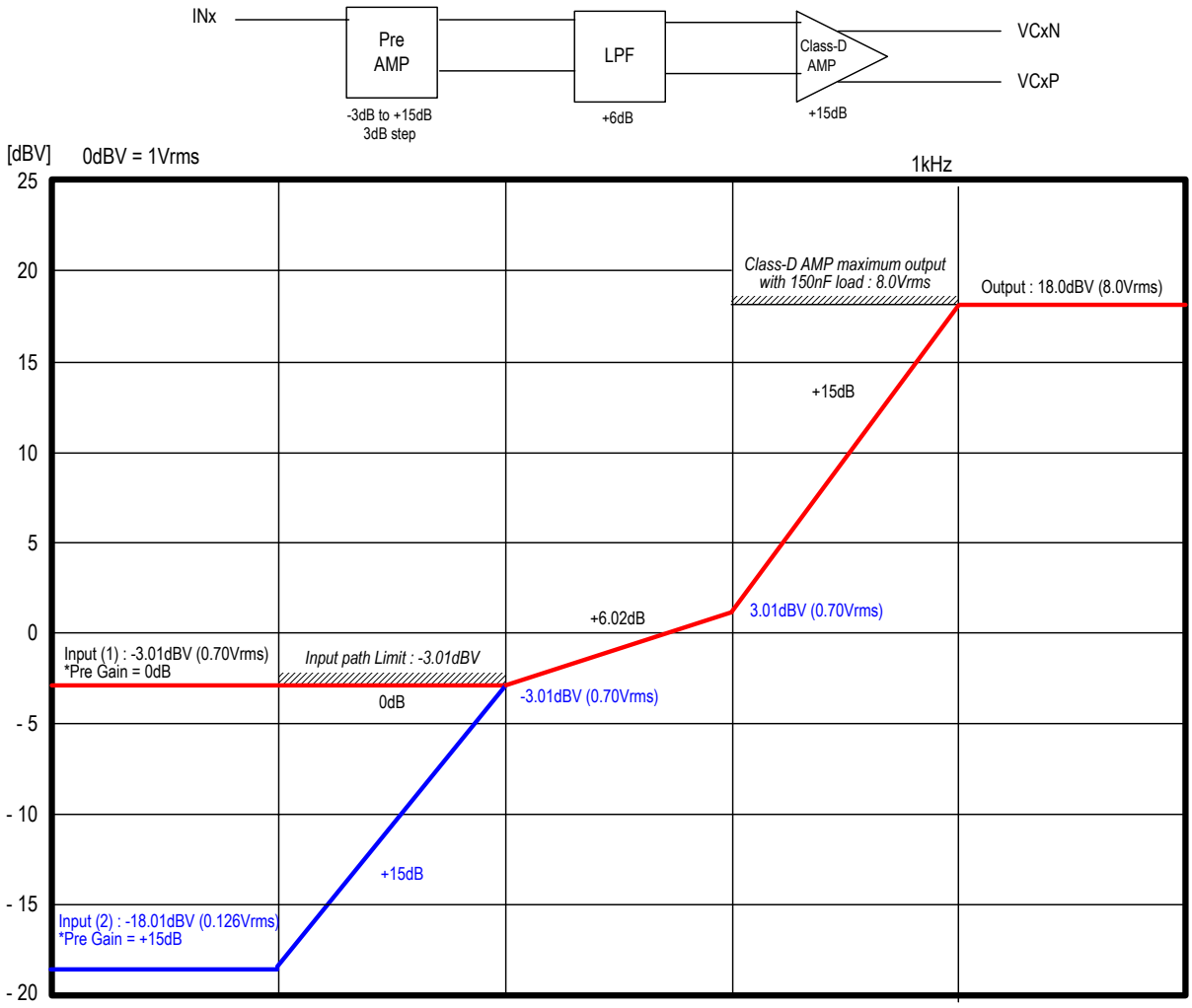



Figure 3. Level Diagram

***1Vrms=0dBV=2.83Vpp (sin wave)**

## TYPICAL APPLICATION CIRCUIT

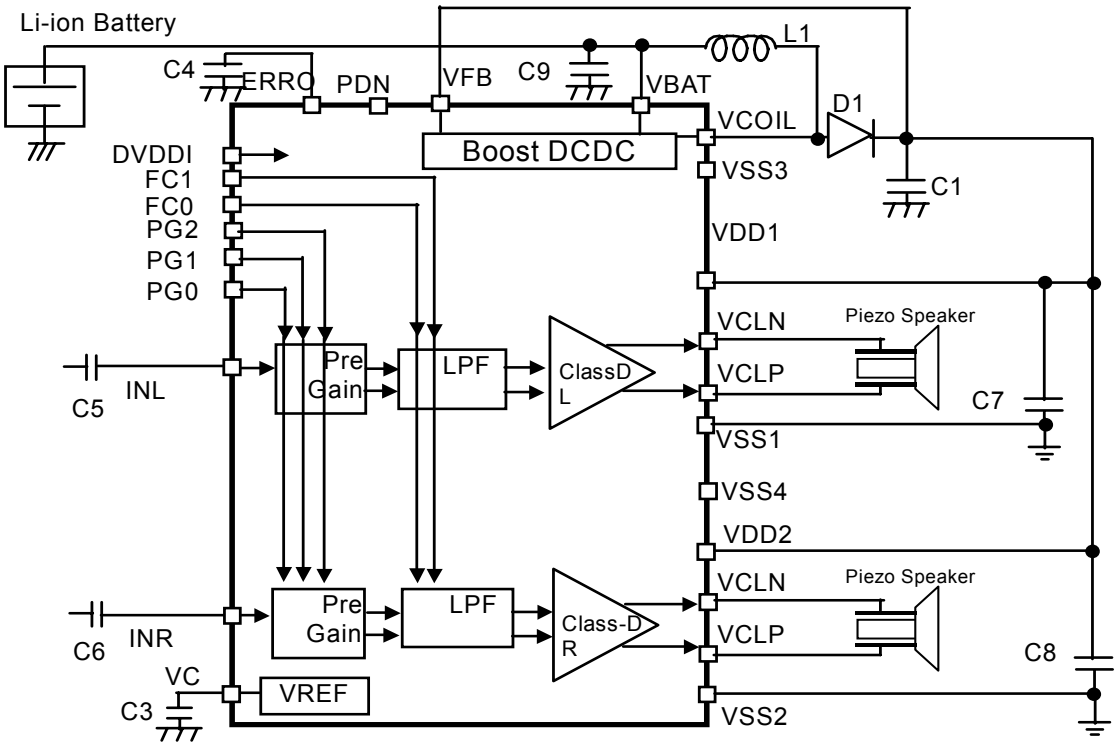



Figure 4 AK7846 Application Schematic

Recommended external components are shown in Table. 3 as follows.

| Reference | Type | Value | Manufacturer | Part No. | Size (mm) |
|---|---|---|---|---|---|
| L1 | Inductor ※ | 1.0uF | CoilCraft | LPS3010-102ML | 2.95 ×2.95 ×0.9 |
| | | | TDK | TFC252008MC-1R0 | 2.5 ×2.0 ×0.8 |
| D1 | Diode / Schottky | (30V, 1A) | SANYO | SS1003EJ | 1.6 × 0.8 × 0.6 |
| C1 | Capacitor / Ceramic | 10μF / 25V | Taiyo Yuden | TMK325BJ106MD-B | 3.2 × 2.5 × 0.85 |
| C3 | Capacitor / Ceramic | 0.01μF / 16V | Taiyo Yuden | EMK105BJ103KV | 1.0 × 0.5 × 0.5 |
| C4, C5, C6 C7,C8 | Capacitor / Ceramic | 0.1μF / 16V | Taiyo Yuden | EMK105BJ104KV-B | 1.0 × 0.5 × 0.5 |
| C9 | Capacitor / Ceramic | 2.2μF / 16V | Taiyo Yuden | EDK107BJ225KA | 1.6 × 0.8 × 0.8 |

Table. 3 External Recommendation Parts

※Chose one of inductors in Table. 3
Selection of L1, C1 and D1 are very important because they affect DCDC converter paformance directly. For stability operation, AKM recommends them described in Table. 3

### 1. Grounding and Power Supply Decoupling

The AK7846 requires careful attention to power supply and grounding arrangements. VBAT is usually supplied from Li-Ion battery in the system. VDD1 and VDD2 are supplied from smoothed boosted voltage. VSS1, VSS2, VSS3 and VSS4 must be connected to analog ground plane. Analog and digital ground in the system should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors with the small value ceramic should be as close to the AK7846 as possible.

### 2. Voltage Reference

VC is a signal ground of this device. A 0.01μF ceramic capacitor (C3) between VC and VSS4 pin eliminates the effects of high frequency noise. This capacitor should be as close to the VC pin as possible. Do not take out load current from the VC pin. All signals, especially clocks should be kept away from the VC pin in order to avoid unwanted coupling.

### 3. Class-D analog Inputs

AC-coupling capacitors are necessary in series to INL and INR respectively.

### 4. Class-D Outputs

The Class-D outputs are in BTL signal format. Locate the outputs close to the speaker to minimize interconnect resistance and capacitance to suppress noise. Match the length and pattern of the plus and minus output interconnect. Keep AK7846 or Class-D outputs away as far away as possible from the devices such as antennas that are sensitive to high frequency noise.

### 5. Effect on RF bands

Power Booster or Class-D Outputs may affect high frequency signal outside the AK7846.
Apply previous section (4. Class-D Outputs) in PCB layout.

### 6. Drivable Piezo Speakers

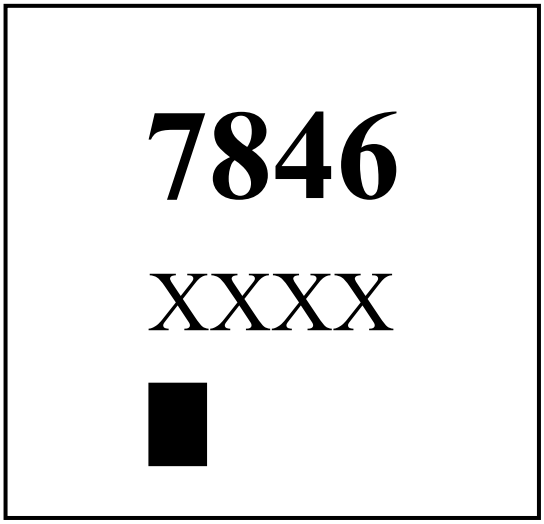
The AK7846 is designed to drive typical piezo speakers but in some cases electric characteristics of the speakers differ by manufacturers. Feel free to ask us whether your speakers can be driven or not before using them.

### 7. Boost DCDC Converter

Ceramic capacitor (C1, C9), Inductance (L1) and Schottky Diode (D1) should be located as close to the AK7846 as possible.

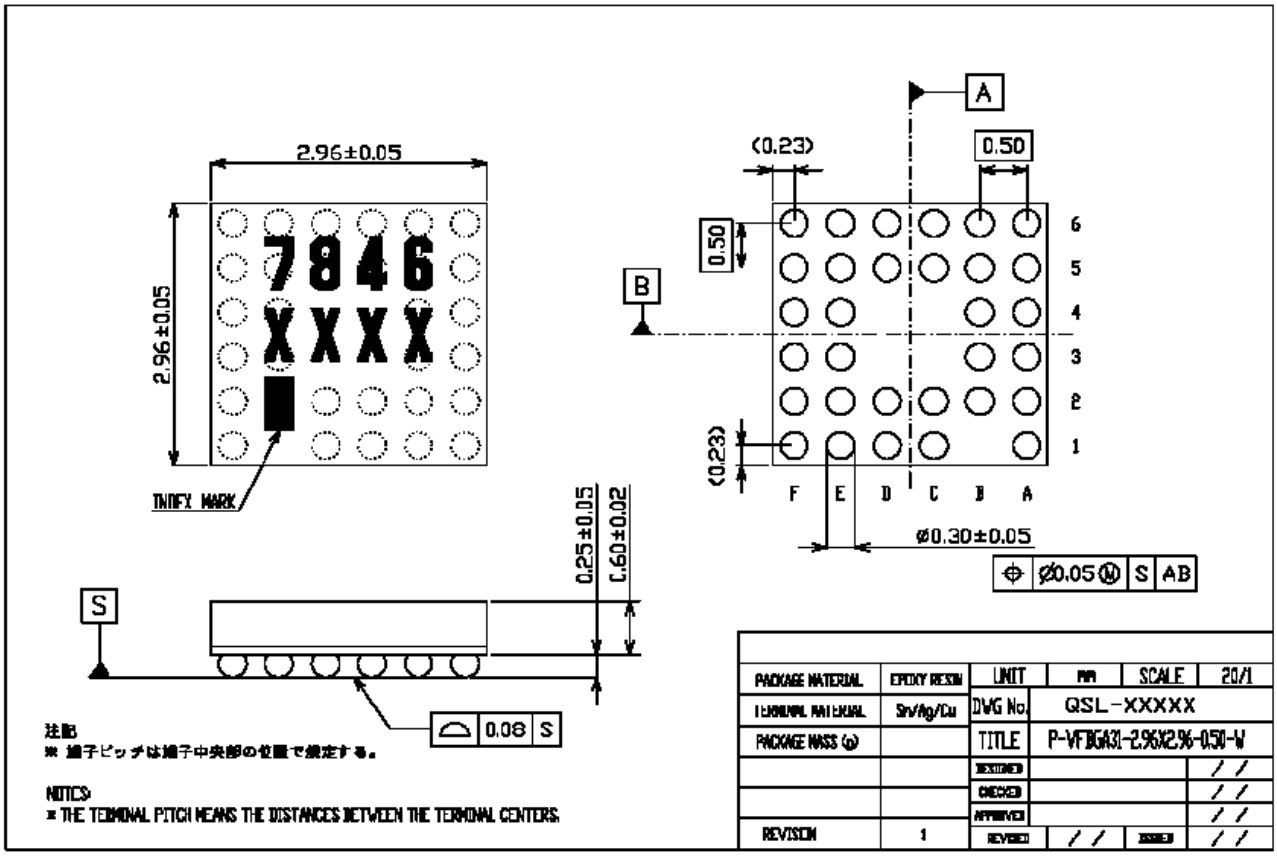
## PACKAGE

### ■ MARKING




XXXX : Date code (4 digit)

### ■ 31pin WL-CSP Package Outline (Unit : mm)



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