Differential Zero Delay Clock Buffer
AK8122

Features

- **Operational Frequency Range:**
  - **160MHz – 400MHz**
- **Output delay:**
  - **-30 ±100ps**
- **Low Jitter Performance:**
  - **20 ps (Period RMS 190 – 360MHz)**
  - **30 ps (cycle – cycle RMS 190 – 360MHz)**
  - **70 ps (Half Period RMS 190 – 250MHz)**
  - **60 ps (Half Period RMS 250 – 300MHz)**
  - **40 ps (Half Period RMS 300 – 360MHz)**
- **Supply Voltage:**
  - **1.8 ±0.1V**
- **Operating Temperature Range:**
  - **-20 to +85℃ : AK8122E**
  - **-40 to +85℃ : AK8122V**
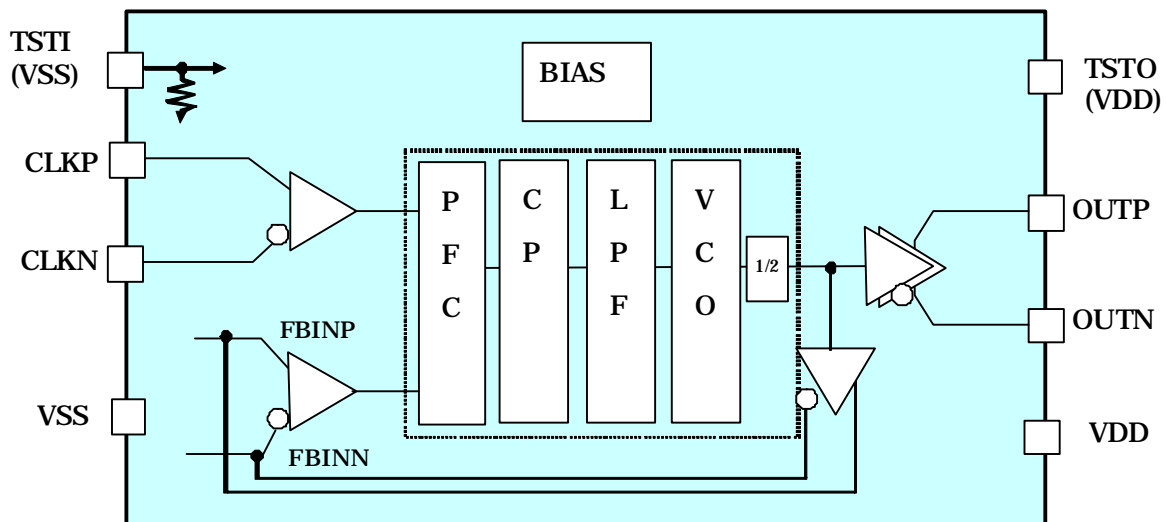- **Package:**
  - **8-pin MSOP(Lead Free)**

Description

The AK8122 is a high performance differential zero delay clock buffer IC with Phase Locked Loop (PLL). Target application is DDR2 SDRAM and characteristics of these ICs are acceptable to standards of JEDEC.
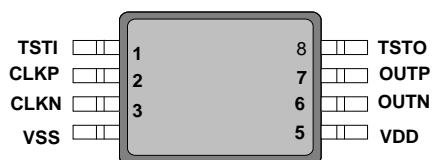
Applications

- DDR2 SDRAM Clock Buffer

Block Diagram

AK8122 Differential Zero Delay Clock Buffer

Pin Descriptions

Pin		
TSTI	1	8 TSTO
CLKP	2	7 OUTP
CLKN	3	6 OUTN
VSS	4	5 VDD

Package: 8-Pin MSOP (Top View)

Pin No.	Pin Name	Pin Type	Description	
1	TSTI	IN	IC Test pin (Input) Please tie VSS to this pin.	(1)
2	CLKP	IN	Differential Clock Input (Positive)	
3	CLKN	IN	Differential Clock Input (Negative)	
4	VSS	--	Ground	
5	VDD	--	Power Supply	
6	OUTN	OUT	Differential Clock Output (Negative)	(2)
7	OUTP	OUT	Differential Clock Output (Positive)	(2)
8	TSTO	OUT	IC Test pin (Output) Please tie VDD to this pin.	(3)

(1) Internal pull down $100k\Omega$ (Typ,)

(2) Output will be "L" level If CLKP = CLKN = "L". Output clock frequency will be lower than 400MHz if CLKP and CLK N are fixed as "H" and "L" (or "L" and CLKN="H"), respectively. Setting CLKP = CLKN = "H" is prohibited.

(3) Output status is Hi-z for normal operation.

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8122V	122V	Tape and Reel	8-pin MSOP	-40 to 85 ℃
AK8122E	122E	Tape and Reel	8-pin MSOP	-20 to 85 ℃

The brand name
of AKEMD's IC's

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted [1]

Items	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to 4.6	V
Input Voltage	Vin	VSS-0.3 to VDD+0.3	V
Input Current (any pins except supplies)	I_{IN}	±10	mA
Storage Temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only.   Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage.   AKEMD recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature 1	Ta1		-40		85	°C
Operating Temperature 2	Ta2		-20		85	°C
Supply Voltage	VDD		1.7	1.8	1.9	V
Input Frequency			160		400	MHz
High Level Input Voltage	V_{IH}	Pin: CLKP, CLKN	0.65VDD			V
Low Level Input Voltage	V_{IL}	Pin: CLKP, CLKN			0.35VDD	V
DC Differential Input Voltage	VIDC	Pin: CLKP, CLKN	0.3			V
AC Differential Input Voltage	VIAC	Pin: CLKP, CLKN	0.6		VDD -0.4	Vpp
Differential Input Reference Voltage	VIREF		0.5VDD -0.15		0.5VDD +0.15	V
Input Slew Rate	ISR		1		4	V/ns

DC Characteristics

All specifications at VDD: over 1.7 to 1.9V, Ta=Ta1(AK8122V) Ta=Ta2(AK8122E)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Current	I_L	Pin: CLKP, CLKN	-10		+10	μA
Differential Output Reference Voltage	VOREF	Pin: OUTP, OUTN	0.5VDD -0.1		0.5VDD +0.1	V
AC Differential Output Voltage [1]	VOAC	Pin: OUTP, OUTN Output Load: Fig.1	0.5		VDD-0.4	V
High Level Output Voltage	V_{OH}	Pin: OUTP, OUTN I_{OH}=-1mA	VDD -0.1			V
Low Level Output Voltage	V_{OL}	Pin: OUTP, OUTN I_{OL}=+1mA			0.1	V
Input Load Capacitance		Pin: CLKP, CLKN		2.1		pF
Input Load Capacitance error		Pin: CLKP, CLKN		0.1		pF
Current Consumption [1]	I_{DD}	[2]		50		mA

(1) See Fig.8 for output load reference.

(2) Output impedance of 60-ohm. No load. VDD = 1.8V, Ta = 25.

AC Characteristics

All specifications at VDD: over 1.7 to 1.9V, Ta: -20 to +85℃, unless otherwise noted

| Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Frequency			160		400	MHz
Output Slew Rate [5]			1		3	V/ns
Input Clock Duty Cycle			40	50	60	%
Delay Time [1]		SFO + DFO + SKEW 250MHz-400MHz	-130	-30	+70	ps
Output Clock Jitter	Jit 1	Period, 1σ, 190–360MHz [2]			20	ps
	Jit 2	Cycle-to-cycle, 1σ, 190–360MHz [3]			30	ps
	Jit 3	Half Period, 1σ, 190–250MHz [4]			70	ps
	Jit 4	Half Period, 1σ, 250–300MHz [4]			60	ps
	Jit 5	Half Period, 1σ, 300–360MHz [4]			40	ps
Start up Time [6]	t_{lock}				200	us

(1) See Fig.1.

(2) See Fig.2.

(3) See Fig.3.

(4) See Fig.4.
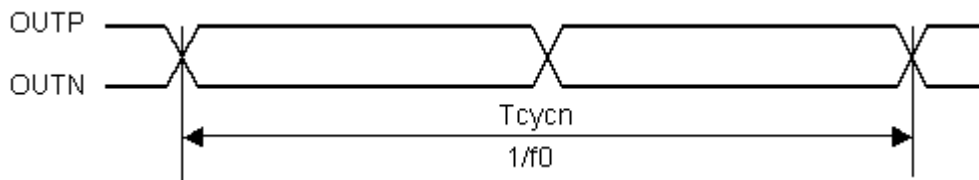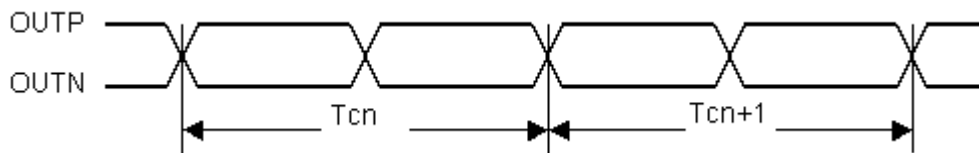
(5) See Fig.8.

(6) A provisional target value.

Standards of Jitter
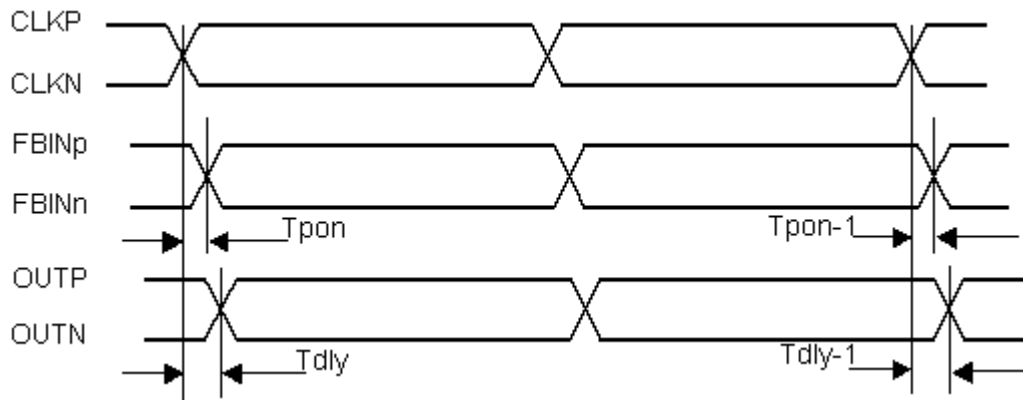
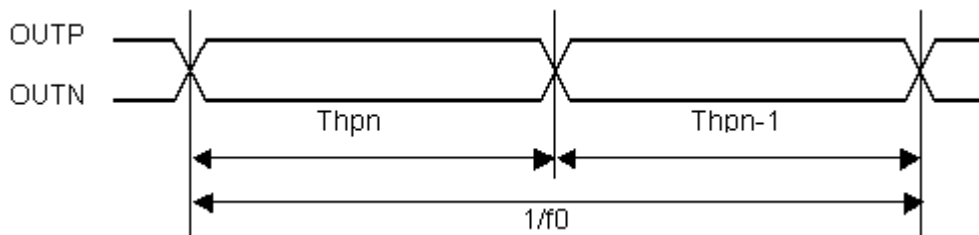

Fig.1 Delay (Static Phase Offset + Skew) : Tdly = ΣTdly/N

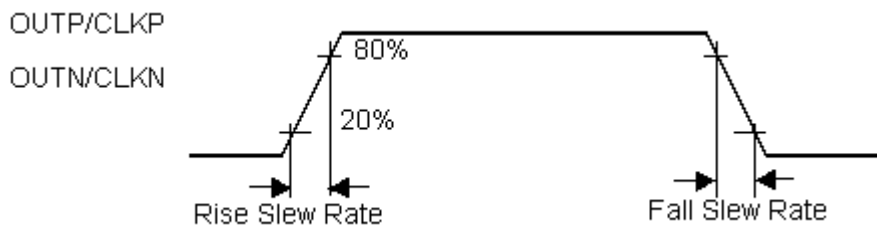**Fig.2 Period jitter: Tpj = Tcycn − 1/f0**

Fig.3 Cycle to cycle jitter: Tc2cj=Tcn-Tcn+1
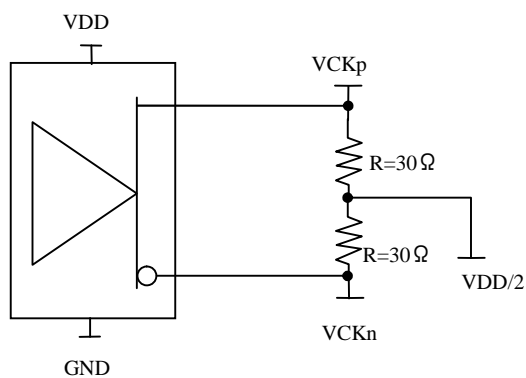

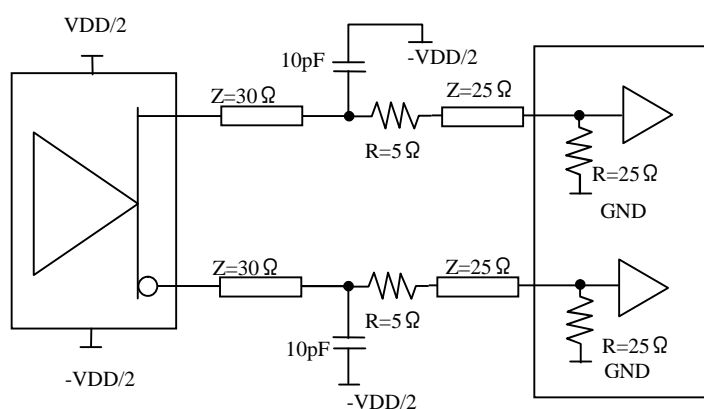**Fig.4 Half period jitter: Thpj = Thp − 1/2*f0**
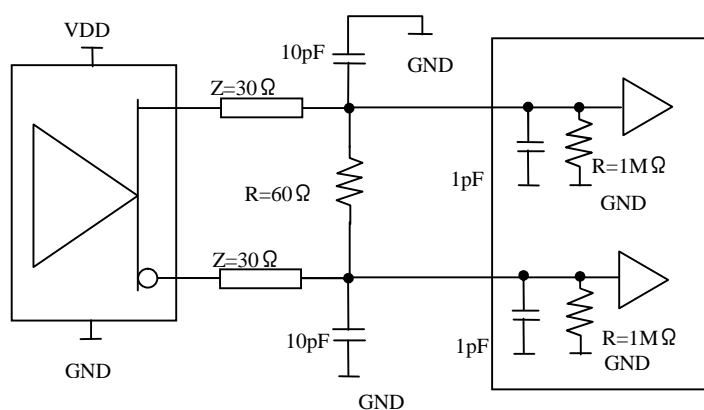

Fig.5 Input and Output Slew Rate

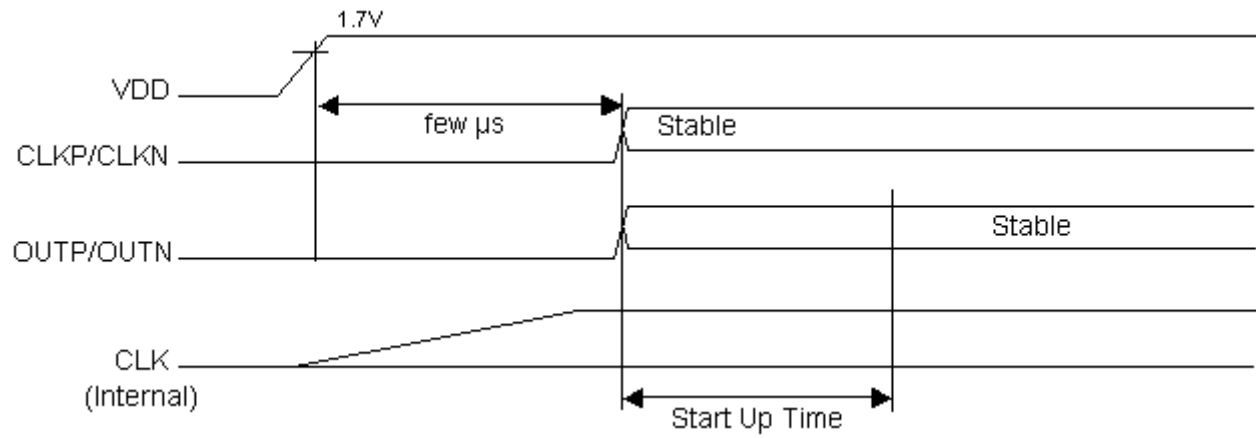## Measurement Condition

Fig.6 IBIS Model Output Load

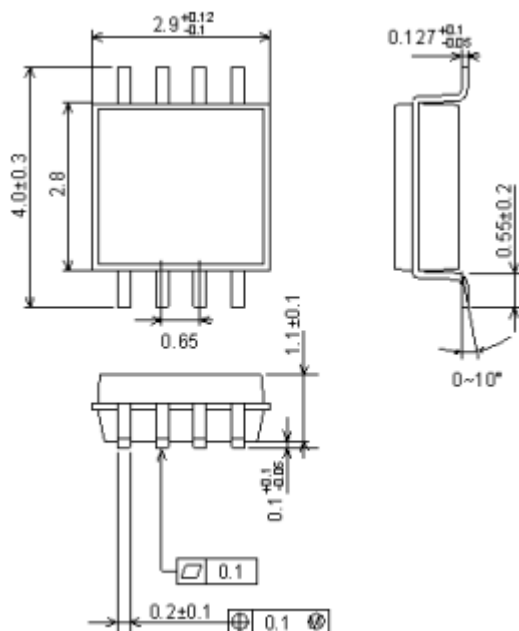**Fig.7 Output Load Test Circuit 1**

Fig.8 Output Load Test Circuit 2
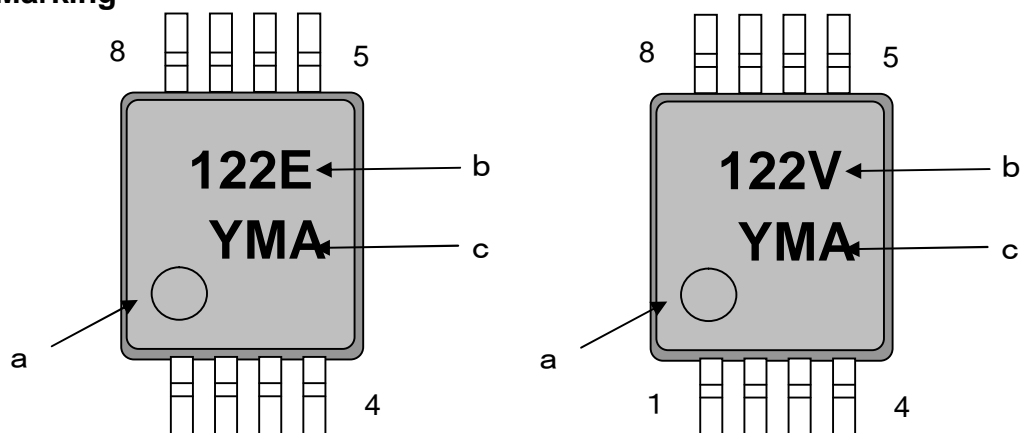
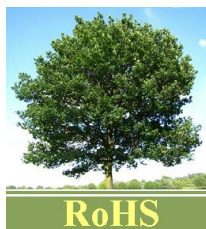## Assumed Power Up Sequence

Package Information

- **Mechanical data**

- **Marking**

    a: #1 Pin Index
    b: Part number
    c: Date code (3 digits)

- **RoHS Compliance**

All integrated circuits form Asahi Kasei EMD Corporation (AKEMD) assembled in "lead-free" packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKEMD are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

IMPORTANT NOTICE

I   These products and their specifications are subject to change without notice.
When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei EMD Corporation (AKEMD) or authorized distributors as to current status of the products.

I   AKEMD assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of any information contained herein.

I   Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.

I   AKEMD products are neither intended nor authorized for use as critical components[Note1] in any safety, life support, or other hazard related device or system[Note2], and AKEMD assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKEMD. As used here:

   Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.

   Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.

I   It is the responsibility of the buyer or distributor of AKEMD products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKEMD harmless from any and all claims arising from the use of said product in the absence of such notification.