Preliminary Low Power Multiclock Generator with VCFS AK8135S

Features

- 30.000MHz Crystal Input
- One 30.000MHz-Reference Output
- Selectable Clock out Frequencies:
  - 25.000 MHz at CLK1
  - 30.000 MHz at CLK2
  - 33.000 MHz at CLK3-5
  - 27.000 MHz at REF1-3
- Built-in two VCFS
  - VCFS1 Pull Range: ±120ppm (typ.)
  - VCFS2 Pull Range: ±135ppm (typ.)
- Low Jitter Performance
  - Cycle to Cycle Jitter:
    33.3 psec (Max.) at CLK1
    50 psec (Typ.) at CLK2-5
  - Period Jitter:
    25 psec (Typ.) at REF1-3
  - Long term jitter:
    66.7 psec (Typ.) at REF1-3
- Low Current Consumption:
  (29) mA (Typ.) at 3.3V
- Supply Voltage:
  3.0 – 3.6V
- Operating Temperature Range:
  -20 to +85℃
- Package:
  48-pin LQFP (Lead free)

Description

AK8135S is a member of AKM's low power multi clock generator family designed for Recorders, DTVs or STBs, requiring a range of system clocks with high performance. AK8135S generates different frequency clocks from a 30.000MHz crystal oscillator and provides them to eight outputs. Th e on-chip VCFS (Voltage Controlled Frequency Synthesizer) accepts a voltage control input to allow the output clocks to vary by ±120/135 ppm for synchronizing to the external clock system.
Both circuitries of VCFS and PLL in AK8135S are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption.
AK8135S is available in a 48-pin LQFP package.

Applications

- HDD, DVD, BD Recorder
- DTV
- Set-Top-Boxes

Block Diagram

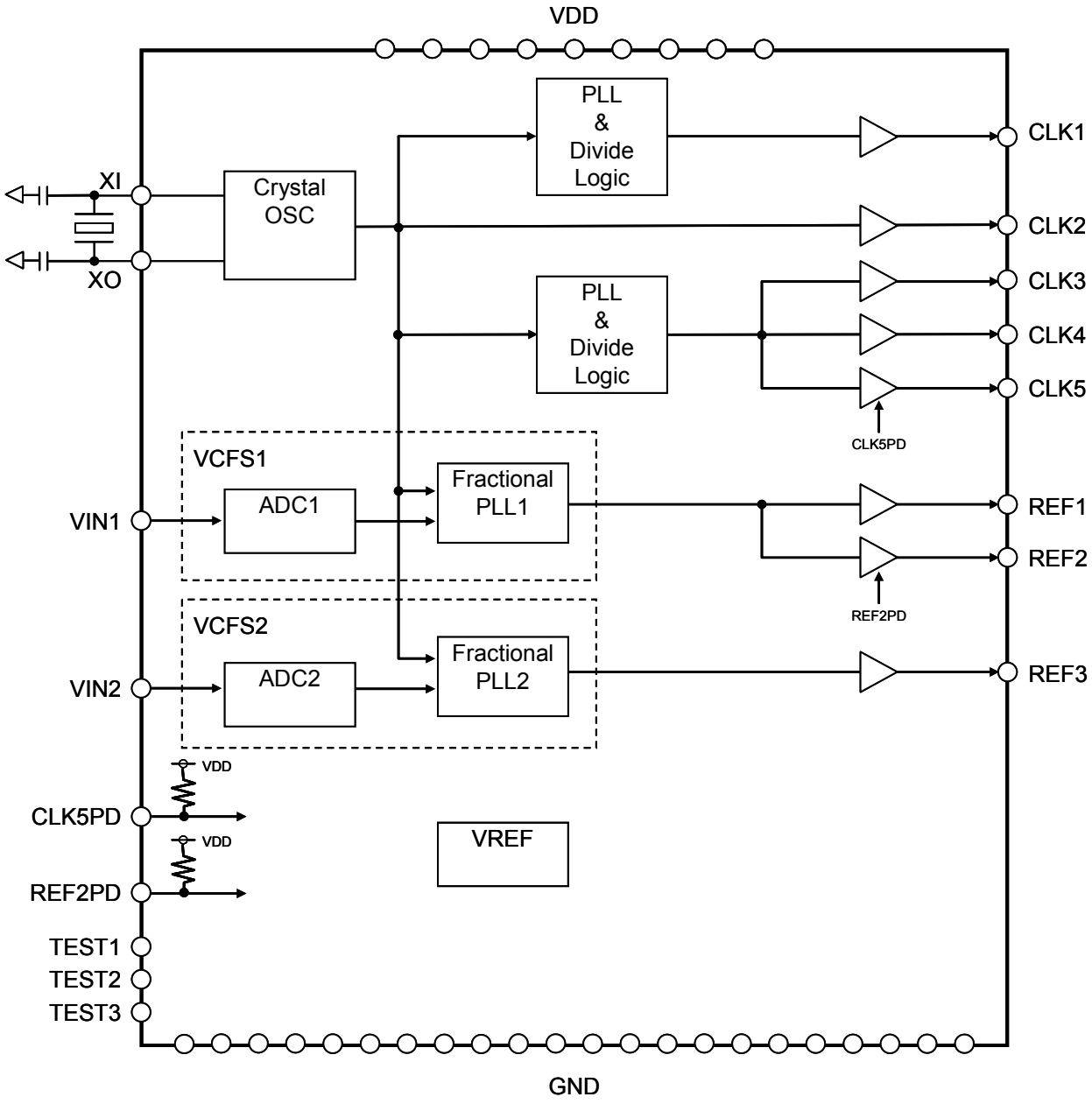


Figure 1: AK8135S Multi Clock Generator

Pin Descriptions

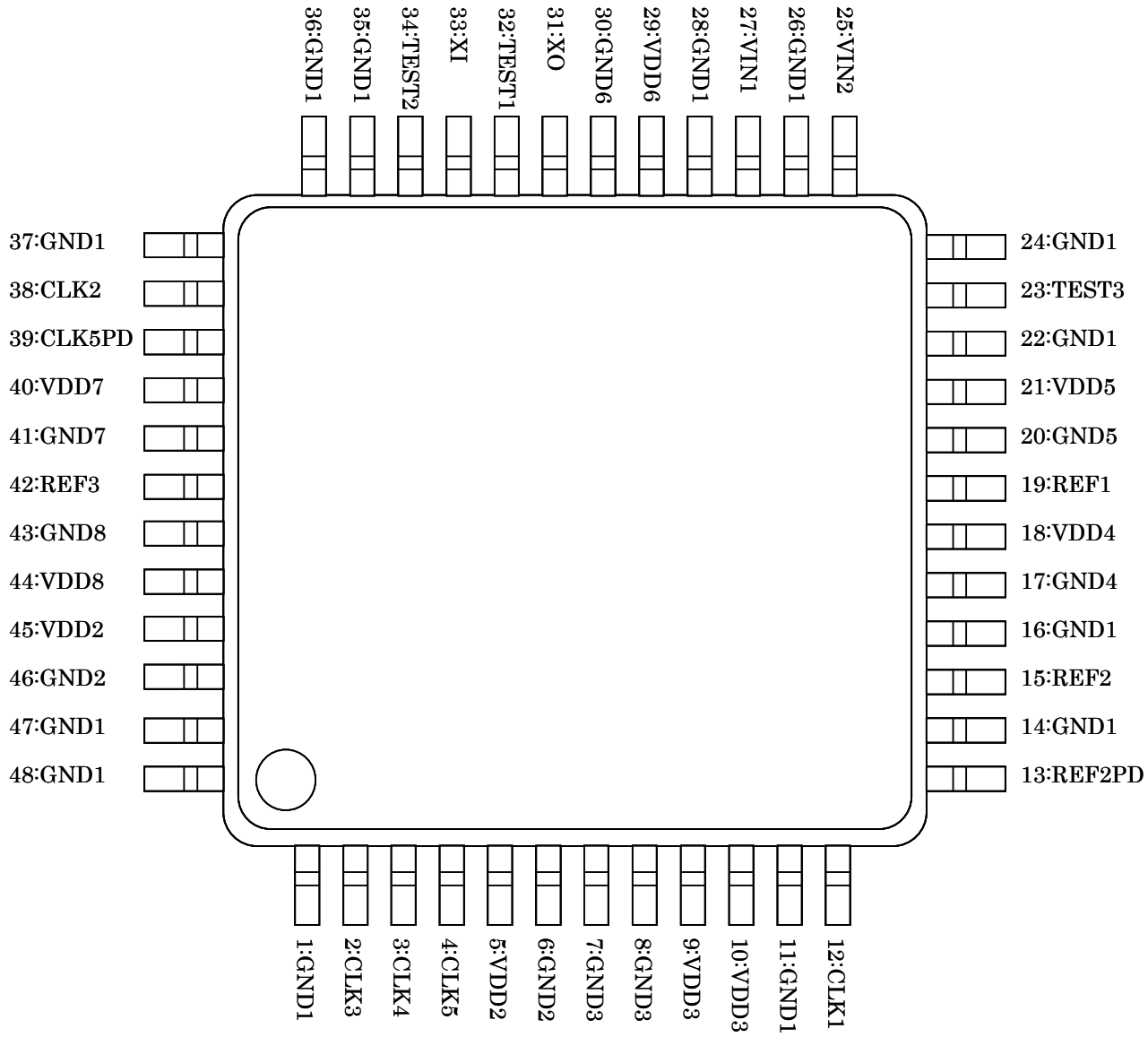


Figure 2: Package: 48-Pin LQFP(Top View)

Pin No.	Pin Name	Pin Type	Description
1	GND1	PWR	Ground 1
2	CLK3	DO	Clock output 3, Output frequency is 33.000MHz.
3	CLK4	DO	Clock output 4, Output frequency is 33.000MHz.
4	CLK5	DO	Clock output 5, Output frequency is 33.000MHz. When CLK5PD pin = “H”, Output frequency is 33.000MHz. When CLK5PD pin = “L”, this pin is “L” output.
5	VDD2	PWR	Power Supply 2
6	GND2	PWR	Ground 2
7	GND3	PWR	Ground 3
8	GND3	PWR	Ground 3
9	VDD3	PWR	Power Supply 3
10	VDD3	PWR	Power Supply 3
11	GND1	PWR	Ground 1
12	CLK1	DO	Clock output 1, Output frequency is 25.000MHz.
13	REF2PD	DI	REF2 pin Mode Select pin “H”: Enable, REF2 pin output 27.000MHz. (1) “L”: Disable, REF2 pin is “L” output.
14	GND1	PWR	Ground 1
15	REF2	DO	Reference Clock Output 2 from VCFS1 When REF2PD pin = “H”, Output frequency is 27.000MHz. When REF2PD pin = “L”, this pin is “L” output.
16	GND1	PWR	Ground 1
17	GND4	PWR	Ground 4
18	VDD4	PWR	Power Supply 4
19	REF1	DO	Reference Clock Output 1 from VCFS1, Output frequency is 27.00MHz.
20	GND5	PWR	Ground 5
21	VDD5	PWR	Power Supply 5
22	GND1	PWR	Ground 1
23	TEST3	D I	TEST input pin, Connect to GND.
24	GND1	PWR	Ground 1
25	VIN2	AI	VCFS2 Control Voltage Input
26	GND1	PWR	Ground 1
27	VIN1	AI	VCFS1 Control Voltage Input
28	GND1	PWR	Ground 1
29	VDD6	PWR	Power Supply 6
30	GND6	PWR	Ground 6
31	XO	A O	Crystal connection, Connect to 30.000MHz crystal.
32	TEST1	D I	TEST input pin, Connect to GND.
33	XI	AI	Crystal connection, Connect to 30.000MHz crystal.
34	TEST2	D I	TEST input pin, Connect to GND.
35	GND1	PWR	Ground 1
36	GND1	PWR	Ground 1
37	GND1	PWR	Ground 1

38	CLK2 DO		Reference Clock Output of XO based on 30.000MHz Crystal
39	CLK5PD	DI	CLK5 pin Mode Select pin "H": Enable, REF1 pin outputs 33.000MHz. "L": Disable, CLK5 pin is "L". (1)
40	VDD7 PWR		Power Supply 7
41	GND7 PWR		Ground 7
42	REF3	DO	Reference Clock Output 3 from VCFS2 Output frequency is 27.00MHz.
43	GND8 PWR		Ground 8
44	VDD8 PWR		Power Supply 8
45	VDD2 PWR		Power Supply 2
46	GND2 PWR		Ground 2
47	GND1 PWR		Ground 1
48	GND1 PWR		Ground 1

(1) Internal pull up 57kΩ

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8135S	AK8135S	Tape and Reel	48-pin LQFP	-20 to 85℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items Sy	mbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	VIN	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	IIN	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter Sy	mbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage(1)	VDD	Pin: VDD2-8	3.0	3.3	3.6	V
Output Load Capacitance	Cpl	Pin: CLK1-5, REF1-3			15	pF

Note:

(1) Power to VDD2-8 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pin.

DC Characteristics

VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 30MHz Crystal, unless otherwise noted

Parameter Sy	mbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: CLK5PD, REF2PD, TEST1-3	0.7VDD			V
Low Level Input Voltage	V_{IL}	Pin: CLK5PD, REF2PD, TEST1-3			0.3VDD	V
Input Current 1	I_L1	Pin: CLK5PD, REF2PD	-134 -58		+1	μA
Input Current 2	I_L2	Pin: TEST1-3	-1		+1	μA
Input Current 3	I_L3	Pin: VIN1, VIN2	-3		+3	μA
High Level Output Voltage	V_{OH}	Pin: CLK1-5, REF1-3 I_{OH}=-4mA	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: CLK1-5, REF1-3 I_{OL}=+4mA			0.2VDD	V
Current Consumption	I_{DD}	No load CLK5PD='H', REF2PD='H'	(29)		TBD	mA

AC Characteristics

VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 30MHz Crystal, unless otherwise noted

Parameter Sy	mbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency (1)	F_{osc} Pin:XI,	XO		30.000		MHz
Output Clock Accuracy (1)	$F_{accuracy}$	Pin:CLK1 25.000MHz Crystal CL=8[pF]	-30	0 +	30	ppm
		Pin:CLK2 30.000MHz Crystal CL=8[pF]	-30	0 +	30	ppm
		Pin:CLK3-5 33.000MHz Crystal CL=8[pF]	-30	0	+30	ppm
		Pin:REF1-3 27.000MHz VIN1/VIN2=0.5VDD Crystal CL=8[pF]	-30	0	+30	ppm
VCFS Pullable Range	PR_{VCFS}	Pin:REF1-2 VIN1=0.0V～VDD	±90	±120		ppm
		Pin:REF3 VIN2=0.0V～VDD	±105	±135		ppm
VCFS Response Time	RT_{VCFS}	Pin:REF1-3 VIN1/VIN2=0.5VDD±1.0		31		ppm/100ms
C/N CN		Pin:REF1-3 with Load Cpl=15pF	72			dB
Output Clock Rise Time	$T_{\_rise}$	Pin:CLK1-5, REF1-3 with Load Cpl=15pF 0.2VDD → 0.8VDD	1.5		4.0	ns
Output Clock Fall Time	$T_{\_fall}$	Pin:CLK1-5, REF1-3 with Load Cpl=15pF 0.8VDD → 0.2VDD	1.5		4.0	ns
Cycle to Cycle Jitter (2) Jit	_Cycle	Pin:CLK1 with Load Cpl=15pF			33.3	ps
		Pin:CLK2-5 with Load Cpl=15pF	50			ps
Period Jitter (2) Jit	_period	Pin:REF1-3 with Load Cpl=15pF	25		TBD	ps
Long Term Jitter (2) Jit	_long	Pin:REF1-3 with Load Cpl1=15pF 1000 cycle delay	66.7		TBD	ps
Output Clock Duty Cycle	DtyCyc	Pin:CLK2 with Load Cpl1=15pF	42	50 58		%
		Pin: CLK1, 3-5, REF1-3 with Load Cpl1=15pF	45	50 55		%
Power-up Time (3)	$T_{\_put}$	Pin:CLK1-5, REF1-3 with Load Cpl1=15pF	1			ms

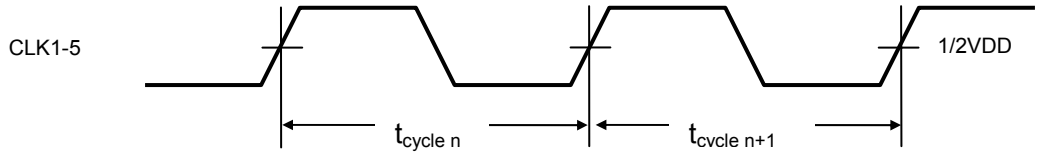
(1) Output Clock Accuracy depends on crystal characteristics, on-chip load capacitance, and stray capacity of PCB. MIN., Max.=±30ppm is applied to AKM's authorized test condition.
Please contact us when you plan the use of other crystal unit.

(2) 1σ in 10000 sampling or more

(3) Time to settle output into 0.1% of specified frequency.

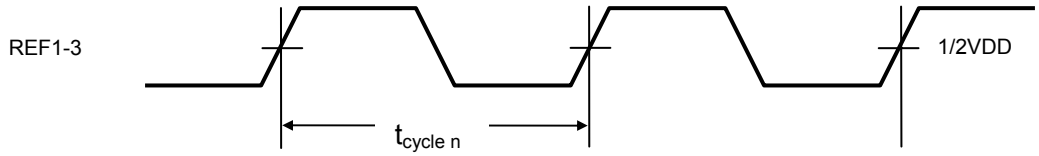
Definition of Jitter

1. Cycle to cycle jitter: The variation in cycle time of a single between adjacent cycles, over a random sample of adjacent cycle pairs.



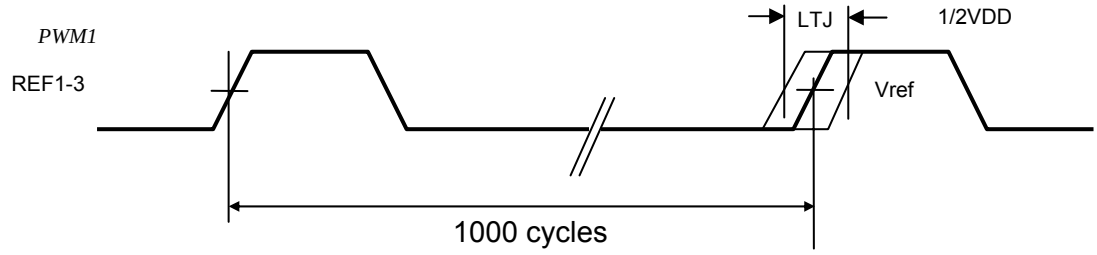
Jit_{cycle} = ($t_{cycle\ n}$ - $t_{\ cycle\ n+1}$) : where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges.

2. Period jitter: The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles. pairs.



Jit_{period} = $t_{\ cycle\ n}$ - 1 / f0 : where f0 is the nominal output frequency and *t*cycle n is any cycle within the sample measured on controlled edges

3. Long Term jitter:



1000Cycles after oscilloscope trigger.

Function Description

Voltage Controlled Frequency Synthesizer (VCFS)

AK8135S has a voltage controlled frequency synthesizer (VCFS), featuring fine frequency tuning for 27MHz of primary clock frequency by external DC voltage control. This tuning enables output clock frequency to synchronize the external clock system.
VCFS is composed of analog-to-digital converter and high resolution PLL as shown in Figure 3. VIN1 (Pin27) and VIN2 (Pin25) accept DC voltage control from a processor or a system controller, and pulls the primary frequency of crystal to higher or lower. This pulling range is determined by supply Voltage to AK8135S. AK8135S is designed to range ±120/135ppm of primary frequency, and the typical pulling profile is shown in Figure 4.

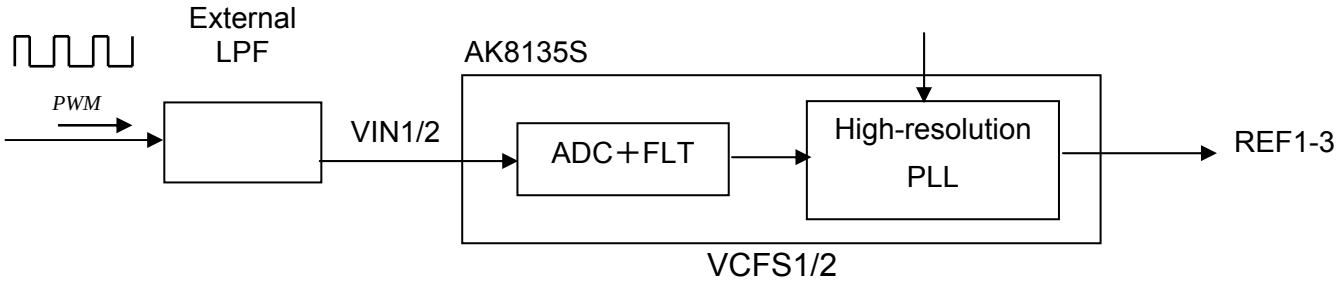


Figure 3: VCFS Diagram

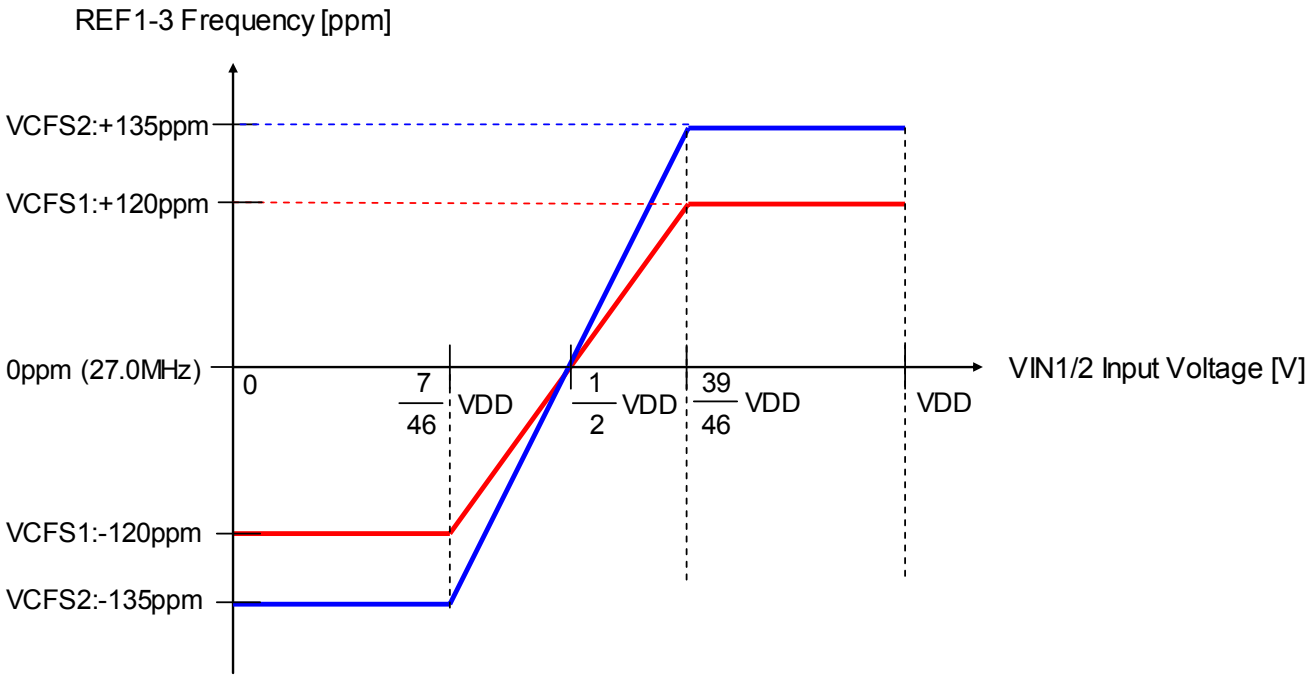


Figure 4: Typical VCFS Pulling Profile

Typical Connection Diagram

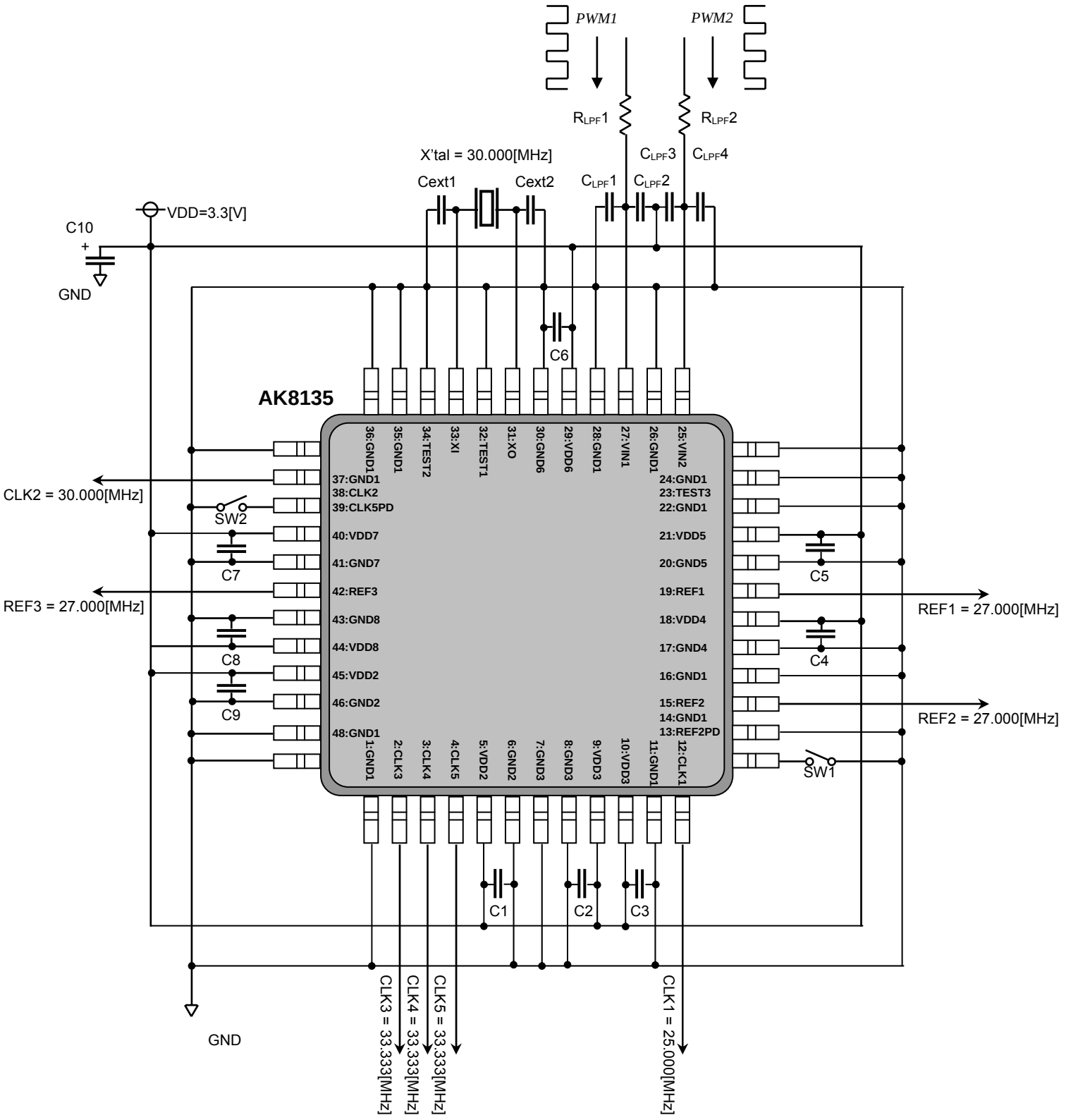


Figure 5: Typical Connection Diagram

C1, C2, C3, C4, C5, C6, C7, C8, C9: 0.1µF
C10 : Electrolytic capacitor
Cext1, Cext2: Depends on crystal characteristics. Refer the specification of the crystal.
SW1, SW2: It is a switch that controls outputs of CLK5 and REF2.
$R_{LPF}1$, $R_{LPF}2$, $C_{LPF}1$, $C_{LPF}2$, $C_{LPF}3$, $C_{LPF}4$: In case of interface by PWM. For right configuration, refer the specification of the applied processor.

PCB Layout Consideration

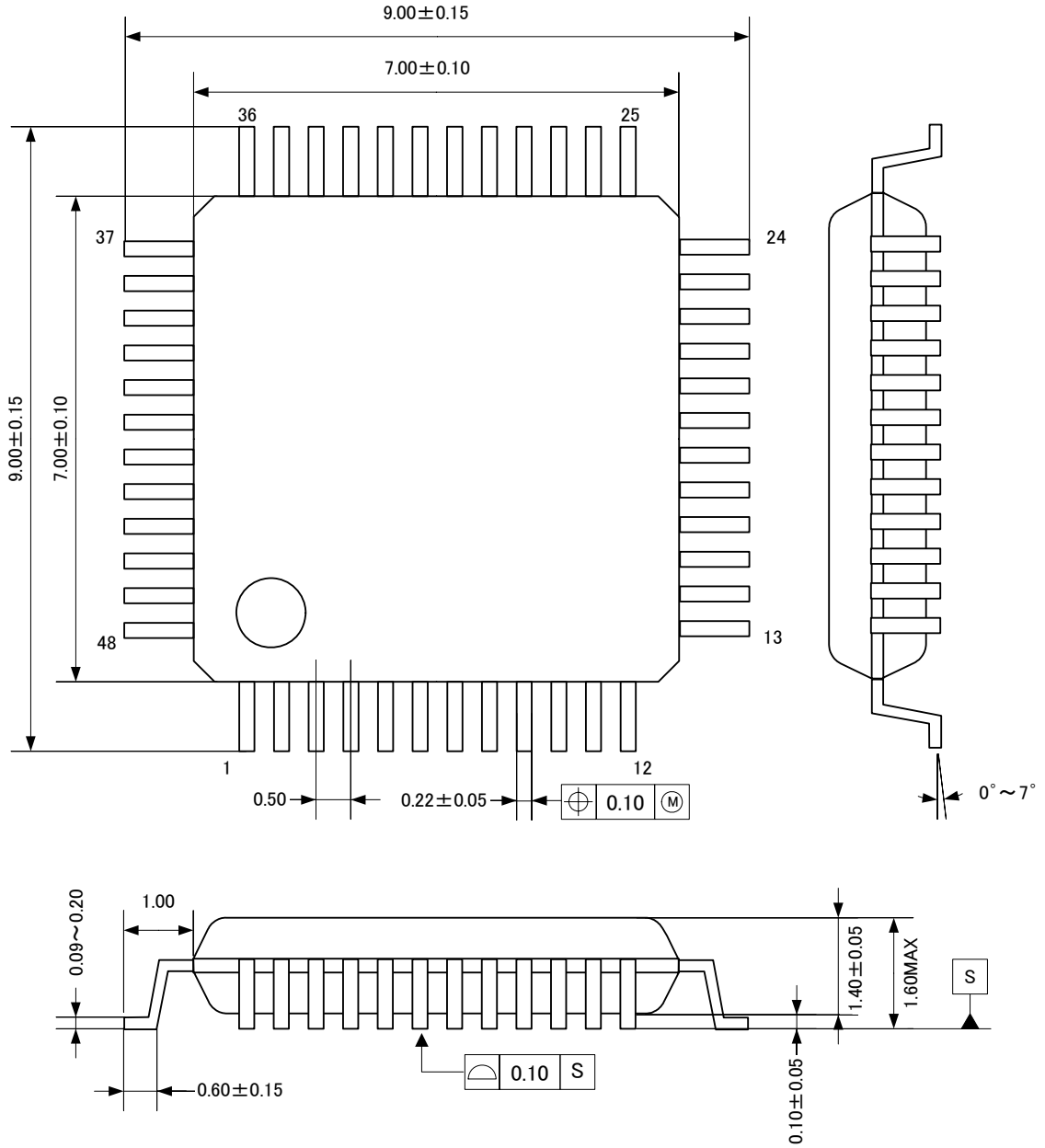
AK8135S is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 5

Power supply line – AK8135S has nine power supply pins (VDD2-8) which deliver power to internal circuitry segments. A 0.1μF decoupling capacitor should be placed as close to each VDD pin as possible.

Ground pin connection – AK8135S has 22 ground pins (GND1-8). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. 0.1μF decoupling capacitors placed at VDD2, VDD3, VDD4, VDD5, VDD6, VDD7 and VDD8 should be grounded at close to the GND2 pin, the GND3 pin, the GND4 pin, the GND5 pin, the GND6 pin, the GND7 and the GND8 pin respectively.

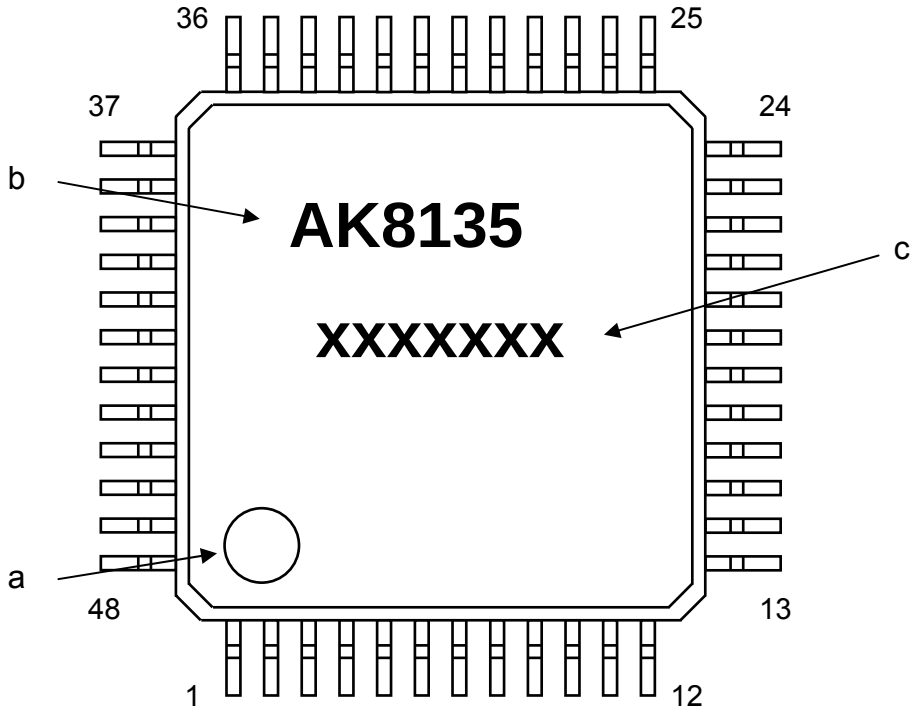
Crystal connection – Proper oscillation performance is susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form XI (Pin 33) and XO (Pin 31) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

Package Information

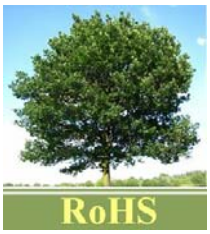


- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (7 digits)



- **RoHS Compliance**



All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in “lead-free” packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.
- Descriptions of external circuits, application circuits, software and other related information contained in this document are provided only to illustrate the operation and application examples of the semiconductor products. You are fully responsible for the incorporation of these external circuits, application circuits, software and other related information in the design of your equipments. AKM assumes no responsibility for any losses incurred by you or third parties arising from the use of these information herein. AKM assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of such information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components$_{Note1)}$ in any safety, life support, or other hazard related device or system$_{Note2)}$, and AKM assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKM. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.