=Preliminary=

26MHz Clock Source Multi Clock Generator

AK8139A

Features

- Input:
  Crystal input: 26.000MHz
- Configured output frequency from:
  - CLK1 output: 19.200MHz / 8.000MHz / Off
  - CLK2 output: 12.000MHz / 24.000MHz / Off
  - CLK3 output: 32.768kHz
  - REF output: 26.000MHz / Off
- Output stand-by mode
  *output only CLK3 output
- Low Jitter Performance
  - Period Jitter:
    25 psec (Typ. / 1 σ) at CLK1, 2, REF
  - Cycle to Cycle Jitter:
    30 psec (Typ. / 1 σ) at CLK1, 2, REF
- Low Current Consumption:
  7.9uA (Typ.) at Stand-by mode.
  S1-3="L", no load
  5.4mA (Typ.) at 1.8V, S1-3="H", no load
- Supply Voltage:
  1.8V PLL
  1.8V to 3.3V for Output
- Operating Temperature Range:
  -30℃ to +85℃
- Package:
  20-pin QFN (Lead free, Halogen free)

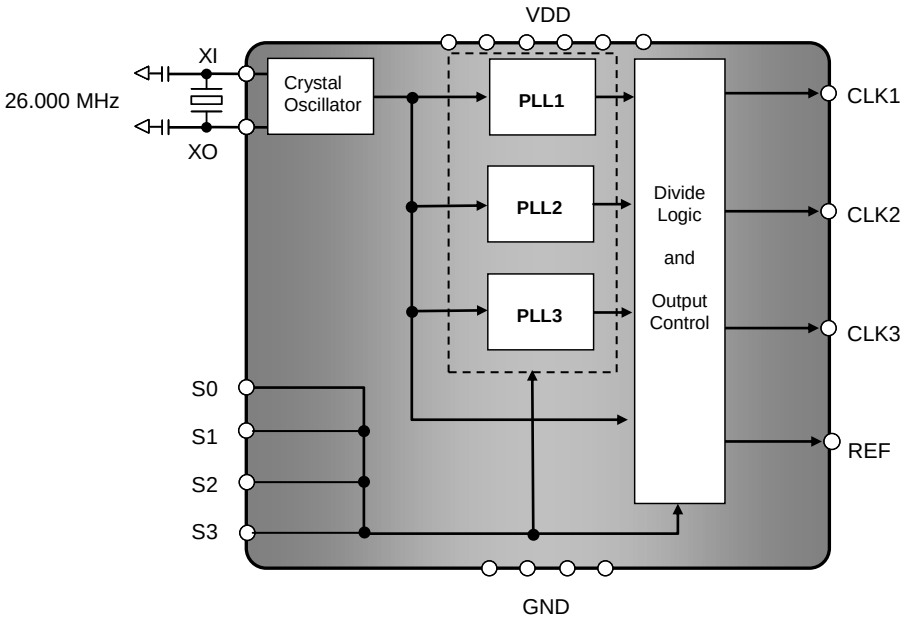
Description

The AK8139A is a member of AKM's low power multi clock generator family designed for digital consumer applications. An AKM's original PLL architecture built in the AK8139A offers low power and low jitter performance enabling a system design to simple and save parts cost. The device operates at 1.8V, and the output voltage can be freely set from 1.8V to 3.3V. And it is supported in a small 20-pin QFN package.

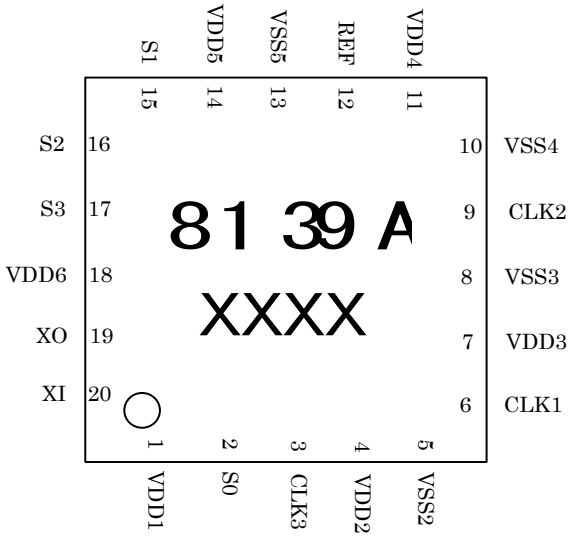
Applications

- Tablet PC
- Digital Video Camcorders
- Digital Still Camera
- Portable system
- Mobile Wi-Fi Router

Block Diagram



Pin Descriptions



Package: 20-Pin QFN(Top View)

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Pin No.	Pin Name	Pin Type	Description
1	VDD1	PWR	Power Supply 1 1.8V
2	S0	DI	Clock Output Frequency setting pin, See Table 1
3	CLK3	DO	Clock output 3, See Table 1
4	VDD2	PWR	Power Supply 2, for CLK1 and CLK3 1.8V to 3.3V
5	VSS2	PWR	Ground 2
6	CLK1	DO	Clock output 1, See Table 1 (1)
7	VDD3	PWR	Power supply 3, for CLK2 1.8V to 3.3V
8	VSS3	PWR	Ground 3
9	CLK2	DO	Clock output 2, See Table 1 (1)
10	VSS4	PWR	Ground 4
11	VDD4	PWR	Power supply 4, for REF 1.8V to 3.3V
12	REF	DO	REF output, See Table 1 (1)
13	VSS5	PWR	Ground 5
14	VDD5	PWR	Power Supply 5 1.8V
15	S1	DI	CLK1 output control pin, See Table 1
16	S2	DI	CLK2 output control pin, See Table 1
17	S3	DI	REF output control pin, See Table 1
18	VDD6	PWR	Power Supply 6 1.8V
19	XO	AO	Crystal Connection (26.000MHz)
20	XI	AI	Crystal Connection (26.000MHz)

(1) Internally pull down by 160kΩ(typ.)

※The heat pad is prepared on its down side of the package. It's needed to connect to ground (VSS).

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8139A	8139A	Tape and Reel	20-pin QFN	-30 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-30		85	°C
Supply voltage (1)	VDD	Pin: VDD1, 5, 6	1.7	1.8	2.0	V
	VDDO	Pin: VDD2, 3, 4	1.7	1.8/3.3	3.6	V
Output Load Capacitance	Cp1	Pin: CLK1, 2, REF			15	pF
	Cp2	Pin: CLK3			25	pF

Note:

(1) Same voltage has to be applied to VDD1, 5 and 6. A decoupling capacitor for power supply line should be installed close to each VDD pin.

DC Characteristics

All specifications at VDD: over 1.7 to 2.0V, VDDO: over 1.7 to 3.6V, Ta: -30 to +85℃, 26.000MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High level input voltage	V_{IH}	Pin: S0-3	0.7VDD			V
Low level input voltage	V_{IL}	Pin: S0-3			0.3VDD	V
Input leak current	I_L	Pin: S0-3	-1	0	+1	μA
High Level output Voltage	V_{OH}	Pin: CLK1, 2, REF I_{OH}=-4mA (@VDDO=3.6V) I_{OH}=-2.18mA (@VDDO=1.7V)	0.8VDDO			V
		Pin: CLK3 I_{OH}=-1.2mA (@VDDO=3.6V) I_{OH}=-0.6mA (@VDDO=1.7V)	0.8VDDO			V
Low level output Voltage	V_{OL}	Pin: CLK1, 2, REF I_{OL}=+4mA (@VDDO=3.6V) I_{OL}=+2.18mA (@VDDO=1.7V)			0.2VDDO	V
		Pin: CLK3 I_{OL}=+1.2mA (@VDDO=3.6V) I_{OL}=+0.6mA (@VDDO=1.7V)			0.2VDDO	V
Current consumption 1 (1)	I_{DD1}	No load, Ta=25℃ S1-3=“L”, S0=”X”		7.9	12	uA
Current consumption 2	I_{DD2}	No load, Ta=25℃ S1-3=”H”, S0=”L”		5.4	9	mA

(1) Average value of intermittent operation.

AC Characteristics

All specifications at VDD: over 1.7 to 2.0V, VDDO: over 1.7 to 3.6V, Ta: -30 to +85℃, 26.000MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal clock frequency		Pin: XI, XO		26.000		MHz
Frequency accuracy (1)		Pin: CLK1, 2, REF	-10		+10	ppm
		Pin: CLK3 (4)		3.13		ppm
Period jitter (1 σ) (2), (3)	Jit_{period}	Pin: CLK1, 2, REF		25		ps
		Pin: CLK3		15		ns
Cycle to cycle jitter (1 σ) (2), (3)	Jit_{cycle}	Pin: CLK1, 2, REF		30		ps
Output clock duty cycle (2)	DtyCyc	Pin: CLK1, 2,	45	50	55	%
		Pin: REF	40	50	60	%
		Pin: CLK3	40	50	60	%
Output clock rise time (2)	t_{rise1}	Pin: CLK1, 2, REF Cp1=15pF, 0.2VDDO→0.8VDDO		1.5	4.0	ns
		Pin: CLK3 VDDO=3.0-3.6V, Cp2=25pF, 0.2VDDO→0.8VDDO		7.0	14.0	ns
		Pin: CLK3 VDDO=1.7-2.0V, Cp2=25pF, 0.2VDDO→0.8VDDO		10.0	20.0	ns
Output clock fall time (2)	t_{fall1}	Pin: CLK1, 2, REF Cp1=15pF, 0.8VDDO→0.2VDDO		1.5	4.0	ns
		Pin: CLK3 VDDO=3.0-3.6V, Cp2=25pF, 0.8VDDO→0.2VDDO		7.0	14.0	ns
		Pin: CLK3 VDDO=1.7-2.0V, Cp2=25pF, 0.8VDDO→0.2VDDO		10.0	20.0	ns
Output lock time	t_{lock}	Pin: CLK1, 2, REF (5)			1	ms
		Pin: CLK3 (6)		30		ms

(1) Additional value through IC. This value is guaranteed only when using AKM's suggested crystal unit. (Refer to page 8)

(2) Design value.

(3) 10000 sampling or more.

(4) Average value, when operating XO.

(5) Time to settle output into ±0.1% of specified frequency after reaching VDD.

(6) Time to initial setup at powered on.

Clock Output Frequency Selection

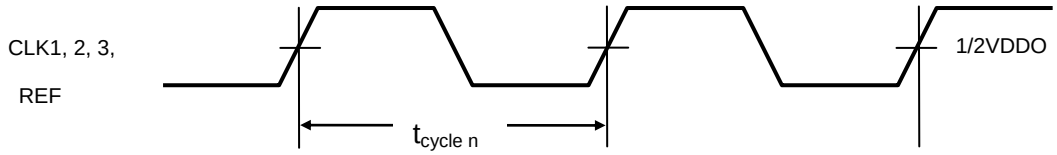
The AK8139A generates a range of low-jitter and high-accuracy clock frequencies with three built-in PLLs and provides to up to four assigned outputs. A frequency selection at assigned output pin is configured by pin-setting of S0-3.
The clock output frequency is shown in Table 1.

Table 1: CLK1, 2, 3, REF Output Frequency

Setting Pin Condition				Crystal Frequency (MHz)	Clock Output Frequency { 32.768 [kHz] another [MHz] }			
S0	S1	S2	S3	XI, XO	CLK1	CLK2	REF	CLK3
X	L	L	L	26.000	L	L	L	32.768
X	L	L	H	26.000	L	L	26.000	32.768
L	L	H	L	26.000	L	24.000	L	32.768
L	H	L	L	26.000	19.200	L	L	32.768
L	L	H	H	26.000	L	24.000	26.000	32.768
L	H	L	H	26.000	19.200	L	26.000	32.768
L	H	H	L	26.000	19.200	24.000	L	32.768
L	H	H	H	26.000	19.200	24.000	26.000	32.768
H	L	H	L	26.000	L	12.000	L	32.768
H	H	L	L	26.000	8.000	L	L	32.768
H	L	H	H	26.000	L	12.000	26.000	32.768
H	H	L	H	26.000	8.000	L	26.000	32.768
H	H	H	L	26.000	8.000	12.000	L	32.768
H	H	H	H	26.000	8.000	12.000	26.000	32.768

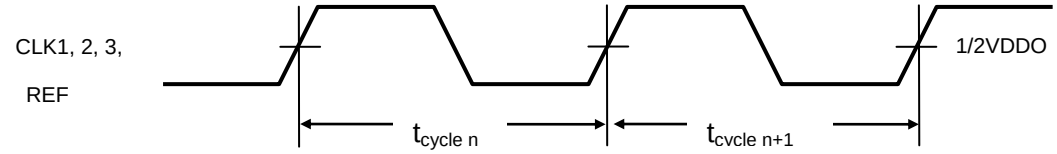
Period Jitter and Cycle to Cycle jitter

1. Period jitter: The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles. pairs.



Jit_{period} = $t_{cycle\ n}$ - 1 / f0 : where fo is the nominal output frequency and *t*cycle n is any cycle within the sample measured on controlled edges

2. Cycle to cycle jitter: The variation in cycle time of a single between adjacent cycles, over a random sample of adjacent cycle pairs.



Jit_{cycle} = | $t_{cycle\ n}$ - $t_{cycle\ n+1}$ | : where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges.

Crystal Unit

NDK NX2520SA

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Nominal frequency	f0		26.000		MHz	CL=8pF
Equivalent resistance	R1		29.0	60	Ω	
Shunt capacitance	C0		0.87		pF	±20%
Motional capacitance	C1		2.40		fF	±20%
Motional inductance	L1		15.6		mH	±20%
Drive Level			30	100	uW	

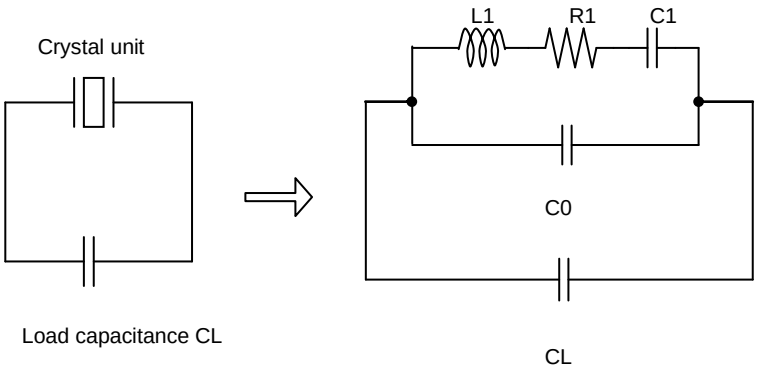


Figure 1: Equivalent parameter and load

Typical Connection Diagram

Package Information

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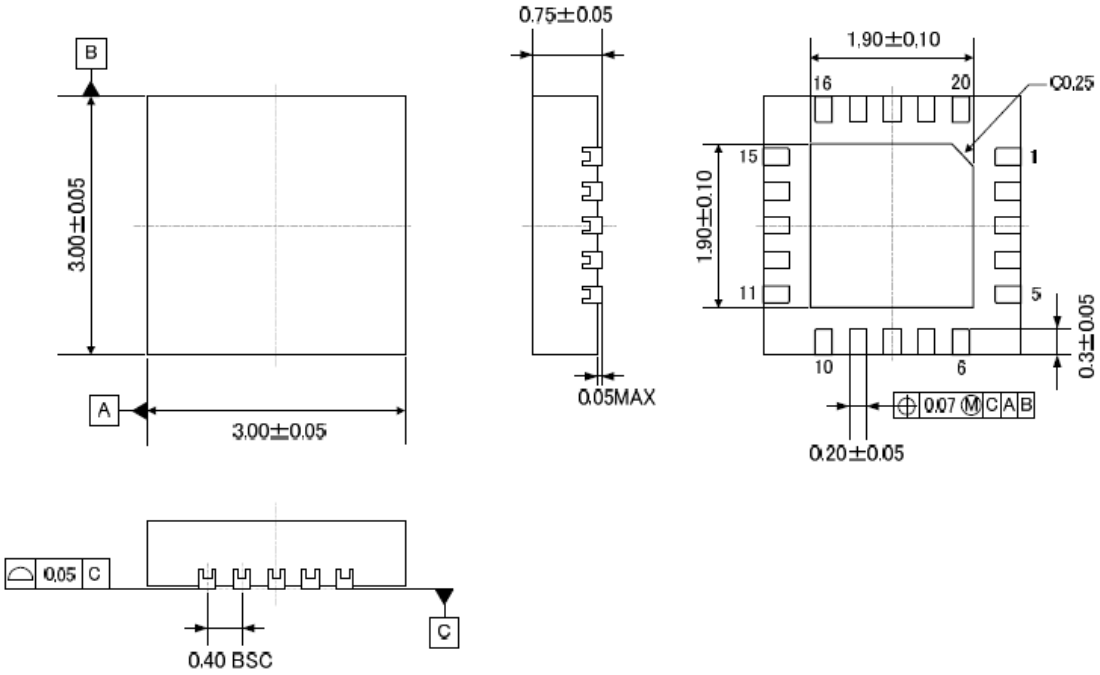
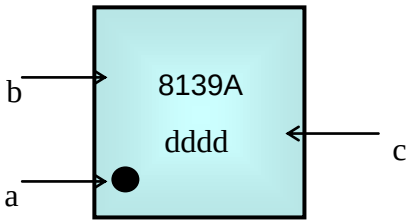
- **Mechanical data**

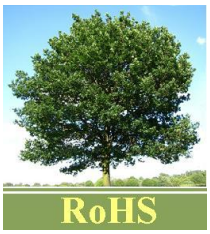


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code : d d d d (4 digits)
- Manufacturing code
- Week code
- Year code

- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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