-Preliminary-

AK8140A

Programmable Clock Generator

Description

AK8140A is AKM's High-performance programmable clock generator.
AK8140A generates up to four output clocks from a single input frequency with two fractional-N PLLs.
Each output can be programmed for any frequency up to 230MHz.
AK8140A is available in a 24-pin ETSSOP package.

Features

- In-system programmability
  serial programmable Register via I2C interface
- High accuracy Clock Generator
- Flexible Input Clock Source
  - Crystal Unit: 16M-60MHz
  - External Clock: 4M-100MHz
- Free Programmable Clock Frequencies
  - LVCMOS: up to 160MHz (CLK1-3)
  - LVDS: up to 230MHz (CLK4)
- Low Jitter Performance
  - Period Jitter (1σ): 8.3 ps(max.)
  - Cycle to Cycle jitter (1σ): 12.8 ps(max.)
  - Long Term Jitter (1000cycle, 1σ): 41.7 ps(max.)
- Supply Voltage:
  - Device power supply
    VDD1-4: 3.0 - 3.6V
  - Output buffer supply
    VDDO1, 2 : 1.7 - 3.6V
- Operating Temperature Range:
  -40 to +85℃
- Package:
  24-pin ETSSOP (Lead free)

Block Diagram

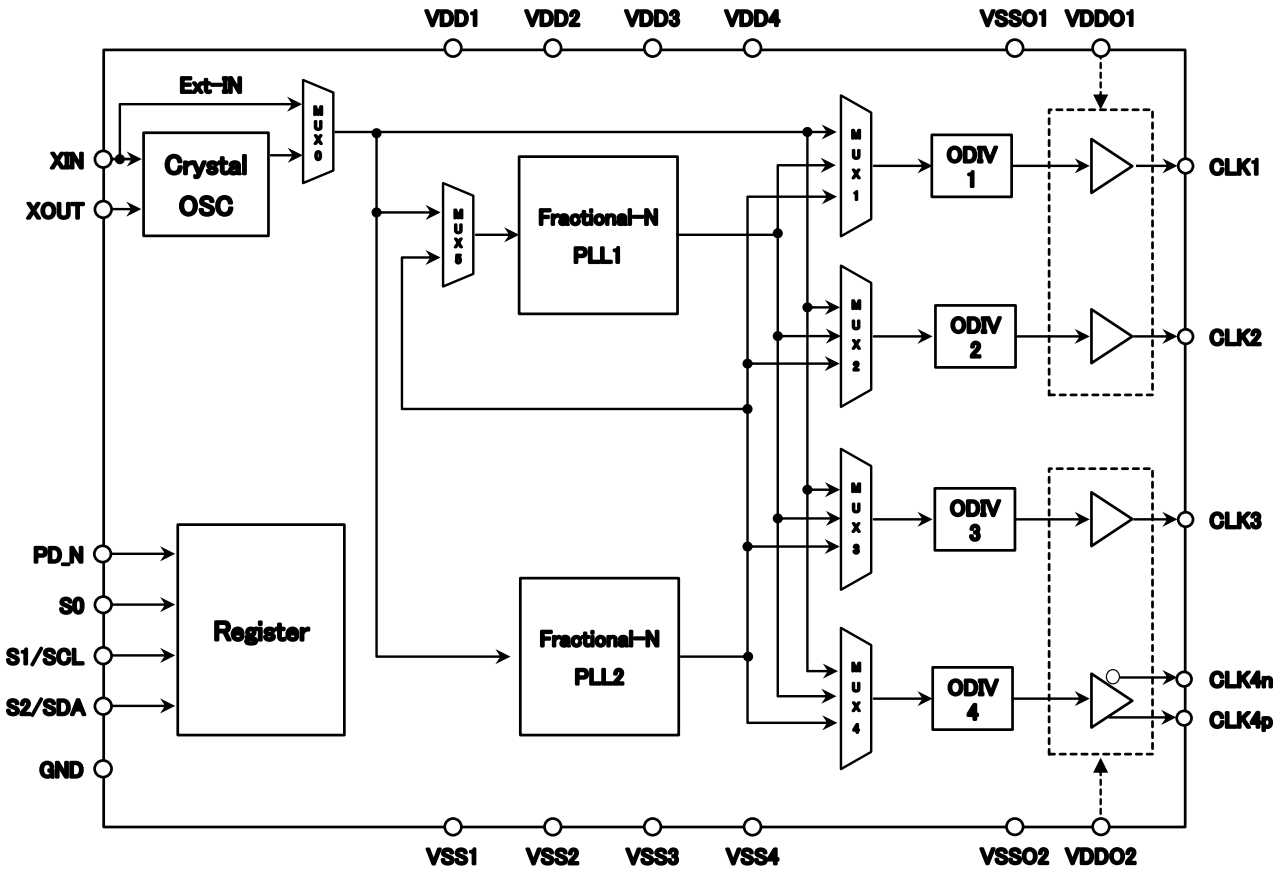


Figure 1: AK8140A Programmable Clock Generator

Pin Descriptions

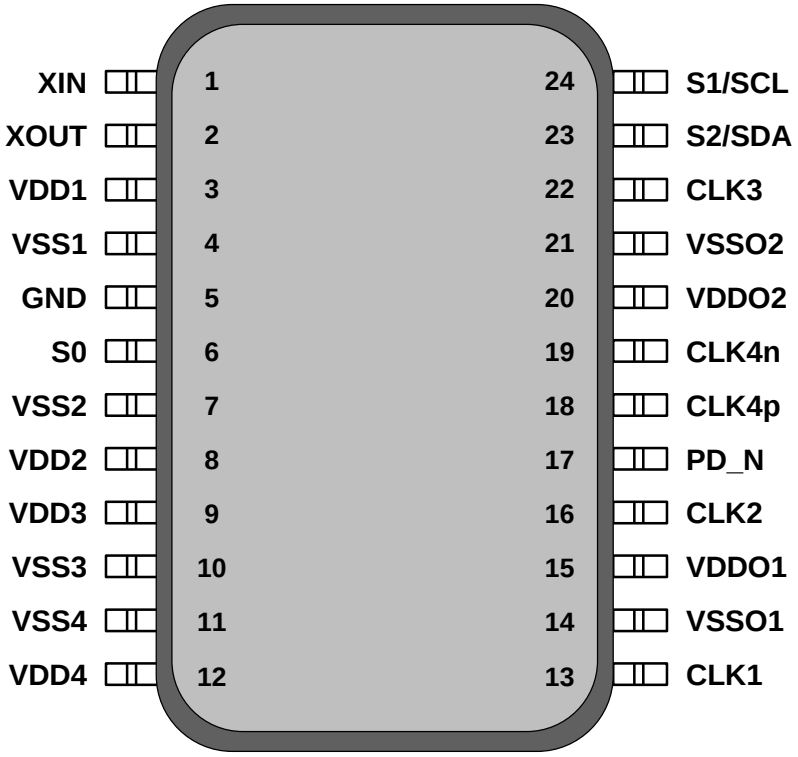


Figure 2: AK8140A Programmable Clock Generator
24-Pin ETSSOP (Top View)

Pin No.	Pin Name	Pin Type	Description
1	XIN	AI	Crystal connection or External Clock signal input
2	XOUT	AO	Crystal connection Please leave open when external clock signal input.
3	VDD1	PWR	Device power supply
4	VSS1	PWR	Ground
5	GND	AI	Connect to Ground
6	S0	AO	Programmable Control Pin0
7	VSS2	PWR	Ground
8	VDD2	PWR	Device power supply
9	VDD3	PWR	Device power supply
10	VSS3	PWR	Ground
11	VSS4	PWR	Ground
12	VDD4	PWR	Device power supply
13	CLK1	DIO	LVCMOS output pin1
14	VSSO1	PWR	Ground for output buffer.
15	VDDO1	PWR	Output Buffer power supply1 Voltage supply for CLK1 and CLK2
16	CLK2	DO	LVCMOS output pin2
17	PD_N	DI	Power Down control pin L : Device is powered down, all outputs are low. H : output Clock and PLL is normal operation.

Pin No.	Pin Name	Pin Type	Description
18	CLK4p	DO	LVCMOS/LVDS output pin4 Output level programmed Register(Address:) CLK4p and CLK4n output is opposite when LVCMOS output.
19	CLK4n	DO	
20	VDDO2	PWR	Output buffer power supply2 Voltage supply for CLK3 and CLK4
21	VSSO2	PWR	Ground for output buffer.
22	CLK3	DO	LVCMOS output pin3
23	S2/SDA	DIO	Dual function pin -S2:Programmable control pin2 -SDA: Serial Data input/output Internal pull-up 500k
24	S1/SCL	DI	Dual function pin -S1:Programmable control pin1 -SCL: Serial Clock input Internal pull-down 500k

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8140A	AK8140A	TBD	24-pin ETSSOP	-40 to 85℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	VIN	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	IIN	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage(1)	VDD	Pin: VDD1-4	3.0	3.3	3.6	V
	VDDO1	Pin: VDDO1 Supply voltage for CLK1/2 output buffer	1.7 3.0	1.8 3.3	1.9 3.6	
	VDDO2	Pin: VDDO2 Supply voltage for CLK3/4 output buffer	1.7 2.3 3.0	1.8 2.5 3.3	1.9 2.7 3.6	
Output Load Capacitance(2)	Cplclk	Pin:CLK1,2,3 Output frequency: up to 50MHz			25	pF
		Pin:CLK1,2,3 Output frequency: 50M to 120MHz			15	
		Pin:CLK1,2,3 Output frequency: 120M to 160MHz			10	
		Pin:CLK4 LVCMOS output Output frequency: up to 160MHz			10	

Note:

(1) Power to VDD1-4 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pin.

(2) Output load capacitance for CLK4p/n pin at LVDS output is descripted on page 9 for details.

Device Characteristics

over VDD1-4: 3.0 to 3.6V, VDDO1-2:1.7 to 3.6V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Overall Parameter						
High Level Input Voltage	V_{IH}	Pin:S0, PD_N, S1/SCL, S2/SDA, XIN	0.7*VDD		VDD	V
Low Level Input Voltage	V_{IL}	Pin:S0, PD_N, S1/SCL, S2/SDA, XIN	VSS		0.3*VDD	V
Input Leak Current 1	I_L1	Pin:S0, PD_N, VIN	-1		+1	μA
Input Leak Current 2	I_L2	Pin:S2/SCL	-1		+20	μA
Input Leak Current 3	I_L3	Pin:S1/SDA	-20		+1	μA
Current Consumption 1	$I_{DD}1$	No load, all outputs on, with setting: XIN input freq:100MHz CLK1-3:160MHz CLK4: 230MHz		58		mA
Current Consumption 2	$I_{DD}2$	No load, all outputs OFF, with setting: XIN input freq:100MHz CLK1, 2, 3: “L” output CLK4: “L” output		15		mA
Power Down mode Current Consumption	SI_{DD}	No load, Power Down mode, PD_N pin =’L’		0.5		μA
Crystal Clock Frequency	F_{osc}	Pin: XI, XO	16		60	MHz
External Clock Input Frequency	F_{in}	Pin: XI When input external input.	4		100	MHz
External Clock Input Duty Cycle	F_{indc}	Pin: XI When input external input. at 1/2*VDD	30	50	70	%
Output Clock Frequency Accuracy (1)	$F_{accuracy}$		-30		+30	ppm
Output Lock Time (2)	T_{lock}	Pin:CLK1-4		3		ms

Note

(1) Additional value through IC. This value is guaranteed only when using AKM’s suggested crystal unit on page 42.

(2) Time to settle output into 0.1% of specified frequency from the point that *PD_N pin is changed “0”* to “1”.

over VDD1-4: 3.0 to 3.6V, VDDO1-2:1.7 to 3.6V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
PLL1 Characteristics						
VCO frequency1	fVCO1	VCO frequency range of PLL1	230		460	MHz
Phase Comparison Frequency1	fcmp1		6.75		13.5	MHz
Period Jitter1 (1)(2)(3)(4)(7)	$Jit_{\_period}$	Jitter of Output clock from PLL1 1σ		8.3		ps
Cycle to Cycle Jitter1(1)(2)(3)(5)(7)	$Jit_{\_C2C}$	Jitter of Output clock from PLL1 1σ		12.8		ps
Long Term Jitter1(1)(2)(3)(6)(7)	$Jit_{\_long}$	Jitter of Output clock from PLL1 1000 cycle delay, 1σ		40		ps
PLL2 Characteristics						
VCO frequency2	fVCO2	VCO frequency range of PLL2	80		230	MHz
Phase Comparison Frequency2	fcmp2		2.5		14.375	MHz
Period Jitter2 (1)(2)(3)(4)(7)	$Jit_{\_period}$	Jitter of Output clock from PLL2 1σ			8.3	ps
Cycle to Cycle Jitter2(1)(2)(3)(5)(7)	$Jit_{\_C2C}$	Jitter of Output clock from PLL2 1σ			12.8	ps
Long Term Jitter2(1)(2)(3)(6)(7)	$Jit_{\_long}$	Jitter of Output clock from PLL2 1000 cycle delay, 1σ			41.7	ps

Note
(1) Design Value
(2) With the load describes on page5.
(3) When only one side is taking out operation or the same frequency among the output buffers which share a power supply pin (VDDO1, 2).
(4) Jitter depends on configuration. Jitter data is for input frequency = 48MHz, output frequency = 27M/48M/50MHz.
(5) Jitter depends on configuration. Jitter data is for input frequency = 25M/30M/50MHz, output frequency = 27M/50MHz.
(6) Jitter depends on configuration. Jitter data is for input frequency = 27MHz, output frequency = 25M/148.5MHz.
(7) 10000 sampling or more

over VDD1-4: 3.0 to 3.6V, VDDO1-2:1.7 to 3.6V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
LVCMOS output parameter						
Output Frequency	fout	Pin:CLK1-4			160	MHz
High Level Output Voltage	V_{OH}	Pin: CLK1-4 I_{OH}=-4mA	0.8*VDDO1, 2			V
Low level Output Voltage	V_{OL}	Pin: CLK1-4 I_{OL}=+4mA			0.2*VDDO1, 2	V
Output Clock Rise Time (1)(2)(3)(4)	$T_{\_rise}$	Pin:CLK1-3 with Load cplclk=10pF(upper), 25pF(lower) 0.2*VDDO1, 2 → 0.8*VDDO1, 2		0.7 1.2		Ns
		Pin:CLK4, VDDO2=3.3V with Load Cplclk=10pF 0.2*VDDO2 → 0.8*VDDO2		0.3		
Output Clock Fall Time (1)(2)(3)(4)	$T_{\_fall}$	Pin:CLK1-3 with Load Cplclk=10pF(upper), 25pF(lower) 0.2*VDDO1, 2 → 0.8*VDDO1, 2		0.7 1.2		Ns
		Pin:CLK4, VDDO2=3.3V with Load Cplclk=10pF 0.2*VDDO2 → 0.8*VDDO2		0.3		
Output Clock Duty Cycle (1)(2)		Pin:CLK1, 2, 3, 4 When ODIVn divides the PLL1/2 clock.	45	50	55	%
		Pin:CLK1, 2, 3, 4 When ODIVn divides the Input Bypass clock by even dividing value.	45	50	55	
		Pin:CLK1, 2, 3, 4 When ODIVn divides the Input Bypass clock by odd dividing value.	20		80	

(1) Design Value
(2) With the load describes on page5.
(3) When VDDO1/2=1.8V :CLKnMOD(n=1-3)='0', when VDDO1/2=3.3V, CLKnMOD(n=1-3) ='1'.
(4) When VDDO1/2=3.3V :CLK4MOD='1'.

over VDD1-4: 3.0 to 3.6V, VDDO1-2:1.7 to 3.6V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
CLK4 LVDS Output Parameter						
Output Frequency	fout				230	MHz
Output Differential Voltage(1)(2)	Vod		250	350	450	mVpp
Offset Voltage(1)(2)	Vos	VDDO2=:2.3 to 3.6V, CLK4MOD="1"	1.125	1.240	1.375	V
		VDDO2=:1.7 to 1.9V, CLK4MOD="0"	0.685	0.800	0.935	
Output Clock Rise Time (1)(2)	$T_{\_rise}$	0.2*VDDO2 → 0.8*VDDO2		0.2		ns
Output Clock Fall Time(1)(2)	$T_{\_fall}$	0.2*VDDO2 → 0.8*VDDO2		0.2		ns
Output Clock Duty Cycle(1)(2)		When ODIV4 divides the PLL1/2 clock	45	50	55	%
		When ODIV4 divides the Input Bypass clock by even dividing value	45	50	55	%
		When ODIV4 divides the Input Bypass clock by odd dividing value	20		80	%

(1) Design Value
(2) LVDS clock measured at the circuit shown in Figure.4

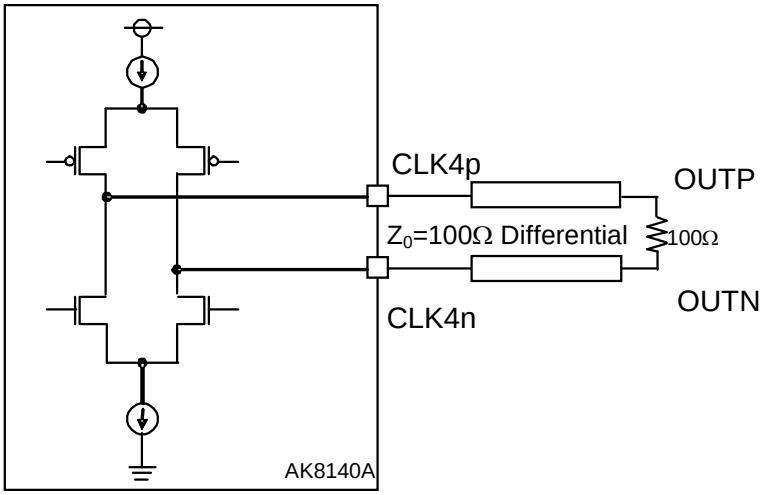


Figure.4 CLK4 LVDS Clock measurement circuit

● Frequency setting procedure

When set the CLKn* output frequency to the same as the XIN input frequency (fin), set MUXn* to 'XIN' by the Register (address:0Ch). *n=1-4

-PLL1 Setting Procedure-

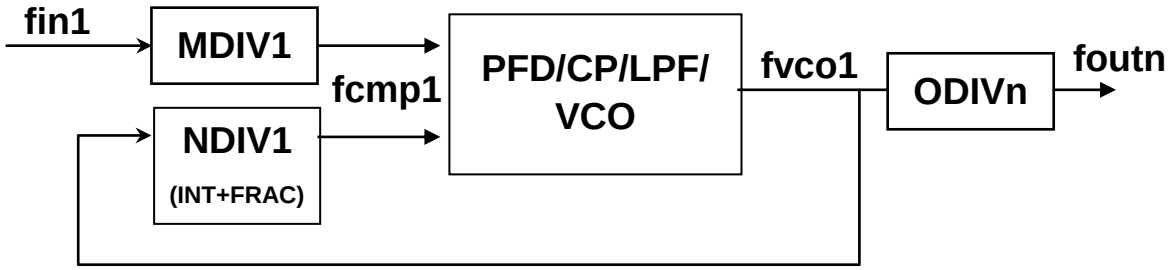


Figure.5 PLL1 Block Diagram

Output frequency from PLL1 is determined by PLL1 parameter: REFCLK Dividing value (MDIV1), Fractional-N1 Dividing value (INT, FRAC), and OUTPUT Dividing value (ODIV1-4).
These parameters should be set as described below.

Step1. Deciding VCO1 target frequency.

This frequency (fvco1) is decided from CLKn Output frequency (foutn) and Output dividing value (ODIVn, set by address: 0Dh~13h).Set fVCO1 frequency between 230MHz to 460MHz.

230MHz≦fVCO1≦460MHz (fVCO1=foutn × ODIVn)

Step2. Deciding Phase comparison frequency.

Set MDIV1 divider as this frequency (fcmp1) becomes between 6.75MHz to 13.5MHz.

6.75MHz≦fcmp1≦13.5MHz (fcmp1 = Fin1 / MDIV1)

Step3. Deciding Feedback dividing value.

This value is decided by VCO1 frequency (fvco1) and Phase comparison frequency (fcmp1).
7 bits integral part and 18 bits fractional part (signed 2's complement) is necessary to be set.

Integral part (INT) = round (fvco1 / fcmp1)
Fractional part (FRAC) = round ((fvco1 / fcmp1) – INT) x 2^{18})

Example1) input 27MHz, output 123.75MHz

1. fVCO1
   VCO1 frequency: 247.5MHz ODIV = 2

2. fcmp1
   Phase comparison frequency1: 9MHz MDIV = 3
   27MHz / 3 = 9MHz

3. NDIV1
   Feedback dividing value: 27.5 INT = 28d, FRAC =-131072d
   INT = round (247.5 / 9) = round(27.5) = 28d
   FRAC = round ((27.5 – 28) x 2^{18}) = -131072d
   Output frequency error: 0ppm

Example2) input 16MHz, output 24.576MHz

1. fVCO1
   VCO frequency: 294.912MHz ODIV = 12

2. fcmp1
   Phase comparison frequency: 8MHz MDIV = 2
   16MHz / 2 = 8MHz

3. NDIV1
   Feedback dividing value: 36.864 INT = 37d, FRAC = -35652d
   INT = round (294.912/ 8) = round(36.864) = 37d
   FRAC = round ((36.864 – 37) x 2^{18}) = -35652d
   Output frequency error: 0.043ppm (1.06Hz)

-PLL2 Setting Procedure-

Output frequency from PLL2 is determined by PLL2 parameter: REFCLK Dividing value (MDIV2), Fractional-N2 Dividing value (INT, FRAC), and OUTPUT Dividing value (ODIV1-4).
These parameters should be set as described below.

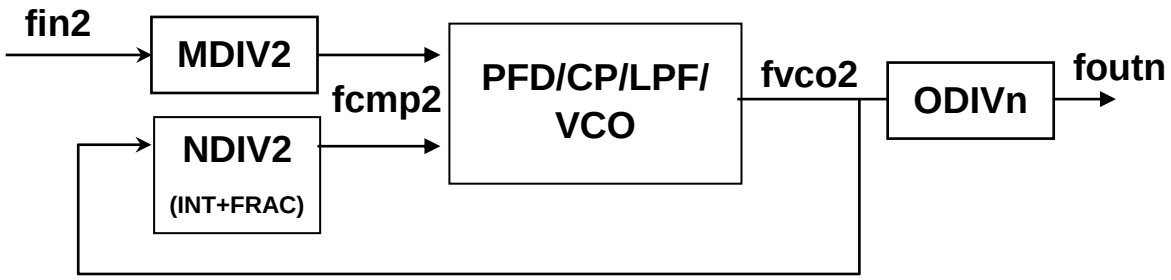


Figure.6 PLL2 Block Diagram

Step1. Deciding VCO2 target frequency.

This frequency (fvco2) is decided from CLKn Output frequency (foutn) and Output dividing value (ODIVn, set by address: 0Dh~13h). Set fVCO2 frequency between 80MHz to 230MHz.

Where

80MHz≦fVCO2≦230MHz (fVCO2=foutn × ODIVn)

Step2. Deciding MDIV2 and NDIV2 value when PLL2 is assumed to be Integer PLL.

Set MDIV2 and NDIV2 divider as fcmp2 becomes the highest common measure of fin2 and fvco2.

Where

6.75MHz≦fcmp2≦13.5MHz (fcmp2= fin2 / MDIV2)
MDIV2 (M2):1 to 511
NDIV2 (N2): 1 to 4095
M2 ≦ N2

Step3. Calculating MDIV2 and NDIV2 values of fractional-N PLL.

Calculate the dividing value of fractional divider, as follows.

$$MDIV2 = 2^P$$
$$NDIV2 = N_{INT} + \frac{N_{NUME}}{N_{DENO}}$$

$$P = 4 - \mathrm{int}\left(\log_2 \frac{N2}{M2}\right)$$

*{if P < 0 then P = 0}

$$N_{INT} = \mathrm{int}\left(\frac{N2 \times 2^P}{M2}\right)$$
$$N_{NUME} = N2 \times 2^P - M2 \times N_{INT}$$
$$N_{DENO} = M2$$

Example1) input 27MHz, output 54MHz

1. fVCO2: 108MHz ODIVn = 2

2. M2: 1
   N2: 4
   As the highest common measure of fin2 and fvco2 is 27MHz

3. P: 2 ={4-int($\log_2 4$)}
   N_{INT}: 16 ={int(4×2^2)/1 }
   N_{NUME}: 0 ={$4 \times 2^2 - 1 \times 16$}
   N_{DEMO}: 1 ={M=1}

   $\therefore$MDIV = 2^2= 4, NDIV = 16 + (0/1) = 16

Example2) input 27MHz, output 24.576MHz

1. fVCO2: 221.184MHz ODIVn = 9

2. M2: 125
   N2: 1024
   As the highest common measure of fin2 and fvco2 is 0.216MHz

3. P: 1 ={4-int($\log_2$ (1204/125))}
   N_{INT}: 16 ={int(1024×2^1)/125 }
   N_{NUME}: 0 ={$1024 \times 2^1 - 125 \times 16$}
   N_{DEMO}: 125 ={M=125}

   $\therefore$MDIV = 2^1= 2, NDIV = 16 + (48/125)

- **Programmable control pin setting**

AK8140A has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. The user can define up to eight different control settings shown in Table.

They can be programmed to any of the following functions:

-PLL1/2 frequency:
select from two variation of fVCO frequency set by the applicable register.

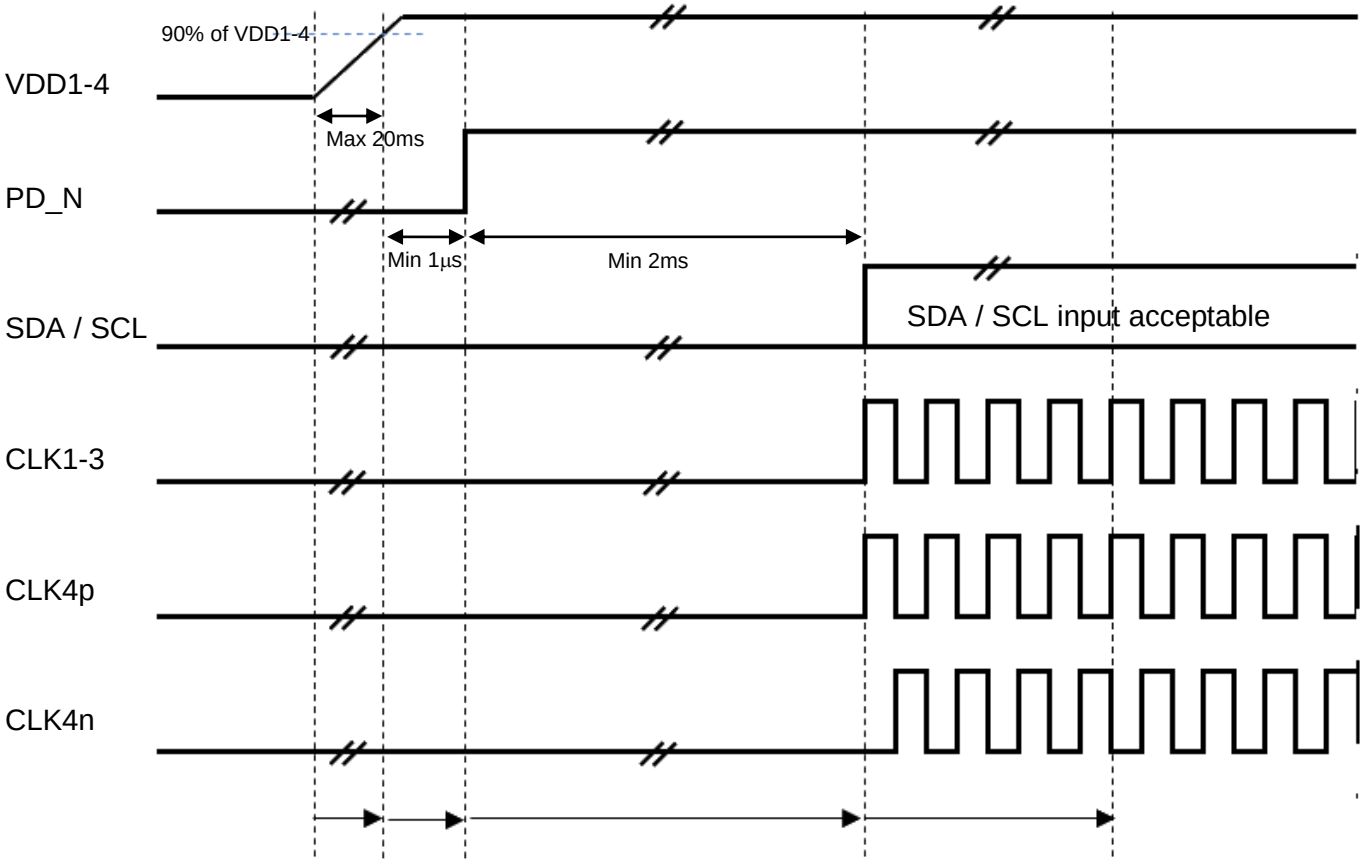
-CLK1-4 output state:
select from four states: enable/Hi-z/disable to L/ disable to H.

Programmable Control Pin			PLL1 frequency	PLL2 frequency	CLK1 Output State	CLK2 Output State	CLK3 Output State	CLK4 Output State
S2	S1	S0						
0	0	0	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
0	0	1	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
0	1	0	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
0	1	1	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
1	0	0	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
1	0	1	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
1	1	0	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
1	1	1	PLL1_0 or PLL1_1	PLL2_0 or PLL2_1	Enable or Disable	Enable or Disable	Enable or Disable	Enable or Disable
Address Offset			20h	30h	04h, 05h	06h, 07h	08h, 09h	0Ah, 0Bh

Function Description

● Power up sequence

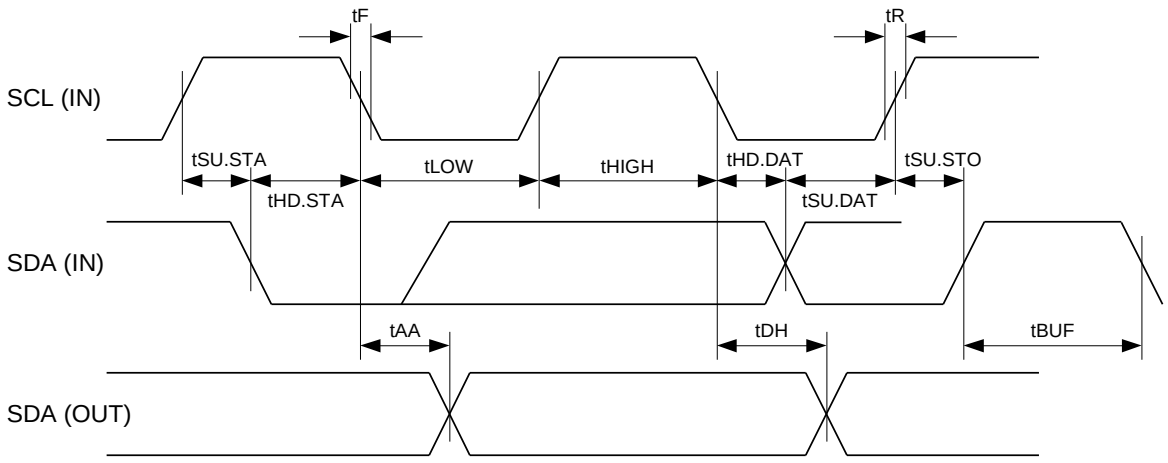
Step1 : Supplying proper voltage to the power pins with PD_N pin =”L”.
*Note: VDD1-4 must be supplied simultaneously.
The assumption power start time to reach 90 % of VDD is within 20 ms.
Step2 : Set the PD_N pin to “H”1 second after the point that the power supply reaches 90% of VDD.
Step3 : SCL / SDA are acceptable min 2ms later.



● Serial interface（I2C：slave mode）Characteristics

All specifications at VDD1: 3.3V, VDD2/VDD3: 1.8V, Ta: -30 to +85℃, unless otherwise noted.
Design value.

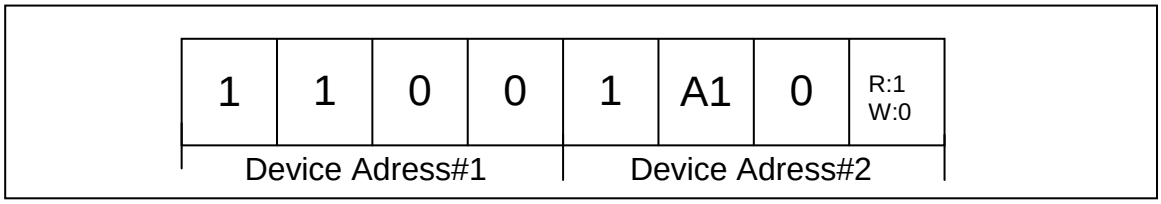
Parameter	Symbol	Conditions	MIN	Typ	MAX	Unit
SCL clock frequency	fSCL				400	kHz
SCL Clock Low Period	tLOW		1.3			us
SCL Clock High Period	tHIGH		0.6			us
Pulse width of spikes which must be suppressed	tI				50	ns
SLC Low to SDA Data Out	tAA		0.3			us
Bus free time between a STOP and START condition	tBUF		1.3			us
Start Condition Hold Time	tHD.STA		0.6			us
Start Condition Setup Time (for a Repeated Start condition)	tSU.STA		0.6			ms
Data in Hold Time	tHD.DAT		0			us
Data in Setup Time	tSU.DAT		100			ns
SDA and SCL Rise Time	tR		-		1.0	us
SDA and SCL Fall Time	tF		-		0.3	us
Stop Condition Setup Time	tSU.STO		0.6			us
Input Capacitance at SCL/SDA	Cb		-		200	pF



Serial interface

Read/Write performance of serial interface is explained as below. The device address of AK8140A is Device Address#1:1100, Device Address#2:1 A1 0.

A1 is set by the register bit “” (Address:03h).

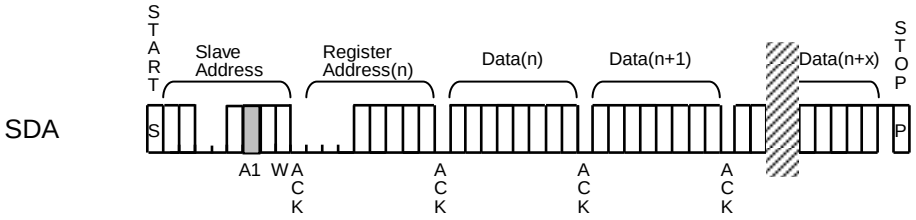


Write operation

Write operation is described below. Data must be sent after sending 8 bits address and receiving ACK. It is possible to write next address sequentially by sending next data instead of stop condition.

The address which is written after “13h/15h/2Bh” becomes “14h/20h/30h”.

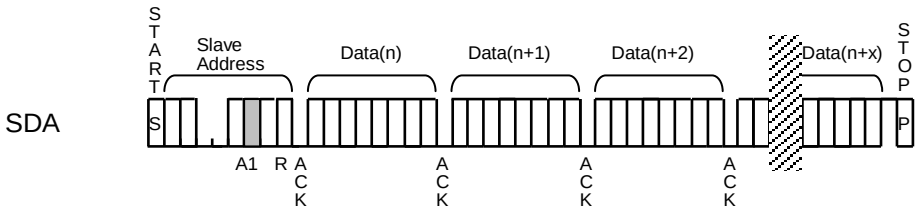
Write operation



Current address read

Current address read operation is described below. The data that is read by this operation is obtained as “last accessed address + 1”. Therefore, it is consequent to return “1111 1110” after accessing the address “1111 1111”.

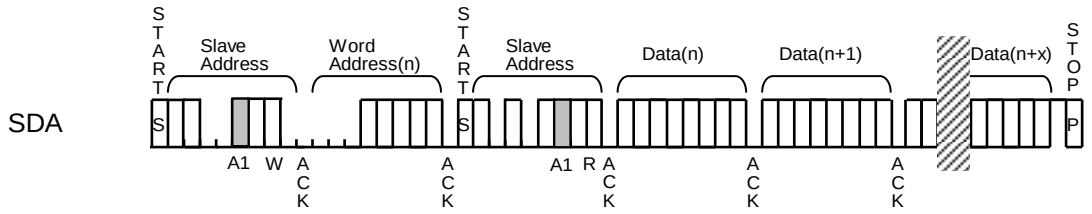
Current address read



Random read

Random read operation is described below. It is necessary to operate “dummy write” before sending read command. Dummy write is to send the address to read. It is possible to read next address sequentially by sending ACK instead of stop condition.

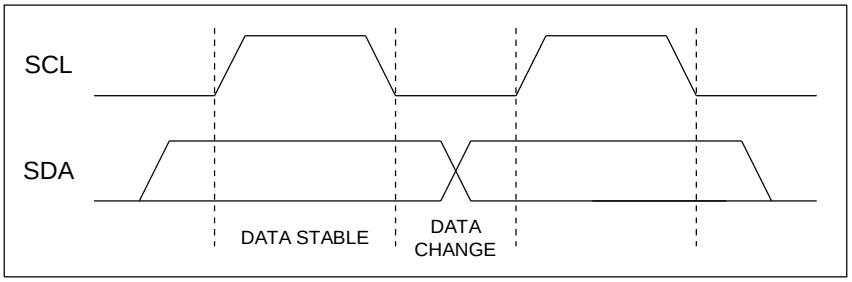
Random read



Change data

Change data operation is described below. It is available when SCL is Low.

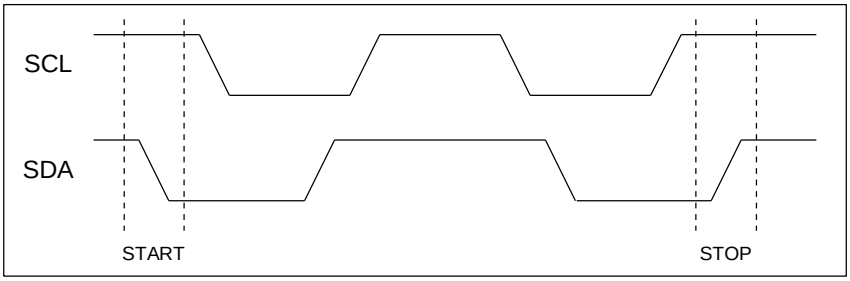
Change data



Start / Stop timing

Start / Stop timing is described below. The sequence is started when SDA goes from high to low during SCL is high. The sequence is stopped when SDA goes from low to high during SCL is high.

Start / Stop timing



●Register Configuration

AK8140A has Register can be programmed via the serial SDA/SCL interface.
The following tables and explanations describe the programmable functions of Ak8140A.

・Default register state is all '0'.
The default setting appears after power is supplied or after power-down/up sequence until it is reprogrammed to a different setting.

・All data transferred with the MSB first.

・When a Certain Setting is set by two or more Address, please write the data to all Address.

・Write '0' to Reserved bits.

Table AK8140A Register Configuration

Address Offset	Register	Remarks	Page
00h	Generic Configuration Register	**Device Setting** ・Device Setting (S0/S1/S2) for Serial Programming mode ・Device Input clock(Crystal or Ext-in) ・Slave Address A1 **CLK1 to 4 Setting** ・CLK1 to 4 Output State （CLK enabled / Disabled to L /Disabled to H / Hi-Z） ・MUX1 to 4 (PLL1 fVCO1/ PLL2 fVCO2/ Input Bypass) ・ODIV1 to 4 Parameter ・CLK1 to 4 Output Buffer Drivability ・CLK4 Output Level LVDS or CMOS	**p.21**
20h	PLL1 Configuration Register	**PLL1 Setting** （Input CLK of PLL1, MDIV1, NDIV1, fVCO1 range）	**p.33**
30h	PLL2 Configuration Register	**PLL2 Setting** （MDIV2,NDIV2,fVCO2 range）	**p.39**

■Generic Configuration Register

Generic Configuration Register(Address：00h～12h)

Address	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
00h	Reserved	Reserved	Reserved	Reserved	Reserved	S[2]	S[1]	S[0]	Device Control Setting for SDA/SCL mode
	–	–	–	–	–	0	0	0	
01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	-
	0	0	0	0	0	0	0	0	
02h	RID[1]	RID[0]	OSC_DIS	Reserved	R / W	R / W	R / W	R / W	Device overall Setting
	0	0	0	0	–	–	–	–	
03h	Reserved	Reserved	PWDN	SLV_ ADD1	Reserved	CLK4_ CMOS	SPICON	SPICON_S ET	
	0	0	0	0	0	0	0	0	
04h	CLK1_0 [1]	CLK1_0 [0]	CLK1_1 [1]	CLK1_1 [0]	CLK1_2 [1]	CLK1_2 [0]	CLK1_3 [1]	CLK1_ [0]	CLK1 Output State Setting
	0	0	0	0	0	0	0	0	
05h	CLK1_4 [1]	CLK1_4 [0]	CLK1_5 [1]	CLK1_5 [0]	CLK1_6 [1]	CLK1_6 [0]	CLK1_7 [1]	CLK1_7 [0]	
	0	0	0	0	0	0	0	0	
06h	CLK2_0 [1]	CLK2_0 [0]	CLK2_1 [1]	CLK2_1 [0]	CLK2_2 [1]	CLK2_2 [0]	CLK2_3 [1]	CLK2_3 [0]	CLK2 Output State Setting
	0	0	0	0	0	0	0	0	

07h	CLK2_4 [1]	CLK2_4 [0]	CLK2_ 5[1]	CLK2_5 [0]	CLK2_6 [1]	CLK2_6 [0]	CLK2_ 7[1]	CLK2_7 [0]	
	0	0	0	0	0	0	0	0	
08h	CLK3_0 [1]	CLK3_0 [0]	CLK3_1 [1]	CLK3_1 [0]	CLK3_2 [1]	CLK3_2 [0]	CLK3_3 [1]	CLK3_3 [0]	CLK3 Output State Setting
	0	0	0	0	0	0	0	0	
09h	CLK3_4 [1]	CLK3_4 [0]	CLK3_5 [1]	CLK3_5 [0]	CLK3_6 [1]	CLK3_6 [0]	CLK3_7 [1]	CLK3_7 [0]	
	0	0	0	0	0	0	0	0	
0Ah	CLK4_0 [1]	CLK4_0 [0]	CLK4_1 [1]	CLK4_1 [0]	CLK4_2 [1]	CLK4_2 [0]	CLK4_3 [1]	CLK4_3 [0]	CLK4 Output State Setting
	0	0	0	0	0	0	0	0	
0Bh	CLK4_4 [1]	CLK4_4 [0]	CLK4_5 [1]	CLK4_ 5[0]	CLK4_6 [1]	CLK4_6 [0]	CLK4_7 [1]	CLK4_7 [0]	
	0	0	0	0	0	0	0	0	
0Ch	MUX1 [1]	MUX1 [0]	MUX2 [1]	MUX2 [0]	MUX3 [1]	MUX3 [0]	MUX4 [1]	MUX4 0]	MUX1～4 Selection
	0	0	0	0	0	0	0	0	
0Dh	Reserved	Reserved	Reserved	Reserved	CLK1 MOD	DIV2_ BYPASS1	ODIV_1 [9]	ODIV_1 [8]	Output Buffer1 Drivability
	–	–	–	–	0	0	0	0	ODIV1 Setting

OEh	ODIV_1 [7]	ODIV_1 [6]	ODIV_1 [5]	ODIV_1 [4]	ODIV_1 [3]	ODIV_1 [2]	ODIV_1 [1]	ODIV_1 [0]	
	0	0	0	0	0	0	0	0	
0Fh	Reserved	Reserved	CLK3 MOD	CLK2 MOD	DIV2_ BYPASS3	DIV2_ BYPASS2	ODIV_2 [9]	ODIV_2 [8]	
	–	–	0	0	0	0	0	0	Output Buffer2/3 Drivability
10h	ODIV_2 [7]	ODIV_2 [6]	ODIV_2 [5]	ODIV_2 [4]	ODIV_2 [3]	ODIV_2 [2]	ODIV_2 [1]	ODIV_1 [0]	ODIV2 Setting
	0	0	0	0	0	0	0	0	
11h	ODIV_3 [7]	ODIV_3 [6]	ODIV_3 [5]	ODIV_3 [4]	ODIV_3 [3]	ODIV_3 [2]	ODIV_3 [1]	ODIV_3 [0]	
	0	0	0	0	0	0	0	0	ODIV3 Setting
12h	Reserved	Reserved	Reserved	Reserved	CLK4 MOD	DIV2_ BYPASS4	ODIV_4 [9]	ODIV_4 [8]	
	–	–	–	–	0	0	0	0	Output Buffer4 Drivability
13h	ODIV_4 [7]	ODIV_4 [6]	ODIV_4 [5]	ODIV_4 [4]	ODIV_4 [3]	ODIV_4 [2]	ODIV_4 [1]	ODIV_4 [0]	ODIV4 Setting
	0	0	0	0	0	0	0	0	

■ Generic Configuration Register

●Address：00h Device Control Setting for Serial Programming mode*

*Valid only when Serial Programming mode (Address：03h SPICON='0')

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reserved	Reserved	Reserved	Reserved	Reserved	S[2]	S[1]	S[0]

S[2:0] ： Device Control Setting for Serial Programming mode

When SPICON bit is set to'0', pin23/24 has SDA/SCL function and S[2:0] bits select the Device Control Setting predefined as the table on page 14).
Table below explains the corresponding Device Control Setting defined in the Table on page14.

S[2:0]:Device Control Setting for Serial Programming mode

S[2:0]	Device Control Setting (see on page14)
000	**[S2:S0]=000**
001	**[S2:S0]=001**
010	**[S2:S0]=010**
011	**[S2:S0]=011**
100	**[S2:S0]=100**
101	**[S2:S0]=101**
110	**[S2:S0]=110**
111	**[S2:S0]=111**

●Address ： 01h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

●Address ： 02h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
02h	RID[1]*	RID[0]*	OSC_DIS	Reserved	R / W	R / W	R / W	R / W

RID[1:0]: Device Identification *read only

RID[1:0]	**Device Identification**
00	AK8140A
01	
10	
11	

OSC_DIS : Crystal Oscillator Circuit Enable/Disable Setting（MUX0）

Set the register followed by ICLK source, as explained in the following table.

OSC_DIS	Crystal Oscillator Circuit State
0	Enable（ICLK=Crystal）
1	Disable（ICLK=Ext-in）

R/W : User arbitrarily programmable bits（D3～D0）

User can freely program these bits if necessary.

●Address：03h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
03h	Reserved	Reserved	PWDN	SLV_ADD1	Reserved	CLK4_CMOS	SPICON	EEWRITE

PWDN : Device Power Down control

.

When set PWDN bit to ’1’, only PLL1/2, ODIVn, is powered down. Register settings are unchanged.
CLKn output state is followed by CLKn output state selection(Address:04h-0Bh) when the device is powered down by this bit. *1

PWDN	Device Setting
0	Device Active
1	Device Powered down*1

*1 It becomes CLKn=L, when CLKn output state is set to ‘01’ as “CLK enabled”.

SLV_ADD1 : Slave Address Bits A1 Selection

SLV_ADD1 sets the A1 of the Slave Receiver Address.

*The default setting SLV_ADD1= ‘0’ appears after power is supplied or after power-down/up sequence until it is reprogrammed to a different setting.
* See page 25 for more information about Slave Address setting.

SLV_ADD1	Device Setting
0	A1 of Slave Address ：0
1	A1 of Slave Address ：1 *1

* 1 Default state is A1=’0’

CLK4_CMOS : CLK4 Output Level Selection LVDS/CMOS

CLK4_CMOS bit sets CLK4 output level, LVDS or LVCMOS.

CLK4_CMOS	CLK4 Output Setting
0	LVDS output
1	LVCMOS output

SPICON : Operation mode selection for pin 23/24

SPICON bit selects the operational mode of a dual functional pin 23/24.
If '1' is written, pin 23/24 become “Programmable Control pin S1/S2”, and impossible to use it as a serial programming terminal. *1
However, S1/S2 pins can be temporarily used as a serial programming terminal, SDA/SCL by connecting VDDO1 to VSS.
These are the bits of the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.

*1 the setup of SPICON= "1" becomes effective by writing ’1’ to “SPICON_SET” bit.

SPICON	Pin 23/24 operation
0	Serial programming interface*2 Pin 23:SDA Pin24:SCL
1	Programmable control pin*3 Pin 23:S2 Pin24:S1

*2 Address：00h,01h becomes effective.

*3 Pin 23/24 can control the Device Setting defined in the table on page 14.

SPICON_SET :SPICON Validation

“SPICON_SET” validates a setup of” SPICON" bit .
A setup written in SPICON by writing '1' in this bit becomes effective.
* When Set “SPICON_SET” =’1’, “SPICON_SET” bit should be written last.

SPICON_SET	SPICON Setting
0	-
1	SPICON bit is Effective *1

*1 “SPICON_SET” bit should be written last.
Setup of “SPICON” bit is validated by the rising edge of a “SPICON_SET” bit.

●Address：04h～0Bh

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
04h	CLK1_0 [1]	CLK1_0 [0]	CLK1_1 [1]	CLK1_1 [0]	CLK1_2 [1]	CLK1_2 [0]	CLK1_3 [1]	CLK1_3 [0]
05h	CLK1_4 [1]	CLK1_4 [0]	CLK1_5 [1]	CLK1_5 [0]	CLK1_6 [1]	CLK1_6 [0]	CLK1_7 [1]	CLK1_7 [0]
06h	CLK2_0 [1]	CLK2_0 [0]	CLK2_1 [1]	CLK2_1 [0]	CLK2_2 [1]	CLK2_2 [0]	CLK2_3 [1]	CLK2_3 [0]
07h	CLK2_4 [1]	CLK2_4 [0]	CLK2_5 [1]	CLK2_5 [0]	CLK2_6 [1]	CLK2_6 [0]	CLK2_7 [1]	CLK2_7 [0]
08h	CLK3_0 [1]	CLK3_0 [0]	CLK3_1 [1]	CLK3_1 [0]	CLK3_2 [1]	CLK3_2 [0]	CLK3_3 [1]	CLK3_3 [0]
09h	CLK3_4 [1]	CLK3_4 [0]	CLK3_5 [1]	CLK3_5 [0]	CLK3_6 [1]	CLK3_6 [0]	CLK3_7 [1]	CLK3_7 [0]
0Ah	CLK4_0 [1]	CLK4_0 [0]	CLK4_1 [1]	CLK4_1 [0]	CLK4_2 [1]	CLK4_2 [0]	CLK4_3 [1]	CLK4_3 [0]
0Bh	CLK4_4 [1]	CLK4_4 [0]	CLK4_5 [1]	CLK4_5 [0]	CLK4_6 [1]	CLK4_6 [0]	CLK4_7 [1]	CLK4_7 [0]

CLKn_x [1:0] ： CLK1～4 Output State Definition

CLKn_x [1:0] bit set output state(CLKn_x) defined in the table on page 15 can be set up. The output frequency at the time CLKn_x is set to “CLK Enabled” (CLKn_x[1:0] ='00') follows MUXn/ODIVn setting.

* ODIVn function is stopped, when CLKn state is set to Disable (CLKn_x[1:0] ='01'/'10'/'11').
* When CLK4 state is set to Disable, CLK4p/4n each pin will be the following state.
CLK4_x[1:0]＝‘01’/‘10’/‘11’：CLK4p/4n ＝ ‘L’/‘L’, ‘H’/‘H’, ‘Hi-Z’/‘Hi-Z

CLKn_x [1:0]	CLKn Output State
00	CLK Enabled
01	Disable to Low
10	Disable to High
11	Disable to Hi-z

(n=1～4、x=0～7)

●Address：0Ch

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	MUX1[1]	MUX1[0]	MUX2[1]	MUX2[0]	MUX3[1]	MUX3[0]	MUX4[1]	MUX4[0]

MUXn [1:0] ： CLK1～4 Output Clock Source Selection

Select output clock signal source of CLK1-4.

MUXn [1:0]	CLKn Output Clock Source
00	－ *1
01	Input Bypass
10	PLL1 output（fvco1）
11	PLL2 output (fvco2)

（n=1～4）

*1 This setting(MUXn='00') is prohibited.

●Address：0Dh～13h

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	Reserved	Reserved	Reserved	Reserved	CLK1 MOD	DIV2_ BYPASS1	ODIV_1 [9]	ODIV_1 [8]
0Eh	ODIV_1 [7]	ODIV_1 [6]	ODIV_1 [5]	ODIV_1 [4]	ODIV_1 [3]	ODIV_1 [2]	ODIV_1 [1]	ODIV_1 [0]
0Fh	Reserved	Reserved	CLK3 MOD	CLK2 MOD	DIV2_ BYPASS3	DIV2_ BYPASS2	ODIV_2 [9]	ODIV_2 [8]
10h	ODIV_2 [7]	ODIV_2 [6]	ODIV_2 [5]	ODIV_2 [4]	ODIV_2 [3]	ODIV_2 [2]	ODIV_2 [1]	ODIV_2 [0]
11h	ODIV_3 [7]	ODIV_3 [6]	ODIV_3 [5]	ODIV_3 [4]	ODIV_3 [3]	ODIV_3 [2]	ODIV_3 [1]	ODIV_3 [0]
12h	Reserved	Reserved	Reserved	Reserved	CLK4 MOD	DIV2_ BYPASS4	ODIV_4 [9]	ODIV_4 [8]
13h	ODIV_4 [7]	ODIV_4 [6]	ODIV_4 [5]	ODIV_4 [4]	ODIV_4 [3]	ODIV_4 [2]	ODIV_4 [1]	ODIV_4 [0]

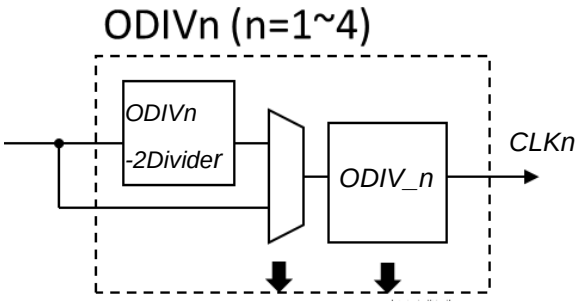
ODIVn Dividing Value Setting（ODIV_n/DIV2_BYPASSn）

The Dividing value of ODIVn is decided by “Frequency setting procedure” on page 10.

(1)The case ODIVn divides the clock signal of Input Bypass. (MUXn = ‘01’)

Set ODIVn dividing value according to explanation below, when ODIVn divides a clock signal of Input Bypass.

ODIVn configuration is as the following Figure.



**ODIVn is calculated number by “Frequency setting procedure” on page 10.*

・When set ODIVn dividing Value = 2 or odd number：
→Bypass ODIVn_2 Divider ,ODIV_n is the same number as ODIVn

Example1：ODIVn=3
Bypass ODIVn_2 Divider (DIV2_BYPASSn = ‘1’)
ODIV_n = ODIVn=3

・When set ODIVn dividing Value even number beyond 4
→Using ODIVn_2 Divider, ODIV_n = ODIVn/2
DIV2_Bypassn *ODIV_n*
Example1：ODIVn=10
(0Dh-13h) *(0Dh-13h)*
Bypass ODIVn_2 Divider (DIV2_BYPASSn = ‘0’)
ODIV_n = ODIVn/2 =5

（2）The case ODIVn divides clock signal of PLL1 or PLL2 (MUXn =’10’ or ‘11’)

Set ODIVn dividing value according to explanation below, when ODIVn divides clock signal of PLL1 or PLL2

・When ODIVn divides fvco1（MUXn=’10’）:
→ODIVn = ODIVn (calculated *value*)/2

・When ODIVn divides fvco2（MUXn=’10’）:
→ODIVn = ODIVn (calculated *value*)

ODIV_n[9:0] : ODIV_n dividing value Control (n=1,2,4)

Set ODIV_n（n=1,2,4）dividing value of ODIV1,2,4 as blow.

ODIV_n[9:0] (n=1,2,4)	Dividing Value
00 0000 0000	1
00 0000 0001	2
00 0000 0010	3
:	
11 1111 1111	1024

ODIV_3[7:0] : ODIV_3 dividing value Control

Set ODIV_3 dividing value of ODIV3 as blow

ODIV_3[7:0]	Dividing Value
0000 0000	1
0000 0001	2
0000 0010	3
:	
1111 1111	256

DIV2_BYPASSn (n=1～4)

DIV2_BYPASSn selects whether ODIVn_2divider used.（n=1-4）

DIV2_BYPASSn	ODIVn_2Divider
0	Use the 2divider
1	Bypass the 2 divider

※ Effective only when MUXn(n=1～4)= ‘00’ / ‘01’

CLKnMOD : CLKn(n=1-3) Output Buffer Drivability Setting

"CLKnMOD" set the drivability of Output Buffer of CLKn as the following table. (n=1～3)

CLKnMOD	CLKn Drivability
0	High Recommended when VDDO1,2=1.8V
1	Low Recommended when VDDO1,2=3.3V

(n=1～3)

CLK4MOD : CLK4 Output Buffer Drivability Setting

"CLK4MOD" set the drivability of Output Buffer of CLK4 as the following table.

CLK4MOD	CLK4 Drivability
0	High Recommended when VDDO2=1.8V
1	Low Recommended when VDDO2=3.3V

■PLL1 Configuration Register

Address	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
20h	FS1_0	FS1_1	FS1_2	FS1_3	FS1_4	FS1_5	FS1_6	FS1_7	PLL1 Frequency Selection
	0	0	0	0	0	0	0	0	
21h	INPUT_CK1	VCO1_RANG0[1]	VCO1_RANG0[0]	VCO1_RANG1[1]	VCO1_RANG1[0]	Reserved	Reserved	Reserved	PLL1 Input Clock Selection fVCO1 Range
	0	0	0	0	0	–	–	–	
22h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRAC0[17]	FRAC0[16]	
	–	–	–	–	–	–	0	0	
23h	FRAC0[15]	FRAC0[14]	FRAC0[13]	FRAC0[12]	FRAC0[11]	FRAC0[10]	FRAC0[9]	FRAC0[8]	PLL1_0 NDIV1 Fractional Part Setting
	0	0	0	0	0	0	0	0	
24h	FRAC0[7]	FRAC0[6]	FRAC0[5]	FRAC0[4]	FRAC0[3]	FRAC0[2]	FRAC0[1]	FRAC0[0]	
	0	0	0	0	0	0	0	0	
25h	Reserved	INT0[6]	INT0[5]	INT0[4]	INT0[3]	INT0[2]	INT0[1]	INT0[0]	PLL1_0 NDIV1 Integral Part Setting
	–	0	0	0	0	0	0	0	
26h	MDIVC0[3]	MDIVC0[2]	MDIVC0[1]	MDIVC0[0]	MDIVP0[3]	MDIVP0[2]	MDIVP0[1]	MDIVP0[0]	PLL1_0 MDIV1 Setting
	0	0	0	0	0	0	0	0	
27h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FRAC1[17]	FRAC1[16]	
	–	–	–	–	–	–	0	0	
28h	FRAC1[15]	FRAC1[14]	FRAC1[13]	FRAC1[12]	FRAC1[11]	FRAC1[10]	FRAC1[9]	FRAC1[8]	PLL1_1 NDIV1 Fractional Part Setting
	0	0	0	0	0	0	0	0	
29h	FRAC1[7]	FRAC1[6]	FRAC1[5]	FRAC1[4]	FRAC1[3]	FRAC1[2]	FRAC1[1]	FRAC1[0]	
	0	0	0	0	0	0	0	0	
2Ah	Reserved	INT1[6]	INT1[5]	INT1[4]	INT1[3]	INT1[2]	INT1[1]	INT1[0]	PLL1_1 NDIV1 Integral Part Setting
	–	0	0	0	0	0	0	0	
2Bh	MDIVC1[3]	MDIVC1[2]	MDIVC1[1]	MDIVC1[0]	MDIVP1[3]	MDIVP1[2]	MDIVP1[1]	MDIVP1[0]	PLL1_1 MDIV1 Setting
	0	0	0	0	0	0	0	0	

PLL1 Configuration Register

PLL1 Block Diagram is as the following Figure.
Please set PLL1 parameter according to .
PLL1 has two Frequency mode predefined as PLL1_0 or PLL1_1 and selected by S0/S1/S2 pin or S[2:0] bits (Address:00h). Refer to Programmable Control pin setting on page 14 for more information about Frequency selection.

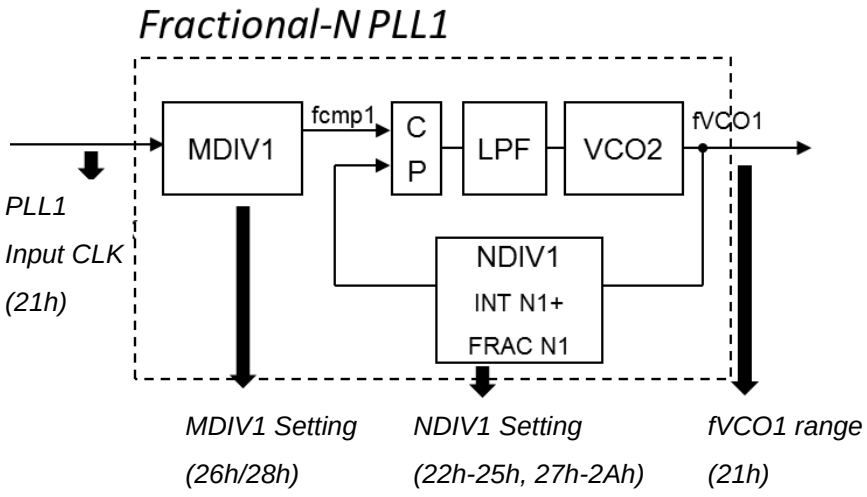


Figure PLL1 Block Diagram

●Address：20h PLL1 Output Frequency selection

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	FS1_0	FS1_1	FS1_2	FS1_3	FS1_4	FS1_5	FS1_6	FS1_7

FS1_x（x=0～7）： PLL1 Output Frequency selection

The output frequency of PLL is chosen from two setups，PLL1_0 and PLL1_1.

FS1_x	PLL1 Frequency
0	PLL1_0 Predefined by address:21h, 22h～26h
1	PLL1_1 Predefined by address:21h, 27h～2Bh

●Address：21h　PLL1 Input Clock Selection/ fVCO1 range

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
21h	INPUT _CK1	VCO1 _RANG0[1]	VCO1 _RANG0[0]	VCO1 _RANG1[1]	VCO1 _RANG1[0]	–	–	–

INPUT_CK1 ： PLL1Input Clock Selection (MUX5)

INPUT_CK1	PLL1Input Clock
0	Input Clock （Crystal Oscillation or External clock input）
1	fvco2 PLL2 output clock

VCO1_RANGEn[1:0] ： fVCO1 range selection　n=0/1

"VCO1_RANGEn[1:0]" selects the fVCO1 frequency range. fVCO1 frequency can be set according to Frequency Setting Procedure on page 10.

VCO1_RANGEn[1:0]	fVCO1 range
00	fVCO1 < 300MHz
01	300MHz <= fvco1 < 370MHz
10	370MHz <= fvco1
11	370MHz <= fvco1

●Address：22h/28h、23h/29h、24h/2Ah　NDIV1 fractional part setting

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
22h 27h							FRACn[17]	FRACn[16]
23h 28h	FRACn[15]	FRACn[14]	FRACn[13]	FRACn[12]	FRACn[11]	FRACn[10]	FRACn[9]	FRACn[8]
24h 29h	FRACn[7]	FRACn[6]	FRACn[5]	FRACn[4]	FRACn[3]	FRACn[2]	FRACn[1]	FRACn[0]

FRACn[17:0] settings are updated after writing register 24h/20h.
Setting procedure should be　(1)22h/27h ,(2)23h/28h, and then (3)24h/29h

FRACn [17:0] ：NDIV1 fractional part setting　n=0/1

NDIV1 fractional part can be set according to Frequency Setting Procedure on page 10. Fractional part of N is expressed by A/218. Here, the numerator A is defined by FRAC bits. FRAC is treated as 2's Complement which is able to set from -217 up to +217. Consequently, it is possible to set from -0.5 to +0.5 for fractional part of N.

FRACn [17:0]	A	Fractional Part
01 1111 1111 1111 1111	+131071	0.49999619..
01 1111 1111 1111 1110	+131070	
01 0000 0000 0000 0000	+65536	0.25
00 0000 0000 0000 0001	+1	0.00000381..
00 0000 0000 0000 0000	0	0
11 1111 1111 1111 1111	-1	-0.00000381..
11 1111 1111 1111 1110	-2	
11 0000 0000 0000 0000	-65536	-0.25
10 0000 0000 0000 0001	-131071	-0.49999619..
10 0000 0000 0000 0000	-131072	-0.5

●Address : 25h/2Ah NDIV1 integral part settings

*n=0/1

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
25h 2Ah	–	INTn[6]	INTn[5]	INTn[4]	INTn[3]	INTn[2]	INTn[1]	INTn[0]

INTn [6:0] : NDIV1 integral part settings n=0/1

NDIV1 Integral part can be set according to Frequency Setting Procedure on page 10.
* Do not set any value except ”17”～”68”

INTn [6:0]	integral part
000 0000～001 0000	*Prohibited*
001 0001	17
001 0010	18
100 0011	67
100 0100	68
100 0101～111 1111	-*1

●Address：26h/2C MDIV1 Setting

*n=0/1

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
26h 2Bh	MDIVCn[3]	MDIVCn[2]	MDIVCn[1]	MDIVCn[0]	MDIVPn[3]	MDIVPn[2]	MDIVPn[1]	MDIVPn[0]

MDIV1 Dividing Value Settings（MDIVCn， MDIVPn）

MDIV1Configuration is as the following Figure.

MDIV1 Dividing Value can be set according to **Frequency Setting Procedure** on page 10.

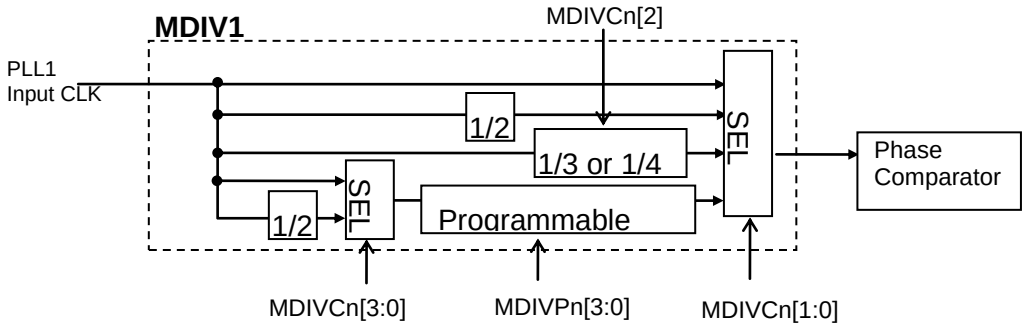


Figure MDIV1Configuration

MDIVCn[3] : Programmable divider input selection *n=0/1

MDIVCn[3]	Input of Programmable divide
0	PLL1 Input CLK
1	PLL1 Input CLK 1/2

MDIVCn[2] : 3or4 divider selection *n=0/1

MDIVCn[2]	Selected divider
0	3 divider
1	4 divider

MDIVCn[1:0] : Input of Phase comparator selection *n=0/1

MDIVCn[1:0]	Input of Phase comparator
0 0	PLL1 Input CLK
0 1	PLL1 Input CLK 1/2
1 0	3 or4 divider output
1 1	Programmable divider Output

※Set MDIVCn[1:0]='11', when INPUT_CK1 is set to'1'(Address=21h)

MDIVPn[3:0] : Programmable divider control *n=0/1

MDIVPn[3:0]	Programmable Divider dividing value
0 0 0 0	*prohibited*
0 0 0 1	2
0 0 1 0	3
0 0 1 1	4
0 1 0 0	5
0 1 0 1	6
0 1 1 0	7
0 1 1 1	8
1 0 0 0	9
1 0 0 1	10
1 0 1 0	11
1 0 1 1	12
1 1 0 0	13
1 1 0 1	14
1 1 1 0	15
1 1 1 1	16

■ PLL2 Configuration Register

Address	Data								Remarks
	D7	D6	D5	D4	D3	D2	D1	D0	
30h	FS2_0	FS2_1	FS2_2	FS2_3	FS2_4	FS2_5	FS2_6	FS2_7	PLL2 Frequency Selection
	0	0	0	0	0	0	0	0	
31h	Reserved	Reserved	MDIV0[2]	MDIV0[1]	MDIV0[0]	VCO2_RANGE0[1]	VCO2_RANGE0[0]	Reserved	PLL2_0 MDIV2Setting fVCO2 Range
	0	0	0	0	0	0	0	0	
32h	NINT0[5]	NINT0[4]	NINT0[3]	NINT0[2]	NINT0[1]	NINT0[0]	NUME0[8]	NUME0[7]	PLL2_0 NDIV2 Setting
	0	0	0	0	0	0	0	0	
33h	NUME0[6]	NUME0[5]	NUME0[4]	NUME0[3]	NUME0[2]	NUME0[1]	NUME0[0]	DENO0[8]	
	0	0	0	0	0	0	0	0	
34h	DENO0[7]	DENO0[6]	DENO0[5]	DENO0[4]	DENO0[3]	DENO0[2]	DENO0[1]	DENO0[0]	
	0	0	0	0	0	0	0	0	
35h	Reserved	Reserved	MDIV1[2]	MDIV1[1]	MDIV1[0]	VCO2_RANGE1[1]	VCO2_RANGE1[0]	Reserved	PLL2_1 MDIV2Setting fVCO2 Range
	0	0	0	0	0	0	0	0	
36h	NINT1[5]	NINT1[4]	NINT1[3]	NINT1[2]	NINT1[1]	NINT1[0]	NUME1[8]	NUME1[7]	PLL2_1 NDIV2 Setting
	0	0	0	0	0	0	0	0	
37h	NUME1[6]	NUME1[5]	NUME1[4]	NUME1[3]	NUME1[2]	NUME1[1]	NUME1[0]	DENO1[8]	
	0	0	0	0	0	0	0	0	
38h	DENO1[7]	DENO1[6]	DENO1[5]	DENO1[4]	DENO1[3]	DENO1[2]	DENO1[1]	DENO1[0]	
	0	0	0	0	0	0	0	0	

PLL2 Configuration Register

PLL2 Block Diagram is as the following Figure.
Please set PLL2 parameter according to. **Frequency Setting Procedure** on page 10.
PLL2 has two Frequency mode predefined as PLL2_0 or PLL2_1 and selected by S0/S1/S2 pin or S[2:0] bits (Address:00h). see on page 10more information about Frequency selection.

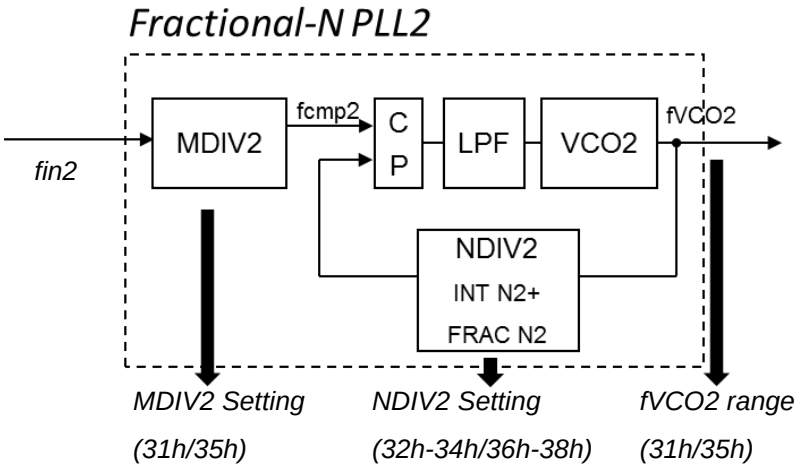


Figure PLL2 Block Diagram

●Address：30h PLL2 Output Frequency selection

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
30h	FS2_0	FS2_1	FS2_2	FS2_3	FS2_4	FS2_5	FS2_6	FS2_7

FS2_x (x=0～7**): PLL1 Output Frequency selection**

The output frequency of PLL2 is chosen from two setups, PLL2_0 or PLL2_1.

FS2_x	PLL2 Frequency
0	PLL2_0 Predefined by address:31h～34h
1	PLL2_1 Predefined by address:35h～38h

●Address：31h/35h　　MDIV2 and fVCO2 frequency range Setting　　*n=0/1

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
31h 35h	Reserved	Reserved	MDIVn[2]	MDIVn[1]	MDIVn[0]	VCO2_RANGEn[1]	VCO2_RANGEn[0]	−

MDIVn[2:0] ：MDIV2Dividing Value Settings　　*n=0/1

MDIV1Configuration is as the following Figure.
MDIV1 Dividing Value can be set according to **Frequency Setting Procedure** on page 10.

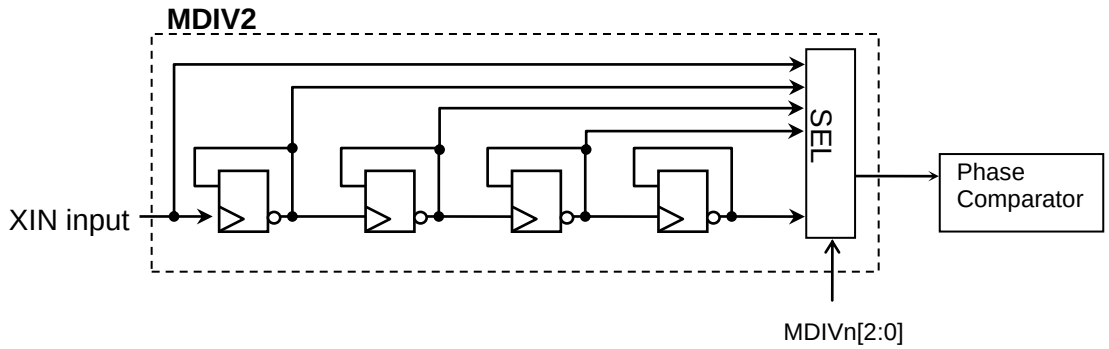


Figure MDIV2 configuration

MDIVn[2:0]	MDIV2 Dividing Value
000	1
001	2
010	4
011	8
100	16
Except the above	*prohibited* （Device is Reset）

VCO2_RANGEn[1:0] ： fVCO2 range selection　*n=0/1

“VCO2_RANGEn[1:0]” selects the fVCO2 frequency range. fVCO2 frequency can be set according to **Frequency Setting Procedure** on page 10.

VCO2_RANGEn[1:0]	fVCO2 range
00	fvco < 117.5MHz
01	117.5MHz <= fvco < 155MHz
10	155MHz <= fvco < 192.5MHz
11	192.5MHz <= fvco

●Address：32h～34h、36h～38h　NDIV2 Dividing Value
*n=0/1

Address	Data							
	D7	D6	D5	D4	D3	D2	D1	D0
32h **36h**	NINTn[5]	NINTn[4]	NINTn[3]	NINTn[2]	NINTn[1]	NINTn[0]	NUMEn[8]	NUMEn[7]
33h **37h**	NUMEn[6]	NUMEn[5]	NUMEn[4]	NUMEn[3]	NUMEn[2]	NUMEn[1]	NUMEn[0]	DENOn[8]
34h **38h**	DENOn[7]	DENOn[6]	DENOn[5]	DENOn[4]	DENOn[3]	DENOn[2]	DENOn[1]	DENOn[0]

After writing register 34h, 32h～34h data settings are updated.

After writing register 38h, 36h～38h data settings are updated.

NDIV2 Dividing Value（**NINTn**, **NUMEn**, **DENOn**）

NDIV2 dividing value can be set according to **Frequency Setting Procedure** on page 10.

NINTn[5:0] : NDIV2 integral part settings　*n=0/1

NINTn[5:0]	NDIV2 Integral Part
000000 ～ 001111	*prohibited*
010000	16
:	:
100011	35
100100	36
100101	37
:	:
111001	57
111010 ～ 111111	*prohibited*

NUMEn[8:0] : NDIV2 Numerator of fractional part setting　*n=0/1

NUMEn[8:0]	NDIV2 Numerator of fractional part setting
000000000	0（fractional-part=0）
000000001	1
:	:
111111110	510
111111111	511

DENOn[8:0] ： NDIV2 Denominator of fractional part setting *n=0、1

DENOn[8:0]	NDIV2 Denominator of fractional part setting
000000000	*prohibited*
000000001	1
:	:
111111110	510
111111111	511

- **Crystal Unit**

DAISHINKU Corp. DSX321G

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Nominal frequency	f0		25.000		MHz	CL=8pF
Equivalent resistance	R1		18.2	60	Ω	
Shunt capacitance	C0		1.22		pF	
Motional capacitance	C1		4.724		fF	
Motional inductance	L1		8.585		mH	
Drive Level			30		uW	±2 uW

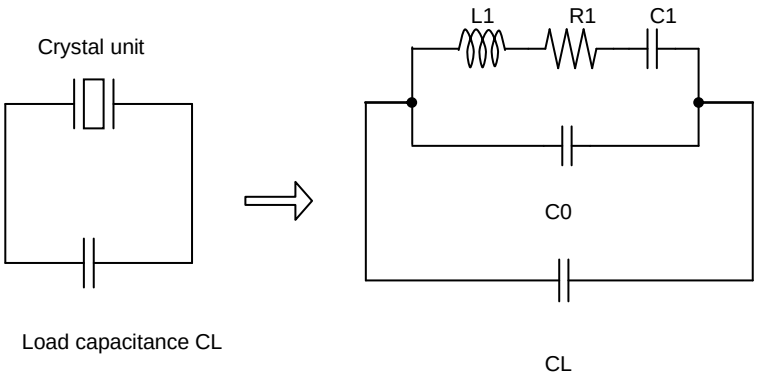
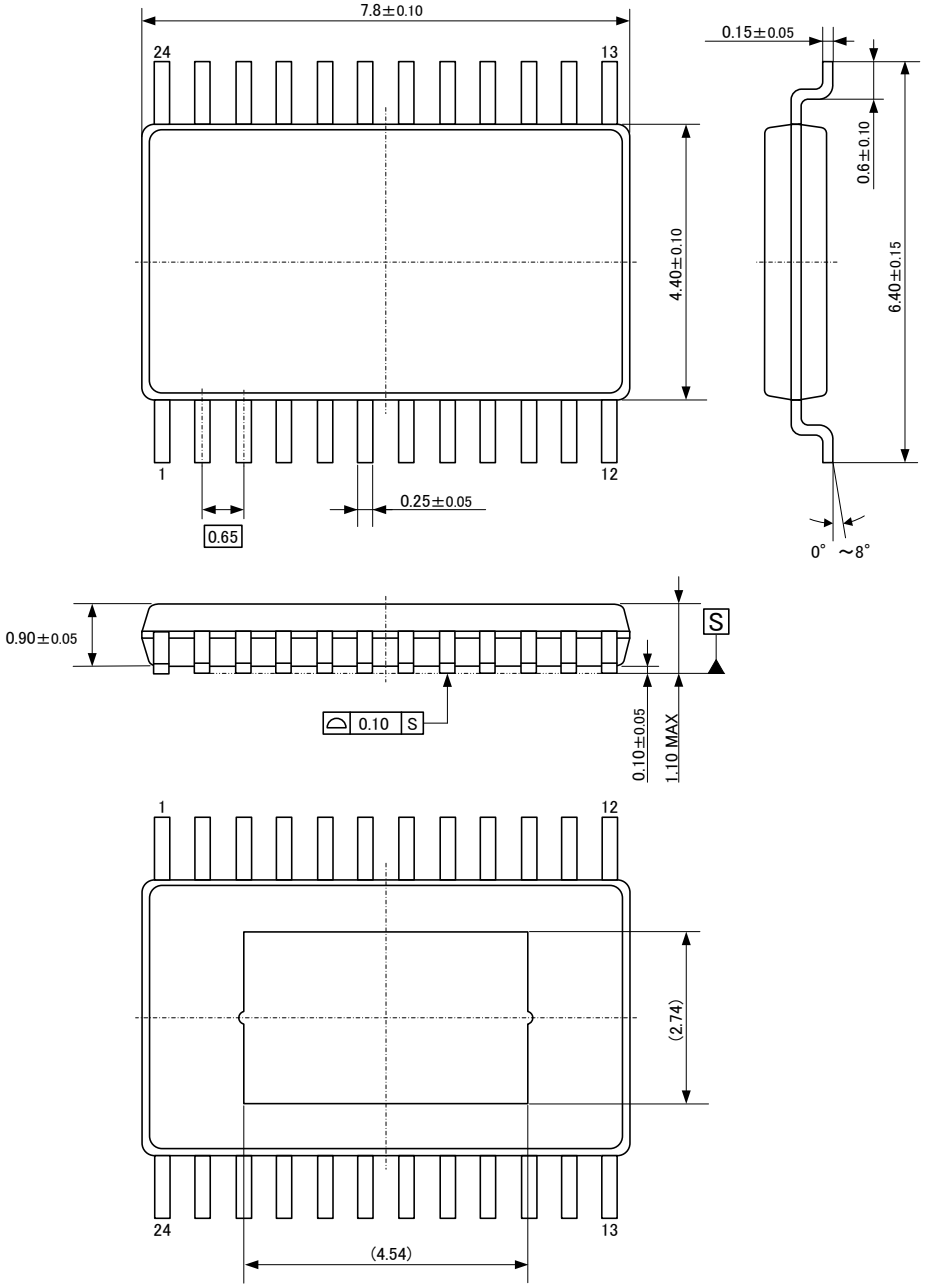


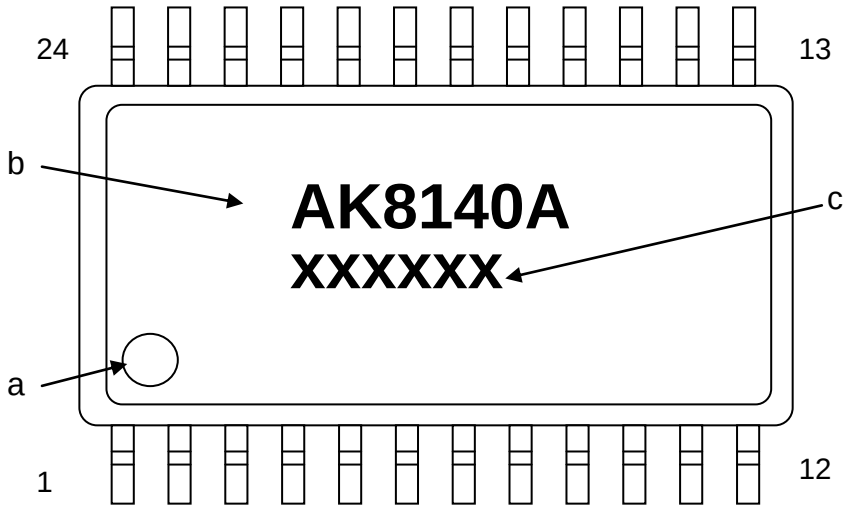
Figure Equivalent parameter and load

Package Information

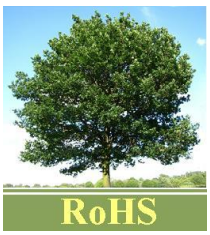


- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (6 digits)



- **RoHS Compliance**



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