



## 3.3V LVPECL 1:4 Clock Fanout Buffer AK8181B

### Features

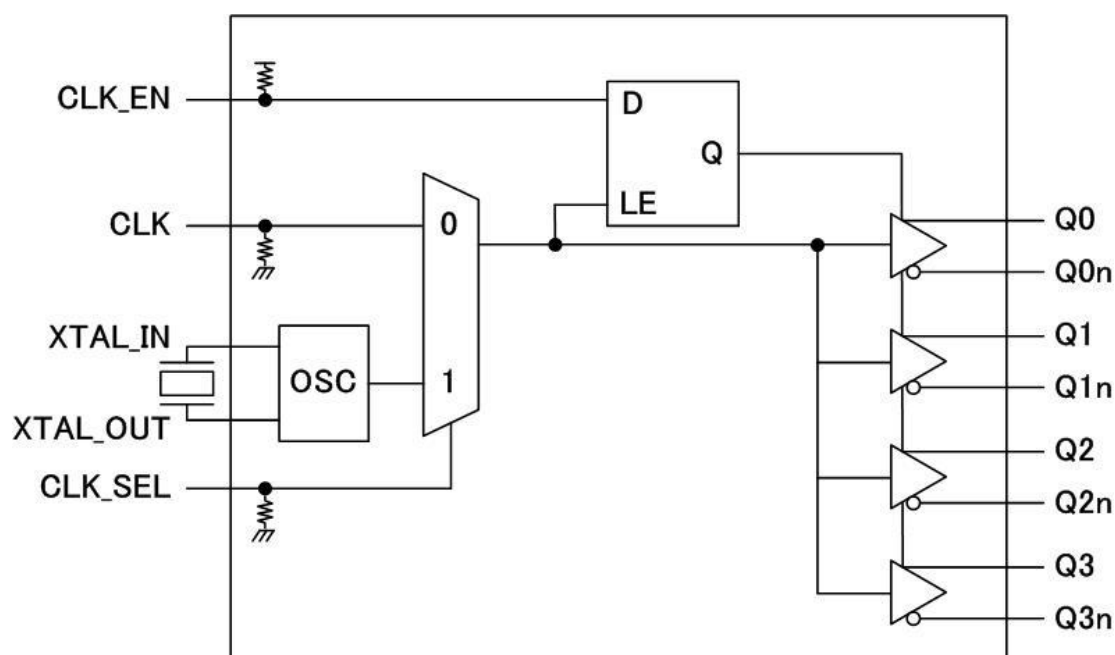
- Four differential 3.3V LVPECL outputs
- Selectable LVTTTL/LVCMOS CLK or crystal input
- Clock output frequency up to 266MHz
- Output skew : 10ps typical
- Part-to-part skew : 200ps maximum
- Propagation delay : 1.4ns maximum
- Additive phase jitter(RMS) : 0.057ps(typical)
- Operating Temperature Range: -40 to +85°C
- Package: 20-pin TSSOP (Pb free)
- Pin compatible with ICS8535I-31

### Description

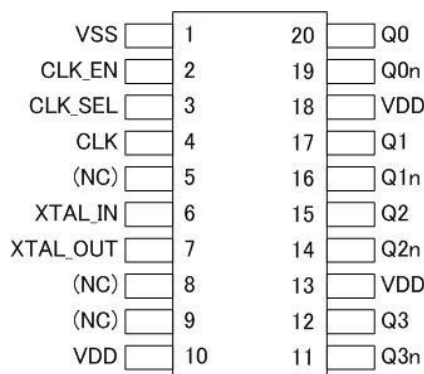
The AK8181B is a member of AKM's LVPECL clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8181B distributes 4 buffered clocks.

AK8181B are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8181B is available in a 20-pin TSSOP package.

### Block Diagram



## Pin Descriptions



**Package: 20-Pin TSSOP (Top View)**

| Pin No. | Pin Name | Pin Type | Pullup down | Description                                                                                                                                                                                                                   |
|---------|----------|----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | VSS      | PWR      | --          | Negative power supply                                                                                                                                                                                                         |
| 2       | CLK_EN   | IN       | Pull up     | Synchronizing clock output enable (LVCMOS/LVTTL)<br>Pin is connected to VDD by internal resistor. (typ. 51kΩ)<br>High (Open): clock outputs follow clock input.<br>Low: Q outputs are forced low, Qn outputs are forced high. |
| 3       | CLK_SEL  | IN       | Pull down   | CLK Select Input (LVCMOS/LVTTL)<br>Pin is connected to VSS by internal resistor. (typ. 51kΩ)<br>High: selects XTAL input    Low (Open): selects CLK input                                                                     |
| 4       | CLK      | IN       | Pull down   | LVCMOS/LVTTL Clock Input<br>Pin is connected to VSS by internal resistor. (typ. 51kΩ)<br>*When using crystal input (CLK_SEL=High), it should be connected to VSS or opened.                                                   |
| 5       | NC       | --       | --          | No connect                                                                                                                                                                                                                    |
| 6       | XTAL_IN  | IN       | --          | Crystal oscillator interface<br>*When using CLK input (CLK_SEL=Low), it should be connected to VSS or opened.                                                                                                                 |
| 7       | XTAL_OUT | OUT      | --          | Crystal oscillator interface<br>*When using CLK input (CLK_SEL=Low), it should be connected to VSS or opened.                                                                                                                 |
| 8       | NC       | --       | --          | No connect                                                                                                                                                                                                                    |
| 9       | NC       | --       | --          | No connect                                                                                                                                                                                                                    |
| 10      | VDD      | PWR      | --          | Positive power supply                                                                                                                                                                                                         |
| 11, 12  | Q3n, Q3  | OUT      | --          | Differential clock output (LVPECL)                                                                                                                                                                                            |
| 13      | VDD      | PWR      | --          | Positive power supply                                                                                                                                                                                                         |
| 14, 15  | Q2n, Q2  | OUT      | --          | Differential clock output (LVPECL)                                                                                                                                                                                            |
| 16, 17  | Q1n, Q1  | OUT      | --          | Differential clock output (LVPECL)                                                                                                                                                                                            |
| 18      | VDD      | PWR      | --          | Positive power supply                                                                                                                                                                                                         |
| 19, 20  | Q0n, Q0  | OUT      | --          | Differential clock output (LVPECL)                                                                                                                                                                                            |

## Ordering Information

| Part Number | Marking | Shipping Packaging | Package      | Temperature Range |
|-------------|---------|--------------------|--------------|-------------------|
| AK8181B     | AK8181B | Tape and Reel      | 20-pin TSSOP | -40 to 85 °C      |

## Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted <sup>(1)</sup>

| Items                                    | Symbol           | Ratings         | Unit |
|------------------------------------------|------------------|-----------------|------|
| Supply voltage <sup>(2)</sup>            | VDD              | -0.3 to 4.6     | V    |
| Input voltage <sup>(2)</sup>             | V <sub>IN</sub>  | -0.5 to VDD+0.5 | V    |
| Input current (any pins except supplies) | I <sub>IN</sub>  | ±10             | mA   |
| Storage temperature                      | T <sub>stg</sub> | -55 to 150      | °C   |

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

(2) VSS=0V



## ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

## Recommended Operation Conditions

| Parameter                     | Symbol         | Conditions     | Min   | Typ | Max   | Unit |
|-------------------------------|----------------|----------------|-------|-----|-------|------|
| Operating temperature         | T <sub>a</sub> |                | -40   |     | 85    | °C   |
| Supply voltage <sup>(1)</sup> | VDD            | VDD±5%, VSS=0V | 3.135 | 3.3 | 3.465 | V    |

(1) Power of 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

## Pin Characteristics

| Parameter               | Symbol          | Conditions | Min | Typ | Max | Unit |
|-------------------------|-----------------|------------|-----|-----|-----|------|
| Input Capacitance       | C <sub>IN</sub> |            |     | 4   |     | pF   |
| Input Pullup Resistor   | R <sub>PU</sub> |            |     | 51  |     | kΩ   |
| Input Pulldown Resistor | R <sub>PD</sub> |            |     | 51  |     | kΩ   |

## DC Characteristics

All specifications at VDD= 3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

| Parameter                          |              | Symbol             | Conditions          | MIN     | TYP | MAX     | Unit |
|------------------------------------|--------------|--------------------|---------------------|---------|-----|---------|------|
| Input High Voltage                 |              | V <sub>IH</sub>    |                     | 2.0     |     | VDD+0.3 | V    |
| Input Low Voltage                  |              | V <sub>IL</sub>    |                     | -0.3    |     | 0.8     | V    |
| Input High Current                 | CLK, CLK_SEL | I <sub>H</sub>     | Vin=VDD=3.465V      |         |     | 150     | μA   |
|                                    | CLK_EN       |                    | Vin=VDD=3.465V      |         |     | 5       | μA   |
| Input Low Current                  | CLK, CLK_SEL | I <sub>L</sub>     | Vin=VSS, VDD=3.465V | -5      |     |         | μA   |
|                                    | CLK_EN       |                    | Vin=VSS, VDD=3.465V | -150    |     |         | μA   |
| Output High Voltage <sup>(1)</sup> |              | V <sub>OH</sub>    |                     | VDD-1.4 |     | VDD-0.9 | V    |
| Output Low Voltage <sup>(1)</sup>  |              | V <sub>OL</sub>    |                     | VDD-2.0 |     | VDD-1.7 | V    |
| Peak-to-Peak Output Voltage Swing  |              | V <sub>SWING</sub> |                     | 0.6     |     | 1.0     | V    |
| Supply Current                     |              | I <sub>DD</sub>    |                     |         |     | 60      | mA   |

(1) Outputs terminated with 50Ω to VDD-2V.

## Crystal Characteristics

All specifications at VDD= 3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

| Parameter                          | Conditions | MIN         | TYP | MAX | Unit |
|------------------------------------|------------|-------------|-----|-----|------|
| Mode of Oscillation                |            | Fundamental |     |     |      |
| Frequency                          |            | 12          |     | 50  | MHz  |
| Equivalent Series Resistance (ESR) |            |             |     | 50  | Ω    |
| Shunt Capacitance                  |            |             |     | 7   | pF   |
| Drive Level                        |            |             |     | 1   | mW   |

## AC Characteristics

All specifications at VDD= 3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

| Parameter                            | Symbol                          | Conditions                | MIN | TYP   | MAX | Unit |
|--------------------------------------|---------------------------------|---------------------------|-----|-------|-----|------|
| Output Frequency                     | f <sub>OUT</sub>                |                           |     |       | 266 | MHz  |
| Propagation Delay <sup>(1)</sup>     | t <sub>PD</sub>                 |                           | 0.6 |       | 1.4 | ns   |
| Output Skew <sup>(2)(3)</sup>        | t <sub>sk(O)</sub>              |                           |     | 10    |     | ps   |
| Part-to-Part Skew <sup>(3)(5)</sup>  | t <sub>skPP</sub>               |                           |     |       | 200 | ps   |
| Buffer Additive Jitter, RMS          | t <sub>jit</sub>                | 155.52MHz (12kHz – 20MHz) |     | 0.057 |     | ps   |
| Output Rise/Fall Time <sup>(4)</sup> | t <sub>r</sub> , t <sub>f</sub> | 20% to 80%                | 200 |       | 600 | ps   |
| Output Duty Cycle                    | DC <sub>OUT</sub>               |                           | 46  | 50    | 54  | %    |

(1) Measured from the VDD/2 of the input to the differential output crossing point.

(2) Defined as skew between outputs at the same supply voltage and with equal load conditions.

(3) This parameter is defined in accordance with JEDEC Standard 65.

(4) Design value.

(5) Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

## Parameter Measurement Information

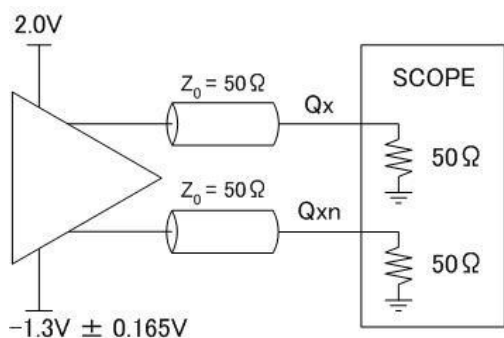


Figure 1 3.3V Output Load Test Circuit

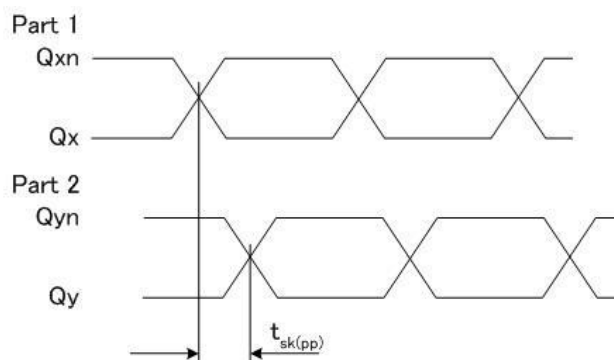


Figure 2 Part-to-Part Skew

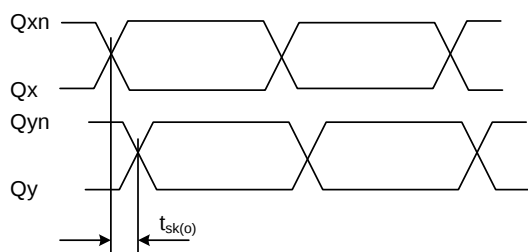


Figure 3 Output Skew

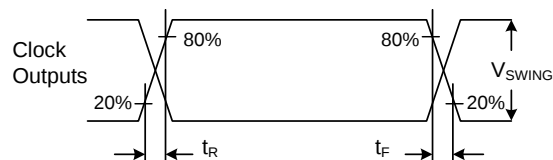


Figure 4 Output Rise/Fall Time

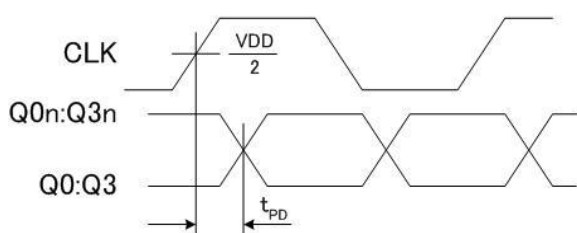


Figure 5 Propagation Delay

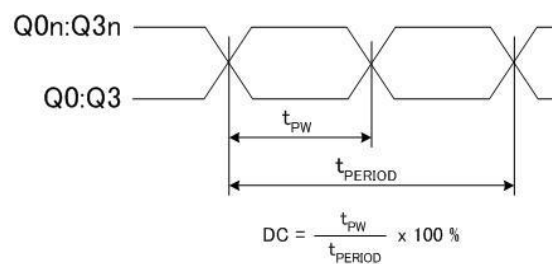


Figure 6 Output Duty/ Pulse Width/ Period

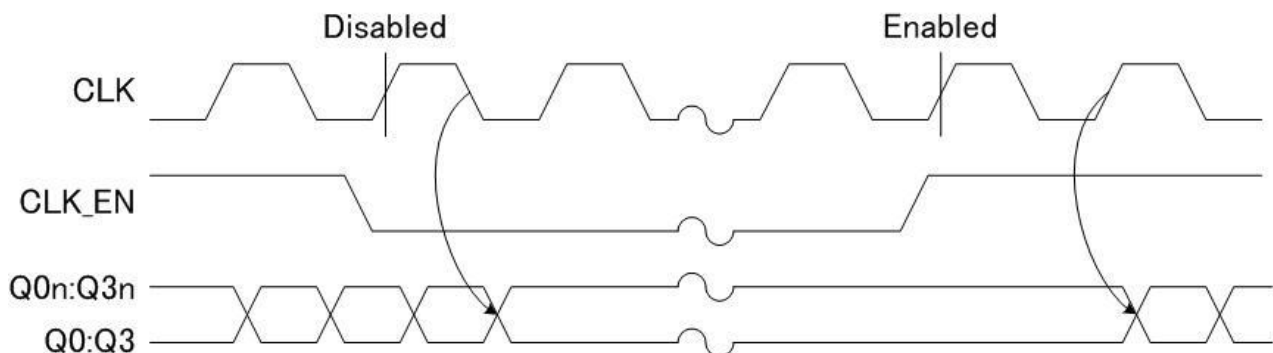
## Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

**Table 1: Control Input Function Table**

| Inputs   |          |                      | Outputs       |                |
|----------|----------|----------------------|---------------|----------------|
| CLK_EN   | CLK_SEL  | Selected Source      | Q0:Q3         | Q0n:Q3n        |
| 0        | 0 (Open) | CLK                  | Disabled: Low | Disabled: High |
| 0        | 1        | XTAL_IN,<br>XTAL_OUT | Disabled: Low | Disabled: High |
| 1 (Open) | 0 (Open) | CLK                  | Enabled       | Enabled        |
| 1 (Open) | 1        | XTAL_IN,<br>XTAL_OUT | Enabled       | Enabled        |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 7. In the active mode, the state of the outputs are a function of the CLK input as described in Table 2.



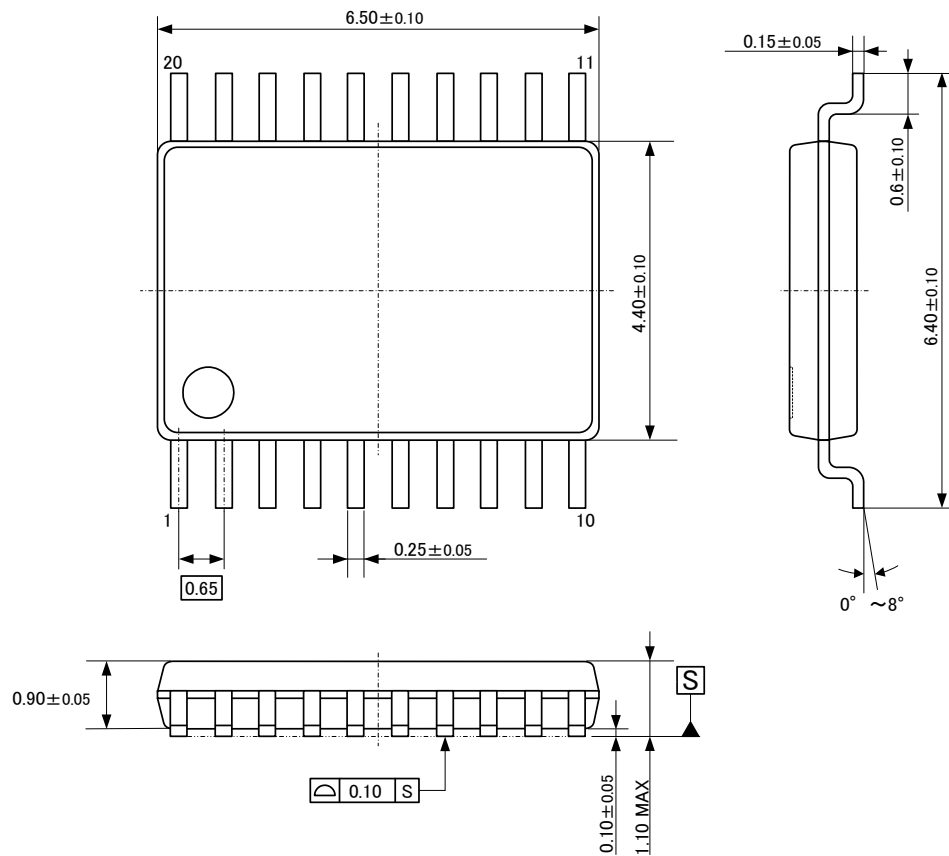
**Figure 7 CLK\_EN Timing Diagram**

**Table 2 Clock Input Function Table**

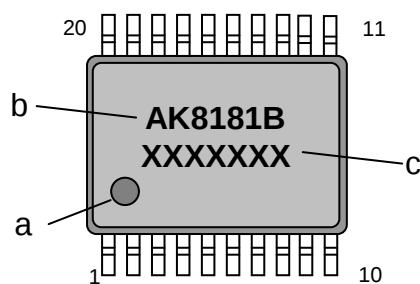
| Inputs | Outputs |           |
|--------|---------|-----------|
| CLK    | Q0 : Q3 | Q0n : Q3n |
| 0      | Low     | High      |
| 1      | High    | Low       |

## Package Information

### • Mechanical data : 20pin TSSOP

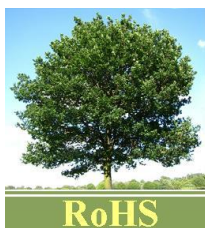


### • Marking



- a: #1 Pin Index
- b: Part number
- c: Date code ( 7 digits)

### • RoHS Compliance



All integrated circuits from Asahi Kasei Microdevices Corporation (AKM) assembled in "lead-free" packages\* are fully compliant with RoHS.

(\*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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