Preliminary

3.3V LVPECL 1:2 Clock Fanout Buffer AK8181C

Features

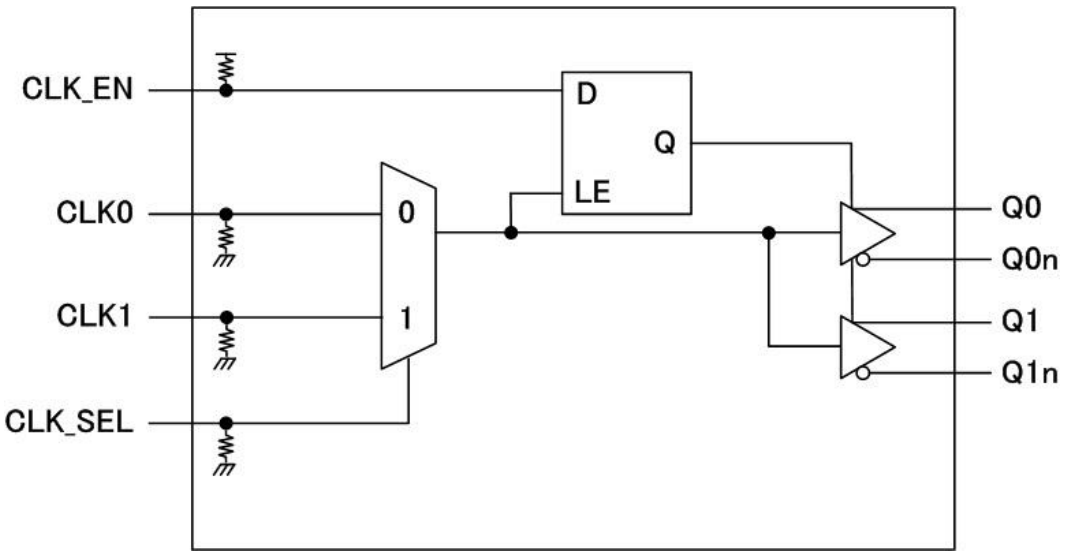
- Two differential 3.3V LVPECL outputs
- Selectable two LVTTL/LVCMOS inputs
- Clock output frequency up to 266MHz
- Output skew : 20ps maximum
- Part-to-part skew : 200ps maximum
- Propagation delay : 1.4ns maximum
- Additive phase jitter(RMS) : 0.03ps(typical)
- Operating Temperature Range: -40 to +85℃
- Package: 14-pin TSSOP (Pb free)
- Pin compatible with ICS8535I-21

Description

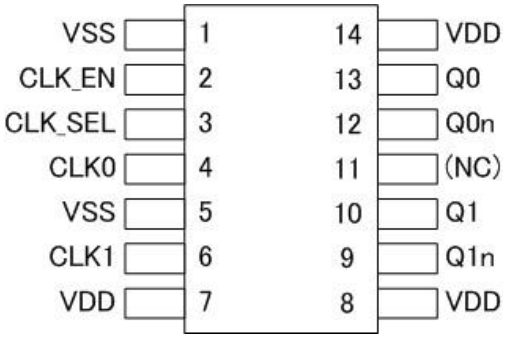
The AK8181C is a member of AKM's LVPECL clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8181C distributes 2 buffered clocks.

AK8181C are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8181C is available in a 14-pin TSSOP package.

Block Diagram



Pin Descriptions



Package: 14-Pin TSSOP(Top View)

Pin No.	Pin Name	Pin Type	Pullup down	Description
1	VSS	PWR	---	Negative power supply
2	CLK_EN	IN	Pull up	Synchronizing clock output enable (LVCMOS/LVTTL) Pin is connected to VDD by internal resistor. (typ. 51kΩ) High (Open): clock outputs follow clock input. Low: Q outputs are forced low, Qn outputs are forced high.
3	CLK_SEL	IN	Pull down	CLK Select Input (LVCMOS/LVTTL) Pin is connected to VSS by internal resistor. (typ. 51kΩ) High: selects CLK1 input Low (Open): selects CLK0 input
4	CLK0	IN	Pull down	LVCMOS/LVTTL Clock Input Pin is connected to VSS by internal resistor. (typ. 51kΩ) *When using CLK1 input (CLK_SEL=High),it should be connected to VSS or opened.
5	VSS	PWR	---	Negative power supply
6	CLK1	IN	Pill down	LVCMOS/LVTTL Clock Input Pin is connected to VSS by internal resistor. (typ. 51kΩ) *When using CLK0 input (CLK_SEL=Low), it should be connected to VSS or opened.
7	VDD	PWR	---	Positive power supply
8	VDD	PWR	---	Positive power supply
9,10	Q1n, Q1	OUT	---	Differential clock output (LVPECL)
11	NC	---	---	No connect
12, 13	Q0n, Q0	OUT	---	Differential clock output (LVPECL)
14	VDD	PWR	---	Positive power supply

PWR: Power pin, IN: Input pin, OUT: Output pin

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage (2)	VDD	-0.3 to 4.6	V
Input voltage (2)	Vin	-0.5 to VDD+0.5	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

(2) VSS=0V

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%, VSS=0V	3.135	3.3	3.465	V

(1) Power of 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}			4		pF
Input Pullup Resistor	R_{PU}			51		kΩ
Input Pulldown Resistor	R_{PD}			51		kΩ

DC Characteristics

All specifications at VDD= 3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage		V_{IH}		2.0		VDD+0.3	V
Input Low Voltage	CLK0, CLK1	V_{IL}		-0.3		1.3	V
	CLK_EN, CLK_SEL			-0.3		0.8	V
Input High Current	CLK0, CLK1, CLK_SEL	I_H	Vin=VDD=3.465V			150	µA
	CLK_EN		Vin=VDD=3.465V			5	µA
Input Low Current	CLK0, CLK1, CLK_SEL	I_L	Vin=VSS, VDD=3.465V	-5			µA
	CLK_EN		Vin=VSS, VDD=3.465V	-150			µA
Output High Voltage(1)		V_{OH}		VDD-1.4		VDD-0.9	V
Output Low Voltage(1)		V_{OL}		VDD-2.0		VDD-1.7	V
Peak-to-Peak Output Voltage Swing		V_{SWING}		0.6		1.0	V
Supply Current		I_{DD}				50	mA

(1) Outputs terminated with 50Ω to VDD-2V.

AC Characteristics

All specifications at VDD= 3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Frequency	f_{OUT}				266	MHz
Propagation Delay(1)	t_{PD}		0.6		1.4	ns
Output Skew(2)(3)	$t_{sk(O)}$				20	ps
Part-to-Part Skew(3)(5)	t_{skPP}				200	ps
Buffer Additive Jitter, RMS	t_{jit}	12kHz to 20MHz@156.25MHz		0.03		ps
Output Rise/Fall Time(4)	t_r, t_f	20% to 80%	200		600	ps
Output Duty Cycle	DC_{OUT}		48	50	52	%

(1) Measured from the VDD/2 of the input to the differential output crossing point.
(2) Defined as skew between outputs at the same supply voltage and with equal load conditions.
(3) This parameter is defined in accordance with JEDEC Standard 65.
(4) Design value.
(5) Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Parameter Measurement Information

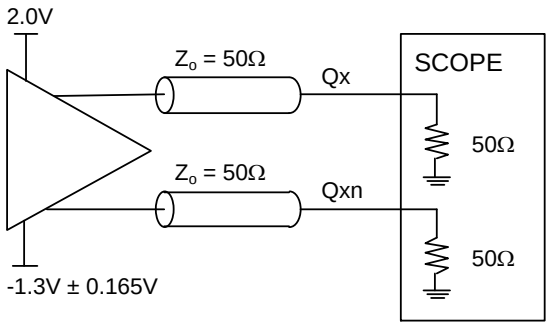


Figure 1 3.3V Output Load Test Circuit

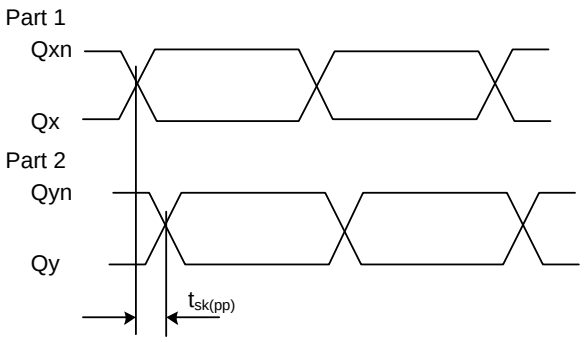


Figure 2 Part-to-Part Skew

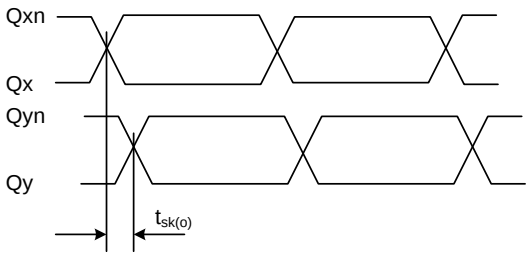


Figure 3 Output Skew

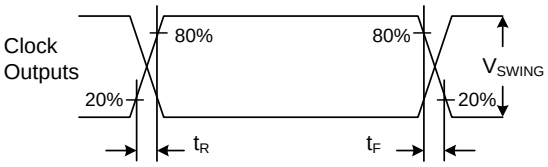


Figure 4 Output Rise/Fall Time

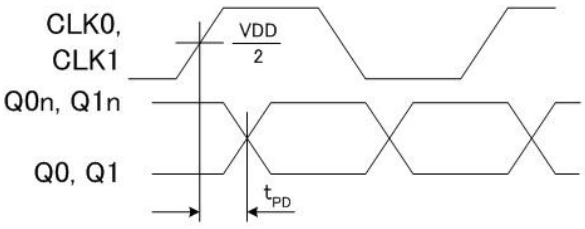


Figure 5 Propagation Delay

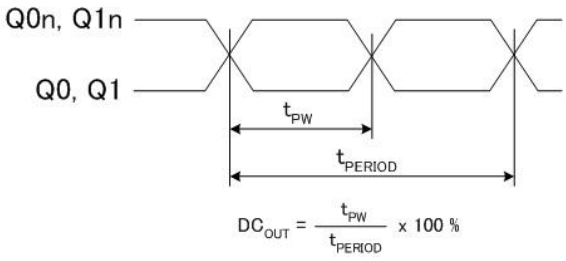


Figure 6 Output Duty/ Pulse Width/ Period

Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0, Q1**	**Q0n, Q1n**
0	0 (Open)	CLK0	Disabled: Low	Disabled: High
0	1	CLK1	Disabled: Low	Disabled: High
1 (Open)	0 (Open)	CLK0	Enabled	Enabled
1 (Open)	1	CLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 7. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 2.

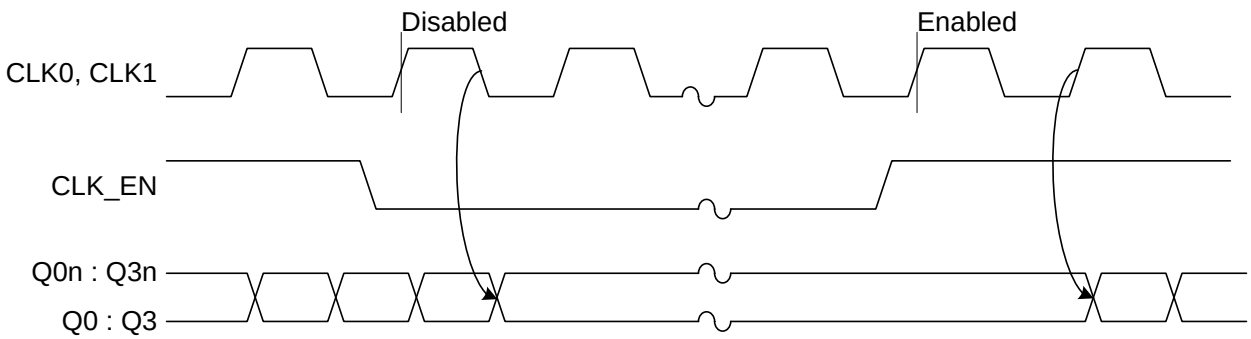


Figure 7 CLK_EN Timing Diagram

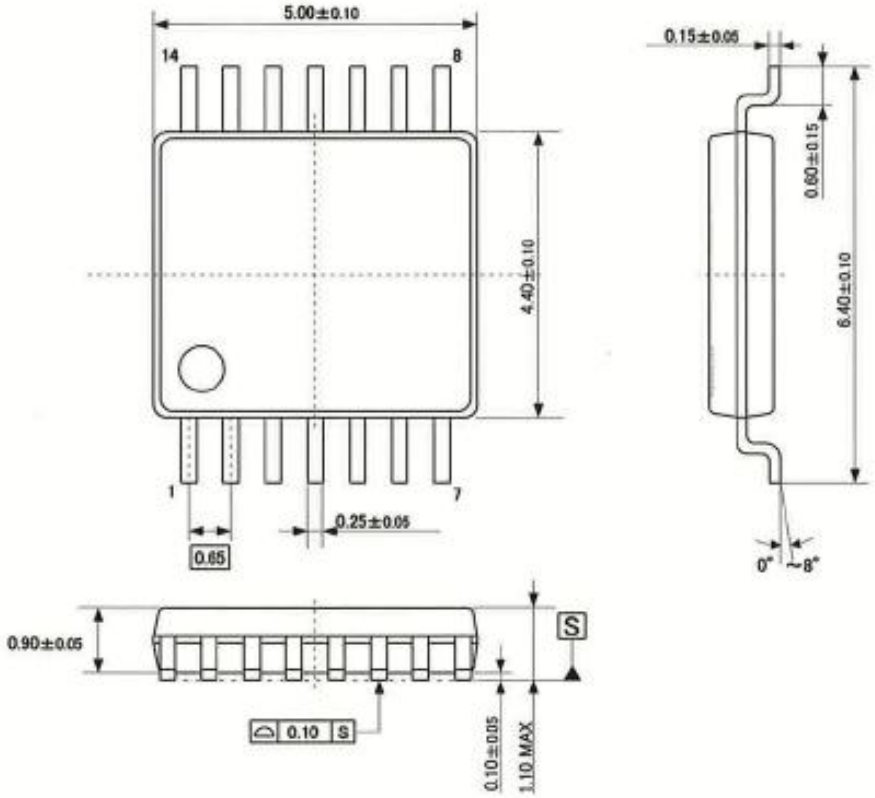
Table 2 Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	**Q0, Q1**	**Q0n, Q1n**
0	Low	High
1	High	Low

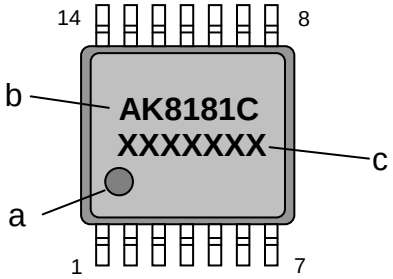
Package Information

- **Mechanical data : 14pin TSSOP**

Preliminary

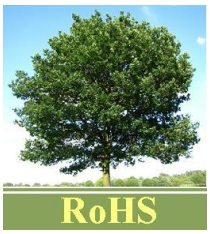


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (7 digits)

- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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