2.5V, 3.3V LVPECL 1:10 Preliminary Clock Fanout Buffer AK8181H

Features

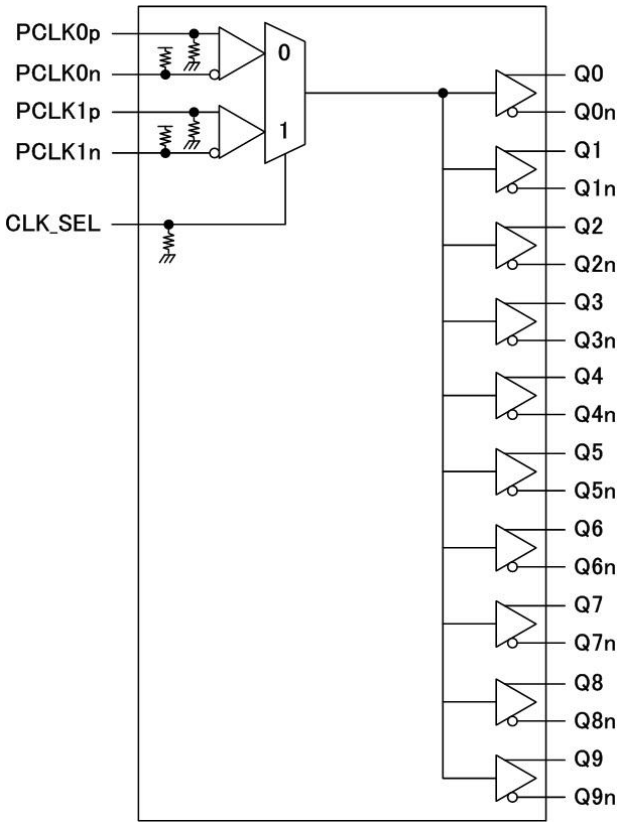
- Ten differential 2.5V, 3.3V LVPECL outputs
- Two Selectable differential inputs
- PCLKxp/n pairs can accept the following differential input levels; LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Clock output frequency up to 700MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on PCLKxn input
- Output skew : 30ps typical
- Part-to-part skew : 340ps maximum
- Propagation delay : (T.B.D)ns maximum
- Additive phase jitter(RMS) : 0.045ps (typical)
- Operating Temperature Range: -40 to +85℃
- Package: 32-pin LQFP (Pb free)
- Pin compatible with ICS85310I-01

Description

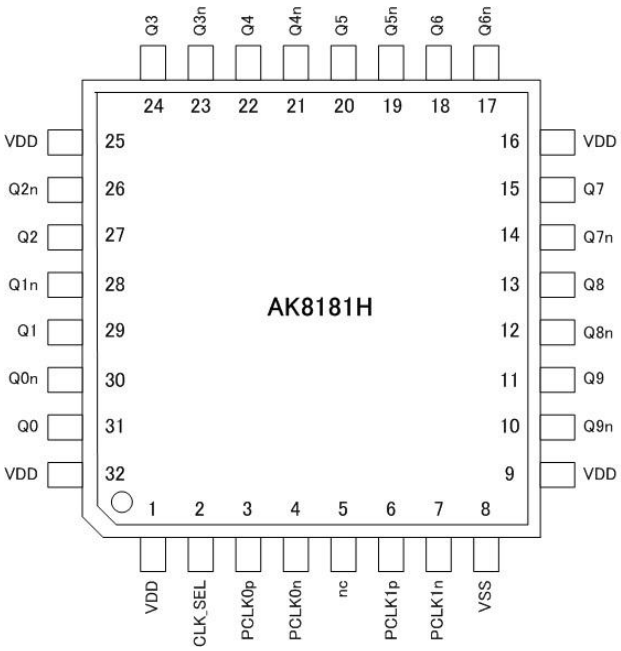
The AK8181H is a member of AKM's LVPECL clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8181H distributes 10 buffered clocks.

AK8181H are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8181H is available in a 32-pin LQFP package.

Block Diagram



Pin Descriptions



Package: 32-Pin LQFP(Top View)

Pin No.	Pin Name	Pin Type	Pullup down	Description
1, 9, 16, 25, 32	VDD	PWR	---	Positive power supply
2	CLK_SEL	IN	Pull down	CLK Select Input (LVCMOS/LVTTL) Pin is connected to VSS by internal resistor. (typ. 51kΩ) High: selects PCLK1p/n inputs Low (Open): selects PCLK0p/n inputs
3	PCLK0p	IN	Pull down	Non-inverting differential clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ) *When using PCLK1 input (CLK_SEL=High), it should be connected to VSS or opened.
4	PCLK0n	IN	Pull up	Inverting differential clock input Pin is connected to VDD by internal resistor. (typ. 51kΩ) *When using PCLK1 input (CLK_SEL=High), it should be connected to VDD or opened.
5	nc		---	No connect
6	PCLK1p	IN	Pull down	Non-inverting differential LVPECL clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ) *When using PCLK0 input (CLK_SEL=Low), it should be connected to VSS or opened.
7	PCLK1n	IN	Pull up	Inverting differential clock input Pin is connected to VDD by internal resistor. (typ. 51kΩ) *When using PCLK0 input (CLK_SEL=Low), it should be connected to VDD or opened.
8	VSS	PWR	---	Negative power supply

Pin No.	Pin Name	Pin Type	Pullup down	Description
10, 11	Q9n, Q9	OUT	---	Differential clock output (LVPECL/ECL)
12, 13	Q8n, Q8	OUT	---	Differential clock output (LVPECL/ECL)
14, 15	Q7n, Q7	OUT	---	Differential clock output (LVPECL/ECL)
17, 18	Q6n Q6	OUT	---	Differential clock output (LVPECL/ECL)
19, 20	Q5n, Q5	OUT	---	Differential clock output (LVPECL/ECL)
21, 22	Q4n, Q4	OUT	---	Differential clock output (LVPECL/ECL)
23, 24	Q3n, Q3	OUT	---	Differential clock output (LVPECL/ECL)
26, 27	Q2n, Q2	OUT	---	Differential clock output (LVPECL/ECL)
28, 29	Q1n, Q1	OUT	---	Differential clock output (LVPECL/ECL)
30, 31	Q0n, Q0	OUT	---	Differential clock output (LVPECL/ECL)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8181H	AK8181H	Tape and Reel	32-pin LQFP	-40 to 85 °C

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage (2)	VDD	-0.3 to 4.6	V
Input voltage (2)	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

(2) VSS=0V

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Positive supply voltage (1)	VDD		2.375	3.3	3.8	V

(1) Power of 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}			4		pF
Input Pullup Resistor	R_{PU}			51		kΩ
Input Pulldown Resistor	R_{PD}			51		kΩ

Power Supply Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Current	I_{DD}				115	mA

DC Characteristics (LVCMOS/LVTTL)

All specifications at VDD = 2.375V to 3.8V, VSS = 0V, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage		V_{IH}	VDD = 3.3V	2.0		VDD+0.3	V
			VDD = 2.5V	1.7		VDD+0.3	V
Input Low Voltage		V_{IL}	VDD = 3.3V	-0.3		0.8	V
			VDD = 2.5V	-0.3		0.7	V
Input High Current	CLK_SEL	I_{IH}	Vin = VDD = 3.8V			150	μA
Input Low Current	CLK_SEL	I_{IL}	Vin = VSS, VDD = 3.8V	-5			μA

DC Characteristics

All specifications at VDD = 2.375V to 3.8V, VSS = 0V, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Current	PCLKxp	I_{IH}	Vin = VDD = 3.8V or 2.625V			150	μA
	PCLKxn		Vin = VDD = 3.8V or 2.625V			5	μA
Input Low Current	PCLKxp	I_{IL}	Vin = VSS, VDD = 3.8V or 2.625V	-5			μA
	PCLKxn		Vin = VSS, VDD = 3.8V or 2.625V	-150			μA
Peak-to-Peak Input Voltage		V_{PP}		0.15		1.3	V
Common Mode Input Voltage (1) (2)		V_{CMR}		VSS+0.5		VDD-0.85	V

(1) V_{IL} should not be less than -0.3V.

(2) Common mode voltage is defined as V_{IH}.

DC Characteristics (LVPECL)

All specifications at VDD = 2.375V to 3.8V, VSS = 0V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output High Voltage (1)	V_{OH}		VDD-1.4		VDD-0.9	V
Output Low Voltage (1)	V_{OL}		VDD-2.0		VDD-1.7	V
Peak-to-Peak Output Voltage Swing	V_{SWING}		0.6		1.0	V

(1) Outputs terminated with 50Ω to VDD-2V.

AC Characteristics

All specifications at VDD = 2.375V to 3.8V or, VSS = 0V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Frequency	f_{OUT}				700	MHz
Propagation Delay (1)	t_{PD}				T.B.D	ns
Output Skew (2) (3)	$t_{sk(O)}$			30		ps
Part-to-Part Skew (3) (4)	t_{skPP}				340	ps
Buffer Additive Jitter, RMS (5)	t_{jit}	155.52MHz (12kHz – 20MHz)		0.045		ps
Output Rise/Fall Time (5)	t_r, t_f	20% to 80%	150		500	ps
Output Duty Cycle	DC_{OUT}		47	50	53	%

All parameters measured at f ≤ 700MHz unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

(1) Measured from the differential input crossing point to the differential output crossing point.

(2) Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

(3) This parameter is defined in accordance with JEDEC Standard 65.

(4) Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

(5) Design value.

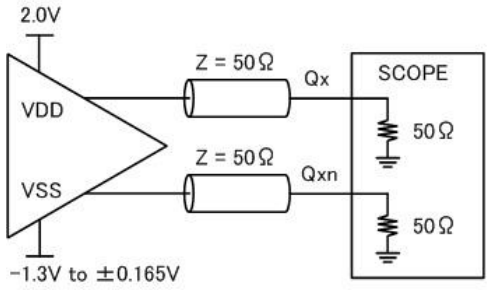


Figure 1 LVPECL Output Load AC Test Circuit

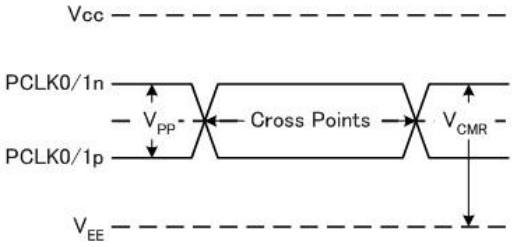


Figure 2 Differential Input Level

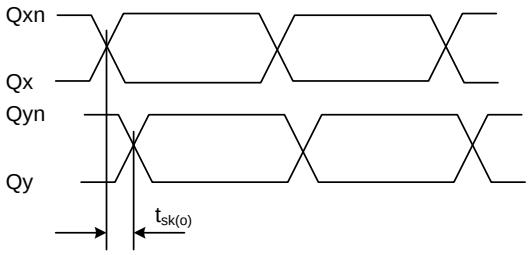


Figure 3 Output Skew

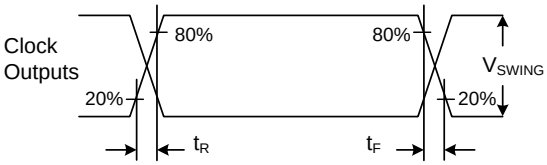


Figure 4 Output Rise/Fall Time

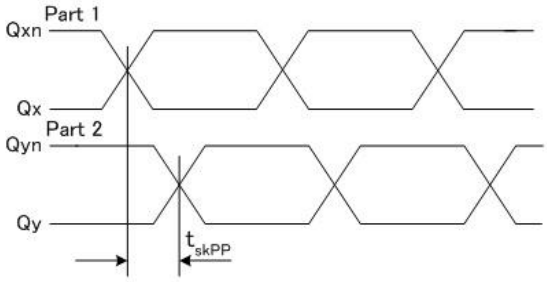


Figure 5 Part-to-Part Skew

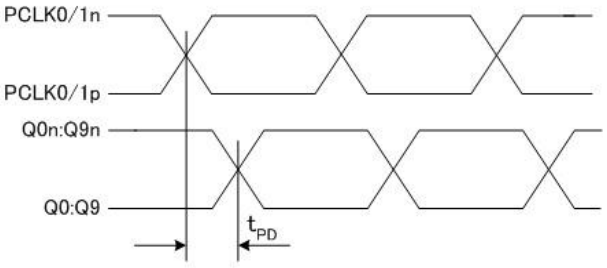


Figure 6 Propagation Delay

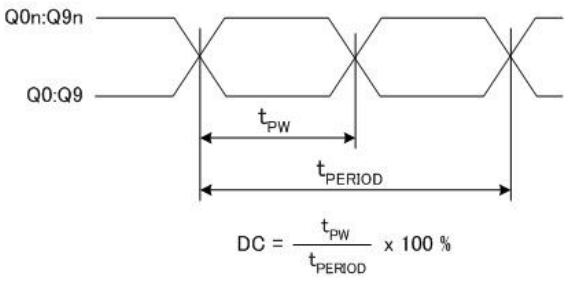


Figure 7 Output Duty/ Pulse Width/ Period

Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control Input Function Table

Inputs		Outputs		Input to Output	Polarity
PCLK0/1p	PCLK0/1n	Q0:Q9	Q0n:Q9n		
0	1	Low	High	Differential to Differential	Non Inverting
1	0	High	Low	Differential to Differential	Non Inverting
0	Biased (1)	Low	High	Single Ended to Differential	Non Inverting
1	Biased (1)	High	Low	Single Ended to Differential	Non Inverting
Biased (1)	0	High	Low	Single Ended to Differential	Inverting
Biased (1)	1	Low	High	Single Ended to Differential	Inverting

(1) Please refer to the application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

Table 2 Clock Input Function Table

Inputs	
CLK_SEL	Selected Source
0	PCLK0p/n
1	PCLK1p/n

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure.8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = VDD/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and VDD = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

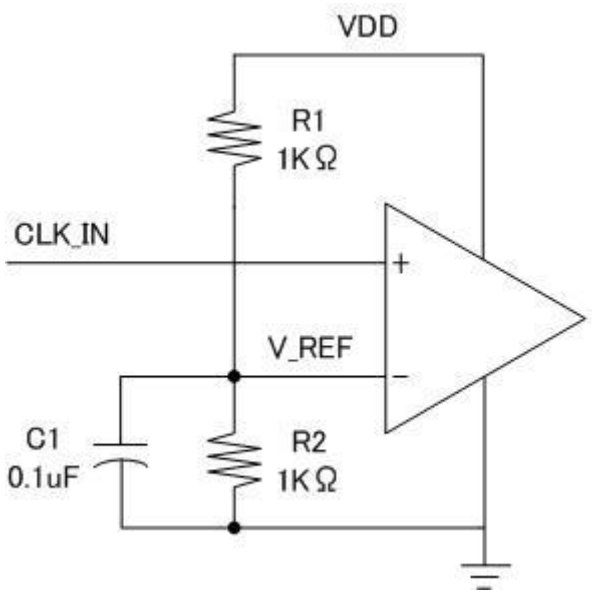
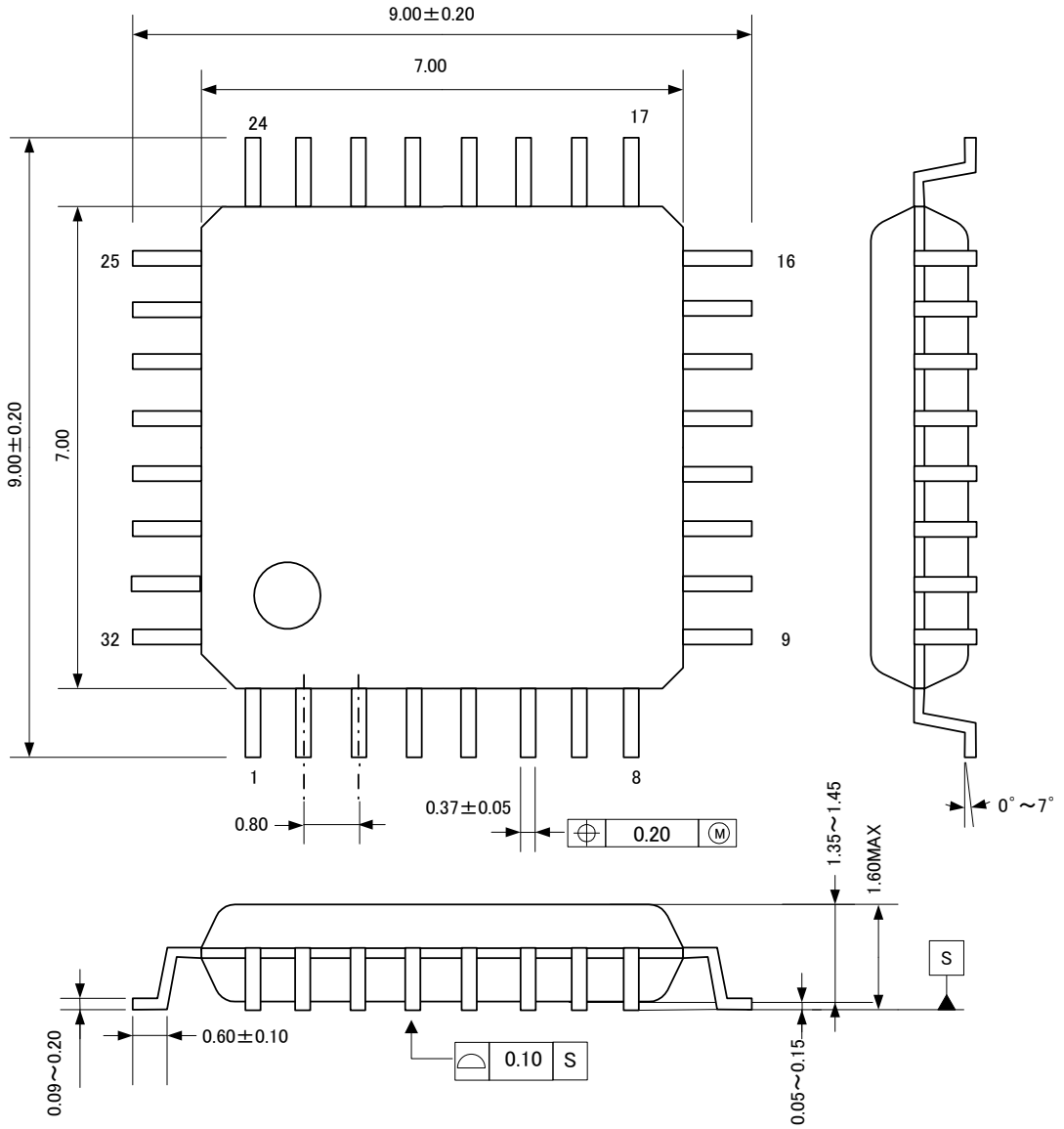


Figure 8 Single Ended Signal Driving Differential Input

Package Information

- **Mechanical data : 32pin LQFP**

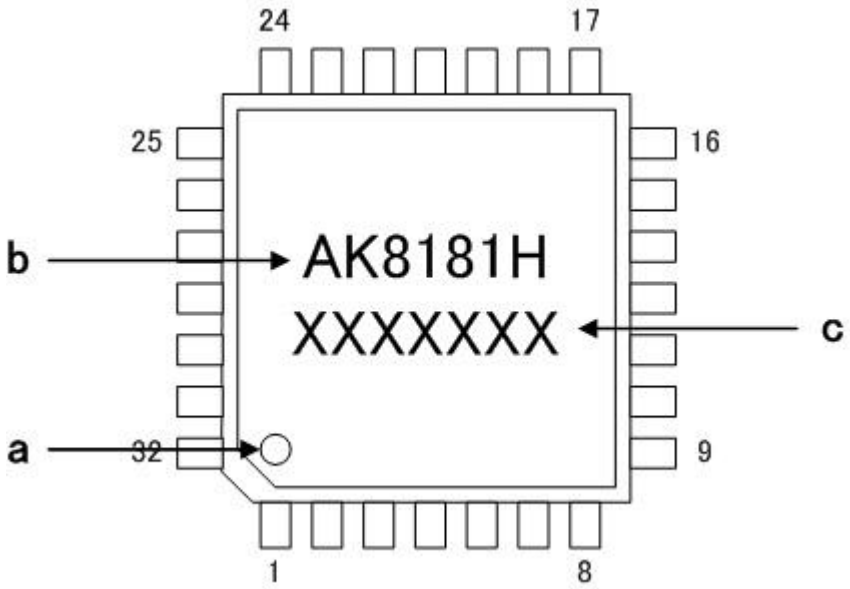
Preliminary



- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (7 digits)

Preliminary



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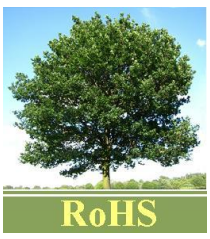
- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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