= PRELIMINARY = AK8408

Shading Correction Pre-Processor for color sensor

Features

☐Shading correction LSI for color sensor

☐Supports various sensor's interface

1ch sensor, G/R/B 3ch sensor

Sensor clock generation

Max. input level 1.25Vp-p

Processing speed:

1ch: 10M samples / sec

3ch: 3.3M×3 samples / sec

Max. sensor length 8192×3 (programmable by 8pixles / step)

Max. dummy pixel 260 (programmable by 1pixel / step)

☐10bit ADC included

Contrast adjustment possible by 2×8bit DACs, which are volumes for black reference voltage and for white reference voltage of ADC.

☐ADC (detector) and programmable gain amplifier (corrector) for white shading

Correction 60% range of peak level (actual correction resolution is near 10bit)

External memory necessary (9bit× number of pixels)

☐ADC(detector) and DAC(corrector) for black shading

Correction range is ±50mV~±200mV. (programmable by ±50mV / step)

Pixel to pixel correction (external memory necessary (8bit× number of pixels)

Internal register for R/G/B access (R/W) possible

Offset adjustment registers for internal black offset

☐8bit PGA for 3ch gain adjustment (×1~×4). Support logic for gain adjustment.

☐Pulse width adjustment type gain control for 1ch CIS

☐8bit peak detect / hold

☐Offset calibration circuit(Input ~ 10bit ADC)

☐Serial I/F

☐Shading memory interface

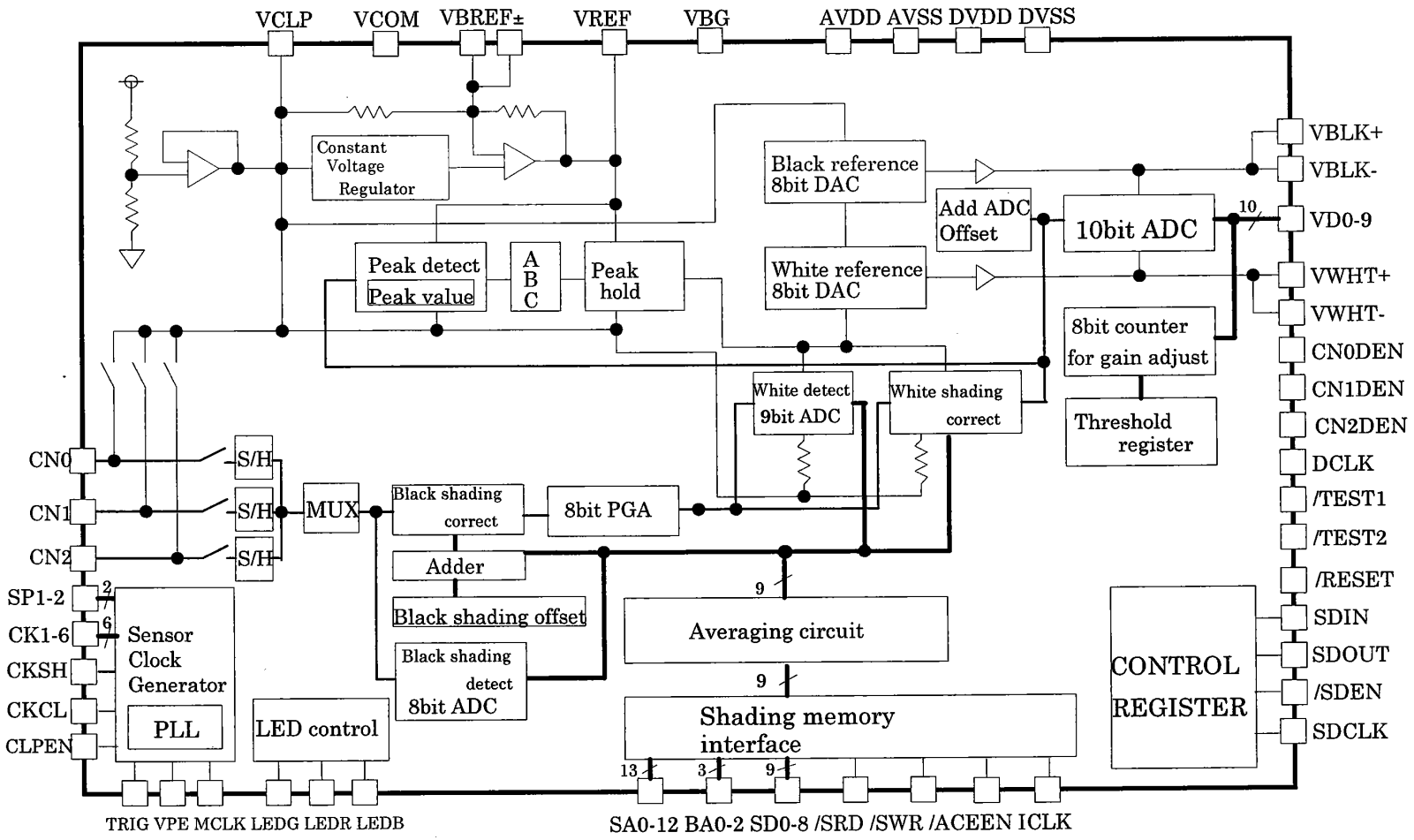
Shading data averaging circuit

Access possible to the shading memory by external device

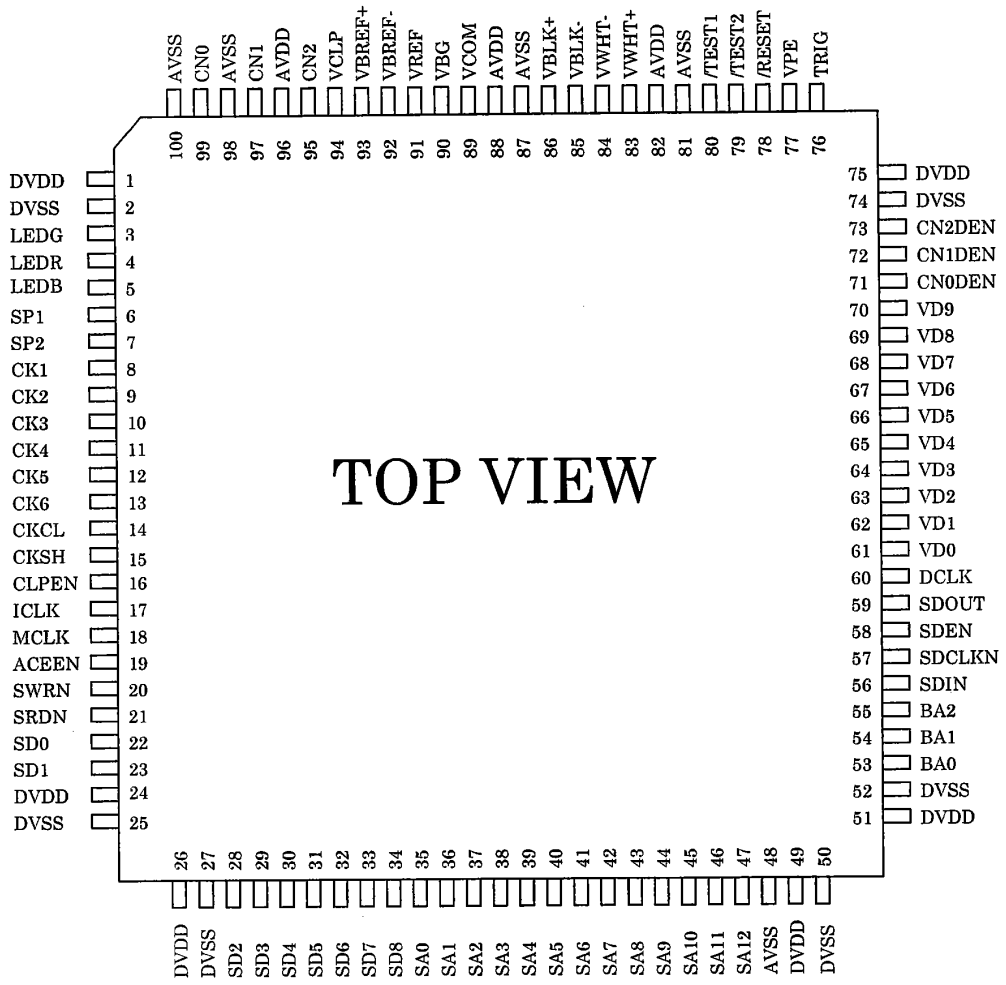
☐Clock frequency 1.5~10MHz (data rate). PLL generate ×4 clock or ×12 clock

☐CMOS monolithic LSI. +5V single power supply (5V±5%). Constant voltage regulator.

☐100pin LQFP


VCLP
VCOM
VBREF±
VREF
VBG
AVDD AVSS DVDD DVSS
Constant Voltage Regulator
Black reference 8bit DAC
Add ADC Offset
10bit ADC
10
VBLK+
VBLK-
VD0-9
Peak detect
Peak value
A
B
C
Peak hold
White reference 8bit DAC
VWHT+
VWHT-
8bit counter for gain adjust
Threshold register
White detect 9bit ADC
White shading correct
CN0DEN
CN1DEN
CN2DEN
DCLK
/TEST1
/TEST2
/RESET
SDIN
SDOUT
/SDEN
SDCLK
CN0
CN1
CN2
S/H
S/H
S/H
MUX
Black shading correct
8bit PGA
Adder
Black shading offset
Black shading detect 8bit ADC
9
Averaging circuit
9
Shading memory interface
CONTROL REGISTER
SP1-2
CK1-6
CKSH
CKCL
CLPEN
2
6
Sensor Clock Generator
PLL
LED control
13
3
9
TRIG VPE MCLK LEDG LEDR LEDB
SA0-12 BA0-2 SD0-8 /SRD /SWR /ACEEN ICLK

Pin Assignment



Pin Function

Pin name	I/O	Function
		Shading memory I/F
SA0-12	O(Tri)	Shading memory address bus.
BA0-2	O(Tri)	Shading memory bank select signal.
SD0-8	I/O(Tri)	Shading memory data bus.
/SRD	O(Tri)	Shading memory read signal.
/SWR	O(Tri)	Shading memory write signal.
/ACEEN	O(Tri)	Shading memory access enable (for external device)
		Control register I/F
/SDEN	I	Serial interface enable signal
SDCLK	I	Serial clock input
SDIN	I	Serial data input
SDOUT	O(Tri)	Serial data output.
		Video output data I/F
VD0-9	O	Video output data bus
CN0DEN	O	Video data enable signal 1ch: The video data which corresponds to LEDG enable signal 3ch: The video data which is sampled at CN0 enable signal
CN1DEN	O	Video data enable signal 1ch: The video data which corresponds to LEDR enable signal 3ch: The video data which is sampled at CN1 enable signal
CN2DEN	O	Video data enable signal 1ch: The video data which corresponds to LEDB enable signal 3ch: The video data which is sampled at CN2 enable signal
DCLK	O	Video data sampling clock Please get the video data at DCLK falling timing externally
		Main clock and etc.
MCLK	I	Main clock input
VPE	I	Image processing enable signal input
TRIG	I	TRIG signal input. This signal should be always running.
ICLK	O	Internal main clock (×4 or ×12 of main clock, which depends on the mode)

Pin name	I/O	Function
		Sensor clock
CKCL	O	Internal clamp switch clock output (for monitoring)
CKSH	O	Internal Sample / Hold clock output (for monitoring)
CLPEN	O	Line clamp enable (for monitoring)
CK1-6	O	Sensor clock
SP1-2	O	Shift pulse for sensor
LED (GRB)	O	LED control signal for sensor
		Other digital pin
/RESET	I	Reset
/TEST1	I	Test pin. Pull up to high level externally
/TEST2	I	Test pin. Pull up to high level externally
		Analog pin
CN0	I	Sensor signal input In case of using 1ch sensor, please input sensor signal to this pin.
CN1	I	Sensor signal input
CN2	I	Sensor signal input
VCLP	O	Clamp voltage buffer output. External capacitor is necessary.
VREF	O	Reference voltage buffer output. External capacitor is necessary.
VCOM	O	Internal reference voltage buffer. External capacitor is necessary.
VBREF+/-	O	Reference voltage buffer output for black correction / detection (differential output). External capacitor is necessary for each pin.
VWHT+/-	O	White-side reference voltage buffer output for 10bit ADC (differential output). External capacitor is necessary for each pin.
VBLK+/-	O	Black-side reference voltage buffer output for 10bit ADC (differential output). External capacitor is necessary for each pin.
BIAS	O	Bias current setting pin. Connect 15KΩ between BIAS and AGND.
VBG	O	Reference voltage buffer output. External capacitor is necessary between this pin and Ground.

Pin name	I/O	Function
Power supply		
DVDD	I	Digital power supply (5V±5%)
DVSS	I	Digital VSS
AVDD	I	Analog power supply (5V±5%)
AVSS	I	Analog VSS

Function Description

■Analog circuit

(1) Reference voltage generator

- •Clamp reference voltage (Vclp = 2.1V typ.) is generated by the resistor ladder network
- •Internal white-side reference voltage (Vref = 0.85V typ.) is generated by the constant voltage regulator.

(2) Sensor signal input circuit

- •Polarity of input signal is white downward. If the polarity is opposite such as CIS sensor, input signal should be inverted externally.
- •3ch clamp circuits and 3ch sample/hold circuits are included. 1ch sensor (10M) or 3ch sensor (3.3M×3) can be selected by a control register.
- •Internal analog switch and external capacitor makes up the clamp circuit.

(3) Black shading detect ADC / correction circuit

- •Correction data, which shows the difference between clamp level and analog signal level of each pixel (pixel to pixel mode) or of the specified pixel (black offset cancel mode) is detected by 8bit ADC. Both of positive and negative black shading to the clamp level can be detected and corrected.
- •Black correction is achieved by subtracting the correction voltage, which is generated by the pre-detected correction data, from analog input signal. It is possible to select the full scale of the range (Brange) from ±50mV to ±200mV by ±50mV step by control register. Please note that 25mV(MAX) of full scale is consumed for LSI internal offset cancel, so actual detection / correction range is decreased to Brange - 25mV.

(4) PGA circuit

- •To adjust the signal level of each channel, AK8408 has a gain adjust circuit.
- •Gain adjustment is achieved by amplifying the black corrected signal. The gain is set by 3 PGA gain setting registers (×1~×4) for each channel.

(5) Peak detection / hold circuit

- Peak detection / hold circuit is structured by a low speed 8bit ADC, a 8bit DAC, and some digital logic.
- Input signal into the peak detection circuit is the black shading corrected signal at the peak detect mode, and black and white shading corrected one when ABC/AGC is on at the document scanning mode.

(6) White shading detect ADC / correction circuit

- White shading detector 9bit ADC, whose full scale is between VPEAK and 40% of VPEAK, detects the white shading data.
- White correction is achieved by amplifying the black corrected analog signal by the pre-detected correction data.

(7) Reference voltage generator for the video ADC (DAC1, DAC2)

- DAC1 and DAC2 are 8bit DACs which generate the black and white reference voltage for the ADC. Reference voltage can be defined by the programmable relative ratio of the difference between VPEAK and VCLP.

(8) 10bit video ADC

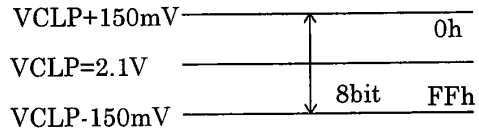
- 10bit ADC which converts the black and white corrected analog signal to digital data finally.
- ADC full scale is controlled by the DAC1 and DAC2.

(9) Black offset adjustment circuit

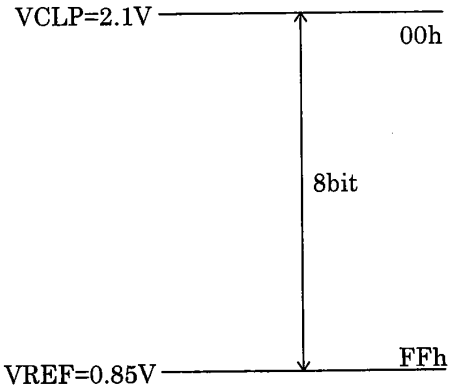
- LSI internal offset(input ~ white shading correction) is canceled by adding or subtracting detected offset automatically. Calibration data are stored in the internal registers(R23, R27, R28) by each channel.

(10) ADC offset adjustment circuit

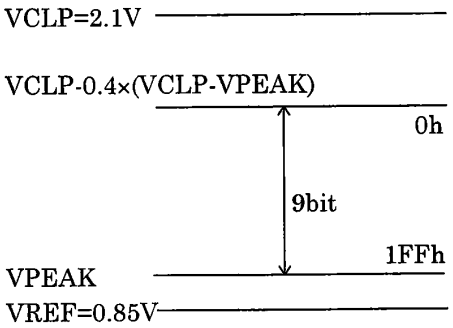
- LSI internal offset(ADC) is canceled by adding or subtracting detected offset automatically. Calibration data is stored in the internal register(R29).



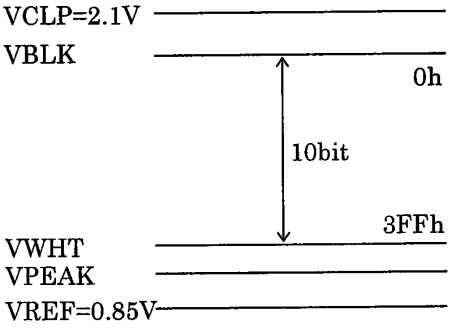
Black shading detection/correction
(In case that correction range is set ±150mV)



Peak detection/hold



White shading detection/correction



Video 10bit ADC

Supported sensors and sensor signal control

■Input multiplexer circuit control

Supported sensors are shown below.

Sensor	color / nomo	R12 / D7	R12 / D6	data rate
3ch color sensor	color	*	1	3.3M×3
	monochrome	*	1	3.3M×1
1ch color sensor	color	0	0	10M
	monochrome	1	0	10M
1ch monochrome sensor	monochrome	1	0	10M

Please refer to the section which describes the "channel enable register" about the details of using for each sensor or each color / monochrome mode.

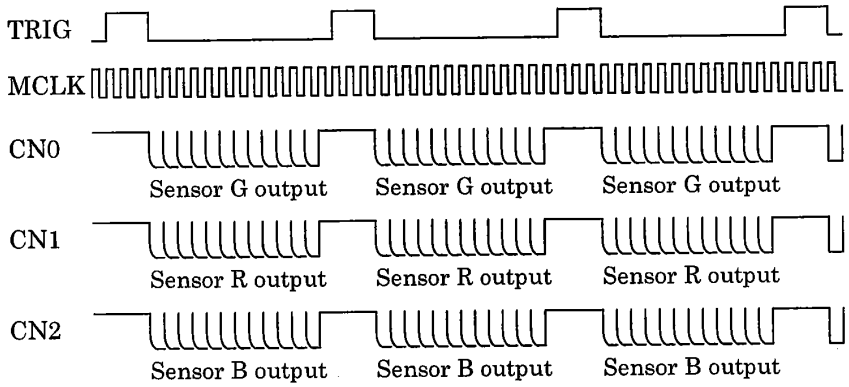
□3ch color sensor (color mode)

(1) Sampling rate is 3.3M/sec (max).
Processing speed is 10M/sec (max).

(2) Input signals from all 3ch are sampled at the same time. And the multiplexer circuit is automatically switched according to the pre-defined processing order.

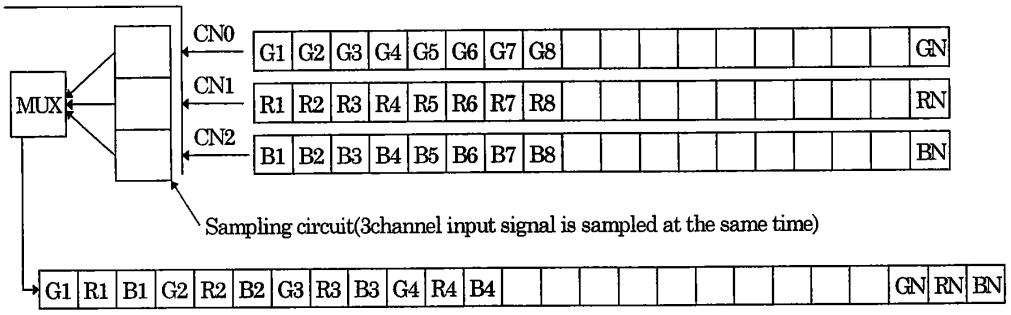
(3) The sampled N×3 data are re-ordering as shown next page, and treat as pseudo 1line data internally.

[3ch sensor output]
(ex. CN0 is green signal, CN1 is red signal, CN2 is blue signal)



[3ch sensor processing]

(ex. Processing order setting is CN0→CN1→CN2)



Nx3 sampled data are treated as 1 line data

□3ch color sensor (monochrome mode)

Monochrome image processing is possible by using the specified channel among 3 channels. In this case, maximum sampling and processing rate is 3.3M samples / sec. The correction data which have detected already may be used as they are.

Or, it is possible to change the main clock to max. 10MHz, and treat as a monochrome sensor. We recommend the correction data should be taken again for the new conditions in this case. Please refer the section 1ch color sensor (monochrome mode) section. And please refer to the sensor data sheet also.

□1ch color sensor (color mode)

(1) Sampling rate and processing speed are 10M/sec (max).

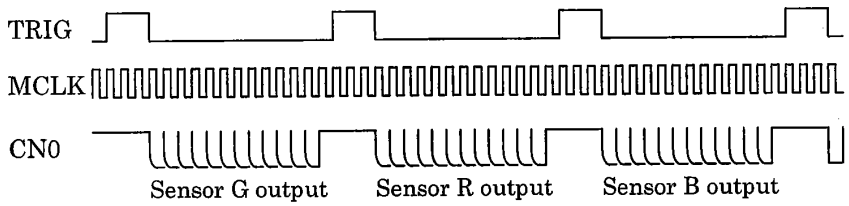
(2) Please input sensor signal to CN0.

(3) The color of sensor signal changes line by line. The processing color in AK8408 automatically changed.

(4) The color processing order is set by the register. The sampled GRB data from consecutive 3lines is treated as a pseudo 1line data.

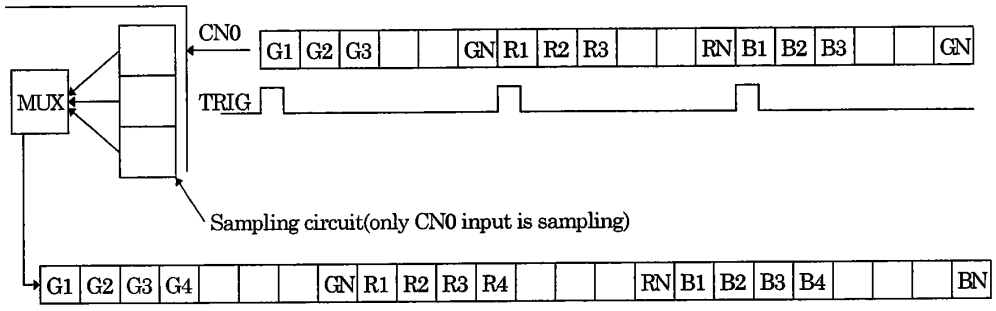
[1ch color sensor output]

(ex. Sampling, Processing order setting is G→R→B)



[1ch color sensor processing]

(ex. Sampling, Processing order setting is G→R→B)



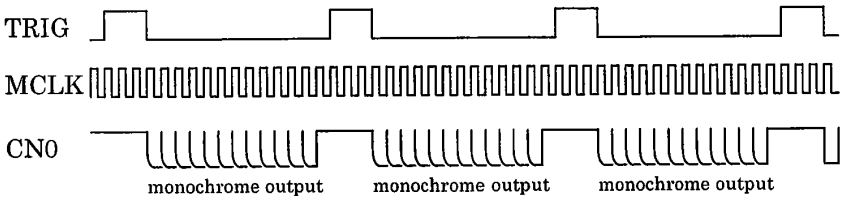
Nx3 sampled data are treated as a pseudo1 line data

□1ch color sensor (monochrome mode)

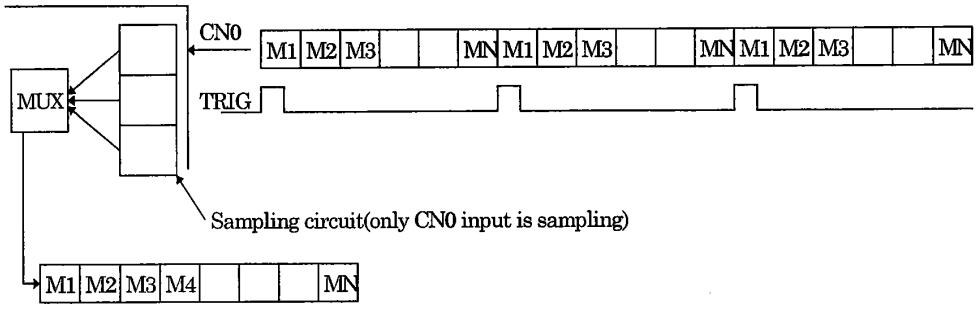
(1) Sampling rate and processing speed are 10M/sec (max).

(2) Please input sensor signal to CN0.

[1ch sensor monochrome output]



[1ch sensor monochrome processing]



□Monochrome sensor

Same as 1ch color sensor (monochrome mode).

□Channel switching mode in CIS(Color)

This is special mode in case of CIS.

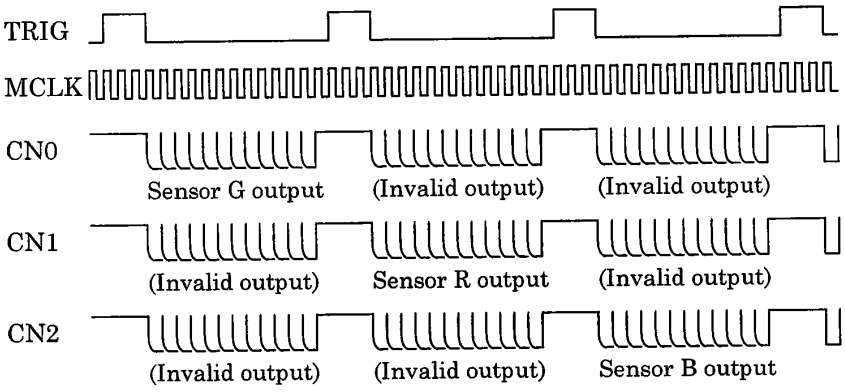
(1) Sampling rate, image processing speed are 10Mpixels/sec.

(2) Sampling channel is switched line by line. The channel multiplexer is switched in accordance with the defined order.

(3) Data set which composed by green, red, blue data is seemed to be 1 set data from peak detect or ABC/AGC point view.

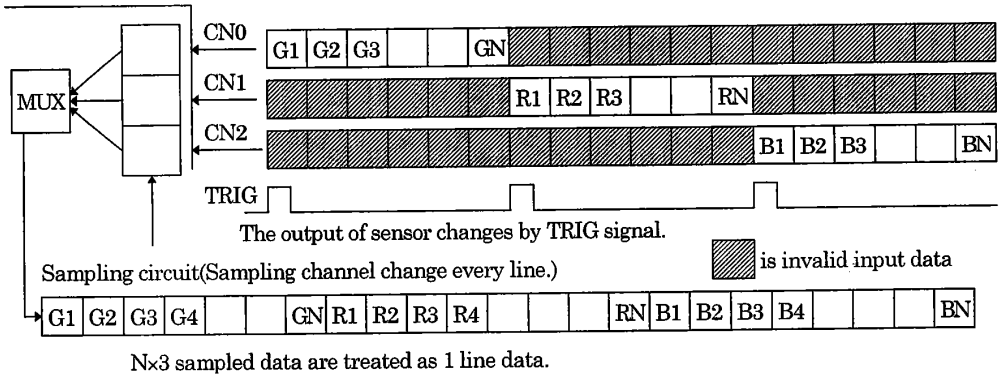
[CIS output]

(Example) Sampling order G→R→B)



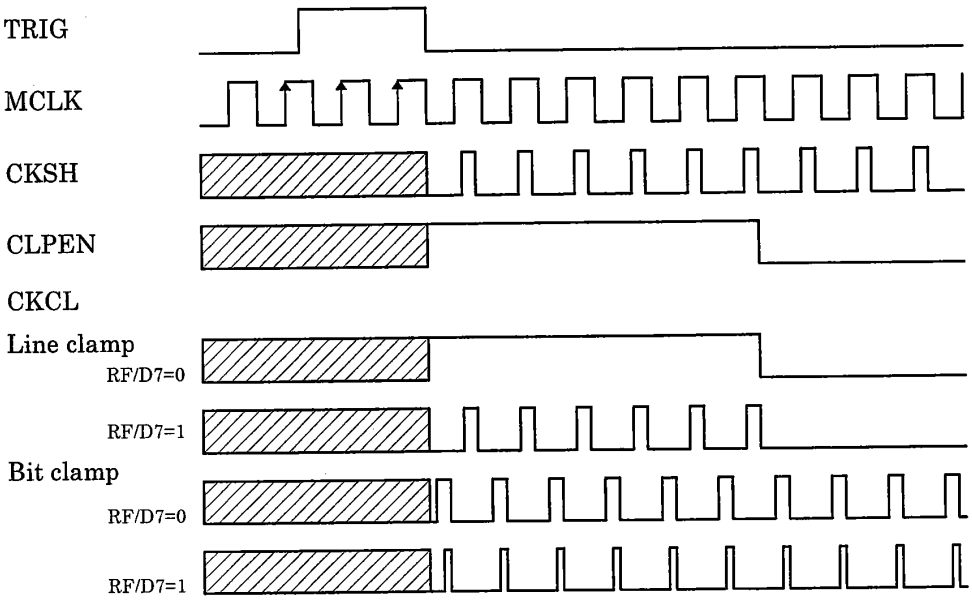
[3 channel image processing]

(Example) Sampling order CN0→CN1→CN2



N×3 sampled data are treated as 1 line data.

□Sample / hold, clamp timing



(1) MCLK frequency is the same as the sensor data rate.
In 1ch mode, maximum rate is 10MHz, and in 3ch mode, maximum rate is 3.3MHz.

(2) In case of 3ch mode, the sample / hold and clamp is done simultaneously for all channels.

(3) In the bit clamp mode (RF/D6=0), clamp pulse can be changed by register RF/D7.

	RF / D7 = 0	RF / D7 = 1
Bit clamp	1/4 MCLK	1/8 MCLK

(4) In the line clamp mode(RF/D6=1), clamp pulse form can be changed by register RF/D7.

	RF / D7 = 0	RF / D7 = 1
Line clamp	CLPEN	CLPEN∩CKSH

Offset calibration

■ Offset calibration mode

Black shading correction circuit, white shading correction circuit, and ADC in this LSI have offsets. There are two modes for canceling the offsets.

Offset calibration mode 1,2 continuously execute before Black shading detection and White shading detection.

□ Offset calibration mode 1

This mode is for canceling internal offset of the path from input to white shading correction circuit. This mode takes 2 lines time.

In this mode input of each channel(CN0, CN1, CN2) signal should not be cared.

(1) 1st line operation

Setting an appropriate practical gain(R15,R16,R17) for each channel, and executing this mode, calibration starting data is detected and stored in the internal register.

(2) 2nd line operation

Updating the starting calibration data for minimizing the code difference between by unity gain and by maximum gain. After that operation, BUSY flag becomes 'L' state.

This sequence must be done for each channel(CN0,CN1,CN2) or each color(B,R,G) one by one. Channel(Color) appointment set Channel enable register(R12/D2-D0)(total 3 times).Monochrome mode(R12/D7=1) don't need channel appointment (total 1 times).

Calibrated offset depends on the black shading correction range. Namely the smaller that range is, the smaller residual offset is.

(Note) In this mode the pixel number setting(R0C/R0D) must be more than 128.

□ Offset calibration mode 2

This mode is for canceling internal offset of 10bit ADC. This mode takes 2 lines time.

In this mode input of each channel(CN0, CN1, CN2) signal should not be cared.

This mode execute 1 times both color mode and monochrome mode.

(1) 1st line operation

Setting the same gain in the offset calibration mode 1 for each channel, and executing this mode, calibration starting data is detected and stored in the internal register.

(2) 2nd line operation

Updating the starting calibration data till 10bit ADC code 0 appears.

Calibrated offset depends on the black shading correction range.

(Note) In this mode the pixel number setting(R0C/R0D) must be more than 128.

(Note) Please set up Pre-dummy pixel counts(RE) register temporarily as showing below before offset calibration mode 1 is operated.

(1)1 ch Mode (R12/D6=0)

- CK1,CK2 clock mode =mode 1,2(CCD)(RF/D3=0)
  Dummy pixel number set up odd.(Ex. 1,3····)
- CK1,CK2 clock mode =mode 3,4(CIS)(RF/D3=1)
  Dummy pixel number set up even. (Ex. 0,2····)

(2)3 ch Mode (R12/D6=1)

- CK1,CK2 clock mode =mode 1,2(CCD)(RF/D3=0)
  Dummy pixel number set up even. (Ex. 0,2····)
- CK1,CK2 clock mode =mode 3,4(CIS)(RF/D3=1)
  Dummy pixel number set up odd. (Ex. 1,3····)

Please set RE register to the original(previous) Dummy pixel number after offset calibration mode 1 is finished.

Black shading detection

■Black shading detection mode setting

□3set data / 1set data

(1) 3set data mode

•In case of detecting each black offset for each channel of 3 channel sensor, or for each color of 1 channel color sensor, this mode should be used. In the black offset cancel mode, internal 3set offset register pairs are available. In the pixel to pixel mode, external 3set memory bank are available.

(2) 1set data mode

•In case of detecting common black offset for every channel of 3 channel sensor, or for every color of 1 channel color sensor, this mode should be used. In the black offset cancel mode, internal 1set offset register pair (Register R04 and R05) is available. In the pixel to pixel mode, external memory bank BA[2..0]=011B is available.

•In case of the 1 channel color sensor (monochrome mode) or 1 channel monochrome sensor, this mode should be used.

□Black offset cancel mode / Pixel to pixel mode

(1) Black offset cancel mode

•The two black shading data whose location is set by black reference register are detected by the black detection 8bit ADC, and these data are stored to internal register pair as even/odd black offset data.

•It is possible to choose whether 3set data mode or 1set data mode.

In 1set data mode, black shading detection is done by scanning the same line 2 times. In 3set data mode, black shading detection is done by scanning the same line 2 times for each channel or color (total 6 times).

In case of 1set data mode,

The first scanning, black shading data of the pixel which is located at (black reference pixel position)×8th is detected and stored as even black offset.

The second scanning, black shading data of the pixel which is located at (black reference pixel position)×8+1th is detected and stored as odd black offset.

In case of 3set data mode,

The first to third scanning, black shading data of the pixel for each channel or color which are located (black reference pixel position)×8th are detected and stored as even black offset.

The 4th to 6th scanning, black shading data of the pixel for each channel or color which are located (black reference pixel position)×8+1th are detected and stored as odd black offset.

•The completion of the execution can be confirmed by BUSY flag (R0 / D7) . But we recommend waiting for the specified time to prevent the noise injection because of the AK8408 is accessed by the microcomputer all the time during the operation.

(2) Pixel to pixel mode

•Detects the black shading data by the black detection 8bit ADC, and all of shading data are stored to external SRAM.

•It is possible to choose whether 3set data mode or 1set data mode.

In 1set data mode, black shading detection is done by scanning the same line 2 times. In 3set data mode, black shading detection is done by scanning the same line 2 times for each channel or color (total 6 times).

At the first scanning, shading data of the pixels which are located 1,17,...,16n+1th are detected.

At the m-th scanning, shading data of the pixels which are located 16n+mth are detected, and stored to external SRAM.

In 3set data mode, repeat this process 3times for each channel or color, and detected data are stored to each memory bank.

•The completion of the execution can be confirmed by BUSY flag (R0 / D7) . But we recommend waiting for the specified time to prevent the noise injection because of the AK8408 is accessed by the microcomputer all the time during the operation.

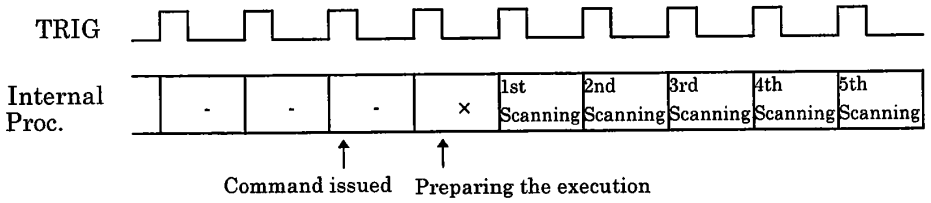
■Procedure for each sensor and mode

□3ch color sensor (color mode)

(1) Select the processing channel by the channel enable register. Only 1 channel must be enabled among 3 channels.

(2) In the pixel to pixel mode, after 17 lines scanning, black shading detection mode is

(2) In the pixel to pixel mode, after 17 lines scanning, black shading detection mode is automatically finished. In the fixed black offset cancel mode, after 3lines or 7lines scanning, black shading detection mode is automatically finished. Shading data is stored to external SRAM bank or internal register correspond to processing channel.



(3) When 1set mode is selected, black shading detect mode is completed at this point.

(4) When 3set mode is selected, repeat this process 3 times for CN0,CN1 and CN2.

(5) The completion of execution needs 17 lines time, but because that the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be verified by BUSY flag (R0 / D7) . But we recommend waiting for 18 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.
(In case of the fixed black offset cancel mode, the completion of execution needs 3 lines time. So, recommended wait time is 4 lines time.)
When 3set mode is selected, 18×3 =54 (pixel to pixel mode) lines time or 4×3=12 (fixed black offset cancel mode) lines time is necessary.

(6) When you change the PGA gain, please get the correction value again.

□3ch color sensor (monochrome mode)

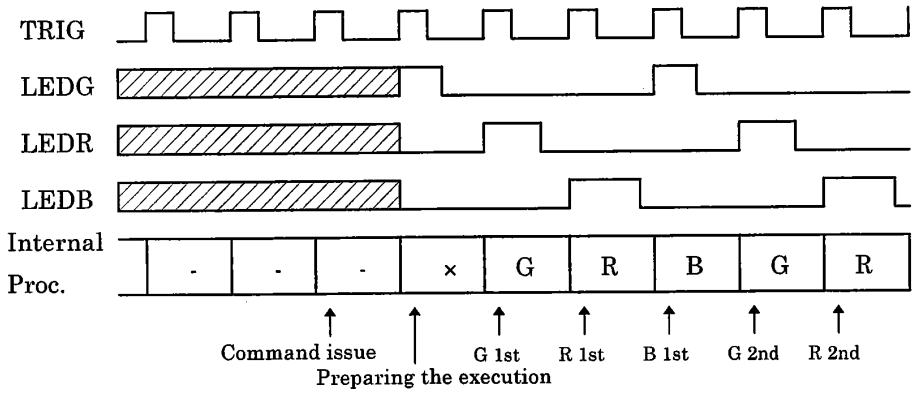
In case that shading data has been detected as a color sensor and the sampling rate may be the same as the color mode, the same shading correction data can be used.
Or, it is possible to change the main clock to 10MHz(max.), and treat as a monochrome sensor. As for details, please refer to the section of 1ch color sensor (monochrome mode).

□1ch color sensor (color mode)

In case of taking each shading data correspond to each color (ex. in case that black reference sheet is available), please set to 3set data mode.

(1) Black shading detection is achieved according to the pre-set processing / sampling order.

(ex. Sampling, Processing order setting is G→R→B)



(2) In the pixel to pixel mode, after 16×3+1 lines scanning (3set mode) or 16+1 lines scanning (1set mode), black shading detection mode is automatically finished. In the black offset cancel mode, after 6+1lines (3set mode) or 2+1lines (1set mode) scanning, black shading detection mode is automatically finished.

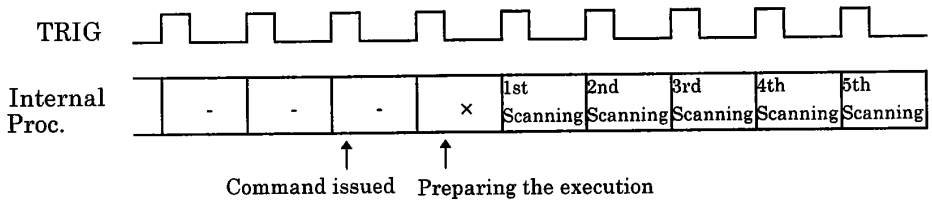
(3) The completion of the execution needs 16×3 + 1 or 16+1 lines time, but because the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be confirmed by BUSY flag (R0 / D7). But we recommend waiting for 50 lines time or 18 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.
(In case of the fixed offset cancel mode, the completion of execution needs 7 or 3 lines time. So, recommended wait is 8 or 4 lines time.)

(4) When you change the PGA gain, please get the correction value gain.

□1ch color sensor (monochrome mode)

(1) The processing channel is automatically set to CN0.

(2) In the pixel to pixel mode, after 16+1 lines scanning, black shading detection mode is automatically finished. In the fixed offset cancel mode, after 2+1lines scanning, black shading detection mode is automatically finished.



(3) In case that black shading correction mode is the fixed offset cancel mode, offset data are stored to R4 and R5 register.

(4) The completion of execution needs 16+1 lines time, but because that the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be verified by BUSY flag (R0 / D7). But we recommend waiting for 18 lines time to prevent the noise injection because AK8408 is accessed by the microcomputer for all time during the operation.
(In case of the fixed offset cancel mode, the completion of execution needs 3 lines time. So, recommended wait time is 4 lines.)

□Monochrome sensor

Same as 1ch color sensor (monochrome mode).

□Offset cancel for internal offset after black shading correction circuit

Because the black correction circuit is not able to cancel the internal offset after black correction circuit, there is some offset remained in video ADC output. It is possible to cancel this offset by setting the black offset adjustment register.

(1) Executes black shading correction for the black reference signal (ex; by using pre-detected black shading detected data), and monitors the video ADC output.

(2) Sets the black offset adjustment register for the video ADC output to become close to 0. Black offset adjustment register value is -128 to 127, and it is possible to increase or decrease black correction voltage for every pixel uniformly.

(3) This function is always available regardless black offset cancel / pixel to pixel mode, or 1set data / 3set data mode.

□Averaging circuit

In the black shading detect mode, it is possible to execute the detection cycle (N+1) times, and to average (N+1) set of shading data automatically. It is possible to reduce the noise of shading data.

(1) Averaging number is set to R24 register. In case that averaging number is N, shading detection cycle is executed (N+1) times, and averaged shading data is stored to the external SRAM automatically. In case that averaging number is 0, averaging function is disabled.

(2) It is possible to reduce the noise error by averaging. Averaging operation precision is about 2LSB (this value may be changed by data pattern).

Gain control

■3ch sensor gain control

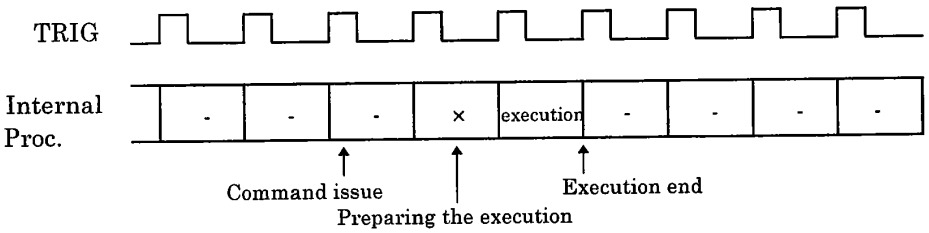
In case of 3ch color sensor, to adjust the signal level of the each channel, it is necessary to adjust PGA gain. For the measurement of signal level, AK8408 has a 8bit counter, a 8bit equal comparator, and a 8bit register for a threshold value, which are used for monitoring 10bit ADC output data. Comparing the threshold value and 10bit ADC output data, and if 10bit ADC output data is greater than the threshold value, the counter is incremented. Gain adjustment can be done by updating the gain data register till contents of the counter for each channel is in almost the same range.
This adjustment is done by each channel.

(1) In this mode, automatically peak hold value is set to FFh, and black / white reference voltage register is set to 00h, as that result 10bit ADC becomes full scale.

(2) Select a processing channel by the channel enable register. Only 1ch must be enabled.

(3) Analog input signal is black shading corrected one. White shading correction is automatically disabled.

(4) The number of pixels whose 10bit ADC output are greater than a preset threshold is detected and accumulated by a equal comparator and a counter. After 2 lines scanning, PGA gain adjust mode is automatically finished.
The completion of execution needs additional 1 line time, but because that the command issue and execution are asynchronous, 1 more line wait is necessary.



(5) Check the counter, and adjust PGA gain according to this value. Repeat these sequence until the counter value becomes an appropriate value.

(6) Repeat the same sequence to each 3 channel.

(7) When you change the PGA gain, please execute the offset calibration mode and the black shading detection mode again.

(Note) In case that (1) 3ch color sensor is used in monochrome mode,(2) 1ch color sensor is used, (3) monochrome sensor is used, PGA gain register corresponded to the used channel should be set for the amplified analog signal to be within the AK8408 input range.

■1ch sensor gain control

In case of 1ch color sensor,

- •Each color signal level should be almost the same.
- •Sensor signal level should be adjusted to be a specified level which are recommended by the sensor suppliers.

To meet these demand, LED on-time and / or PGA gain value must be set. For the measurement of signal level, AK8408 has a 8bit counter, a 8bit equal comparator and a 8bit register for a threshold value, which are used for monitoring 10bit ADC output data. Comparing the threshold value and 10bit ADC output data, and if 10bit ADC output data is greater than threshold value, the counter is incremented. Gain adjustment can be done by updating the LED on-time register or PGA gain till contents of the counter for each channel is in almost the same range.

(1) This mode consists of
- •LED pre-lighting cycle,
- •Detecting cycle,

and execution time is 2 lines time.
(Because command issue and starting this mode are asynchronous, additional 1 line time is necessary. Total execution time is 3 lines time.)

(2) In this mode, peak hold value is set to FFh, black / white reference voltage register is set to 00h automatically, as that result 10bit ADC becomes full scale.

(3) Select a processing channel by the channel enable register. Only 1 color must be enabled.

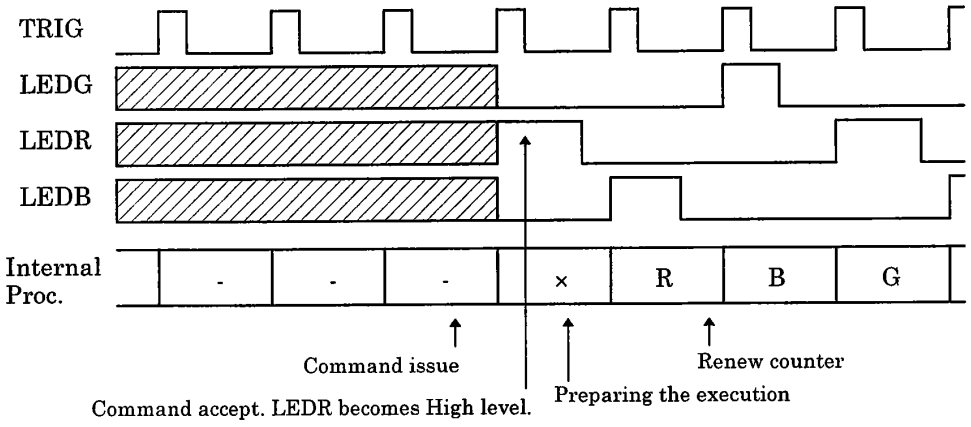
(4) Set an appropriate value to LED on-time register and PGA gain register, and execute this mode. This mode starts synchronized with the next TRIG signal.

(5) Analog input signal is black shading corrected one. White shading detection is automatically disabled.

(6) In the first cycle, the LED control pin which is enabled by the channel enable register becomes High level during the time which is defined by a LED on-time register. Other color LED control pins become Low level.

(7) In the second cycle, the number of the pixels whose 10bit ADC output are greater than a pre-set threshold is detected and accumulated by a equal comparator and a counter. After 1 line scanning, this mode is automatically finished.

(ex. Sampling order setting is G→R→B , adjust color is Red.)



(8) Check the counter, and adjust LED on-time according to this value. Repeat these sequence until the counter value becomes an appropriate value.

(9) Repeat the same sequence to each 3 colors.

(Note1) All of PGA gain registers should be set for the amplified analog signal to be within the AK8408 input range when gain control is done by LED on-time control.

(Note2) All of LED control register should be set for the amplified analog signal to be within the AK8408 input range when gain control is done by PGA gain control.

(Note3) In case that the 1ch color sensor is used as monochrome mode, the LED on-time register contents should be 1/3.

Peak detect and ABC / AGC

■Peak detection before the white shading detection

Before the white shading detection, the peak signal level is detected to be matched with ADC full scale. This mode is executed after finishing the black shading detection mode, and PGA gain adjustment or LED on-time control, and as a result signal level of each 3 colors has been adjusted to almost the same level. This mode consists of peak detection cycle and peak hold cycle.

(1) In this mode, peak hold value is set to FFh, and black / white reference voltage register is set to 00h automatically, as a result 10bit ADC becomes full scale.

(2) Peak detect cycle

•The white reference signal is scanned by 10bit video ADC, and detects the maximum signal level (PPK). Internally, analog black correction to the white reference signal is achieved as shown below.

(Pixel to pixel mode)

(black corrected signal)i = (input white reference signal)i
-{A(black shading data)i±A(offset adjust data)}

(Black offset cancel mode)

(black corrected signal)2i = (input white reference signal)2i
- {A(even pixel offset data)±A(offset adjust data)}
(black corrected signal)2i+1 = (input white reference signal)2i+1
- {A(odd pixel offset data)±A(offset adjust data)}

Besides, A(D) is an analog value which is DA-converted voltage of D.

And, signal level is amplified by PGA circuit.

(3) Peak fix cycle

•The peak value is fixed by 8bit peak detect circuit with re-scanning the same white reference signal after the initial value around PPK being set to the peak detect counter internally.

Detection width is the same as the available full length of a sensor. A limitter function for ABC is automatically inhibited. Following speed is 1LSB per a pixel.

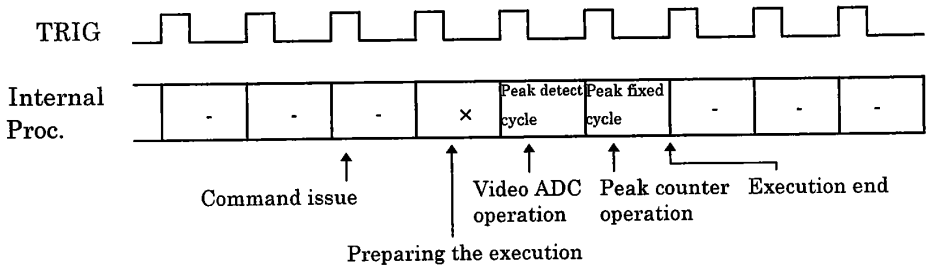
(4) Finishing these 2 cycles, the peak detect counter value is automatically loaded into the peak hold register.

(5) The completion of the execution can be confirmed by BUSY flag (R0 / D7). But we recommend waiting for the specified time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

■Procedure for each sensor and mode

□3ch color sensor (color mode)

(1) The peak value of pseudo 1ch signal that consists of 3ch signal after multiplexing is detected. Each signal levels of 3ch should be adjusted to almost the same level by PGA gain control.



(2) The completion of execution needs 3 lines time, but because that the command issue and execution are asynchronous, additional 1 line wait time is necessary. The completion of execution can be verified by BUSY flag (R0 / D7) . But we recommend waiting for 4 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

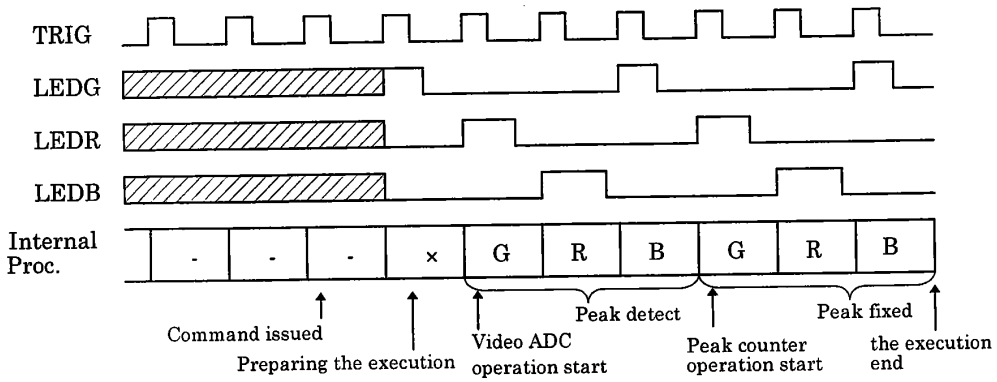
□3ch color sensor (monochrome mode)

The peak value of the input signal that selected by the channel enable register is detected.

Or, it is possible to change the main clock to max. 10MHz, and treat as a monochrome sensor. As for details, please refer to the section of 1ch color sensor (monochrome mode).

□1ch color sensor (color mode)

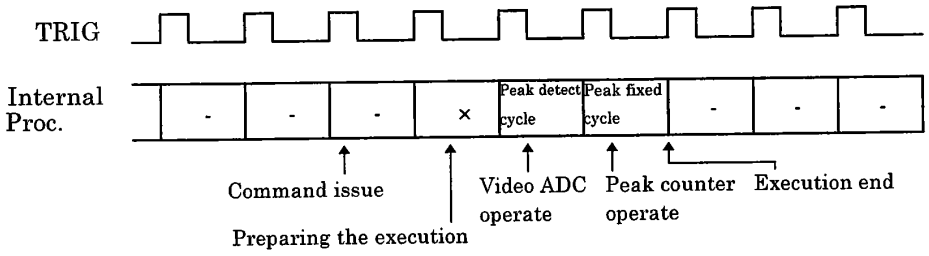
(1) The peak value of pseudo 1ch signal that consists of 3 color signal for GRB is detected. Each signal levels of 3 colors should be adjusted to almost the same level by LED on-time control or PGA gain adjustment.



(2) The completion of the execution needs 6+1 lines time, and also because that the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be confirmed by BUSY flag (R0 / D7). But we recommended waiting for 8 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

□1ch color sensor (monochrome mode)

(1) The peak value after being adjusted the LED on-time is detected.



(2) The completion of the execution needs 2 lines time, but because that the command issue and execution are asynchronous, 1 more line wait is necessary. The completion of the execution can be confirmed by BUSY flag (R0 / D7).

But we recommend waiting for 3 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

□Monochrome sensor

Same as 1ch color sensor (monochrome mode).

■ABC,AGC function

The purpose of ABC function is to read clearly regardless groundwork density by following the white reference voltage of the video ADC to the change of groundwork density line by line.

ABC function supports two mode, which are called "ABC mode (for the document with characters) " and "AGC mode (for the document with photograph) ".

(1) Enable or disable of ABC / AGC mode is selected by register R1 / D3.

(2) ABC / AGC following speed is selected by register R1 / D2-0.

D2	D1	D0	Mode / Following speed
0	0	0	ABC mode / 1/4LSB
0	0	1	ABC mode / 1/2LSB
0	1	0	ABC mode / 1LSB
0	1	1	ABC mode / 2LSB
1	*	*	AGC mode

(3) The peak detection counter is reset to 00h at the head of line. And detects the peak value (PEAK) among the selected pixels by R2 and R3 registers.

(4) The next line peak hold value (PHDk+1) is decided by the following formula.

ABC mode

PEAK ≥ PHDk → PHDk+1 = PEAK

PEAK < PHDk → PHDk+1 = PHDk - (following speed)

AGC mode

PEAK ≥ PHDk → PHDk+1 = PEAK

PEAK < PHDk → PHDk+1 = PHDk

Disabled channel or disabled color which is set by channel enable register is not effect to peak value.

(5) ABC / AGC peak following range is selected by R1E and R1F registers.

R1E : the limit value of black side.

R1F : the limit value of white side.

The peak hold value (PHDk) is changed within the range of the following formula.

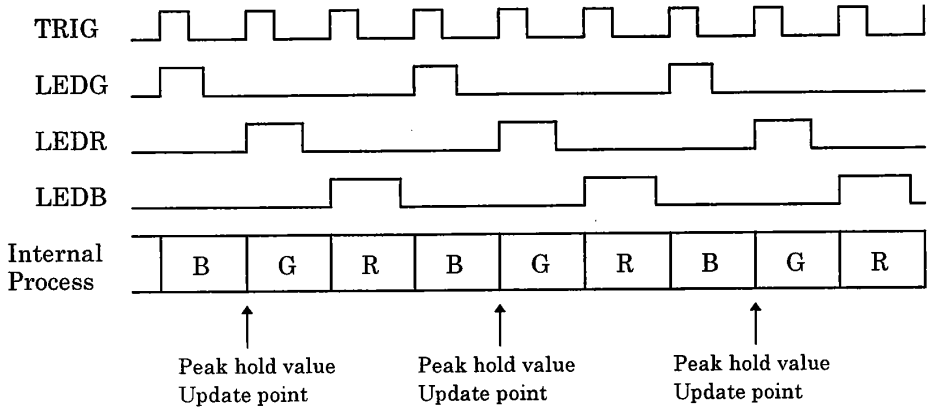
(R1E) ≤ PHDk ≤ (R1F)

Please take case that the initial peak hold value at the top of the page should be satisfied this formula also.

(6) In case of using 3ch color sensor (color or monochrome mode) , 1ch color sensor (monochrome mode) or monochrome sensor, peak hold value is up-dated by every line.

(7) In case of using 1ch color sensor (color mode), three line data are treated as a pseudo 1line data, and peak hold value is updated by every 3 lines.

(ex. 1ch color sensor, Sampling and processing order setting is G→R→B)



White shading detection

■White shading detection

The purpose of white shading correction is to remove the deviation of the light emission and the sensor sensitivity among pixels. Correction value is detected before the scanning.

(1) In this mode, black reference of the 8bit ADC for white shading detection is automatically set to 40% of Vpeak (typ.), and full scale of the ADC is from 0.4Vpeak to Vpeak. The Vpeak is the voltage, which correspond to the peak hold register value, and usually this value is detected in peak detect mode.

(2) The input signal to the white shading detection circuit is black corrected by the black shading data and gain amplified by PGA.

(3) Scanning white reference signal, the output of 9bit ADC for white shading detection is stored to the external SRAM.

(4) The white shading detection is done with the same scanning line 16 times.
The first scanning, the position of 1,17,...,16n+1 pixel's shading data are detected.
The m-th scanning, the position of 16n+m pixel's shading data are detected and stored into the external memory bank.

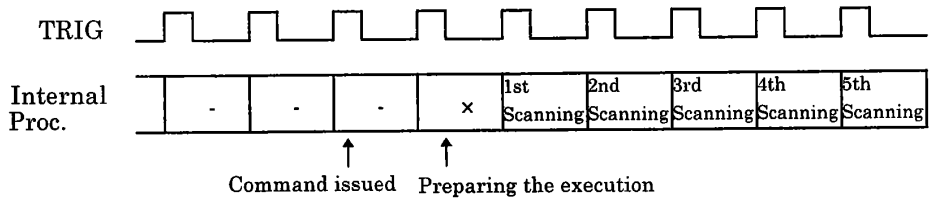
(5) The completion of the execution can be confirmed by BUSY flag (R0 / D7). But we recommend waiting for the specified time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

■Procedure for each sensor and mode

□3ch color sensor (color mode)

Detect the white shading data by each channel.

(1) Select the processing channel by channel enable register. Only 1 channel must be enabled.



(2) After scanning 16+1 lines, white shading detection mode is automatically finished.

(3) Repeat this process 3 times for CN0,CN1 and CN2.

(4) The completion of the execution for each channel needs 17 lines time, but because the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be confirmed by BUSY flag (R0 / D7). But we recommend waiting for 18 lines time to prevent the noise injection because of the AK8408 is accessed by the microcomputer all the time during the operation.

□3ch color sensor (monochrome mode)

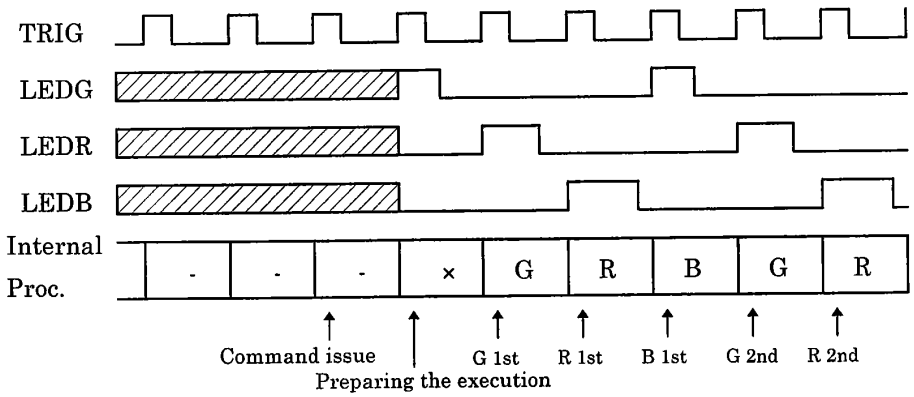
In case that shading data has been detected as a color sensor and the sampling rate may be the same as color mode, the same shading correction data may be used.

Or, it is possible to change the main clock to max. 10MHz, and treat as monochrome sensor. As for details, please refer to the section of 1ch color sensor (monochrome mode).

□1ch color sensor (color mode)

(1) White shading detection is achieved according to the pre-set processing / sampling order.

(ex. Sampling order setting is G→R→B)

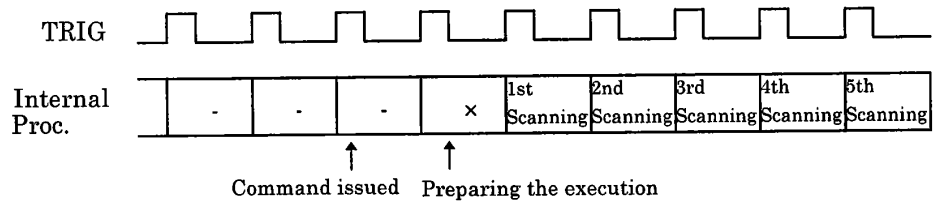


(2) After 16×3+1 lines scanning, white shading detection mode is automatically finished.

(3) The completion of the execution needs 16×3+1 lines wait, but because the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be confirmed by BUSY flag (R0 / D7) . But we recommend waiting for 50 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

□1ch color sensor (monochrome mode)

(1) The processing channel is automatically set to CN0.



(2) After 16+1 lines scanning, white shading detection is automatically finished. Shading data is stored to fixed external memory bank.

(3) The completion of the execution needs 16+1 lines time, but because the command issue and execution are asynchronous, additional 1 line time is necessary. The completion of execution can be confirmed by BUSY flag (R0 / D7). But we recommend waiting for 18 lines time to prevent the noise injection because the AK8408 is accessed by the microcomputer all the time during the operation.

□Monochrome sensor

Same as 1ch color sensor (monochrome mode).

□Averaging circuit

In the white shading detect mode, it is possible to execute the detection cycle (N+1) times, and to average (N+1) set of shading data automatically. It is possible to reduce the noise of shading data.

(1) Averaging number is set to R24 register. In case that averaging number is N, shading detection cycle is executed (N+1) times, and averaged shading data is stored to the external SRAM automatically. In case that averaging number is 0, averaging function is disabled.

(2) It is possible to reduce the noise error by averaging. Averaging operation precision is about 2LSB (this value may be changed by data pattern).

Channel enable register

To select a processing channel or channels, the AK8408 has 3bit control register.

3ch mode	CN2 enable	CN1 enable	CN0 enable
1ch mode	B enable	R enable	G enable

0: Disable
1: Enable

Following is recommended register setting for each sensor.

□3ch color sensor (color mode)

(1) Offset calibration mode 1 must be done channel by channel, and a processing channel should be selected by this register. In this mode, please take case that only 1 channel must be selected.

(2) In the offset calibration mode 2, all channels are enabled automatically regardless of register setting.

(3) Black shading detection must be done channel by channel, and a processing channel should be selected by this register. Black shading detection and storing the shading data to the external SRAM is done for only the enabled channel. In this mode, please take case that only 1 channel must be enabled.

(4) PGA gain control must be done channel by channel, and a processing channel should be selected by this register. By monitoring the counter, gain adjustment should be done. In this mode, please take case that only 1 channel must be enabled.

(5) In the peak detect mode, all channels are enabled automatically regardless of register setting.

(6) White shading detection must be done channel by channel, and a processing channel should be selected by this register. White shading detection and storing the shading data to the external SRAM is done for only the enabled channel. In

this mode, please take case that only 1 channel must be enabled.

(7) In the document scanning mode, all channels should be enabled.

□3ch color sensor (monochrome mode)

(1) In case that 3ch color sensor is used at monochrome mode, a specified 1ch is set to enable state. Maximum sampling rate is 3.3M samples / sec. The correction data which is detected in color mode can be used.

(2) It is possible to change the main clock to max. 10MHz, and treat as monochrome sensor. In this case, the correction data should be taken again. Please refer to the section 1ch color sensor (monochrome mode).

□1ch color sensor (color mode)

(1) Offset calibration mode 1 must be done by each color and the processing color should be selected by this register. Only 1 color must be enabled.

(2) In Offset calibration mode 2, all channels are enabled regardless of register setting.

(3) In the black shading detection mode, all channels are enabled regardless of register setting.

(4) The LED on-time control or PGA gain control must be done by each color corresponding to LEDG, LEDR and LEDB, and the processing color should be selected by this register. By monitoring the counter, gain adjustment or LED on-time control is done color by color. In the LED on-time control mode, only 1 color must be enabled.

(5) In the peak detect mode, all colors are enabled automatically regardless of register setting.

(6) In the white shading detection mode, all colors are enabled automatically regardless of register setting.

(7) In the document scanning mode, all colors should be enabled.

(Note) In case of using 1ch color sensor (monochrome mode) or monochrome sensor, this register doesn't have to be set.

Document scanning mode

(1) Black correction is done by the following formula.

(Pixel to pixel mode)

(black corrected signal)i = (input signal)i

-{A(black shading data)i±A(offset adjust data)}

(Black offset cancel mode)

(black corrected signal)2i = (input signal)2i

- {A(even pixel offset data)±A(offset adjust data)}

(black corrected signal)2i+1 = (input signal)2i+1

- {A(odd pixel offset data)±A(offset adjust data)}

Besides, A(D) is an analog value which is DA-converted voltage of D.

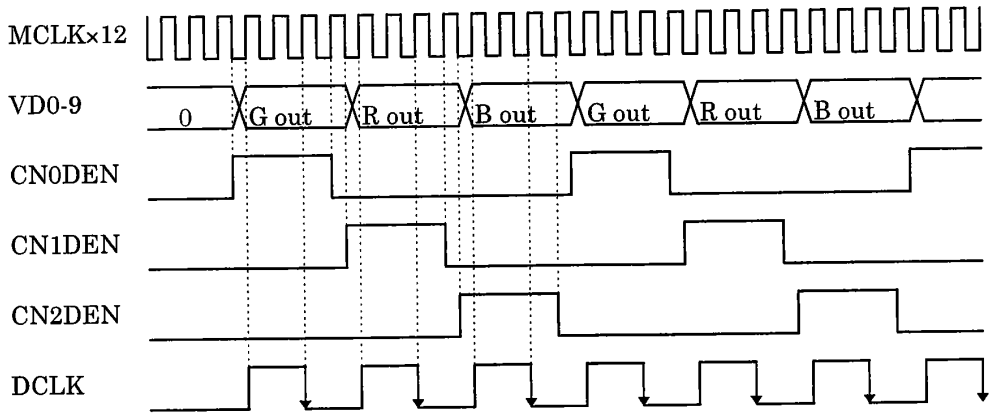
(2) White correction is done by the following formula.

(black and white corrected signal)i =

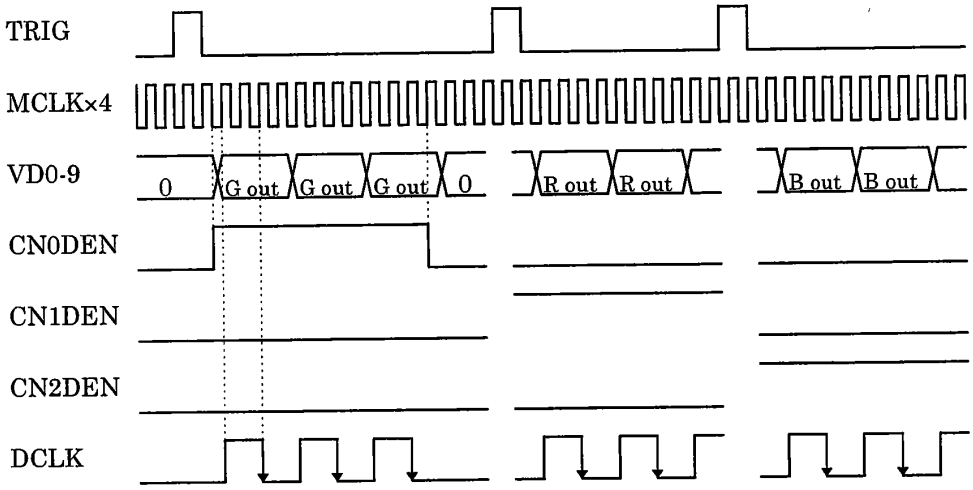
(black corrected signal)i × 2555 / (1022 + 3×(white shading data)i)

(3) CN0DEN, CN1DEN, CN2DEN and DCLK timing is shown below.

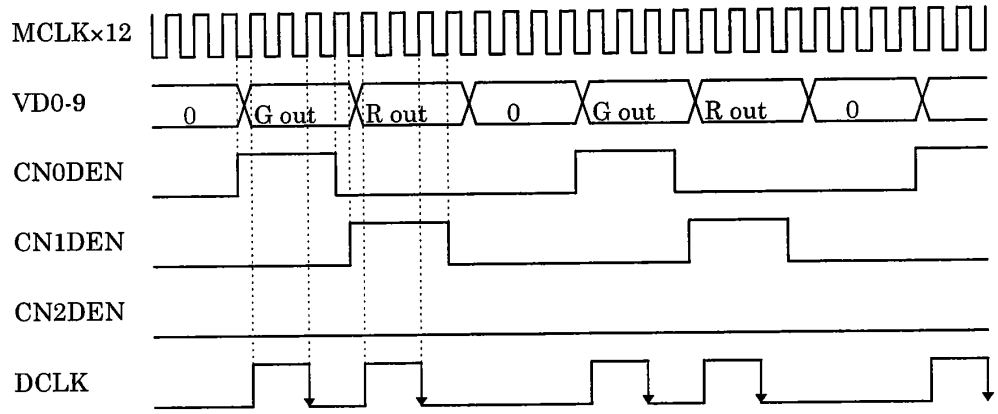
•3ch color sensor (color mode)



•1ch color sensor (color mode)

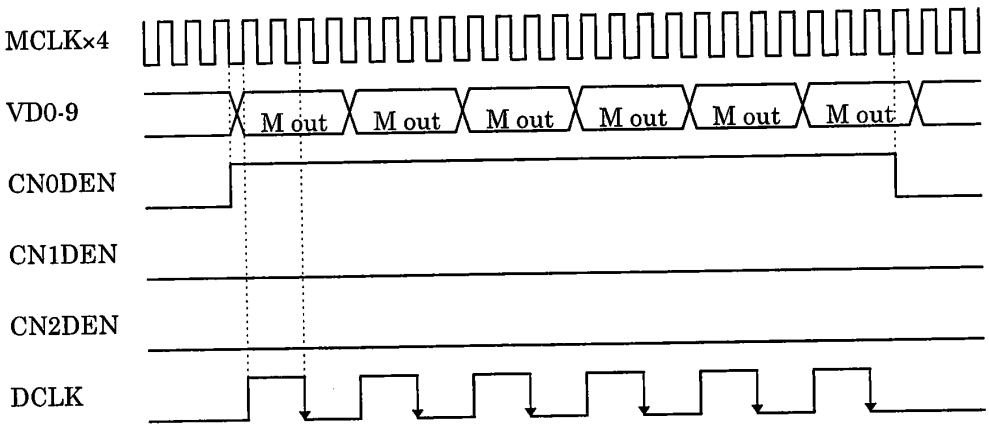


•3ch mode (in case that CN2 is disabled)



Because that CN2 is disabled, CN2DEN and DCLK correspond to CN2 are not outputting. VD0-9 become low level.

•1ch color sensor (monochrome mode) , monochrome sensor



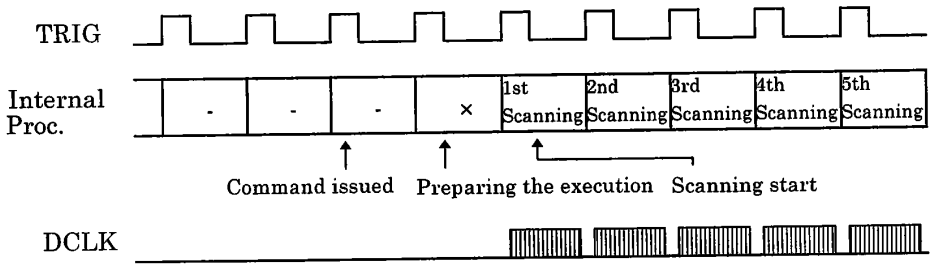
□3ch color sensor (color mode / monochrome mode)

(1) Input signals from all 3ch are sampled at the same time.

(2) The multiplexer circuit is automatically switched according to the pre-defined processing order.

(3) The 10bit video data outputs according to the pre-defined processing order.

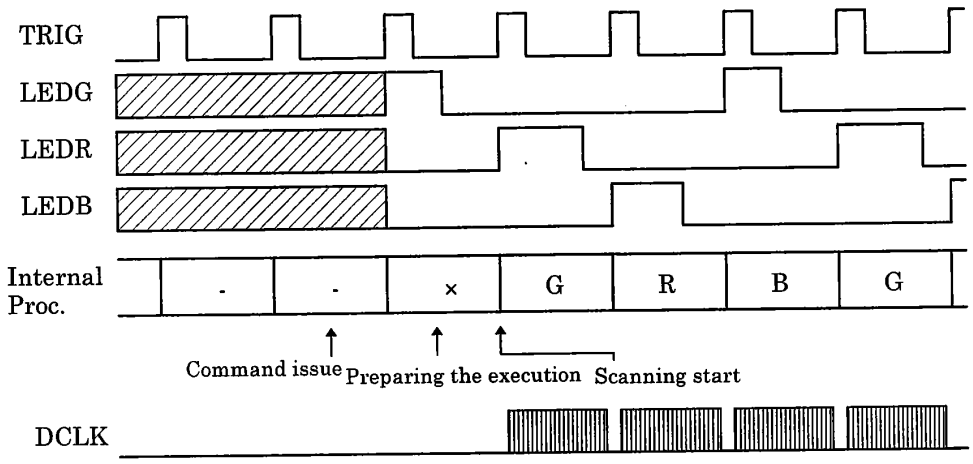
(4) It is possible to use monochrome mode by using specified 1ch among 3ch color sensor. In this case, maximum sampling rate is 3.3M samples / sec. The correction data which is detected in color mode is used.
Or, it is possible to change the main clock to max. 10MHz, and treat as monochrome sensor. In this case, the correction data should be taken again. Please refer the section 1ch color sensor (monochrome mode).



□1ch color sensor (color mode)

(1) Scanning is started with 1 line delayed from command issue.

(ex. Sampling order setting is G→R→B)



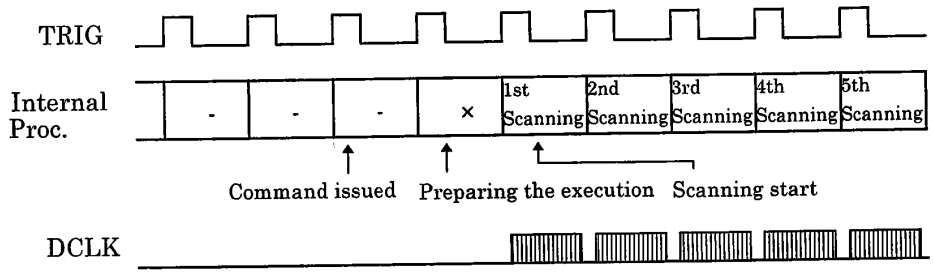
(2) Stop and re-start of processing are controlled by the VPE pin. At the re-starting, it is possible to select the start color by re-writing the sampling and processing order register.

(Ex) In case that the processing order is G→R→B, and image processing is stopped during the color B, it is possible to restart at color B by the re-writing the processing order register to B→G→R.

(3) As for the disabled color by the channel enable register, 10bit video data and its sampling clock are not generated.

□1ch color sensor (monochrome mode)

(1) Scanning is started with 1 line delayed from command issue.



(2) Stop and re-start of processing are controlled by the VPE pin.

(3) Channel Enable register setting is invalid. Channel fixed CN0 pin.

LED on-time control

(1) For the purpose of CIS LED on-time control or CCD shutter function control, the AK8408 supports LEDG, LEDR and LEDB pins.

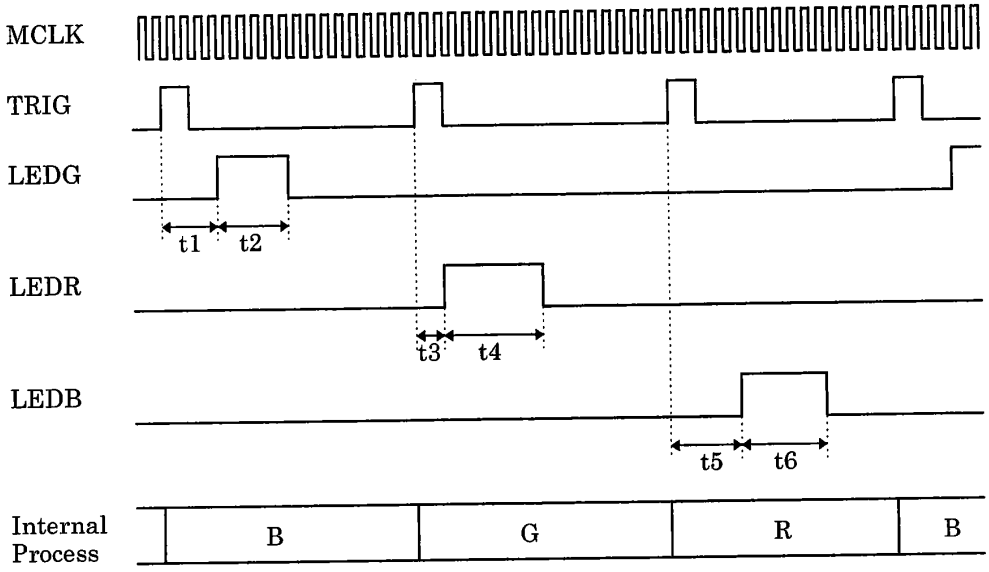
(2) It is possible to program the LEDG, LEDR and LEDB pins' high level period by following registers. (In the example below, register is for Green)

LEDGs : LED on start point.

LEDGw: LED on-time period

Each register is 8bit and unit is 32 pixels.

(ex. LED on timing 1ch color sensor (color mode))



t1: LEDGs×32 pixel

t2: LEDGw×32 pixel

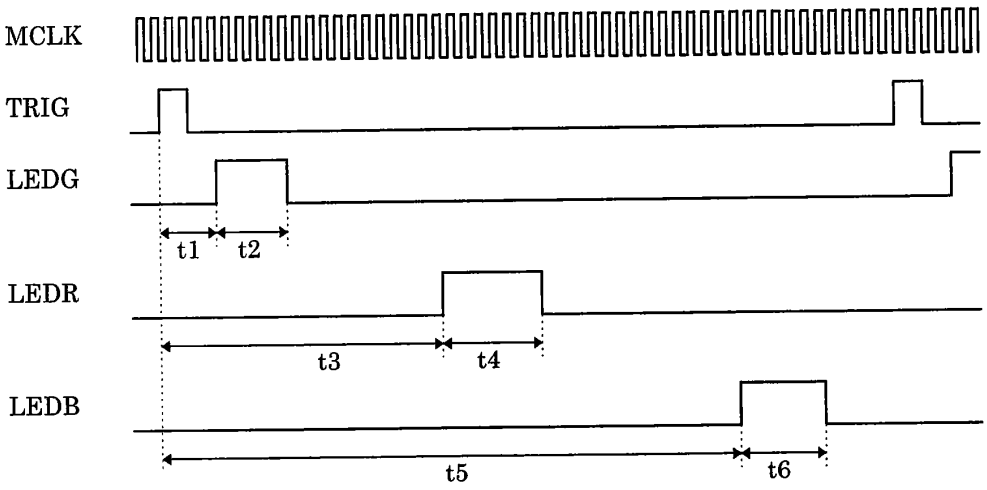
t3: LEDRs×32 pixel

t4: LEDRw×32 pixel

t5: LEDBs×32 pixel

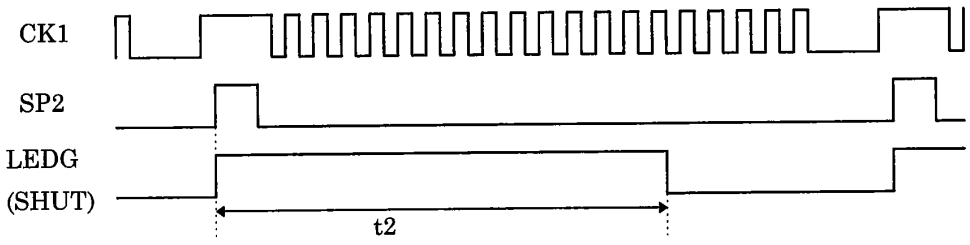
t6: LEDBw×32 pixel

(ex. LED on timing 1ch color sensor (monochrome mode))



t1: LEDGs×32 pixel
t2: LEDGw×32 pixel
t3: LEDRs×32 pixel
t4: LEDRw×32 pixel
t5: LEDBs×32 pixel
t6: LEDBw×32 pixel

(ex. CCD sensor with shutter function)

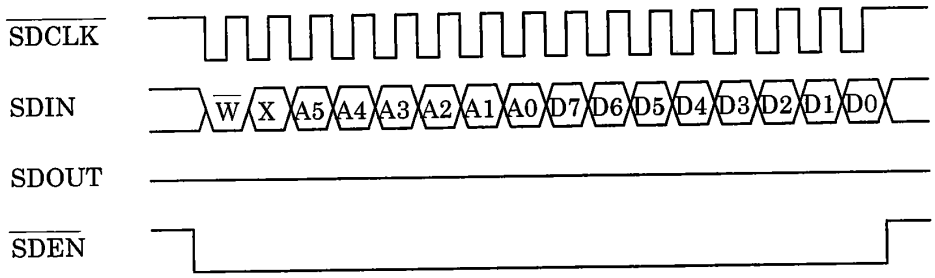


t1: LEDGs = 0
t2: LEDGw× 32pixel

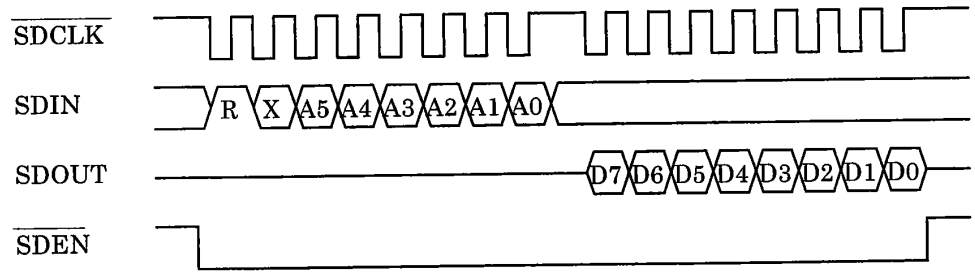
Serial interface

It is possible to access to control register and/or shading memory access window by 4 wired serial interface. Timing chart is as following diagram.

(1) Write to AK8408



(2) Read from AK8408

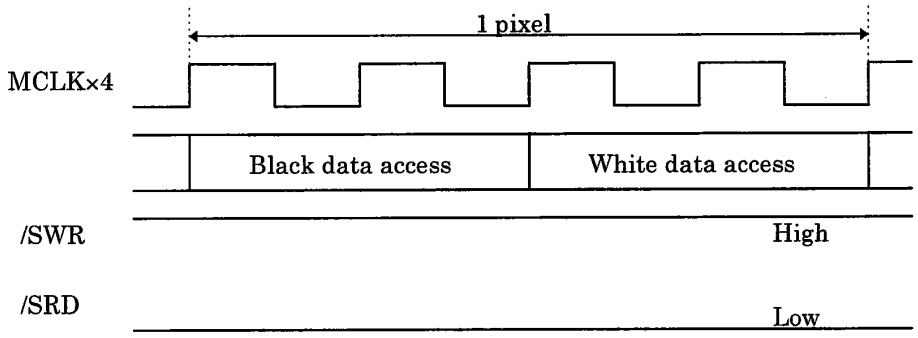


Shading memory interface

■Shading memory interface

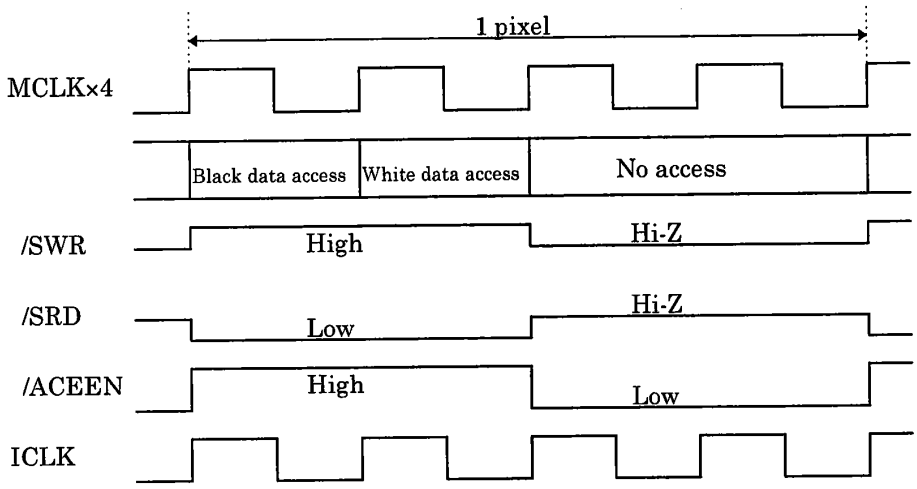
AK8408 supports two kind of shading memory access modes. In mode2, address buses, data buses and control signals are becomes Hi-Z while the AK8408 does not access to shading memory. So it is possible for external device to access to shading memory.
(following charts are in document scanning mode.)
When AK8408 is in the idle mode (R0/D7=0), it is possible for external device to access to shading memory at access mode 2.

•mode1



Mode 1 has long access period for black data or white data access, so it is suitable for high speed sampling or low speed memory.
Required access speed of shading memory is about
(Access speed) = 1 / (2F) -20 (nS): 1ch mode
=1 / (6F) -20 (nS): 3ch mode
Besides, F is sampling rate (MHz).

•mode2



In this mode, it is possible for external device to access to shading memory at /ACEEN signal low level period.

Required access speed of shading memory is about

(Access speed) = 1 / (4F) -10 (nS): 1ch mode

= 1/(12F) -10 (nS):3ch mode

Besides, F is sampling rate (MHz).

If sampling rate is high, this mode can not be used. We recommend that in case that sampling rate is over 4Mpixel / sec, mode1 should be used.

□SRAM connection

Because AK8408 white shading correction is done by 9bit resolution, 9bit width external shading memory is required. If white shading correction do 8bit, it is possible to use 8bit width memory.

(1) 9bit width SRAM is used
- •Set white shading correction precision to 9bit (R25 / D3 = 1).
- •Connect SD0-8 to SRAM data bus.

(2) 8bit width SRAM is used
- •Set white shading correction precision to 8bit (R25 / D3 = 0).
- •Connect SD1-8 to SRAM data bus.

  SD0 should be opened.

You can access to SRAM by two method. One is the access through window register of AK8408 and another one is direct access. In case of direct access, memory interface signals become Hi-Z when AK8408 is in idle mode and shading memory access mode is mode 2. Please note that address bus is output by block gray code.

□Address bus output

Shading memory address bus (13bit) is output by block gray code.

(MSB)

12	11	10	9	8	7	6	5	4	3	2	1	0
liner			6bit gray code						4bit gray code			

(LSB)

When the size of SRAM is selected, please take case of this addressing method.

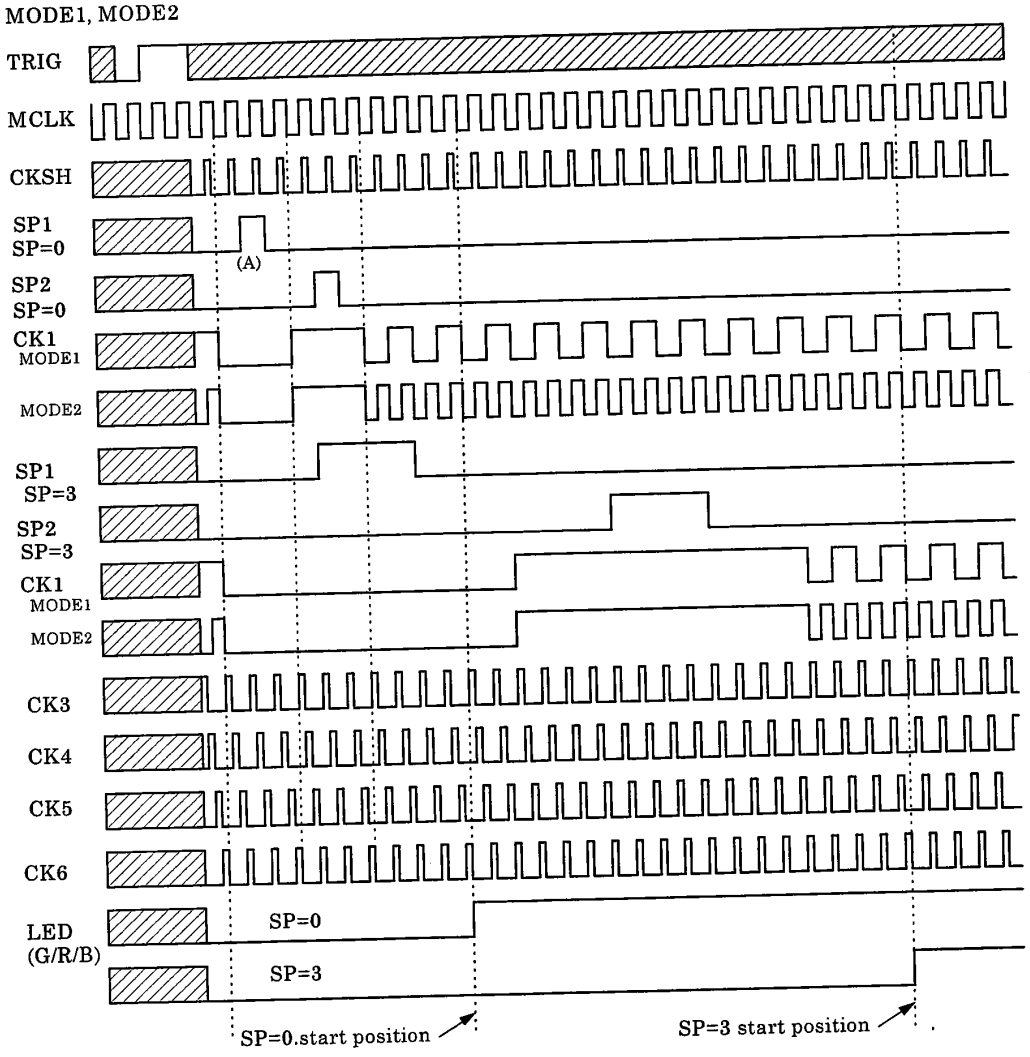
(ex) Black shading data 1 set data mode
White shading data R,G,B 3set data
Pixel number 2,592
4Kbyte×4bank = 16Kbyte = 128Kbits

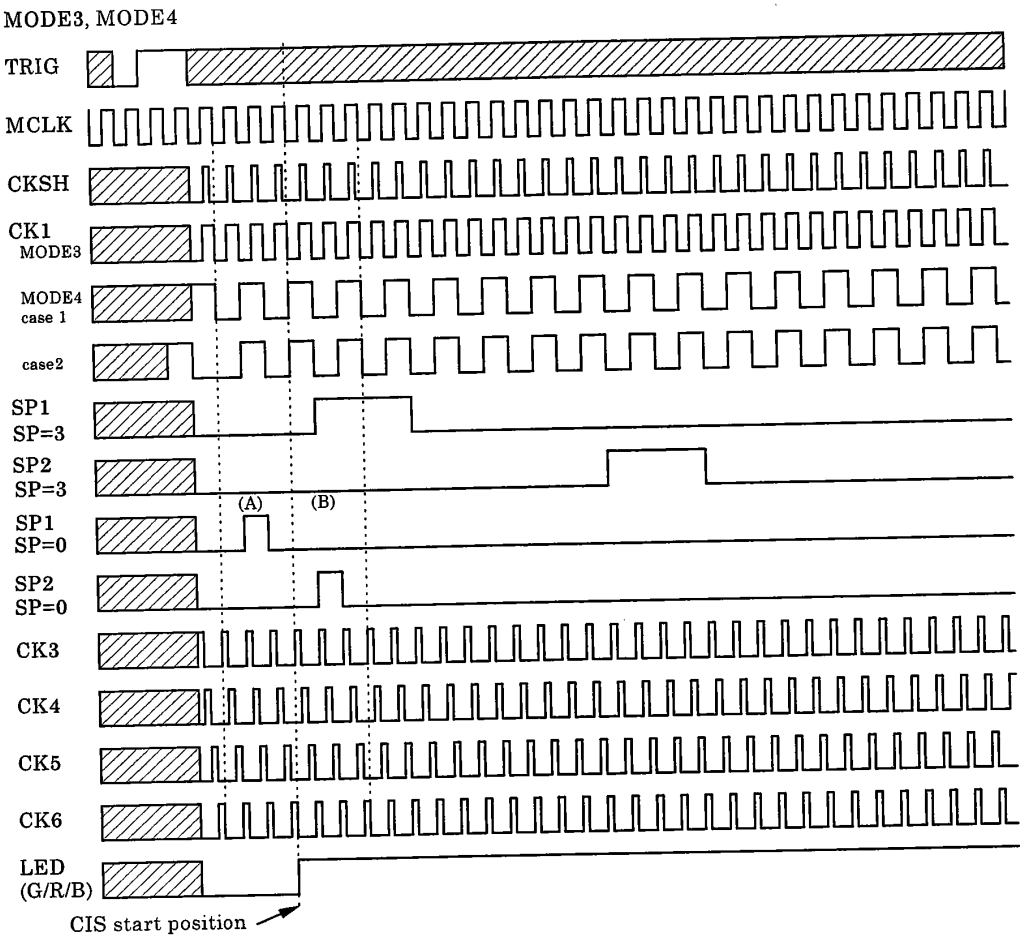
Please use SRAM whose size is bigger than 128Kbits.

Sensor clock generation

■Sensor clock generation circuit

(1) The AK8408 generates following clocks for the sensor.
(2) There are 4 kinds of CK1 output modes, which is selected by a register.
(3) The CK2 is an inverted output of the CK1.
(4) It is possible to delay CK1, CK2, SP1 and SP2 by MCLK/4 unit by a register.
(5) It is possible to invert the SP1, SP2, CK3-6 by a register.



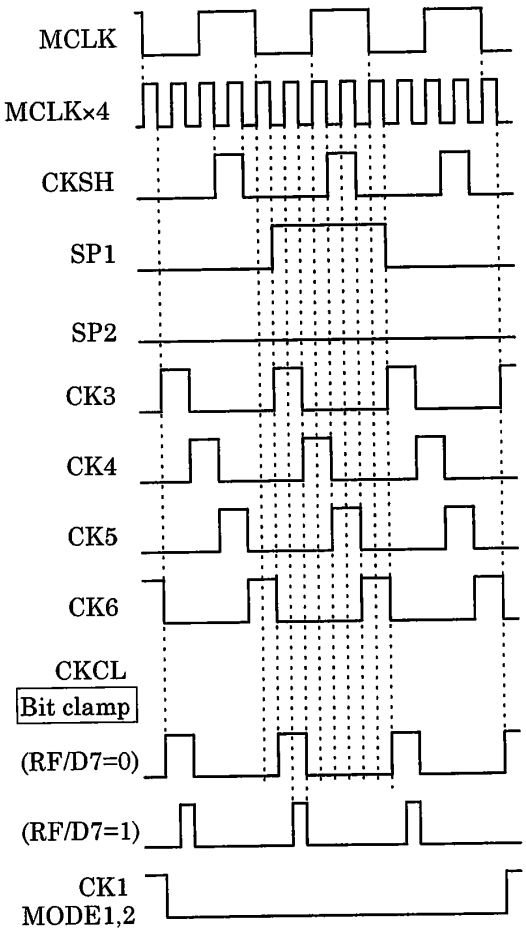


The above timing diagram shows the case of LED ON start timing position=0 (R19,R1B,R1D).

Details of timing is shown in the next page.

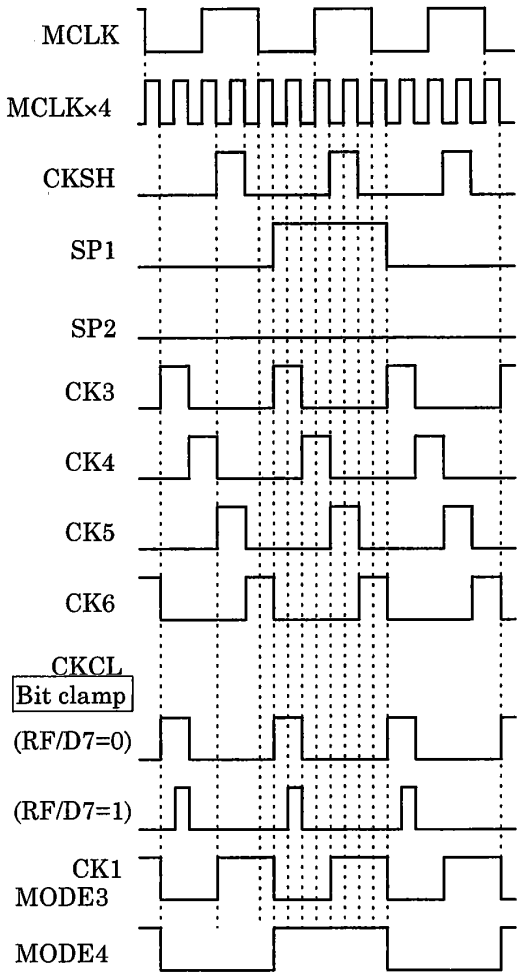
□Details timing diagram(A)

Mode1,2



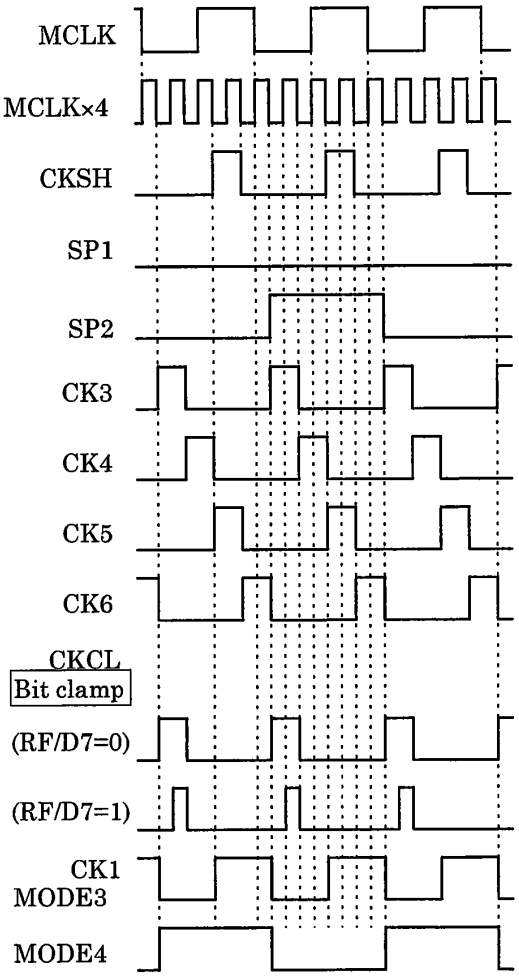
□Details timing diagram(A)

Mode3,4



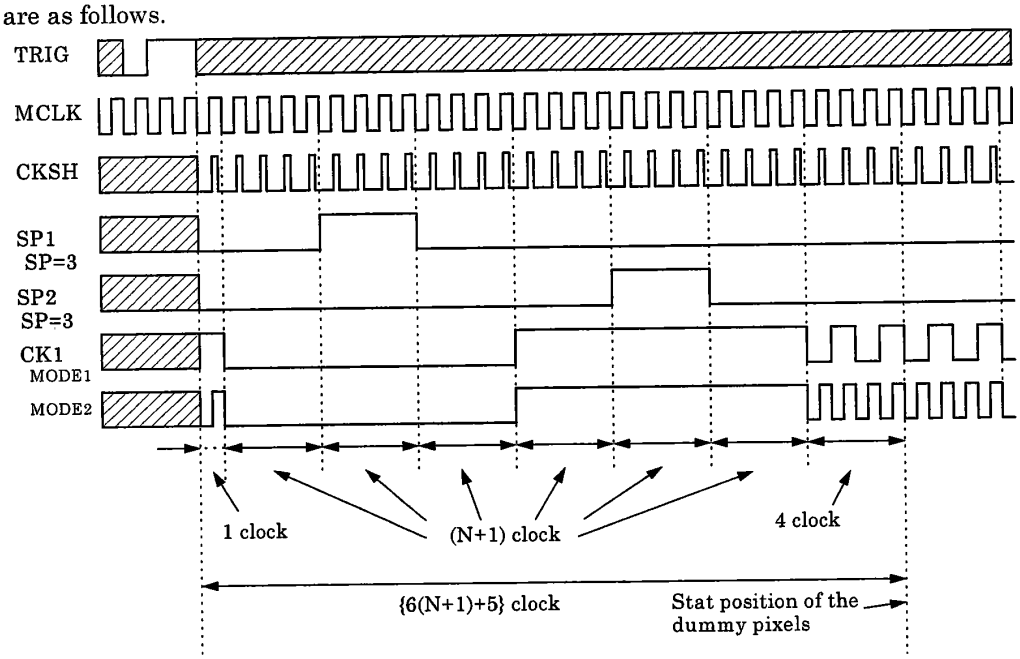
□Details timing diagram(B)

Mode3,4



□Relationship between SP pulse width and SP1, SP2, CK1(Mode1,2)

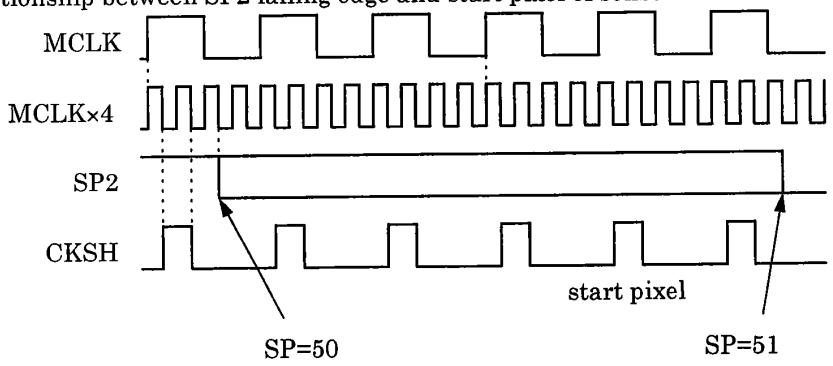
When SP width register(R26) = N, the timing of SP1/SP2/CK1 in mode1, mode2, are as follows.



Start position of the dummy pixels number in mode3 or mode4 doesn't change regardless of SP width, namely 5 clocks after the TRIG is detected. That one in mode1 or mode2 change depending on the SP width, namely {6×(N+1)+6} clocks after TRIG is detected .

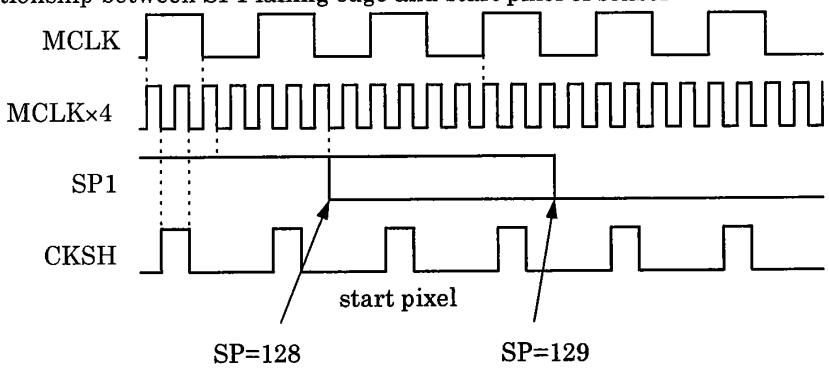
There is some limits in timing adjustment range as follows.

(1)Relationship between SP2 falling edge and start pixel of sensor



The above timing diagram is when dummy pixel number is 255 and, SP width is 50. Every increasing of 1 clock(MCLK) timing, SP2 falling edge is shifted 5 clocks after. The limitation of SP width is 50, because SP2 falling edge is after the starting pixel.

(2)Relationship between SP1 falling edge and start pixel of sensor



Because of the same reason with the case of SP1, the limitation of SP pulse width is 128.

Both SP1 and SP2 are applicable as the sensor start clock, please take care of following points.

•Case of SP1

Pulse width limitation is 128. But there is 1clock gap between LED control timing signal and SP1 falling edge.

•Case of SP2

Pulse width limitation is 50. The timing of SP1 falling edge can be adjusted not to make any gaps.

Registers

Addr.	R/W	init	D7	D6	D5	D4	D3	D2	D1	D0
00	R/W	00h	Oper. Enable	VPE	LED control		SME control	Processing mode setting		
01	W	01h	PLL stop	Black correct. mode 1	Black correct. Mode 2	Limitter enable	ABC/ AGC enable	ABC/ AGC select	ABC speed	
02	W	---	ABC start pixel position							
03	W	---	ABC end pixel position							
04	R/W	---	Even pixel offset register 0 (CN0 or Green)							
05	R/W	---	Odd pixel offset register 0 (CN0 or Green)							
06	R/W	---	Even pixel offset register 1 (CN1 or Red)							
07	R/W	---	Odd pixel offset register 1 (CN1 or Red)							
08	R/W	---	Even pixel offset register 2 (CN2 or Blue)							
09	R/W	---	Odd pixel offset register 2 (CN2 or Blue)							
0A	W	00h	White reference voltage DAC							
0B	W	00h	Black reference voltage DAC							
0C	W	*1	CIS CN sel	Black correction reference pixel position					Sensor pixel counts(MSB2bit)	
0D	W	---	Sensor pixel counts (LSB 8bit)							
0E	W	---	Pre-dummy pixel counts							
0F	W	00h	Clamp pulse width	Clamp mode	SP polarity	CK 3-6 polarity	CK 1,2 mode		SP,CK3-6 phase	
10	W	00h	Line clamp enable start position							
11	W	00h	Line clamp enable end position							
12	W	---	color/ mono select	1ch/3ch select	Processing channel order			Processing channel enable		
13	W	---	Gain adjustment threshold							
14	R	00h	Gain adjustment counter							
15	W	00h	PGA gain 0 (CN0)							
16	W	00h	PGA gain 1 (CN1)							
17	W	00h	PGA gain 2 (CN2)							

Addr.	R/W	init	D7	D6	D5	D4	D3	D2	D1	D0
18	W	00h	LED G period							
19	W	00h	LED G start position							
1A	W	00h	LED R period							
1B	W	00h	LED R start position							
1C	W	00h	LED B period							
1D	W	00h	LED B start position							
1E	W	00h	ABC limitter for black side							
1F	W	FFh	ABC / AGC limitter for white side							
20	R	---	Peak detect counter							
21	R/W	80h	Peak hold register							
22	R/W *3	*2			White ×1	Peak detect / hold circuit calibration value				
23	R/W	00h	Black shading data offset adjustment(CN0)							
24	W	00h	White shading detection averaging line count					Black shading detection averaging line count		
25	W	00h	Black correction range		ICLK enable	SM access method		WSD access width	Shading memory bank select	
26	W	00h	SP width							
27	R/W	00h	Black shading data offset adjustment(CN1)							
28	R/W	00h	Black shading data offset adjustment(CN2)							
29	R/W	00h	ADC offset adjustment							
2A	R/W	---	Shading memory access window							

(Note)

1. ☐ is initialized by /RESET.(Only D7 is initialized *1.Initial value set 0. Only D5 is initialized *2.Initial value set 0.)
2. ☐ is enabled by the first TRIG↑ after command issued.
3. D5 is enable write, D4-D0 is enable read/write for *3.
4. R21 register cannot be accessed during the execution of peak detection and the white shading detection modes. Setting value become effective ,after effective pixel of next section finish. This register set 80h,before black shading detect mode. This register set FFh, before peak detect mode and gain adjustment mode and LED on-time adjustment mode.(Peak hold register is set fix value on one line after mode setting. Each mode operation start from two line.
5. R21 register write inside limit value than R1E,R1F register setting value.
6. For confirmation of R/W of R21 register ,supply TRIG signal and 1 line at minimum

before reading back the data after writing it.

7.RA,RB register setting value keep after setting value. RA and RB registers become effective when operation enable is set.

8.R4-R9 register cannot be accessed during the black shading detect mode.

9.R22 register cannot be accessed during the black shading detect mode.

Register explanation

•R0 register

D7: Operation enable (read possible)

0: Disable (after reset)

1: Operation enable

When R0/D7=1, the operation which is selected by the operation mode register starts at the next TRIG. In case of black shading detection mode, white shading detection mode, peak detect mode, gain adjust mode and LED on-time control mode, this register is automatically reset after the execution is completed. In case of scanning mode, the operation continues till this register is reset.

This bit can read, and can be used for the purpose of checking that pre-processing like black shading detection etc. is completed or not.

D6: Video processing enable

0: Video processing disable (after reset)

1: Video processing enable

This register has the same function with VPE pin. When VPE pin is used, this register must be 0.

D5,D4: LED control

Controls LEDG, LEDR and LEDB pins.

D5	D4	Function
0	0	LED pins become low level regardless of R18-1D register.
0	1	LED pins become high level regardless of R18-1D register.
1	0	LED pins are automatically changes corresponding to R12, R18-1D register.
1	1	LED pin output in reverse D5,D4=10 case.

(After reset : 00)

D3: Shading memory access enable

0: Shading memory access disable (after reset)

1: Shading memory access enable

In case that this register is set to 1, it is possible to access the shading data through R2A register (shading memory access window). Shading memory address counter is reset by changing this register data 0 to 1, and automatically incremented by accessing R2A register one by one.

D2,D1,D0: Operation mode

Select the operation mode.

D2	D1	D0	Processing mode
0	0	0	Document scanning mode (after reset)
0	0	1	Black shading detect mode
0	1	0	White shading detect mode
0	1	1	Peak detect mode
1	0	0	Gain adjustment mode
1	0	1	LED on-time adjustment mode
1	1	0	Offset calibration mode 1
1	1	1	Offset calibration mode 2

In case of using 3ch sensor (R12/D6=1), please use gain adjustment mode.

In case of using 1ch sensor (R12/D6=0), please use LED on-time adjustment mode.

When R0/D7=1,Offset calibration mode start at first TRIG after mode setting and the other mode start at second TRIG after mode setting.

•R1 register

D7: PLL control

0: PLL on (after reset)

1: PLL off

D6: Black shading correction mode 1

Select the black shading correction mode.

0: pixel to pixel mode (after reset)

1: fixed offset cancel mode

D5: Black shading correction mode 2

Select the black shading correction method.

0: 3set register mode that is each black shading data for GRB or CN0-2 (after reset)

1: 1set register mode that is common black shading data for GRB or CN0-2

In case of using the common black shading data for GRB or CN0-2, shading data is stored to bank BA[2..0] = 011.

D4: ABC / AGC limitter enable

0: disable (after reset)

1: enable

D3: ABC / AGC enable

0: disable (after reset)

1: enable

When R0/D7=1,this operation start at first TRIG after read mode setting.

D2: ABC / AGC mode

0: ABC mode (after reset)

1: AGC mode

When R0/D7=1,this operation start at first TRIG after read mode setting.

D1,D0: ABC speed

Set the following speed in ABC mode.

D1	D0	Following speed
0	0	1/4 LSB
0	1	1/2 LSB (after reset)
1	0	1 LSB
1	1	2 LSB

When R0/D7=1,this operation start at first TRIG after read mode setting.

•R2 register: ABC start pixel position

Set the peak detect start pixel in ABC / AGC mode. The unit is 32 pixels.
Dummy pixel is not included.
PS = 32×(register value) (register value = 0~255)

•R3 register: ABC end pixel position

Set the peak detect end pixel in ABC / AGC mode. The unit is 32 pixels.
Dummy pixel is not included.
PE = 32×(register value + 1) (register value = 0~255)

•R4, R6, R8 register: Even pixel offset

In case of the fixed black offset cancel mode, a detected even pixel offset data is set. In case that the same fixed black offset data for GRB or CN0-2 is used, offset data is set to R4 register.

•R5, R7, R9 register: Odd pixel offset

In case of the fixed black offset cancel mode, a detected odd pixel offset data is set. In case that the same fixed black offset data for GRB or CN0-2 is used, offset data is set to R5 register.

•RA, RB register: Reference voltage DAC

Set the white reference voltage (VWHT) and the black reference voltage (VBLK) of 10bit video ADC. Resolution is (0.45 / 255) of (VCLP - VPEAK), and actual reference voltages and coefficient (α,β) are shown below.

(After reset : 00h)

VWHT=VCLP - α (VCLP-VPEAK)

VBLK=VCLP - β (VCLP-VPEAK)

Setting value	α	β
00h	1.0000	0.0000
01h	0.9982	0.0018
02h	0.9965	0.0035
03h	0.9947	0.0053
04h	0.9929	0.0071
:	:	:
:	:	:
FCh	0.5553	0.4447
FDh	0.5535	0.4465
Feh	0.5518	0.4482
FFh	0.5500	0.4500

•RC register

D7: Select input channel CIS sensor

Select input channel CIS sensor.

0:Fixed CN0

1:Input channel change each color.

D6-2: Fixed offset cancel reference pixel

In case of black offset cancel mode, set the reference pixel to take correction data. It is possible to set by 8 pixels unit.

D1,D0, RD register: Sensor pixel number

Set the sensor pixel number. The unit is 8 pixels. Dummy pixel is not included.

Sensor pixel count S = 8×(register value + 1)

•RE register: Dummy pixel number

Set the dummy pixel number. The unit is 1 pixel.

•RF register

D7: Clamp pulse

Set the clamp pulse width.

	RF / D7 = 0 (after reset)	RF / D7 = 1
RF/D6=0 (after reset) Bit clamp mode	1/4 MCLK	1/8 MCLK
RF/D6=1 Line clamp mode	CLPEN	CLPEN∩CKSH

D6: Clamp mode

Select the clamp mode.

0: Bit clamp (after reset)

1: Line clamp

D5: SP clock polarity

Select the sensor clock SP1 and SP2 polarity.

0: Active high (after reset)

1: Active low

D4: CK3-6 clock polarity

Select the sensor clock CK3-6 polarity.

0: Active high (after reset)

1: Active low

D3,D2: CK1, CK2 clock mode

Select the sensor clock CK1 and CK2 mode.

D3	D2	mode
0	0	mode1 (CCD) (after reset)
0	1	mode2 (CCD)
1	0	mode3 (CIS)
1	1	mode4 (CIS)

CK2 is inverted one of CK1.

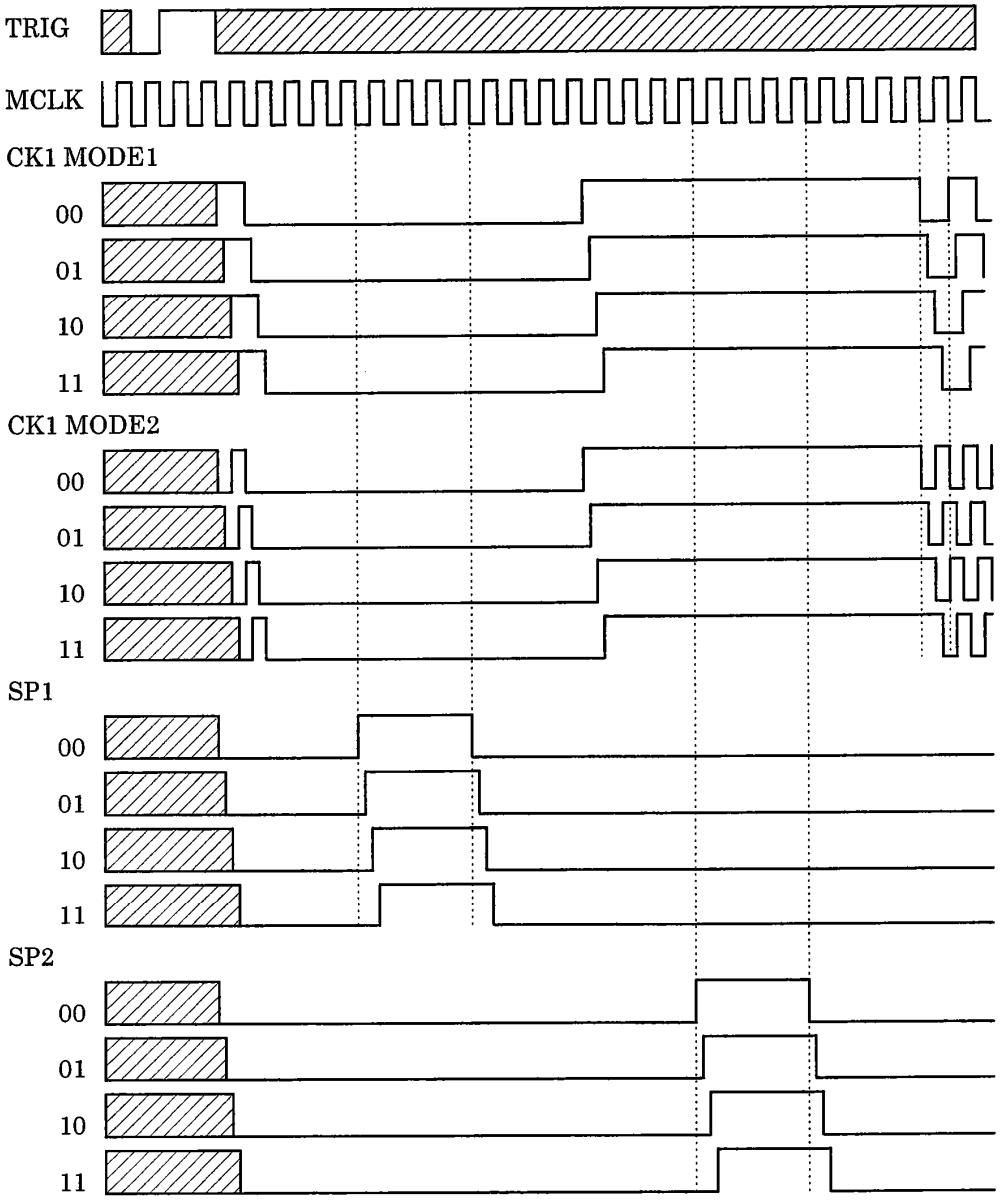
D1,D0: CK1, CK2, SP1, SP2 phase

Select the sensor clock SP1,SP2,CK1 and CK2 phase.

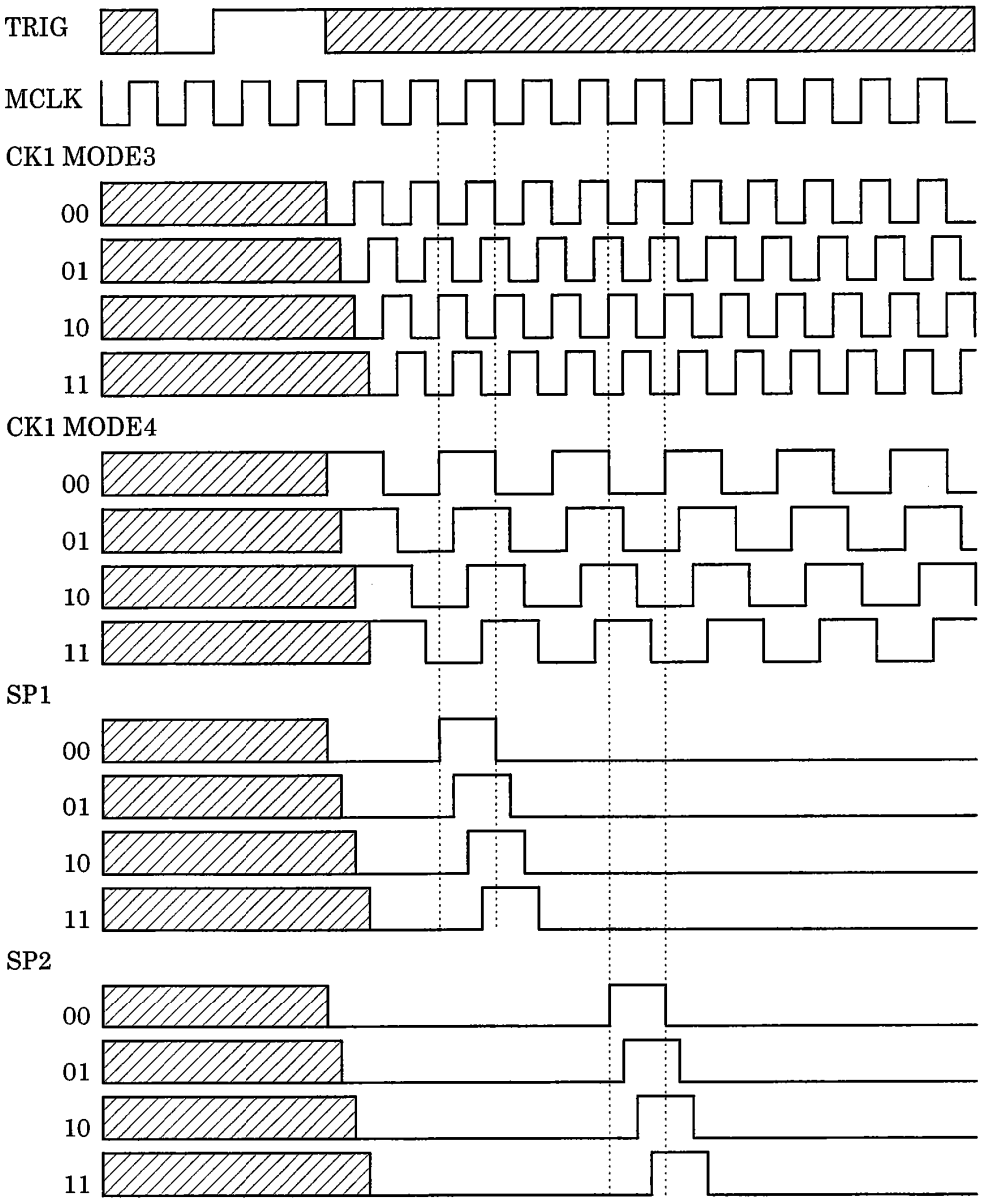
D1	D0	phase
0	0	Not delayed (after reset)
0	1	1×MCLK / 4 delayed
1	0	2×MCLK / 4 delayed
1	1	3×MCLK / 4 delayed

The relationship between RF register D1,D0 setting and sensor clock CK1,CK2,SP1 and SP2 shown below (CK2 is inverted to CK1).

MODE1, MODE2



MODE3,MODE4


TRIG
MCLK
CK1 MODE3
00
01
10
11
CK1 MODE4
00
01
10
11
SP1
00
01
10
11
SP2
00
01
10
11

•R10 register: Line clamp start pixel position

In case of line clamp mode, set the clamp start pixel position. The unit is 1 pixel.

Dummy pixel is include.

Register set data = N, and actual rising edge position is CLP↑

CLP↑=N(N=0~255)

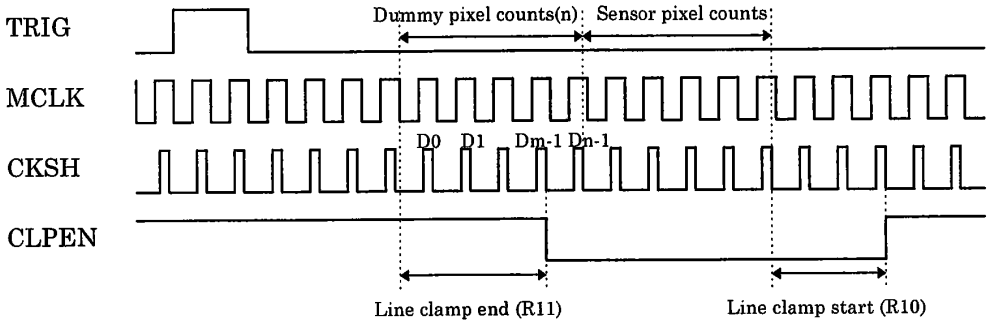
(After reset : 00h)

•R11 register: Line clamp end pixel position

In case of line clamp mode, set the clamp end pixel position. The unit is 1 pixel.

Set CLPEN to fall in dummy pixel section.

(After reset : 00h)



•R12 register

D7: Color / monochrome mode

Select color / monochrome mode.

0: color mode

1: monochrome mode

This register is available when R12 / D6 =0 (1ch sensor mode).

(Note) This register is not initialized by reset.

D6: Sensor type

Select color sensor type and internal clock.

0: 1ch color sensor MCLK ×4

1: 3ch color sensor MCLK ×12

When this register is changed, please wait about 100mS for PLL stabilization and reset AK8408.

(Note) This register is not initialized by reset.

D5,D4,D3: sampling order

Set the sampling order.

D5	D4	D3	Processing order	
0	0	0	G→R→B	(1ch mode)
			CN0→CN1→CN2	(3ch mode)
0	0	1	B→G→R	(1ch mode)
			CN2→CN0→CN1	(3ch mode)
0	1	X	R→B→G	(1ch mode)
			CN1→CN2→CN0	(3ch mode)
1	0	0	G→B→R	(1ch mode)
			CN0→CN2→CN1	(3ch mode)
1	0	1	R→G→B	(1ch mode)
			CN1→CN0→CN2	(3ch mode)
1	1	X	B→R→G	(1ch mode)
			CN2→CN1→CN0	(3ch mode)

(Note) This register is not initialized by reset.

D2,D1,D0: Channel enable register

Select the processing channel or the processing color.

0: disable

1: enable

	D2	D1	D0
3ch mode	CN2 enable	CN1 enable	CN0 enable
1ch mode	B enable	R enable	G enable

(Note) This register is not initialized by reset.

•R13 register: Gain / LED on-time adjustment threshold

Set the gain / LED on-time adjustment threshold.

(threshold) = (register value) × 4 + 2 (register value = 0~255)

•R14 register: Gain / LED on-time adjustment counter

In gain adjustment mode and LED on-time adjustment mode, the pixel number whose level is bigger than the threshold(R13) is set to this register. At the execution starting, this counter is reset to 0.

(After reset : 00h) (register value = 0~255)

•R15, R16, R17 register: PGA gain

Set the PGA gain (CN0,CN1,CN2 or GRB).

(After reset : 00h)

Gain = 335 / (335 - register value)

Register value	Gain
FFh	4.1875(12.43dB)
:	:
C1h	2.3591(7.46dB)
:	:
81h	1.6262(4.22dB)
:	:
41h	1.2407(1.87dB)
:	:
00h	1.0000(0.00dB)

(Note) Please don't use the code which are multiple of 4.

•R18, R1A, R1C register: LED on-time period

Set the LED on-time period(GRB). The unit is 32 pixels.

LED(GRB) active period = 32×(register value) (register value = 0~255)

(After reset : 00h)

•R19, R1B, R1D register: LED on start pixel

Set the starting pixel of LEDG, LEDR, LEDB. The unit is 32 pixels. Dummy pixel is include.

(After reset : 00h)

•R1E register: ABC black side limitter

Set the limitter for black side in ABC mode.

(After reset : 00h)

•R1F register: ABC white side limitter

Set the limitter for white side in ABC / AGC mode.

(After reset : FFh)

•R20 register: Peak detect counter

It is possible to read peak detection counter value.

This register cannot be accessed during the execution of the peak detect and the white shading detect modes. Generally, R21 register read is recommended for the peak value read.

•R21 register: Peak hold register

After the peak detection mode, peak value is set.

•R22 register: calibration value of peak detect circuit

D0~D4: Peak detect circuit calibration

After the black shading detection mode, internal calibration value is set. This register can be written.

D4	D3	D2	D1	D0	calibration data
0	0	0	0	0	+16
0	0	0	0	1	+15
0	0	0	1	0	+14
:	:	:	:	:	:
0	1	1	0	1	+3
0	1	1	1	0	+2
0	1	1	1	1	+1
1	0	0	0	0	0
1	0	0	0	1	-1
1	0	0	1	0	-2
1	0	0	1	1	-3
:	:	:	:	:	:
1	1	1	0	1	-13
1	1	1	1	0	-14
1	1	1	1	1	-15

(After reset 00h)

D5:White shading correction by unity gain

0: Disable(Reset)

1: Enable

This bit is set to be enabled, white shading correction gain is fixed to unity gain.

•R23/R27/R28 register: Offset calibration data

The results of offset calibration mode1 is stored in this register.

(actual black shading data) = (black shading data) + (register value)

(-128 ≤ register value ≤ 127)

In case that the calculated value is under 0 or over 255, automatically set to 0 or 255 respectively.

(After reset : 00h)

•R24 register

D7-4: White shading detection averaging number

Set the average number of white shading detection.

In the white shading detection mode, white shading detect mode is automatically executed (register value + 1) times and detected (register value + 1) set of shading data are automatically averaged, and the results are set to the external SRAM.

It is possible to reduce the noise error by averaging. Averaging operation precision is about 2LSB (this value may be changed by data pattern).

(After reset : 0) (register value = 0~15)

D3-0: Black shading detection averaging time

Set the average number of black shading detection.

In the black shading detection mode, black shading detect mode is automatically executed (register value + 1) times and detected (register value + 1) set of shading data are automatically averaged, and the results are set to the external SRAM.

It is possible to reduce the noise error by averaging. Averaging operation precision is about 2LSB (this value may be changed by data pattern).

(After reset : 0) (register value = 0~15)

•R25 register

D7-6: Black correction range

Select the black shading detection / correction range.

D7	D6	Detection / Correction range
0	0	±50mV
0	1	±100mV
1	0	±150mV
1	1	±200mV

(After reset: 01)

D5: ICLK output enable

Select Internal main clock output enable.

0: Output disable

1: Output enable (after reset)

D4: Shading memory access method

Shading memory access mode select

0: mode1 (after reset)

1: mode2

In case that sampling rate is over 4Mpixel / sec, mode2 is not available.

D3: White shading data accessing bit width

Select the white shading data accessing bit width.

0: 8bit (after reset)

1: 9bit

1. 8bit access

It is possible to access MSB 8bit at one time read / write.

2. 9bit access

It is possible to access

MSB 8bit at first read / write

LSB 1bit at second read / write.

	D7	D6	D5	D4	D3	D2	D1	D0
First	W8	W7	W6	W5	W4	W3	W2	W1
Second	0	0	0	0	0	0	0	W0

The address counter of shading memory is automatically incremented after the second access.

(Note) White shading detection is done by 9bit regardless this register setting.

D2,D1,D0: Shading memory bank select

Shading memory bank can be selected as following table.

D2	D1	D0	memory bank	BA2	BA1	BA0
0	0	0	3ch CN0 White shading data 1ch White shading data(Green) Also 1ch monochrome mode is supported	0	0	0
0	0	1	3ch CN1 White shading data 1ch White shading data(Red)	0	0	1
0	1	0	3ch CN2 White shading data 1ch White shading data(Blue)	0	1	0
0	1	1	1set data mode Black shading data Also 1ch monochrome mode is supported	0	1	1
1	0	0	3ch CN0 Black shading data 1ch Black shading data(Green)	1	0	0
1	0	1	3ch CN1 Black shading data 1ch Black shading data(Red)	1	0	1
1	1	0	3ch CN1 Black shading data 1ch Black shading data(Blue)	1	1	0

(After reset 000)

•R26 register: SP width

SP pulse width can be set by every 1 pixel unit.

W=N+1(N=0~255,Reset:N=0)

•R29 register: ADC offset adjustment

The results of offset calibration mode2 is stored in this register.

(-128 ≤ register value ≤ 127)

(After reset : 00h)

•R2A register

It is possible to access shading data through this register.

The address counter is automatically incremented by accessing this register.

Absolute maximum rating

Parameters	Sym.	Min.	max.	Unit	Remarks
Supply voltage					Must be VA≥VD
Digital	VD	-0.3	6.5	V	at all time.
Analog	VA	-0.3	6.5	V	
Digital applied voltage	VTD	-0.3	VD+0.3	V	
Analog applied voltage	VTA	-0.3	VA+0.3	V	
Operating temp.	Ta	0	70	°C	
Storage temp.	Tstg	-55	125	°C	
Soldering temp. and time	Tsol	260°C,10sec			

All voltage defined to their corresponding ground,AVSS,DVSS=0V

Recommended operating condition

Parameters	Sym.	min.	typ.	max.	Unit	Remarks
Supply voltage						Must be VA≥VD
Digital	VD	4.75	5.0	5.25	V	at all time.
Analog	VA	4.75	5.0	5.25	V	
Operating temp.	Ta	0		70	°C	

All voltage defined to their corresponding ground,AVSS,DVSS=0V

Electronic specification

■DC specification

(Unless otherwise specified, VD, VA=5V±5%, Ta=0~70°C)

Parameters	Sym.	Pins	min.	typ.	max.	Unit	Conditions
Supply current							1ch mode
Digital	ID				30	mA	MCLK=10MHz
Analog	IA				80	mA	3ch mode
							MCLK=3.3MHz
							No load
High level input voltage	VIH	Digital input pins	2.4			V	except /TEST2 and /RESET pin
			3.5			V	/TEST2 and /RESET pin
Low level input voltage	VIL	Digital input pins			0.8	V	except /TEST1 and /TEST2 pin
					0.2	V	/TEST1 and /TEST2 pin
High level output voltage	VOH	Digital output pins	3.0			V	IOH= - 1mA
Low level output voltage	VOL	Digital output pins			0.4	V	IOL=4mA
Leakage current	IL	Digital input pins	-10		10	μA	VI=DVDD VI=DVSS

■Analog specification

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

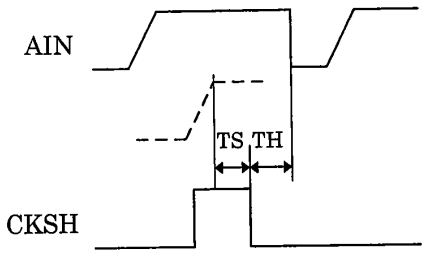
Parameters	min.	typ.	Max.	Unit	Remark
Analog input					
Maximum signal input level		1.25		Vp-p	
Sampling rate	1.5 0.5		10 3.3	Mpix/S	1ch mode 3ch mode
Input capacitance			20	pF	CN0-CN2
Input resistance	1			MΩ	CN0-CN2
Black shading detection / correction circuit					
Detect/correction enable voltage		100 ~400		mV	Set up 100mV units
Minimum correction range	VCLP±25	VCLP±50		mV	range setting=100mV
	VCLP±75	VCLP±100		mV	range setting=200mV
	VCLP±125	VCLP±150		mV	range setting=300mV
	VCLP±175	VCLP±200		mV	range setting=400mV
Resolution		8		bit	
Correction accuracy		±3	±4	LSB	10MHz sampling. Black correction range:200mV Video ADC full scale
Remain offset voltage after offset calibration 1,2		13		mV	
Voltage reference					
VCLP voltage		2.1		V	
VREF voltage		0.85		V	
Peak detection / hold circuit					
Maximum detection / output voltage	1.15	1.25	1.35	Vp-p	White side is positive against VCLP.
Resolution		8		bit	
Settling time			70	μS	10LSB change:C=0.1uF
			40	μS	1LSB change:C=0.1uF

(Unless otherwise specified VD,VA=5V±5%,Ta=0~70°C)

Parameters	min.	typ.	Max.	Unit	Remarks
DACs for reference voltage generation of 10bit video ADC					
Resolution		8		bit	
Settling time			70	μS	10LSB change:C=0.1uF
			40	μS	1LSB change:C=0.1uF
Clamp circuit					
Switch ON resistance			50	Ω	Analog input=2.0V Include Amp. ON resistance
Sample and hold circuit					
Set up time	20			nS	show next page
Hold time	10			nS	show next page
Dloop voltage at line clamp			5	mV	C=1uF 8192pixels VCLP-1.25V
Remain offset voltage after Dloop recovery time finish			13	mV	C=1uF 8192pixels MCLK=10MHz VCLP-1.25V RF/D7=1 Dloop recovery time=100μS (Note1)
PGA circuit					
Resolution		8		bit	(Note2)
Maximum Gain range	4	4.187		times	
White shading detection / correction circuit					
Resolution		9		bit	
Detection / correction range			60	%Vpk	Rate of VPEAK-VCLP
Correction accuracy		±4	±5	LSB	Video ADC calculation VWHT-VBLK=1.25V
Video 10bit ADC					
Resolution		10		bit	No code missing
Maximum signal input level		1.25		Vp-p	

(Note1)Not production tested. Parameters guaranteed by design and characterization.

(Note2) PGA gain is not linear. Please don't use the codes which are multiple of 4.


AIN
TS
TH
CKSH

■ Digital AC timing

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
1	MCLK cycle time (T)	MCLK	100		667	nS	1ch mode
			300		2000	nS	3ch mode
2	MCLK high level width	MCLK	30%		70%	T	
3	MCLK low level width	MCLK	30%		70%	T	
4	TRIG set up time (to MCLK↑)	TRIG	20			nS	
5	TRIG hold time (to MCLK↑)	TRIG	20			nS	
6	VPE set up time (to MCLK↑)	VPE	0			nS	
7	VPE hold time (to MCLK↑)	VPE	T/2+20			nS	
8	/RESET pulse width	/RESET	20			nS	
9	ICLK cycle time	ICLK		1/4		T	1ch mode
				1/12		T	3ch mode
10	ICLK high level width	ICLK		1/8		T	1ch mode
				1/24		T	3ch mode
11	ICLK low level width	ICLK		1/8		T	1ch mode
				1/24		T	3ch mode
12	ICLK delay time (to MCLK↑)	ICLK			25	nS	C=20pF
13	(PLLCLK) delay time (to MCLK↑)	(PLLCLK)	-5		+5	nS	
14	ICLK delay time (to PLLCLK↑)	ICLK			20	nS	C=20pF
15	CK1,2 low level width(3) (mode1, after TRIG)	CK1,CK2		3(N+1)		T	(Note)
16	CK1,2 high level width(3) (mode1, after TRIG)	CK1,CK2		3(N+1)		T	(Note)
17	CK1,2 cycle time(1) (mode1, mode4)	CK1,CK2		2		T	
18	CK1,2 high level width(1) (mode1, mode4)	CK1,CK2		1		T	

(Note)N is SP width register set up value.

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
19	CK1,2 low level width(1) (mode1, mode4)	CK1,CK2		1		T	
20	CK1,2 delay time(1) (mode1, mode4) (to MCLK↑)	CK1,CK2			5T/8 +33	nS	C=20pF
21	CK1,2 delay time(2) (mode1, mode4) (to MCLK↑)	CK1,CK2			7T/8 +33	nS	C=20pF
22	CK1,2 delay time(3) (mode1, mode4) (to MCLK↑)	CK1,CK2			9T/8 +33	nS	C=20pF
23	CK1,2 delay time(4) (mode1, mode4) (to MCLK↑)	CK1,CK2			11T/8 +33	nS	C=20pF
24	CK1,2 low level width(4) (mode2, after TRIG)	CK1,CK2		3(N+1)		T	
25	CK1,2 high level width(4) (mode2, after TRIG)	CK1,CK2		3(N+1)		T	
26	CK1,2 cycle time(2) (mode2, mode3)	CK1,CK2		1		T	
27	CK1,2 high level width(2) (mode2, mode3)	CK1,CK2		1/2		T	
28	CK1,2 low level width(2) (mode2, mode3)	CK1,CK2		1/2		T	
29	CK1,2 delay time(5) (mode2, mode3) (to MCLK↑)	CK1,CK2			T/8 +33	nS	C=20pF
30	CK1,2 delay time(6) (mode2, mode3) (to MCLK↑)	CK1,CK2			3T/8 +33	nS	C=20pF
31	CK1,2 delay time(7) (mode2, mode3) (to MCLK↑)	CK1,CK2			5T/8 +33	nS	C=20pF
32	CK1,2 delay time(8) (mode2, mode3) (to MCLK↑)	CK1,CK2			7T/8 +33	nS	C=20pF

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	Max.	unit	Condition
33	SP1,2 delay time (to MCLK↑)	SP1,SP2			5T/8 +33	nS	C=20pF
34	SP1,2 pulse width (to MCLK↑)	SP1,SP2		N+1		T	mode 1,2
				1		T	mode 3,4
35	CK3 delay time (to MCLK↑)	CK3			5T/8 +33	nS	C=20pF
36	CK4 delay time (to MCLK↑)	CK4			7T/8 +33	nS	C=20pF
37	CK5 delay time (to MCLK↑)	CK5			T/8 +33	nS	C=20pF
38	CK6 delay time (to MCLK↑)	CK6			5T/8 +33	nS	C=20pF
39	CK6~3 cycle time	CK6~3		1		T	
40	CK6~3 high level width	CK6~3		1/4		T	
41	CK6~3 low level width	CK6~3		3/4		T	
42	CKSH delay time (to MCLK↑)	CKSH			T/8 +35	nS	C=20pF
43	CKSH cycle time	CKSH		1		T	
44	CKSH high level width	CKSH		1/4		T	
45	CKSH low level width	CKSH		3/4		T	
46	CLPEN delay time (to MCLK↑)	CLPEN			5T/8 +35	nS	1ch mode C=20pF
					11T/24 +35	nS	3ch mode C=20pF
47	CKCL delay time (line clamp, mode0) (to MCLK↑)	CKCL			5T/8 +35	nS	1ch mode C=20pF
					11T/24 +35	nS	3ch mode C=20pF
48	CKCL delay time (line clamp, mode1) (to MCLK↑)	CKCL			5T/8 +35	nS	C=20pF
49	CKCL cycle time (line clamp, mode1)	CKCL		1		T	

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70℃)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
50	CKCL high level width (line clamp, mode1)	CKCL		1/4		T	
51	CKCL low level width (line clamp, mode1)	CKCL		3/4		T	
52	CKCL delay time (bit clamp, mode0) (to MCLK↑)	CKCL			5T/8 +35	nS	C=20pF
53	CKCL cycle time (bit clamp, mode0)	CKCL		1		T	
54	CKCL high level width (bit clamp, mode0)	CKCL		1/4		T	
55	CKCL low level width (bit clamp, mode0)	CKCL		3/4		T	
56	CKCL delay time (bit clamp, mode1) (to MCLK↑)	CKCL			3T/4 +35	nS	C=20pF
57	CKCL cycle time (bit clamp, mode1)	CKCL		1		T	
58	CKCL high level width (bit clamp, mode1)	CKCL		1/8		T	
59	CKCL low level width (bit clamp, mode1)	CKCL		7/8		T	
60	LED(G/R/B) delay time (to MCLK↑)	LED (G/R/B)			T/2 +37	nS	C=20pF
61	VD9~0 delay time (1ch mode) (to MCLK↑)	VD9~0			T/2 +33	nS	C=20pF
62	DCLK delay time (1ch mode) (to MCLK↑)	DCLK			T/2 +33	nS	C=20pF
63	DCLK cycle time	DCLK		1		T	1ch mode
				1/3		T	3ch mode
64	DCLK high level width	DCLK		1/2		T	1ch mode
				1/6		T	3ch mode

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
65	DCLK low level width	DCLK		1/2		T	1ch mode
				1/6		T	3ch mode
66	VD9~0 set up time (1ch mode) (to DCLK↓)	VD9~0	T/2 -10			nS	C=20pF
67	VD9~0 hold time (1ch mode) (to DCLK↓)	VD9~0	T/2 -10			nS	C=20pF
68	CN0DEN delay time (1ch mode) (to MCLK↑)	CN0DEN			T/2 +33	nS	C=20pF
69	CN2~0DEN set up time (to DCLK↓)	CN0DEN CN1DEN CN2DEN	T/2 -10			nS	C=20pF
70	CN2~0DEN hold time (to DCLK↓)	CN0DEN CN1DEN CN2DEN	T/2 -10			nS	C=20pF
71	VD9~0 delay time(1) (3ch mode) (to MCLK↑)	VD9~0			3T/4 +33	nS	C=20pF
72	VD9~0 delay time(2) (3ch mode) (to MCLK↑)	VD9~0			T/12 +33	nS	C=20pF
73	VD9~0 delay time(3) (3ch mode) (to MCLK↑)	VD9~0			5T/12 +33	nS	C=20pF
74	VD9~0 set up time (3ch mode) (to DCLK↓)	VD9~0	T/6 -10			nS	C=20pF
75	VD9~0 hold time (3ch mode) (to DCLK↓)	VD9~0	T/6 -10			nS	C=20pF
76	DCLK delay time(1) (3ch mode) (to MCLK↑)	DCLK			3T/4 +33	nS	C=20pF

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	Max.	unit	Condition
77	DCLK delay time(2) (3ch mode) (to MCLK↑)	DCLK			T/12 +33	nS	C=20pF
78	DCLK delay time(3) (3ch mode) (to MCLK↑)	DCLK			5T/12 +33	nS	C=20pF
79	CN0DEN delay time (3ch mode) (to MCLK↑)	CN0DEN			3T/4 +33	nS	C=20pF
80	CN1DEN delay time (3ch mode) (to MCLK↑)	CN1DEN			T/12 +33	nS	C=20pF
81	CN2DEN delay time (3ch mode) (to MCLK↑)	CN2DEN			5T/12 +33	nS	C=20pF
82	CN2~0DEN pulse width (3ch mode)	CN0DEN CN1DEN CN2DEN		1/3		T	
83	SA12~0 set up time (to /SWR↑)	SA12~0	14T-10			nS	1ch mode C=20pF
			7T-10			nS	3ch mode C=20pF
84	SA12~0 hold time (to /SWR↑)	SA12~0	2T-10			nS	1ch mode C=20pF
			9T-10			nS	3ch mode C=20pF
85	/SWR pulse width	/SWR		1/2		T	1ch mode
				1/6		T	3ch mode
86	/SWR delay time (to /SRD↑)	/SWR	2T-10			nS	1ch mode C=20pF
			2T/3 -10			nS	3ch mode C=20pF
87	/SRD pulse width	/SRD		1/2		T	1ch mode
				1/6		T	3ch mode

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
88	SA12~0 hold time (to /SRD↑)	SA12~0	2T/9 -10			nS	1ch mode C=20pF
			59T/6 -10			nS	3ch mode C=20pF
89	SD8~0 acceptable delay time (to SA12~0)	SD8~0			23T/2 -20	nS	1ch mode C=20pF
					37T/6 -20	nS	3ch mode C=20pF
90	SD8~0 acceptable delay time (to /SRD↓)	SD8~0			T/2 -20	nS	1ch mode C=20pF
					T/6 -20	nS	3ch mode C=20pF
91	SD8~0 hold time (to /SRD↑)	SD8~0	0			nS	C=20pF
92	SD8~0→Hi-Z acceptable delay time (to /SRD↑)	SD8~0			2T-10	nS	1ch mode C=20pF
					2T/3 -10	nS	3ch mode C=20pF
93	SD8~0 set up time (to /SWR↑)	SD8~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
94	SD8~0 hold time (to /SWR↑)	SD8~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
95	SD8~0 acceptable delay time (to SA12~0, BA2~0)	SD8~0			T/2 -20	nS	1ch mode C=20pF
					T/6 -20	nS	3ch mode C=20pF
96	SA12~0, BA2~0 hold time (to /SRD↑)	SA12~0 BA2~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
97	/SRD cycle time	/SRD		1		T	1ch mode
				1/3		T	3ch mode
98	/SRD low level width	/SRD		1/2		T	1ch mode
				1/6		T	3ch mode
99	/SRD high level width	/SRD		1/2		T	1ch mode
				1/6		T	3ch mode
100	SD8~0 acceptable delay time (to /SRD↓)	SD8~0			T/2 -20	nS	1ch mode C=20pF
					T/6 -20	nS	3ch mode C=20pF
101	SD8~0 hold time (to /SRD↑)	SD8~0	0			nS	C=20pF
102	SA12~0 set up time (to /SWR↑)	SA12~0	15T-10			nS	1ch mode C=20pF
			5T-10			nS	3ch mode C=20pF
103	BA2~0 set up time (to /SWR↑)	BA2~0	55T/4 -10			nS	1ch mode C=20pF
			55T/12 -10			nS	3ch mode C=20pF
104	SA12~0 hold time (to /SWR↑)	SA12~0	T-10			nS	1ch mode C=20pF
			11T -10			nS	3ch mode C=20pF
105	SD8~0 acceptable delay time (to BA2~0)	SD8~0			3T/4 -20	nS	1ch mode C=20pF
					T/4 -20	nS	3ch mode C=20pF
106	BA2~0 hold time (to /SRD↑)	BA2~0	T/4 -10			nS	1ch mode C=20pF
			T/12 -10			nS	3ch mode C=20pF
107	/SWR pulse width	/SWR		1/2		T	1ch mode
				1/6		T	3ch mode

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
108	/SRD pulse width	/SRD		1/2		T	1ch mode
				1/6		T	3ch mode
109	/SWR delay time (to /SRD↑)	/SWR	2T-10			nS	1ch mode C=20pF
			2T/3 -10			nS	3ch mode C=20pF
110	SA12~0 hold time (to /SRD↑)	SA12~0	7T/2 -10			nS	1ch mode C=20pF
			71T/6 -10			nS	3ch mode C=20pF
111	SD8~0 acceptable delay time (to /SRD↓)	SD8~0			T/2 -20	nS	1ch mode C=20pF
					T/6 -20	nS	3ch mode C=20pF
112	SD8~0 acceptable delay time (to SA12~0)	SD8~0			T-20	nS	1ch mode C=20pF
					T/3 -20	nS	3ch mode C=20pF
113	SD8~0 hold time (to /SRD↑)	SD8~0	0			nS	C=20pF
114	SD8~0→Hi-Z acceptable delay time (to /SRD↑)	SD8~0			2T-10	nS	1ch mode C=20pF
					2T/3 -10	nS	3ch mode C=20pF
115	SD8~0 set up time (to /SWR↑)	SD8~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
116	SD8~0 hold time (to /SWR↑)	SD8~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
117	SA12~0, BA2~0 delay time (to PLLCLK↑)	SA12~0 BA2~0			33	nS	C=20pF
118	SD8~0 acceptable delay time (to SA12~0, BA2~0)	SD8~0			T/2 -20	nS	1ch mode C=20pF
					T/6 -20	nS	3ch mode C=20pF
119	SD8~0 hold time (to PLLCLK↑)	SD8~0	0			nS	C=20pF
120	SA12~0, BA2~0, /SWR, /SRD Hi-Z→output delay time (to PLLCLK↑)	SA12~0 BA2~0 /SWR /SRD			33	nS	C=20pF
121	/ACCEEN delay time	/ACEEN			33	nS	C=20pF
122	SD8~0 acceptable delay time (to SA12~0,BA2~0,/SRD)	SD8~0			T/2 -20	nS	1ch mode C=20pF
					T/6 -20		3ch mode C=20pF
123	SA12~0, BA2~0, /SWR, /SRD hold time (to PLLCLK↑)	SA12~0 BA2~0 /SWR /SRD	0			nS	C=20pF
124	/SWR,/SRD output period (at read timing)	/SWR		1/2		T	1ch mode
		/SRD		1/6		T	3ch mode
125	/ACEEN high level width (at read timing)	/ACEEN		1/2		T	1ch mode
				1/6		T	3ch mode
126	/SWR delay time (to /SRD↑)	/SWR	2T-10			nS	1ch mode C=20pF
			2T/3 -10			nS	3ch mode C=20pF
127	SD8~0 hold time (to PLLCLK↑)	SD8~0	0			nS	C=20pF

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
128	SD8~0 →Hi-z acceptable delay time (to PLLCLK↑)	SD8~0			2T	nS	1ch mode C=20pF
					2T/3	nS	3ch mode C=20pF
129	SA12~0, BA2~0 set up time (to /SWR↑)	SA12~0 BA2~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
130	SA12~0, BA2~0 hold time (to /SWR↑)	SA12~0 BA2~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
131	/SWR low level width (at write timing)	/SWR		1/2		T	1ch mode
				1/6		T	3ch mode
132	/SWR high level width (at write timing)	/SWR		1/2		T	1ch mode
				1/6		T	3ch mode
133	/SRD output period (at write timing)	/SRD		1		T	1ch mode
				1/3		T	3ch mode
134	SD8~0 set up time (to /SWR↑)	SD8~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
135	SD8~0 hold time (to /SWR↑)	SD8~0	T/2 -10			nS	1ch mode C=20pF
			T/6 -10			nS	3ch mode C=20pF
136	/ACEEN high level width (at write timing)	/ACEEN		1		T	1ch mode
				1/3		T	3ch mode
137	/SWR, /SRD cycle time	/SWR		1		T	1ch mode
		/SRD		1/3		T	3ch mode
138	/SWR, /SRD Hi-Z width	/SWR		1/2		T	1ch mode
		/SRD		1/6		T	3ch mode
139	/ACEEN cycle time	/ACEEN		1		T	1ch mode
				1/3		T	3ch mode

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70℃)

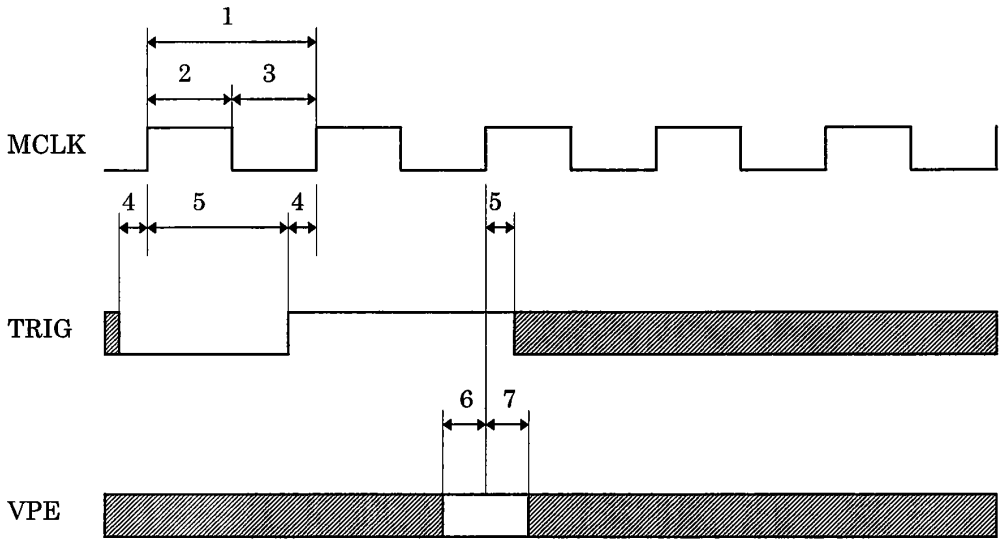
No.	Parameters	Pins	min.	typ.	max.	unit	Condition
140	/ACEEN low level width	/ACEEN		1/2		T	1ch mode
				1/6		T	3ch mode
141	SD8~0 acceptable delay time (to SA12~0, BA2~0,/SRD)	SD8~0			T/4 -20	nS	1ch mode C=20pF
					T/12 -20	nS	3ch mode C=20pF
142	/SDCLK cycle time	/SDCLK	160			nS	memory access
			80			nS	
143	/SDCLK low level width	/SDCLK	80			nS	memory access
			40			nS	
144	/SDCLK high level width	/SDCLK	80			nS	memory access
			40			nS	
145	serial access cycle time	/SDCLK	2600			nS	memory access
			1360			nS	
146	SDIN set up time (to /SDCLK↑)	SDIN	20			nS	
147	SDIN hold time (to /SDCLK↑)	SDIN	20			nS	
148	/SDEN set up time (to SDCLK↓)	/SDEN	40			nS	
149	/SDEN hold time (to /SDCLK↑)	/SDEN	40			nS	
150	/SDEN high level width	/SDEN	40			nS	
151	/SWR delay time (to /SDCLK↑)	/SWR			30	nS	C=20pF
152	/SWR pulse width	/SWR	No.149 -15			nS	C=20pF
153	/SWR delay time (to /SDEN↑)	/SWR			25	nS	C=20pF

(Unless otherwise specified, VD,VA=5±5%, Ta=0~70°C)

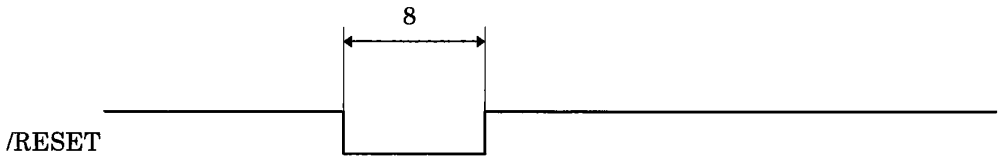
No.	Parameters	Pins	min.	typ.	max.	unit	Condition
154	SA12~0 hold time (to /SWR↑)	SA12~0	T/4 -10			nS	1ch mode C=20pF
			T/12 -10			nS	3ch mode C=20pF
155	SD8~0 set up time (to /SWR↑)	SD8~0	No.149 -25			nS	C=20pF
156	SD8~0 hold time (to /SWR↑)	SD8~0	0			nS	C=20pF
157	SDOUT delay time (to /SDCLK↓)	SDOUT			30	nS	C=20pF
158	SDOUT hold time (to /SDEN↑)	SDOUT	0			nS	C=20pF
159	/SRD delay time (to /SDCLK↑)	/SRD			40	nS	C=20pF
160	/SRD delay time (to /SDCLK↓)	/SRD			30	nS	C=20pF
161	SA12~0 hold time (to /SRD↑)	SA12~0	T/4 -10			nS	1ch mode C=20pF
			T/12 -10			nS	3ch mode C=20pF
162	SD8~0 acceptable delay time (to /SRD↓)	SD8~0			No. 144 -40	nS	C=20pF
163	SD8~0 hold time (to /SDCLK↓)	SD8~0	0			nS	C=20pF
164	/SRD pulse width	/SRD	No.144 -20			nS	C=20pF
165	LED(G/R/B) delay time	LED (G/R/B)			T/2 +33	nS	1ch mode C=20pF
					T/6 +33	nS	3ch mode C=20pF

■Timing specifications

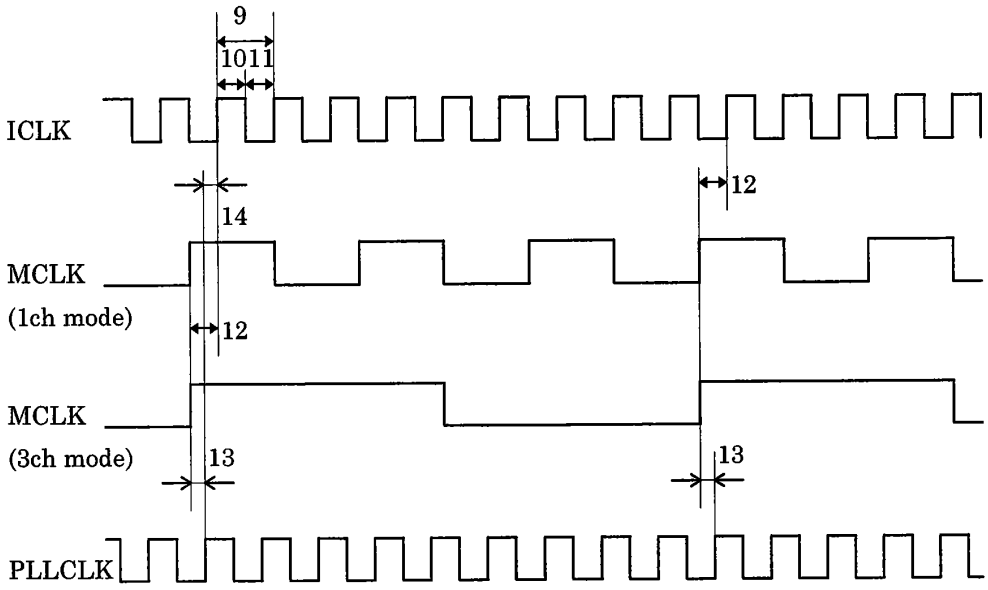
(1) Basic clocks



(2) Reset

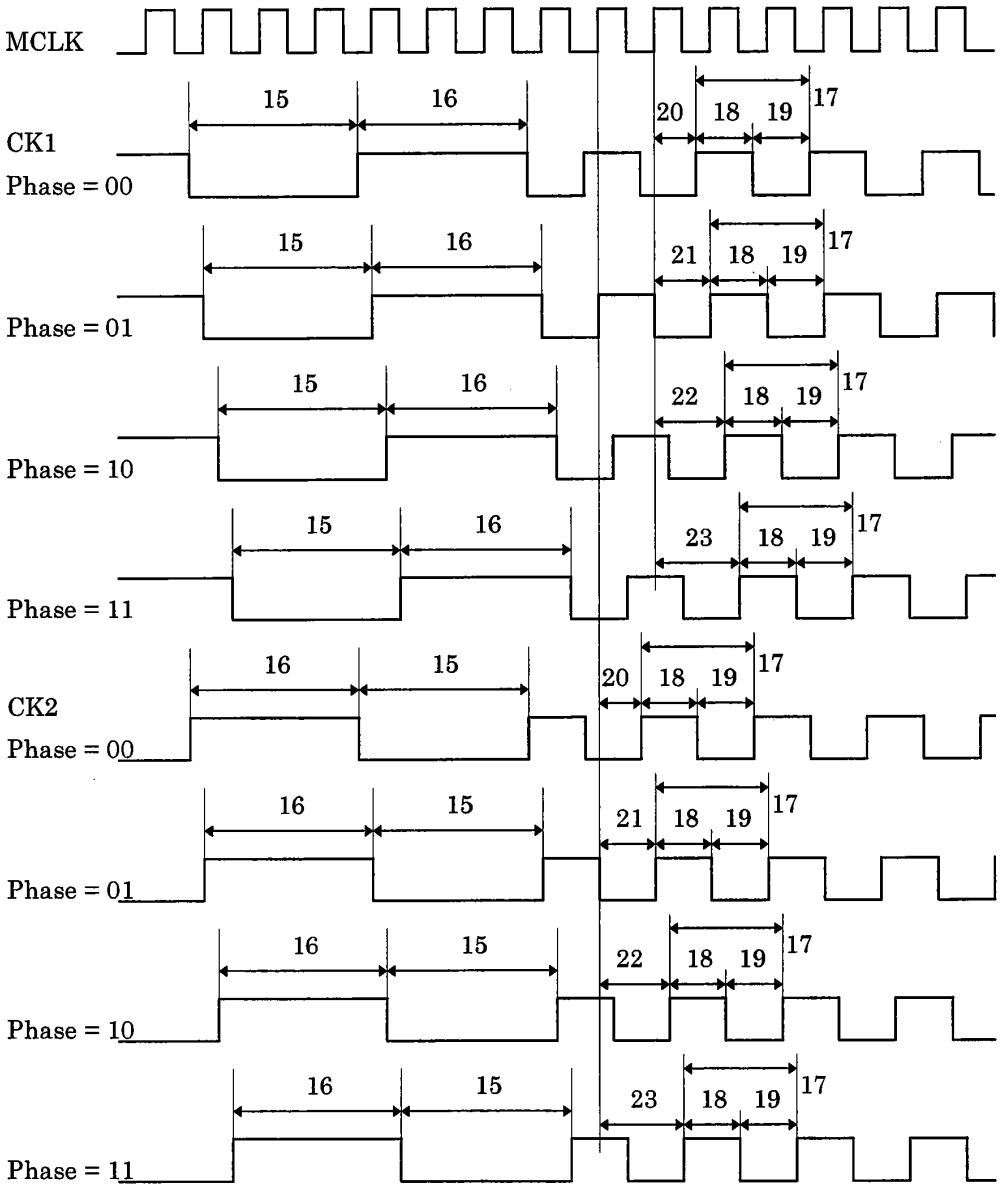


(3) PLL clock

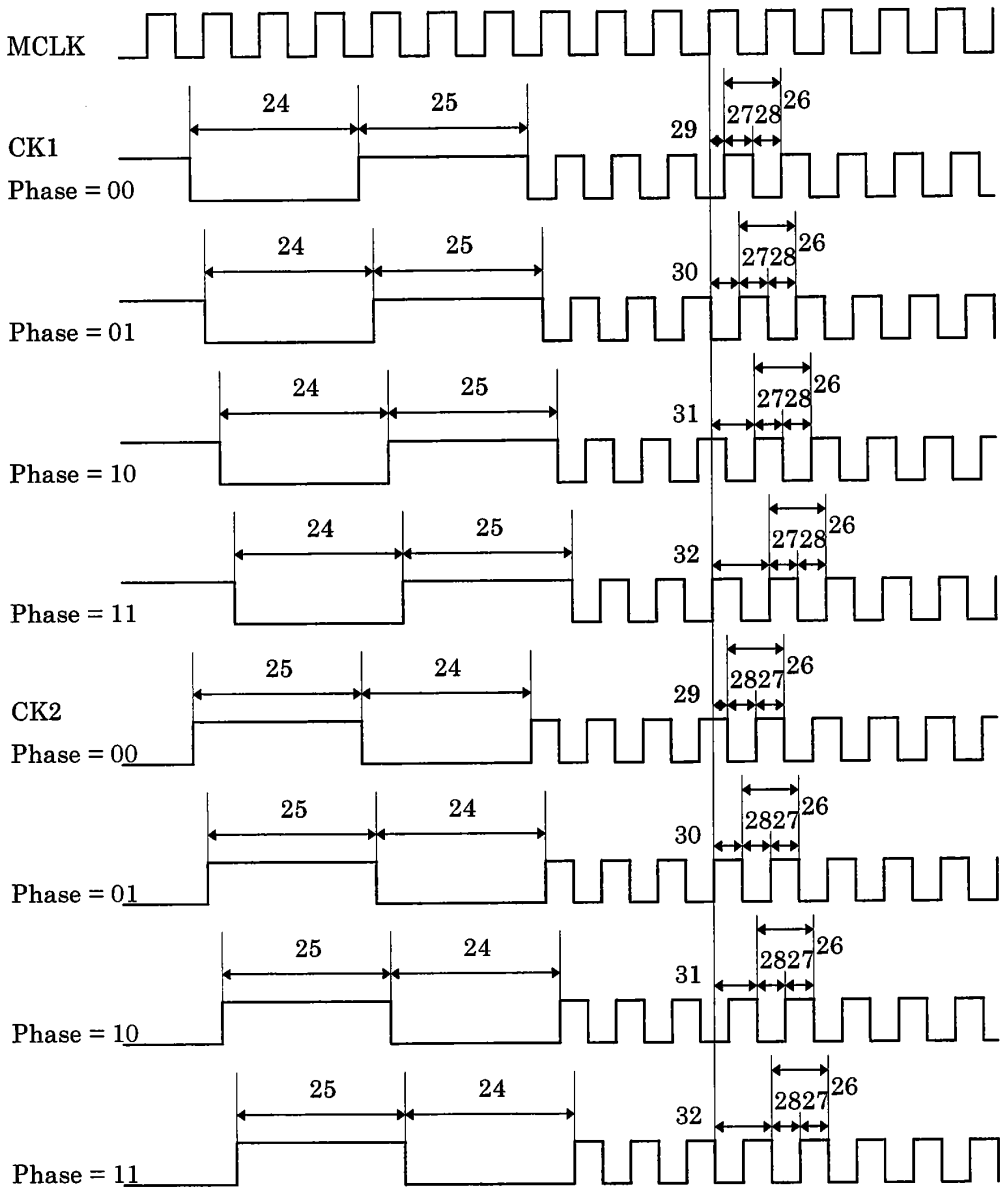


(Note) PLLCLK is internal basic clock which is generated by internal PLL.

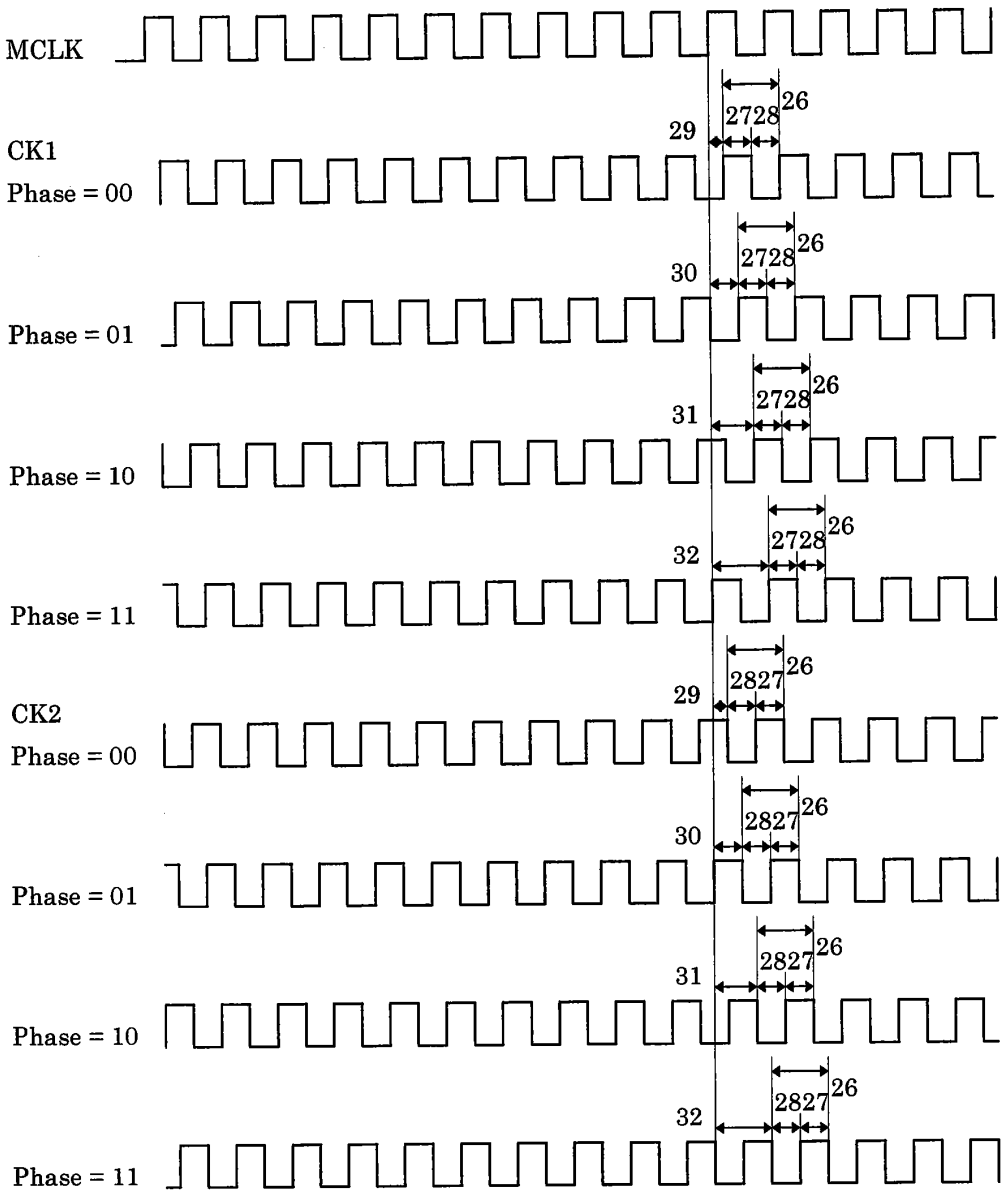
(4) Sensor clock timing (mode1)



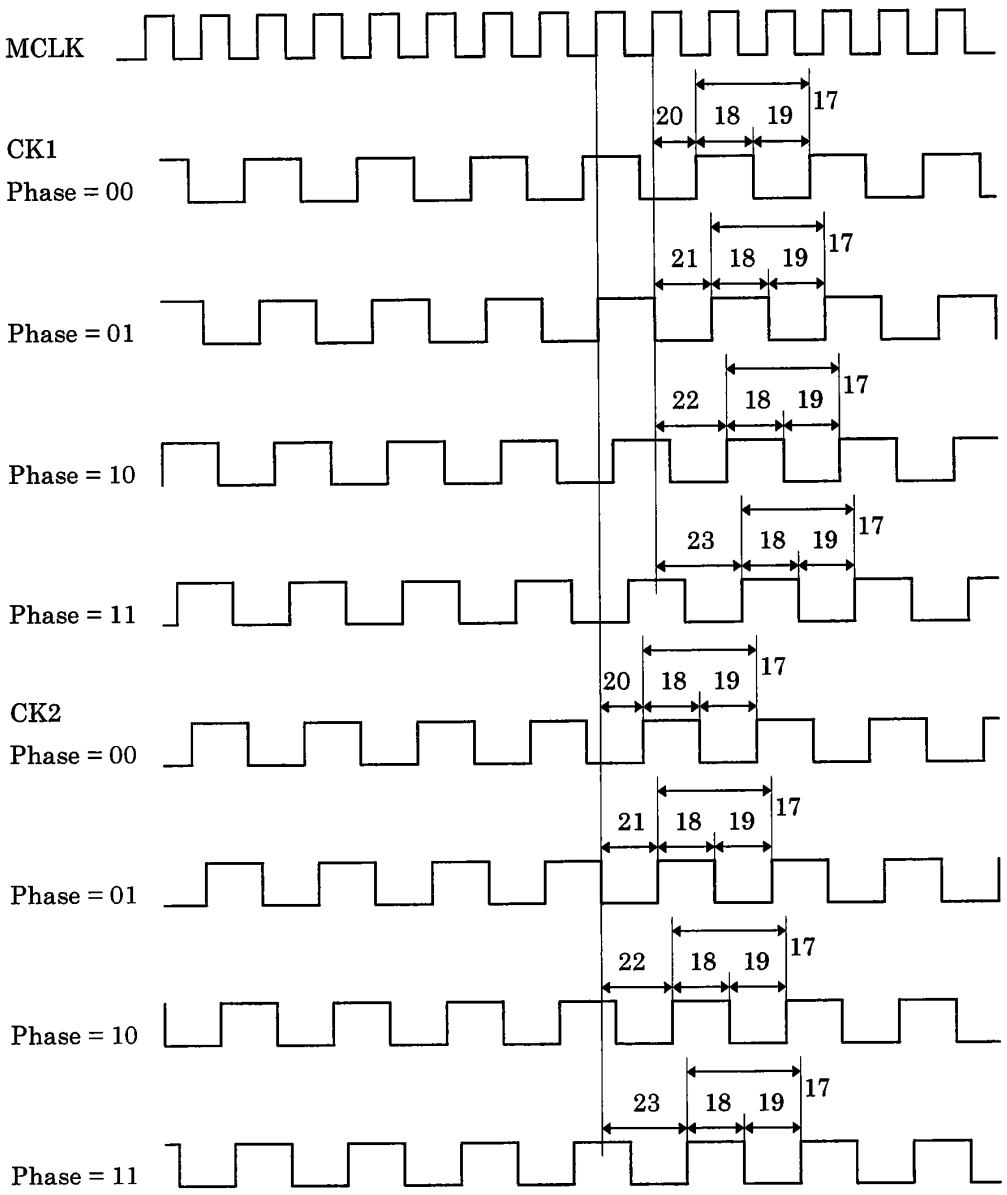
(5) Sensor clock timing (mode2)



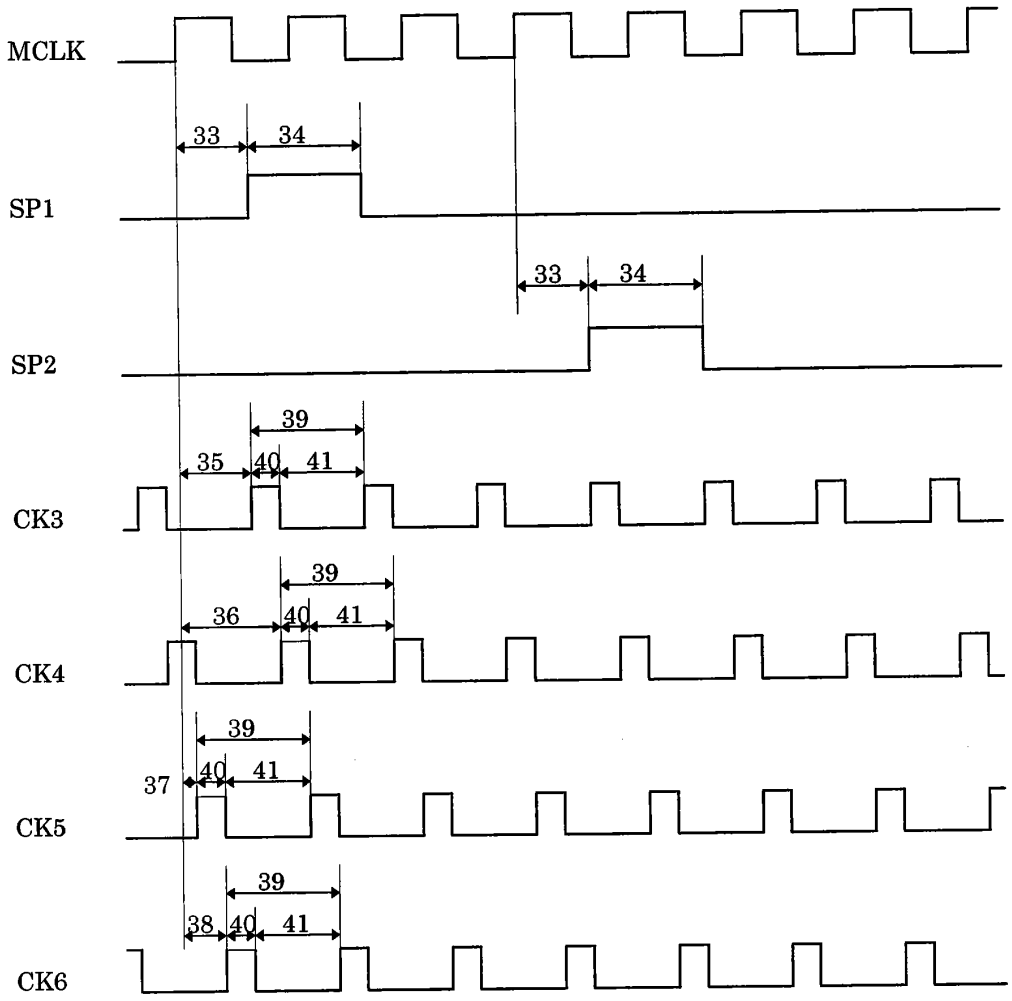
(6) Sensor clock timing (mode3)



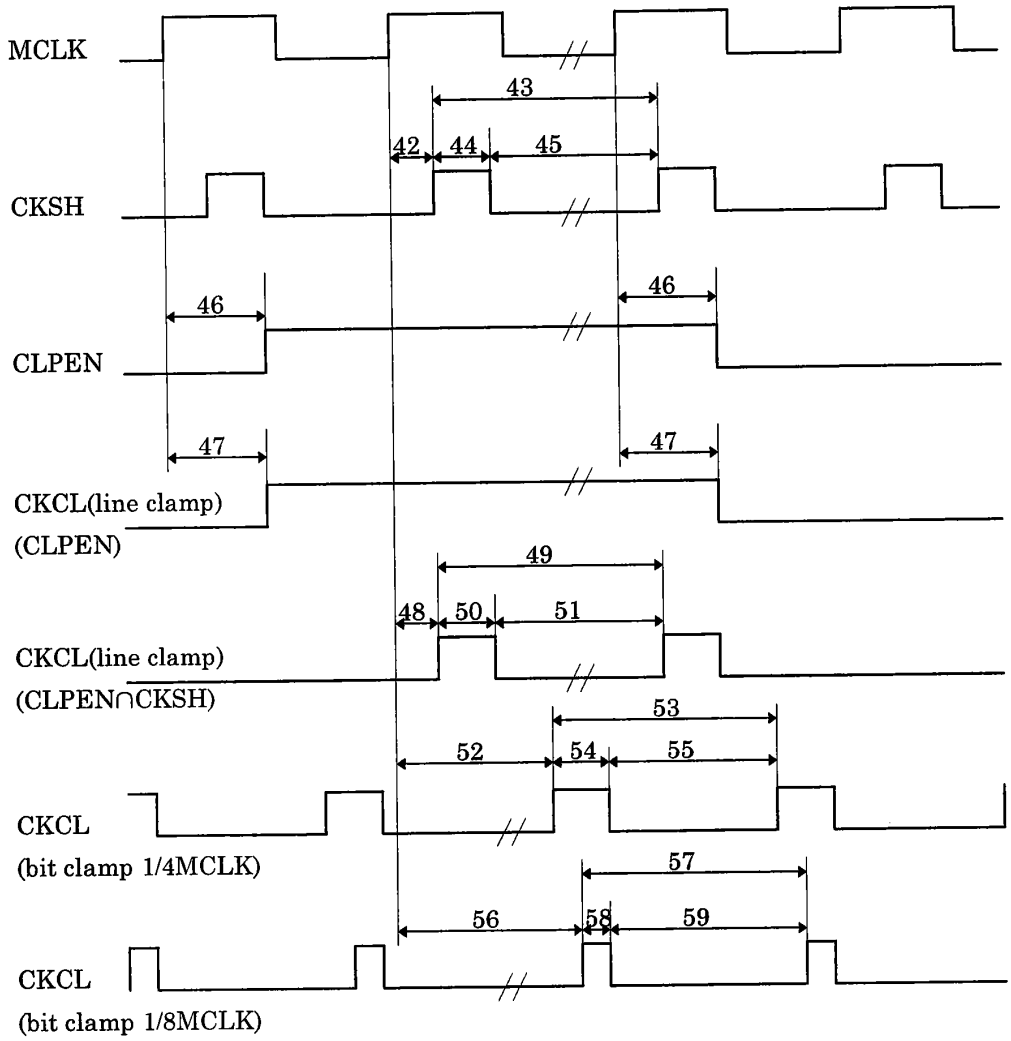
(7) Sensor clock timing (mode4)



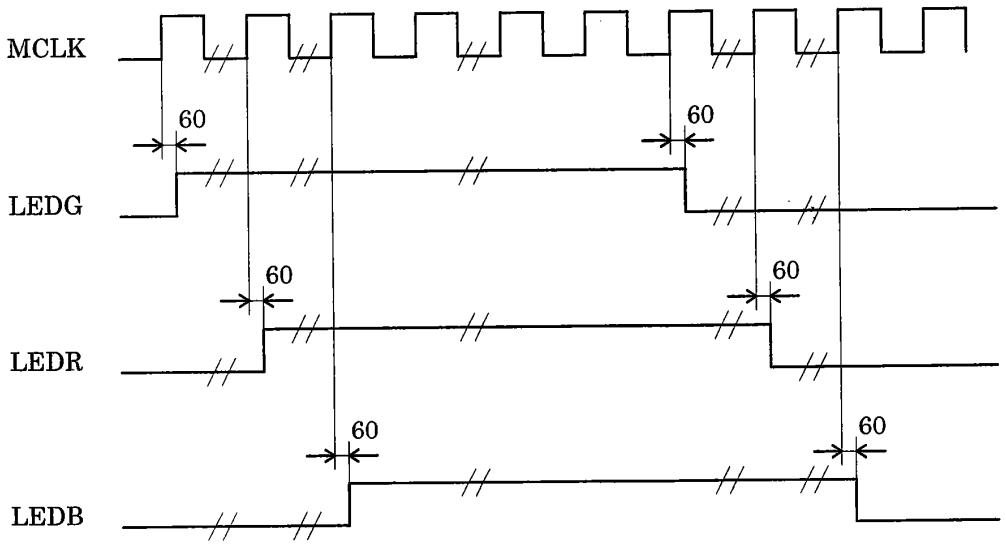
(8) Sensor clock timing (SP1~2, CK3~6)



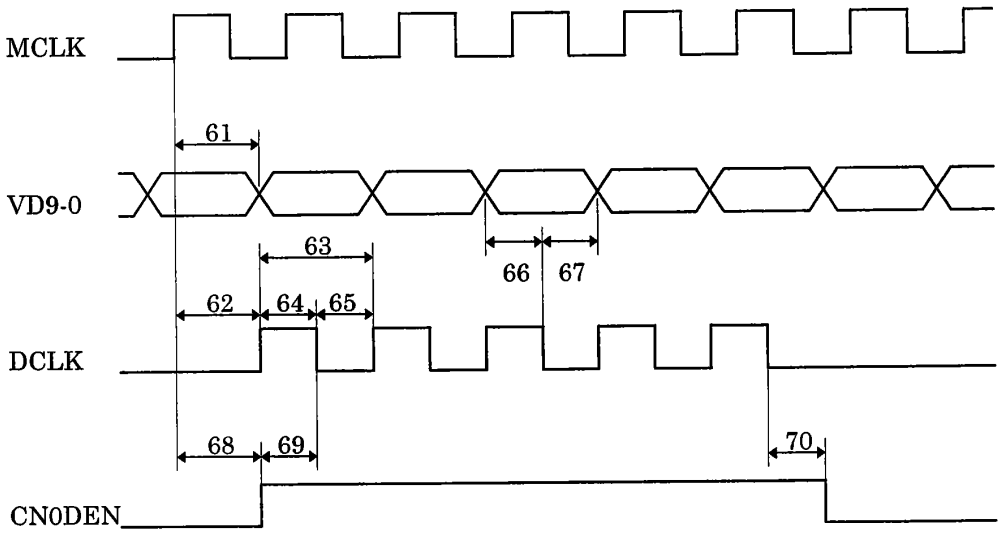
(9) Sensor clock timing (S/H, clamp)



(10) LED (G/R/B) timing (variable setting)

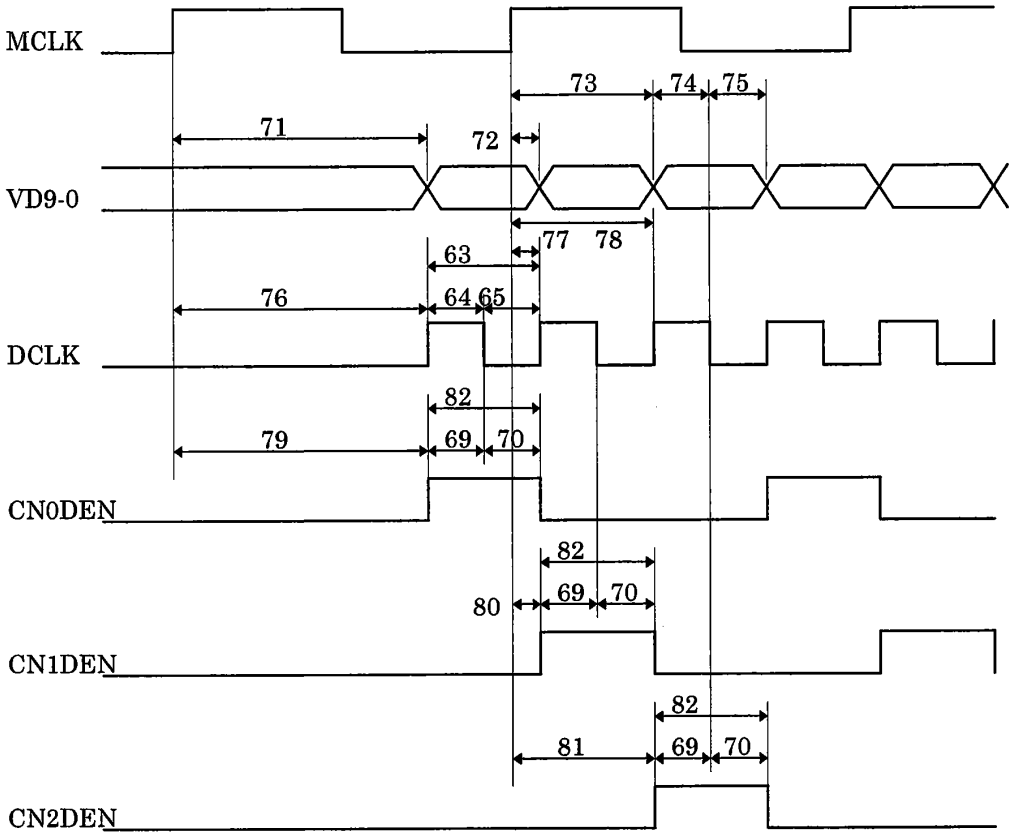


(11) Video data I/F (1ch mode)

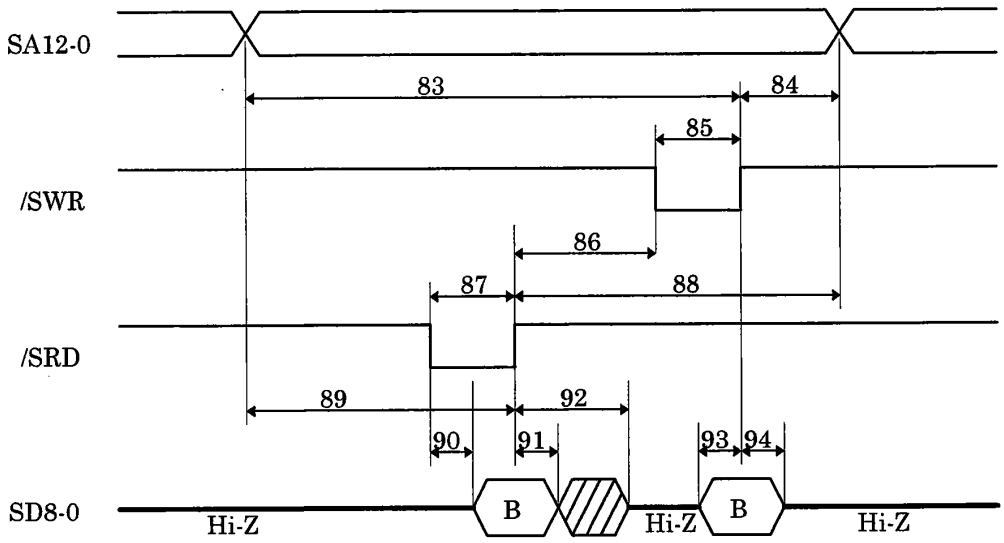


CN1DEN and CN2DEN are low level fix.

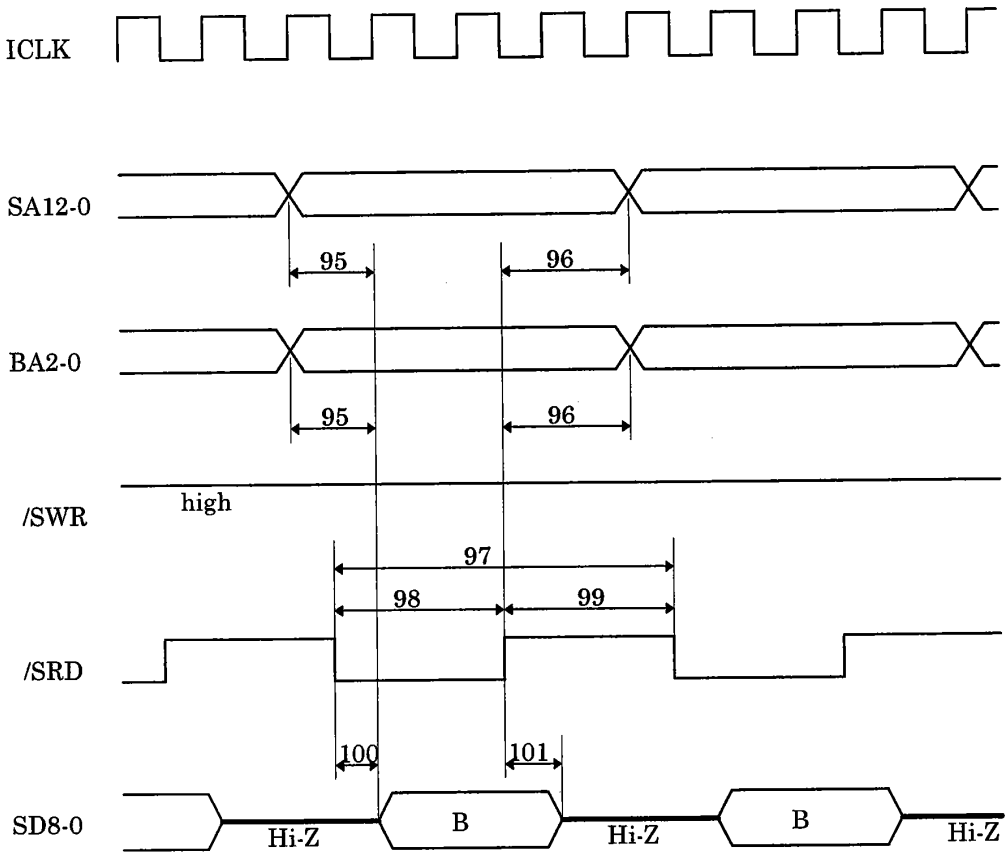
(12) Video data I/F (3ch mode)



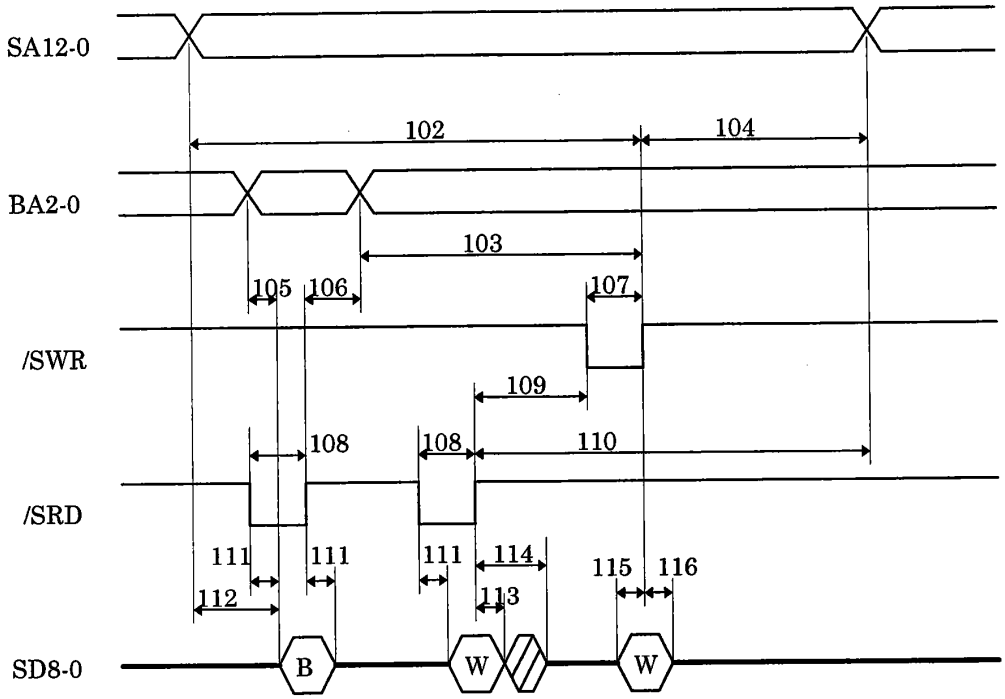
(13) Memory access timing (black shading detect)



(14) Memory access timing (gain adjustment, peak detect)

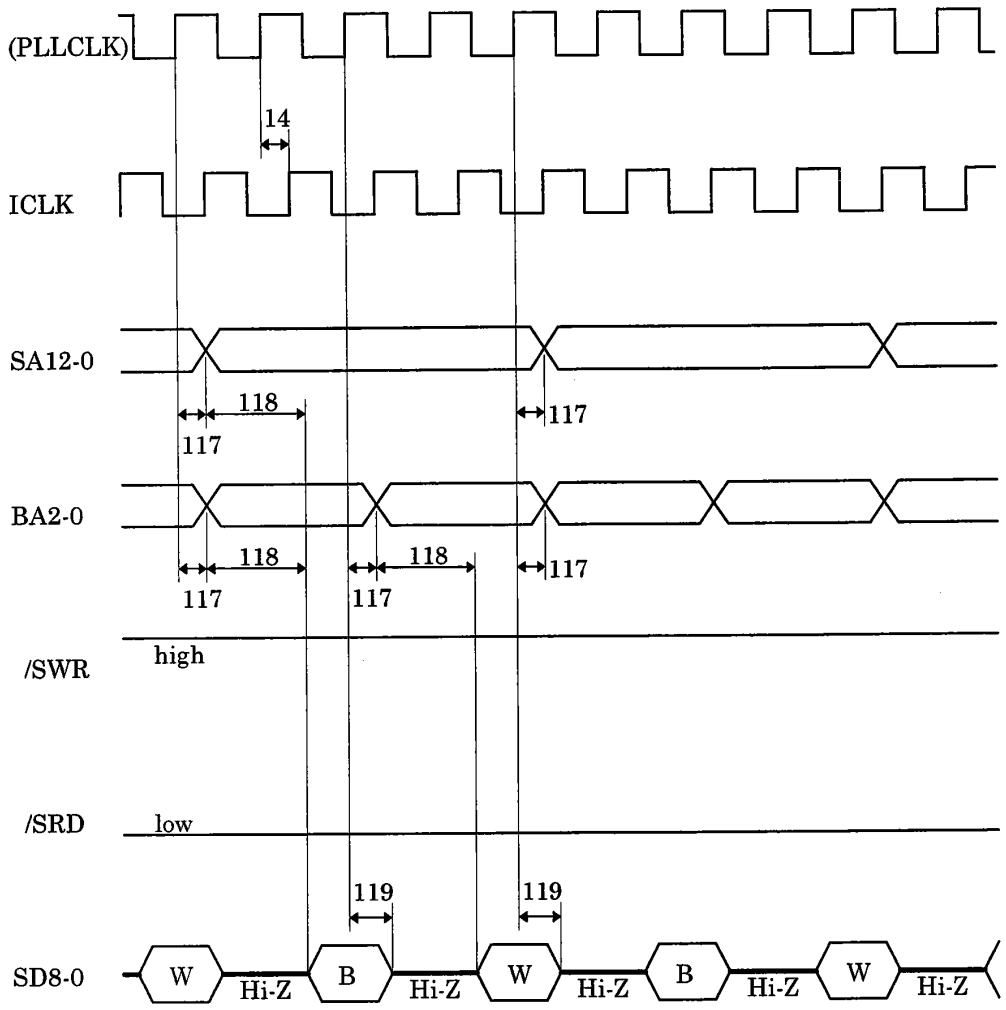


(15) Memory access timing (white shading detect)

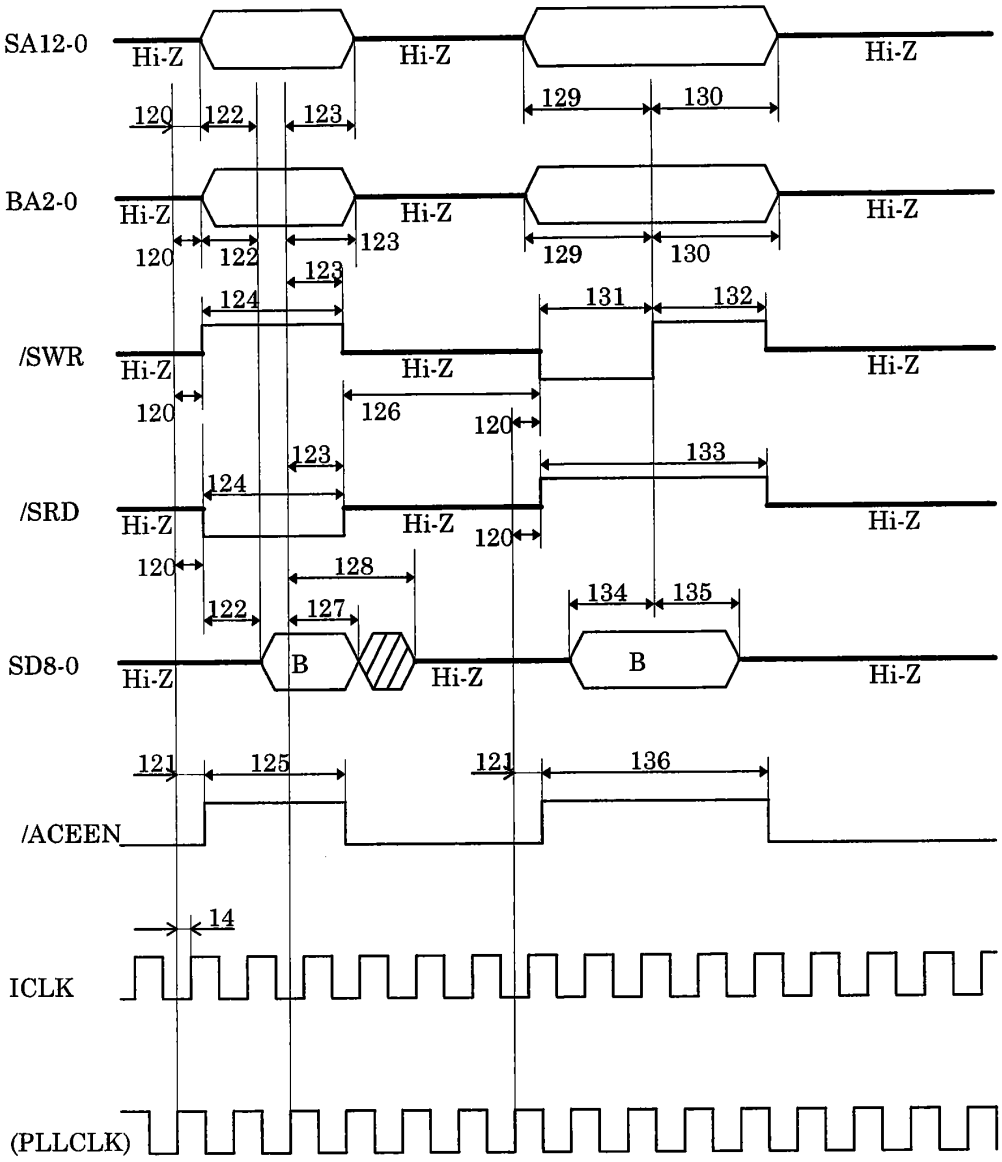


(Note) In case of black offset cancel mode, black data read does not read.
(/SRD will be high level and SD8~0 will be Hi-Z at black data read timing.)

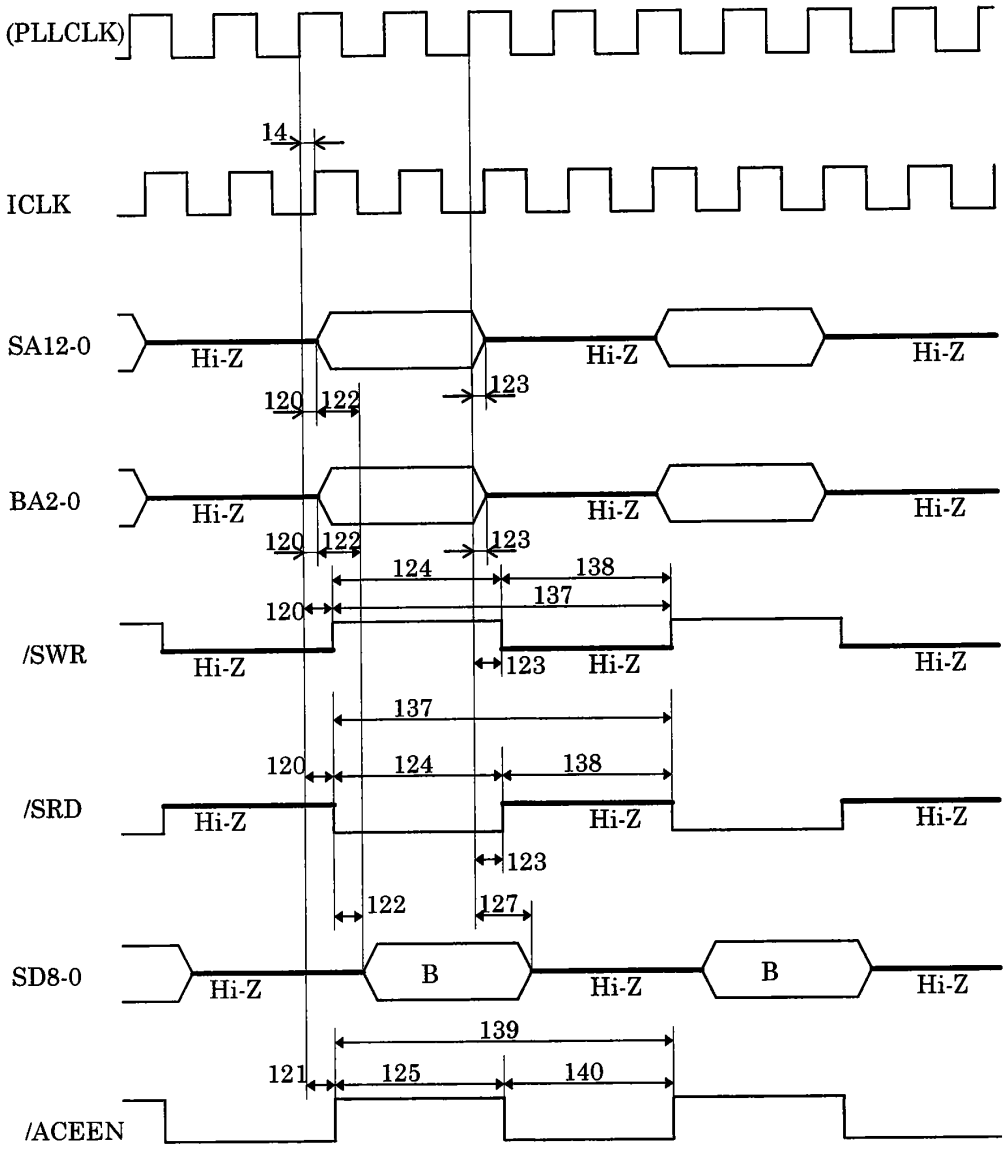
(16) Memory access timing (document scanning)



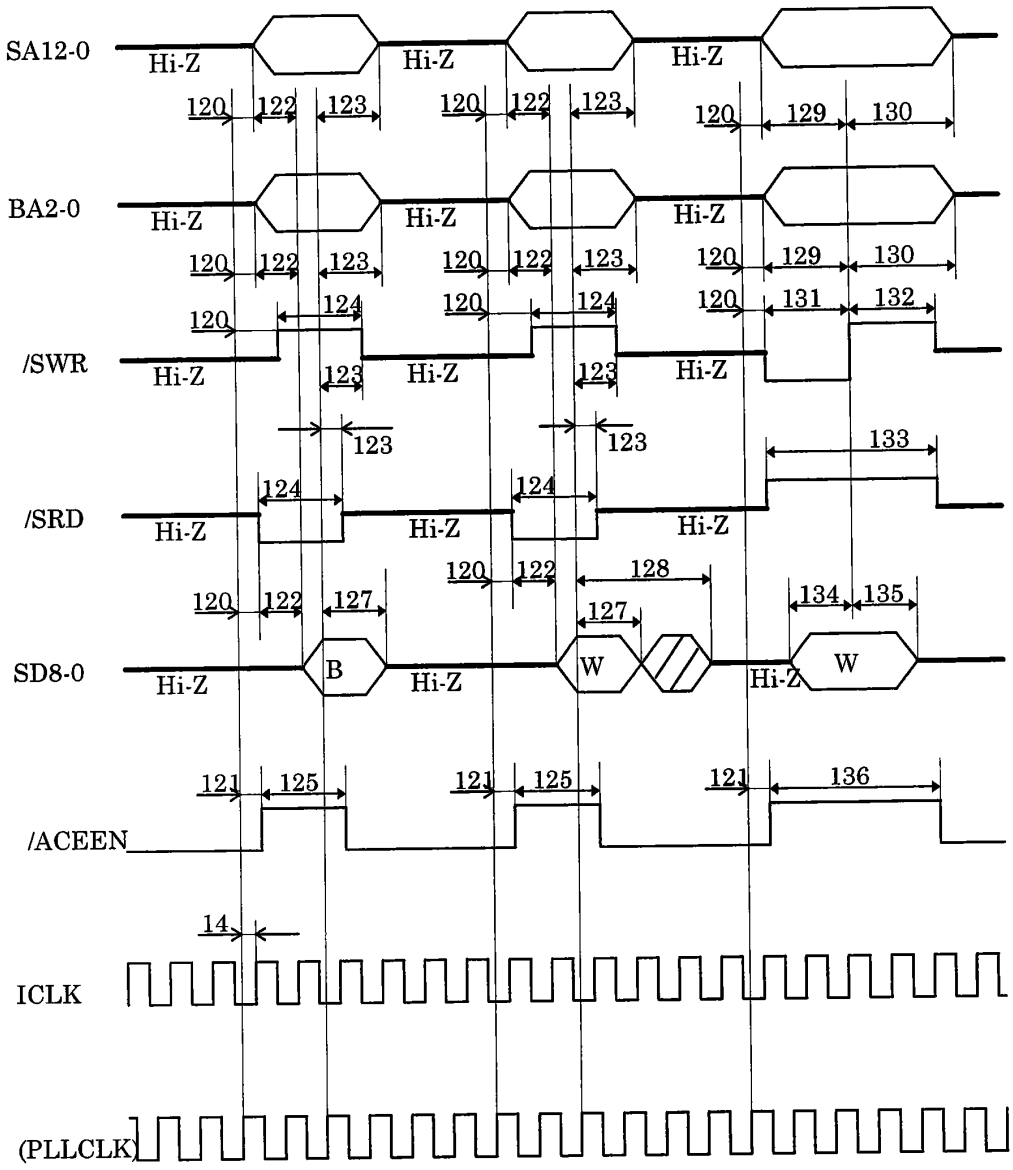
(17) Memory access timing in external access mode (black shading detect)



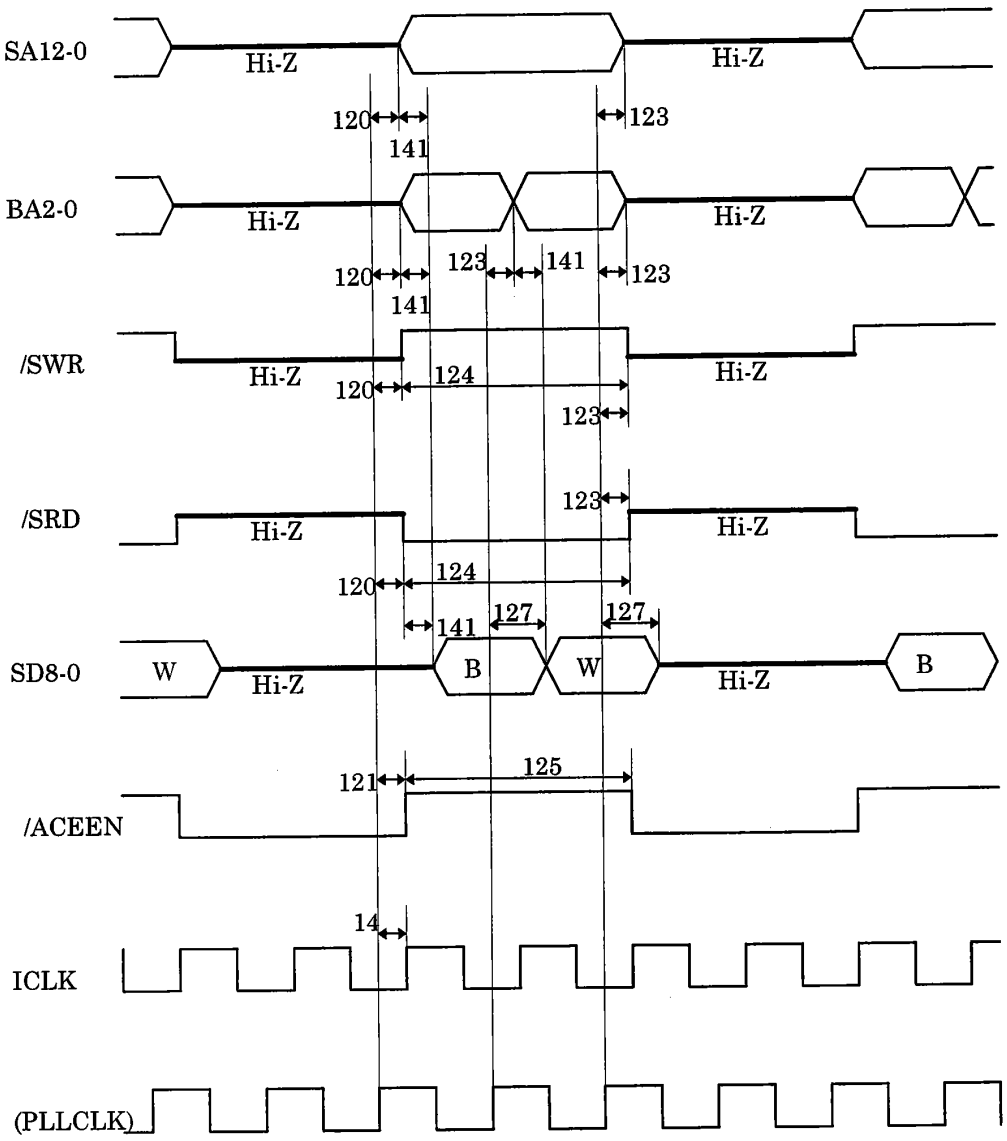
(18) Memory access timing in external access mode (gain adjust, peak detect)



(19) Memory access timing in external access mode (white shading detect)

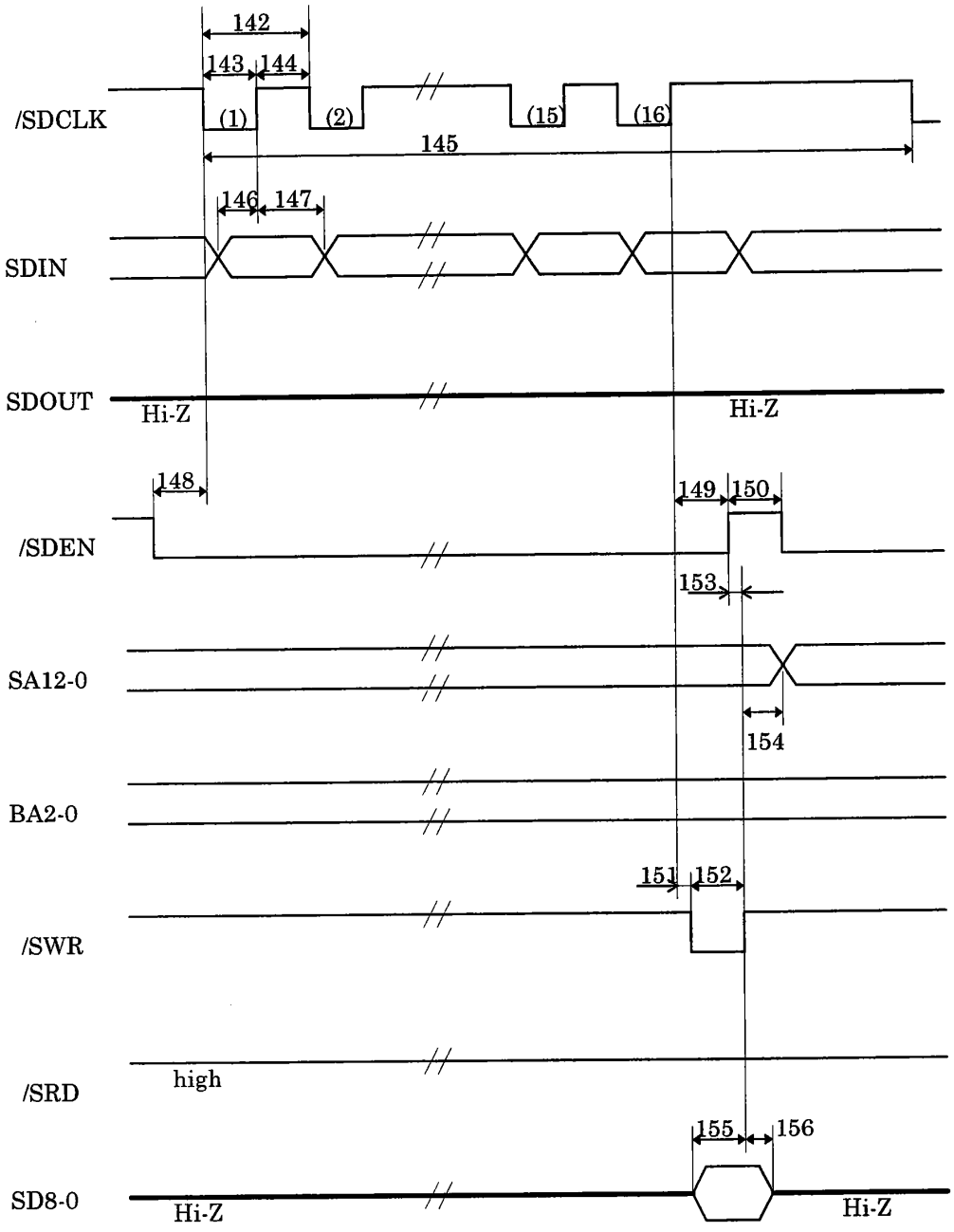


(20) Memory access timing in external access mode (document scanning)



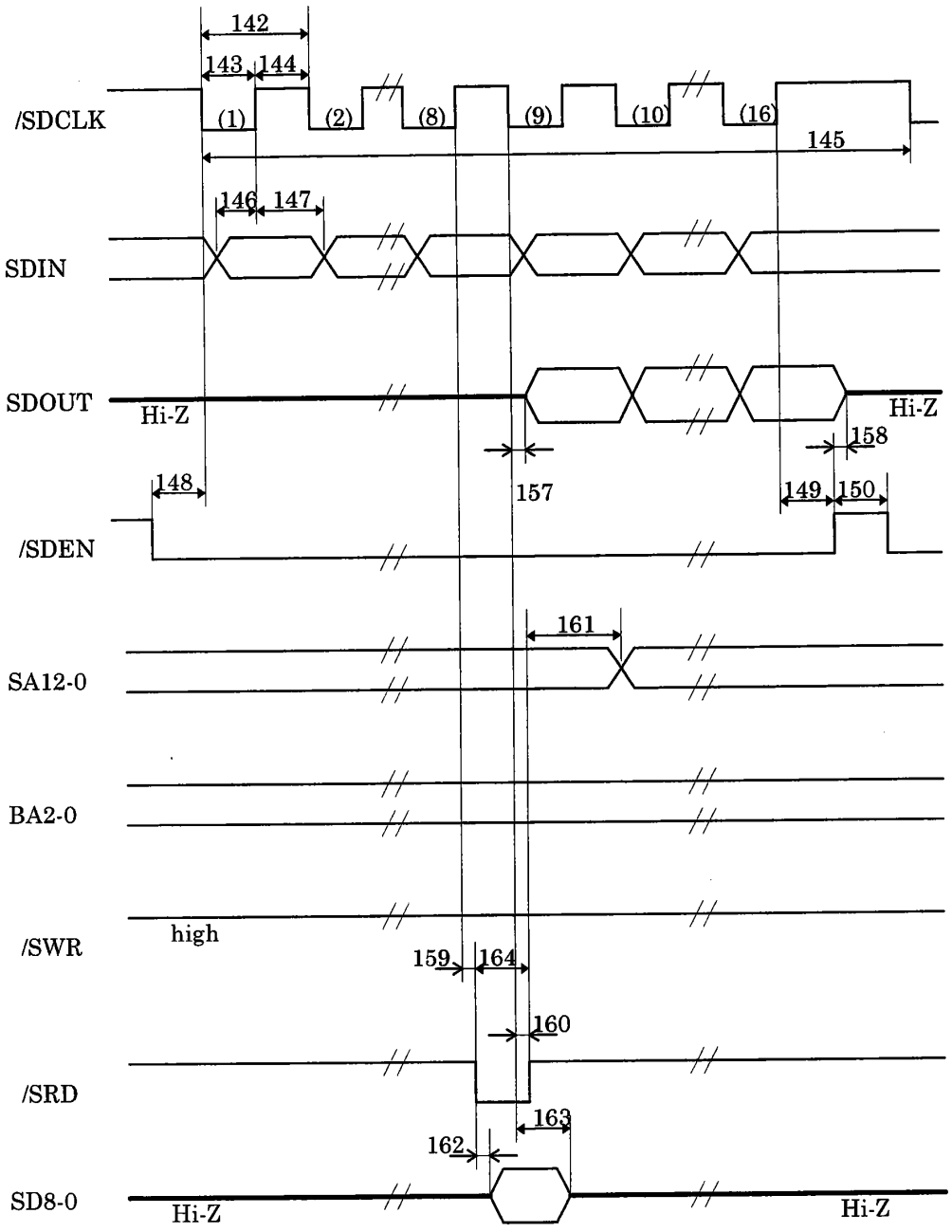
(21) Memory access timing (shading memory access)

1. Data write



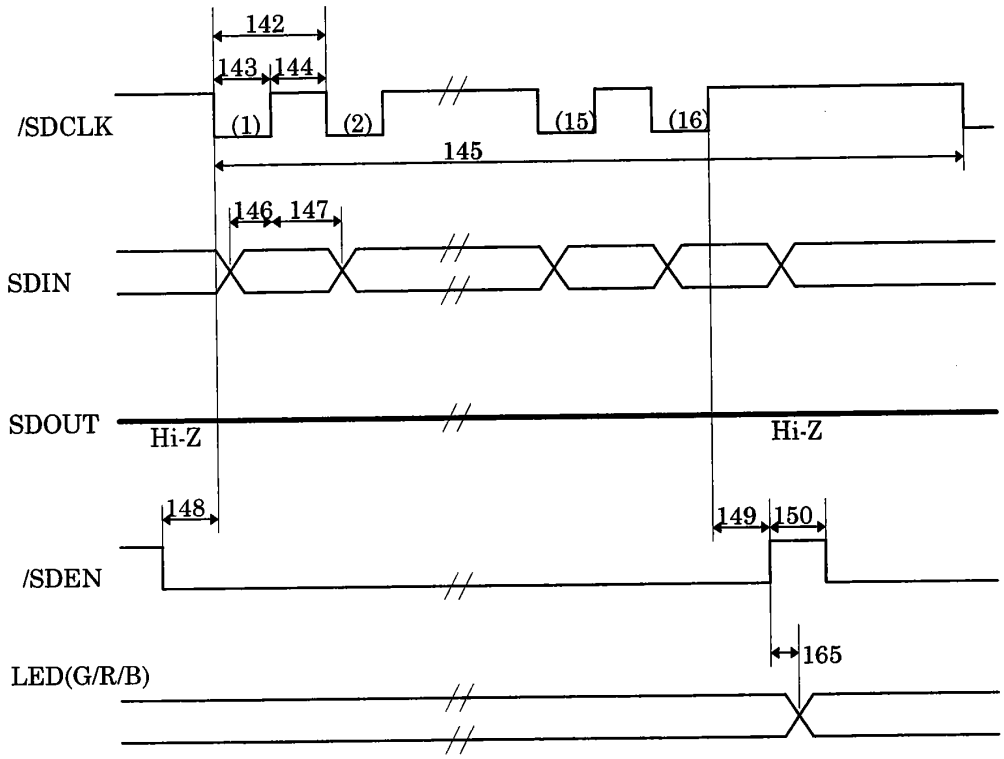
(21) Memory access timing (shading memory access)

2. Data read

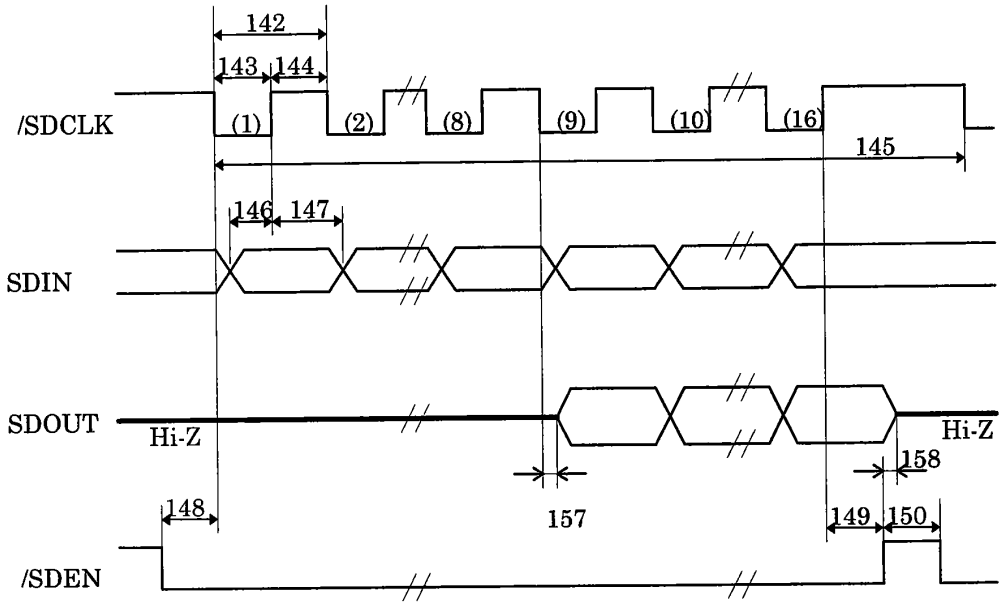


(22) Serial I/F timing

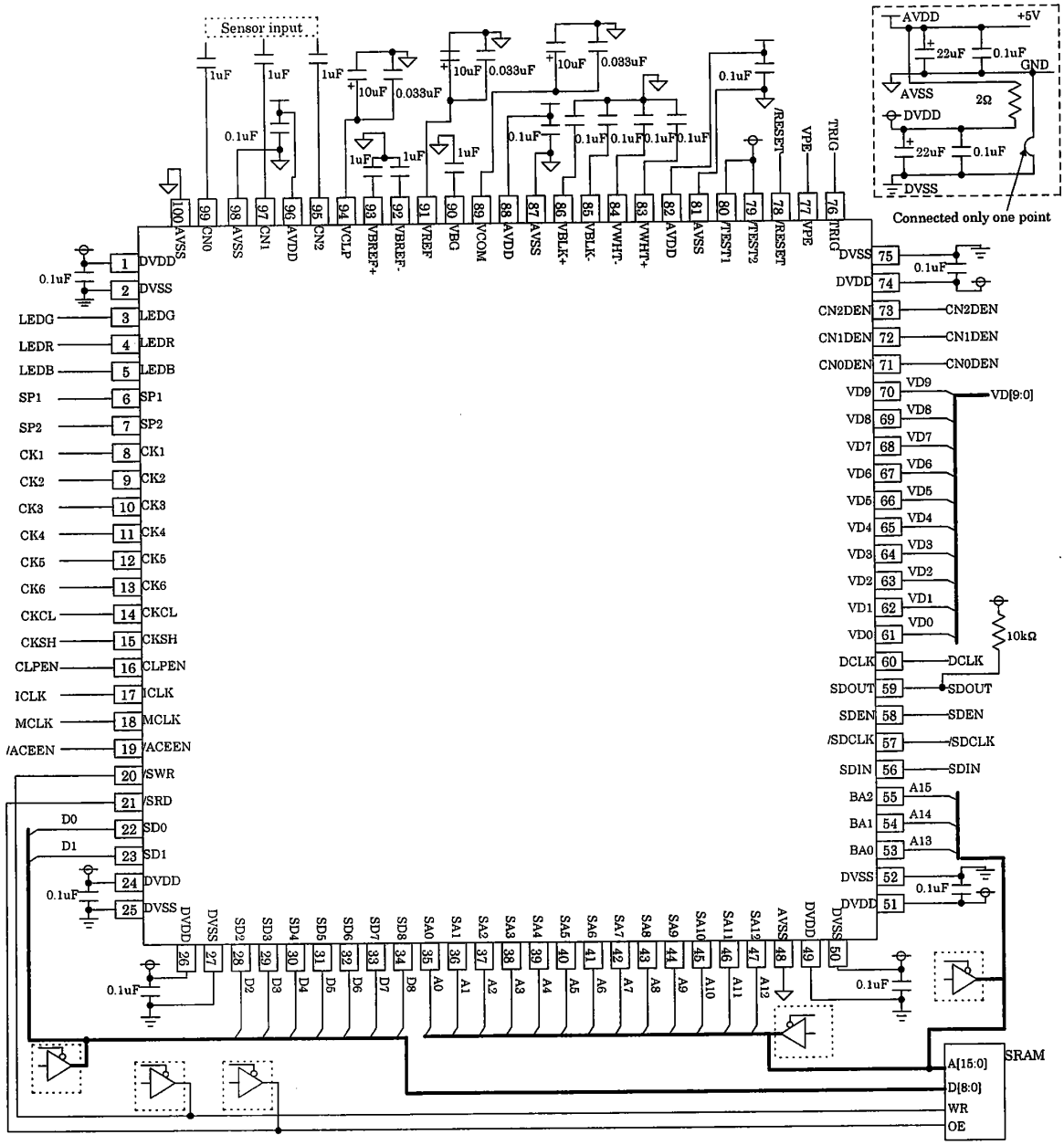
1. Data write



2. Data read


142
143
144
/SDCLK
(1)
(2)
(8)
(9)
(10)
(16)
145
146
147
SDIN
SDOUT
Hi-Z
Hi-Z
158
148
157
149
150
/SDEN

External recommended circuit example



(Note)

(1) When there is the other device than AK8408(ex.CPU) which accesses to SRAM(shading memory),tri-state buffer in above figure is necessary. If there isn't ,the buffer is not necessary.

(2) When bit clamp mode select, capacitor is 0.01uF-0.1uF to connect sensor input.

Package

■Marking

(1) Pin 1 indicated (The chamfered corner indicates pin number 1.)

(2) Date code : XXXXXXX (7 digits)

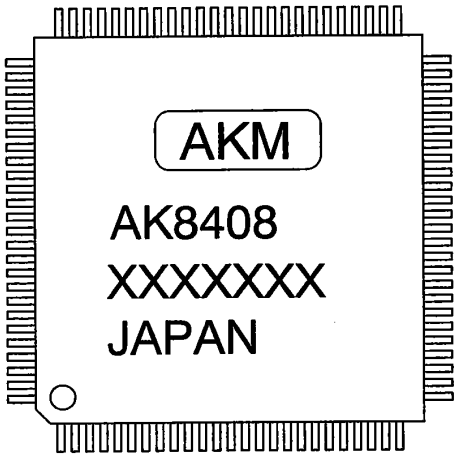
Higher order four digits : week code

Lower order three digits: In-house control code

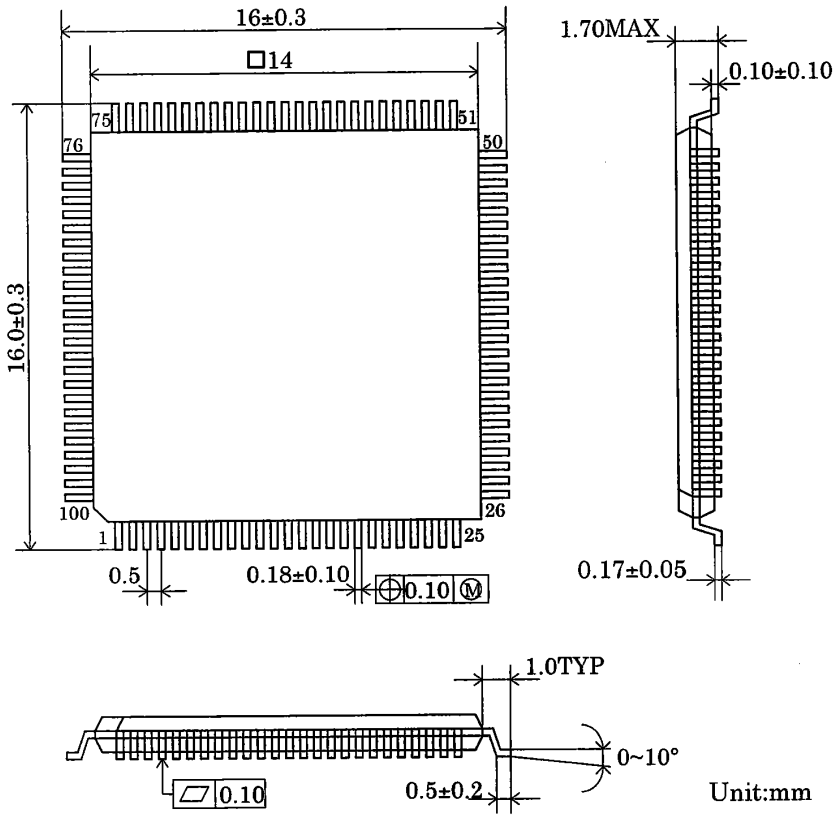
(3) Marking code : AK8408

(4) Manufacturing Country Name Indication : Japan

(5) Asahi Kasei Logo



■Package


16±0.3
□14
1.70MAX
0.10±0.10
75
51
76
50
16.0±0.3
100
26
1
25
0.5
0.18±0.10
0.10 M
0.17±0.05
1.0TYP
0~10°
0.10
0.5±0.2
Unit:mm

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