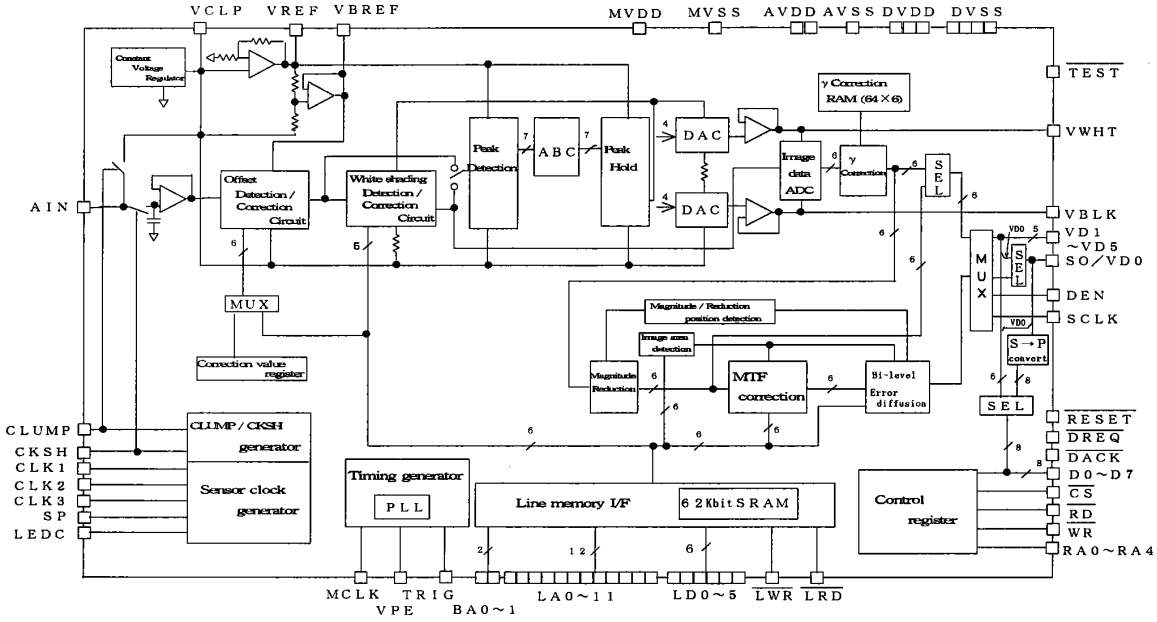
= PRELIMINARY = AK8414

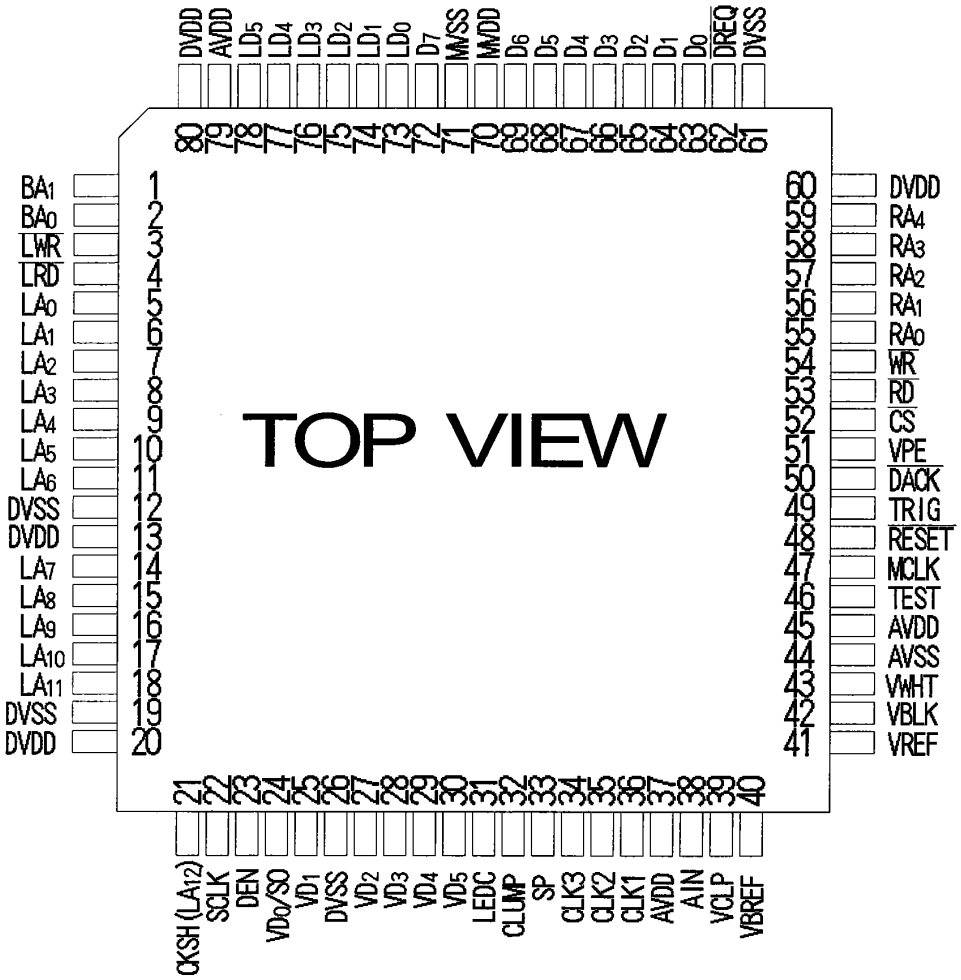
1Chip Image Processing LSI

Features

- ☐Shading correction and Image processing LSI for CCD/CIS sensor
- ☐Input signal level 400mVp-p~1.2Vp-p
- ☐Processing speed max 2Msamples/sec
- ☐Max. sensor length 8192 (programmable by 32pixels/step)
- ☐6bit ADC included (max 64scales)
  Contrast adjustment possible 2×4bit DAC, which are volumes for black reference voltage and for white reference voltage of ADC.
- ☐ADC(detector) and programmable gain amplifier(corrector) for white correction
  Correction 60% range of peak level by 5bit (actual correction resolution is 6bit)
- ☐6bit ADC(detector) and DAC(corrector) for black correction
  Correction resolution 8mV (typ.), correction range -270mV ~ 210mV (typ.)
- ☐ABC function (7bit peak detection/peak hold circuit included)
  Programmable tracking range(black/white limitter)
  ABC mode when binary scale, AGC mode when gray scale
- ☐Image data control function
  Error diffusion (programmable threshold level)
  Image area separation, MTF correction (2 dimension, 3×3 or 3×2)
  Tracking threshold binary coding
  Magnification and reduction (programmable mag/red ratio: 1% step)
- ☐On-chip line-memory (2592×6×4 = 62208 bit)
  Black shading correction data (0 or 1 line) / White shading correction data (1 line) / Error (1 line) / Image processing data (1 or 2 lines)
- ☐On-chip RAMs for γ correction (64×6 bit)
- ☐Sensor clock generation (CCD,CIS)
- ☐Serial output or Parallel output(DMA) are available for video data
- ☐Clock frequency:450KHz~2MHz (data rate), PLL included
- ☐CMOS monolithics LSI, +5V single power supply(5V±5%), Constant voltage regulator included
- ☐80pin LQFP



Pin Assignment



Pin Description

Pin No.	Pin Name	I/O	Function
			Power Supply Pins
13,20,60, 80	DVDD	-	Digital power supply pins (5V typ.)
12,19,26, 61	DVSS	-	Digital VSS pins
70	MVDD	-	Digital power supply pin (5V typ.) for RAM
71	MVSS	-	Digital VSS pin for RAM
37,45,79	AVDD	-	Analog power supply pins (5V typ.)
44	AVSS	-	Analog VSS pin
			Analog Pins
38	AIN	I	Analog input pin. External capacitor for clump is necessary.
39	VCLP	O	Clump voltage(1.3V) buffer output. Black correction is done to be matched to this voltage. External capacitor is necessary.
40	VBREF	O	Reference voltage buffer for black correction.
41	VREF	O	White-side reference voltage(2.6V) buffer output.
42	VBLK	O	Black-side reference voltage buffer output for image data ADC.
43	VWHT	O	White-side reference voltage buffer output for image data ADC.
			Clock and Test Pins
47	MCLK	I	Master clock input. Clock rate is same as the data rate (max 2MHz).
46	(/TEST)	I	Test pin. Pull up to 'H' level.
49	TRIG	I	Line start signal input.
			CCD/CIS Drive Clock Pins
36,35,34	CLK1,CLK2,CLK3	O	Clock output pins for the sensor.
33	SP	O	Shift clock output pin for the sensor.
			Sensor signal input clock Pins
21	CKSH	O	Internal S/H clock output pin. (for monitoring) Sampled by 'H' level and holded by 'L' level.
32	CLUMP	O	Internal clump switch clock output pin. Turned ON by 'H' level and turned OFF by 'L' level.
			Video Data Bus
25,27~30	VD1~VD5	O	6bit image data outputs. VD0 is common to SO.
23	DEN	O	Video data enable signal, which shows data valid period.
24	SO(VD0)	O	Image processed binary data output pin.
22	SCLK	O	Sampling clock output for binary or 6bit data.

Pin No.	Pin Name	I/O	Function
Micro-computer Interface Pins			
52	/CS	I	Chip select signal.
53	/RD	I	Internal register read signal.
54	/WR	I	Internal register write signal.
55~59	RA0~RA4	I	Internal register address bus.
48	/RESET	I	Internal register reset signal. Registers which are reset are shown in the section of "Register Function".
63~69,72	D0~D7	I/O (3state)	System data bus.
62	/DREQ	O	DMA request output pin.
50	/DACK	I	DMA acknowledge input pin.
Line memory Interface Pins (note 1)			
5~11 14~18	LA0~LA11	O	Line memory address pins.
21	(LA12)	O	LA12 is common to CKSH. Setting pixel has over 4096 pixels,21 pin is automatically LA12.
2,1	BA0~BA1	O	Line memory bank select signal.
73~78	LD0~LD5	I/O (3state)	Line memory data bus.
4	/LRD	O	Line memory read signal.
3	/LWR	O	Line memory write signal.
Other Pins			
31	LEDC	O	Peripheral output port for On/Off control of the sensor LED. Cleared by /RESET signal.
51	VPE	I	Processing enable signal which determines whether to do processing the next line, or not.

(note 1) Line memory interface related pins is useful for the sensor, which has over 2,592 pixels.

Function Description

■Analog circuit

□Reference Voltage generator

(1)Clump reference voltage(V_{CLP})is generated by constant voltage regulator

V_{CLP}=1.3V(typ.)

(2)White-side reference voltage(V_{REF})is generated by 2×V_{CLP}.

V_{REF}=V_{CLP}×2=2.6V(typ.)

□Sensor signal input circuit

(1)Polarity of input signal is white upward. If the polarity is inverted such as CCD sensor, input signal should be inverted outside.

(2)Internal analog switch and external capacitor makes up the clump circuit.

(3)Bit-clump and line-clump modes are supported. In the line-clump mode, clump period is determined by (CLPEN). (CLPEN) is programmed by the control register.

□Black distortion detect ADC/correction circuit.

(1)Correction data, which is the difference between the clump level and the signal level of each pixel is detected by 6bit ADC, when the light of sensor is off.

(2)Correction is achieved by subtracting the correction voltage, which is generated by the pre-detected correction data, from analog input signal.

(3)Detection range is 480mV(Typ.). (black side:-270mV , white side:210mV)

□Peak detection/hold circuit

(1)Peak detect circuit is a low speed 7bit ADC.

(2)Peak hold circuit is 7bit DAC.

(3)Input signal into the peak detect circuit is the black shading corrected signal at the peak detect mode, and black and white shading corrected one when ABC/AGC is on at the scanning mode.

□White shading detect ADC/correction circuit

(1)White correction value is detected by 5bit ADC.(Full-scale is 60%(typ.) of the difference between V_{PEAK} and V_{CLP}.)

(2)Correction is achieved to amplify the black corrected analog signal by the pre-detected correction data.

□Reference voltage generator for the video ADC (DAC1,DAC2)

DAC1,DAC2 are 4bit DACs which generate the black and white reference voltage for the ADC, which voltage defined by the programmable relative ratio of the difference between V_{PEAK} and V_{CLP}.

□6bit video ADC

6bit ADC which converts the normalized analog signal finally. Reference voltage is programmable by setting above mentioned DACs.

□PLL

(1)Generate ×16 clock from sensor data rate clock (2MHz max).

(2)It is possible to stop PLL oscillation by register setting.

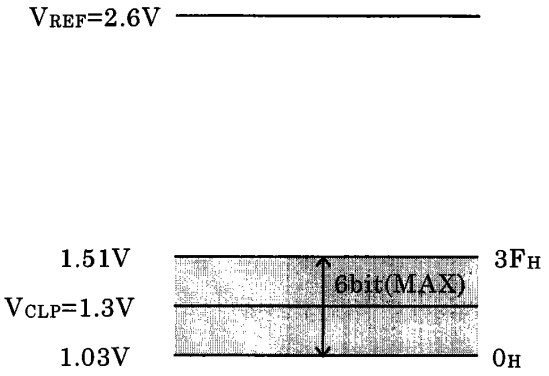


Fig.1-1 Black shading detect/correct

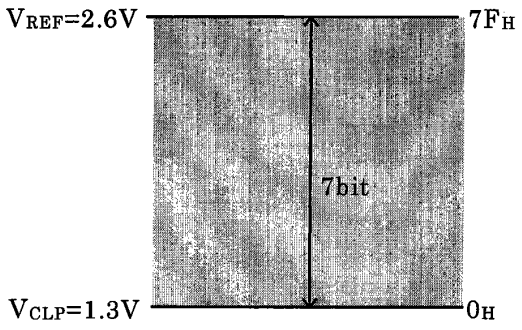


Fig.1-2 Peak detect/hold

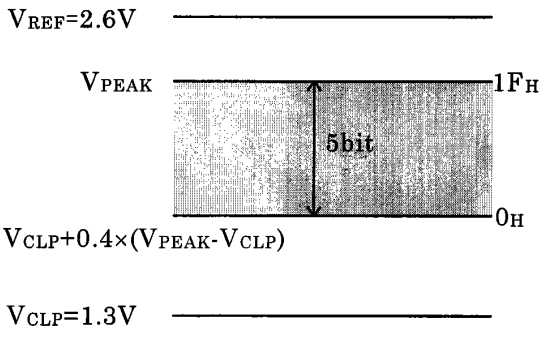


Fig.1-3 White shading detect/correct

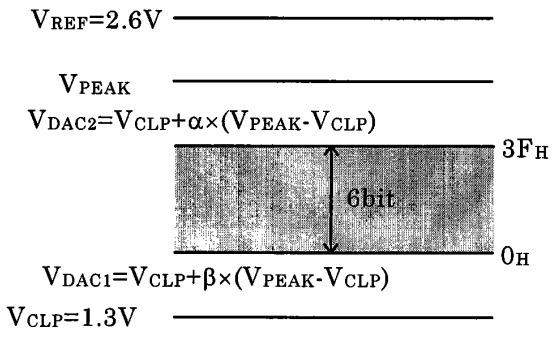


Fig.1-4 Image ADC

**1)V_{DAC1} and V_{DAC2} are the output voltage of DAC1 and DAC2 that generate reference voltage of a 6bit video ADC

■Black shading detect

Analog input includes following error.

(1)Pre-amplifier offset, AK8414 internal switch feed-through, and internal amplifier offset.

(2)Sensor offset and its deviation .

AK8414 supports following correction mode.

(1)Pixel to pixel correction mode (uses internal or external memory, depending on a sensor pixel count).

(2)Fixed offset cancel mode (uses only internal register)

□Pixel to pixel correction mode

Detects the black shading data by 6bit ADC and stores the data into the memory with scanning black reference signal.

If the sensor pixel count is equal or less than 2,592 , internal memory is available. If it's greater than 2,592 , external memory is necessary.

□Fixed offset cancel mode (uses internal register)

Detects the black shading data by 6bit ADC and stores the data into internal register with scanning black reference signal. Before that, the position of the reference pixel for this mode has to be set into the control register.

NOTE:In this mode, a calibration sequence for cancelling offset around the peak-detect and peak-hold circuit automatically starts in parallel, and this value is stored to an internal register.

If this calibration value is cleared because of the equipment's initialization or the equipment's processing sequence (ex. power-down, reset), you have to execute this mode again or re-write the same data into the register.

■Peak detect

This mode is used to prepare the peak value before white shading detect or document scanning,(for the signal amplitude to be matched with the full scale of the white shading detect ADC or the video ADC).
This mode consists of the 2 cycles.

□Peak pre-detect cycle

(1)AK8414 detects the maximum value (PPK) of a video ADC output data to scan the white reference signal, with DAC1, DAC2 and peak hold circuit are set to the full scale. (Internally, analog black correction to the white reference signal is achieved as shown below.)

(Pixel to pixel correction mode)

(black corrected white reference signal)$_i$ =

(white reference signal)$_i$ -A(black shading data)$_i$ ····· (1)

(Fixed offset cancel mode)

(black corrected white reference signal)$_i$ =

(white reference signal)$_i$ -A(BOFF)

Besides, A(D)is an analog value which is DA-converted voltage of D.
BOFF is the contents of a register.

(2)Detect width is the available full length of a sensor.(Register value is ignored.)

□Peak fix cycle

(1)The peak value is fixed by 7bit peak detect circuit with re-scanning the same white reference signal after the initial value around PPK being set to the peak detect counter internally.

(2)Detection width is same as the available full length of a sensor. A limitting function for ABC is automatically inhibited. Following speed is 1LSB per a pixel.

(3)Finishing this cycle, the peak detect counter value is automatically loaded into the peak hold register.

■White shading detect

The purpose of white shading correction is to remove the deviation of the light emission and the sensor sensitivity. Correction value is detected before the scanning.

Black reference of white correction detect use 5bit ADC is automatically set to 40% of V_{PEAK} and white reference is set to V_{PEAK}. Full scale of the ADC is from $0.4 \times V_{PEAK}$ to V_{PEAK}.
The white shading data are detected by a 5bit ADC and are stored into the internal or the external memory, which is depending on the pixel count of sensor, with scanning white reference signal.
(White reference signal is black shading corrected automatically by the pre-stored black shading data.)

■Shading correction in the scanning mode

□Black correction

Gets the black shading corrected video signal by the following way.

(Pixel to pixel correction mode)
(Black corrected video signal)$_i$ =
(Video signal)$_i$-A(Black correction value)$_i$
(Fixed offset cancel correction mode)
(Black corrected video signal)$_i$ =
(Video signal)$_i$-A(BOFF)
Besides, A(D)is an analog value which is DA-converted voltage of D.
BOFF is the contents of a register.

□White correction

Gets black/white shading corrected video signal by the following way.

(Black & White corrected video signal)$_i$ =
(Black corrected video signal)$_i \times 51.7$ /(20.7+(White correction data)$_i$)

■ABC function

The purpose of ABC function is to read clearly regardless groundwork density by following the white reference voltage of a video ADC to the change of groundwork density.
ABC function supports two modes, which are called "ABC mode (for the document with characters)" and "AGC mode (for the document with photograph)".
ABC function are enabled or disabled by the control register, and are also automatically disabled when the VPE(line active)=0 is detected at the start of a line.

□ABC mode

A peak value of video signal which is black and white shading corrected, is detected during ABC enabled period(PHEW). This value should be as the $PEAK_k$.
The peak hold value of the next line (PHD_{k+1}) is determined by comparing the peak value ($PEAK_k$) with the peak hold value of the present line (PHD_k) according to the following equation.

$PEAK_k < PHD_k \rightarrow PHD_{k+1}=PHD_k - f$ [peak value down]
$PEAK_k \geq PHD_k \rightarrow PHD_{k+1}=PEAK_k$ [peak value up]

Peak detect counter starts from reset state(0_H) for the every each line.

ABC range is programmable by black and white limitter registers.
Following speed to the black-side is selectable as shown below.

FSEL	Following speed (f)
0	1 LSB is by 4 LINE (1/4 LSB)
1	1 LSB is by 2 LINE (1/2 LSB)
2	1 LSB is by 1 LINE (1 LSB)
3	2 LSB is by 1 LINE (2 LSB)

ABC following speed to the black-side

□AGC mode

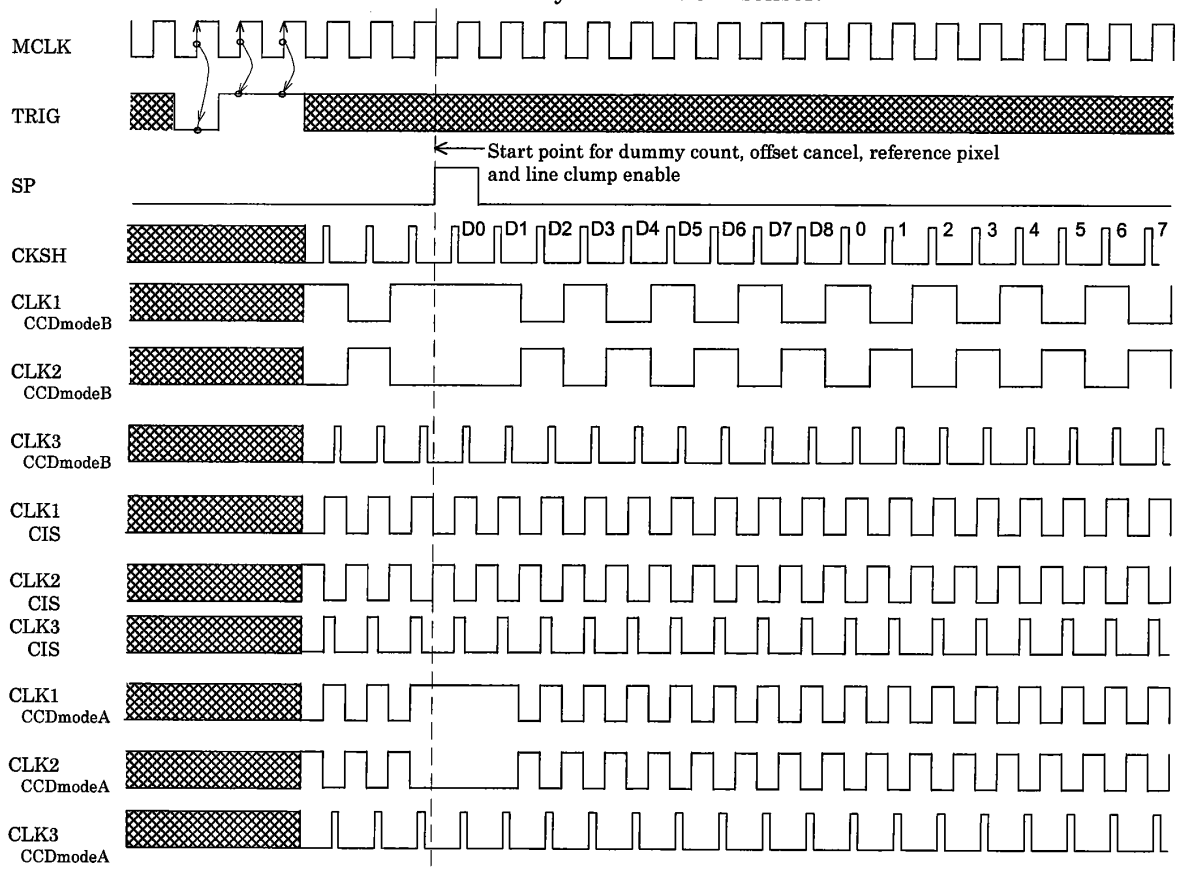
In AGC mode, peak value is determined by the following equations.

$PEAK_k < PHD_k \rightarrow PHD_{k+1}=PHD_k$ [peak value hold]
$PEAK_k \geq PHD_k \rightarrow PHD_{k+1}=PEAK_k$ [peak value up]

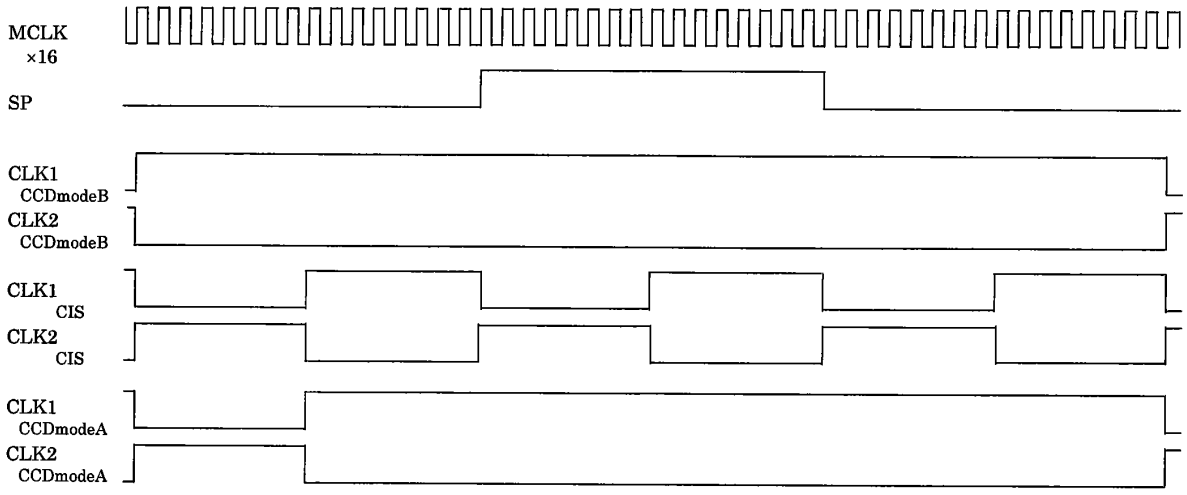
AGC range is programmable by a white limitter register.

■Sensor clocks generator

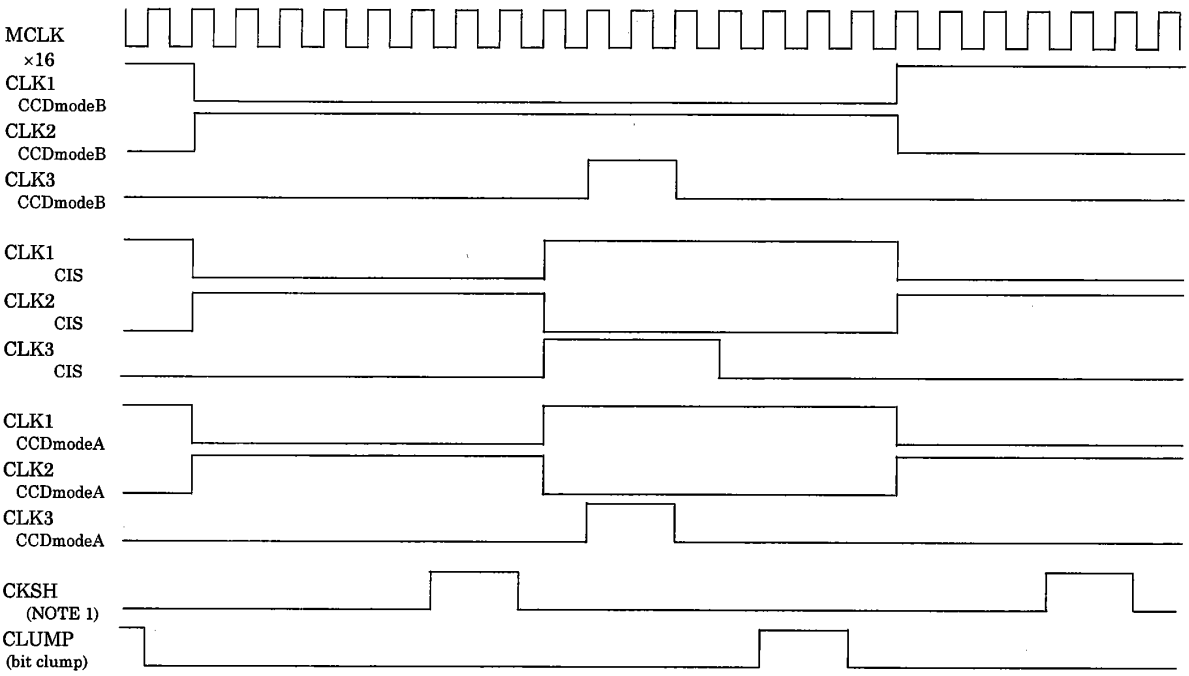
AK8414 supports three types of clock generation mode, which are called as "CCD MODE A", "CCD MODE B" and "CIS MODE" for every CIS or CCD sensor.



Detail timing for the above (A)



Detail timing for the above (B)



(NOTE 1)CLUMP clock is generated by logical "and" between CKSH and CLPEN(clump enable) in line clump mode B.
CLUMP clock is the same as CLPEN in line clump mode A.

■Timing control signals generator

AK8414 generates following 5 signals for timing control internally.

1.(EN)	:Input video signal enable
2.(PWEN)	:ABC enable
3.(CLPEN)	:Line clump enable
4.(BOFFEN)	:Black reference pixel enable
5. DEN	:Output data enable

□Input video signal enable (EN)

This is the video signal enable width in a line, which is determined by dummy pixel count and pixel count register.

□ABC enable (PWEN)

This signal is the ABC enable width in a line when scanning mode.
Start pixel and end pixel can be set by each every 256 pixels by the control registers.

□Line clump enable (CLPEN)

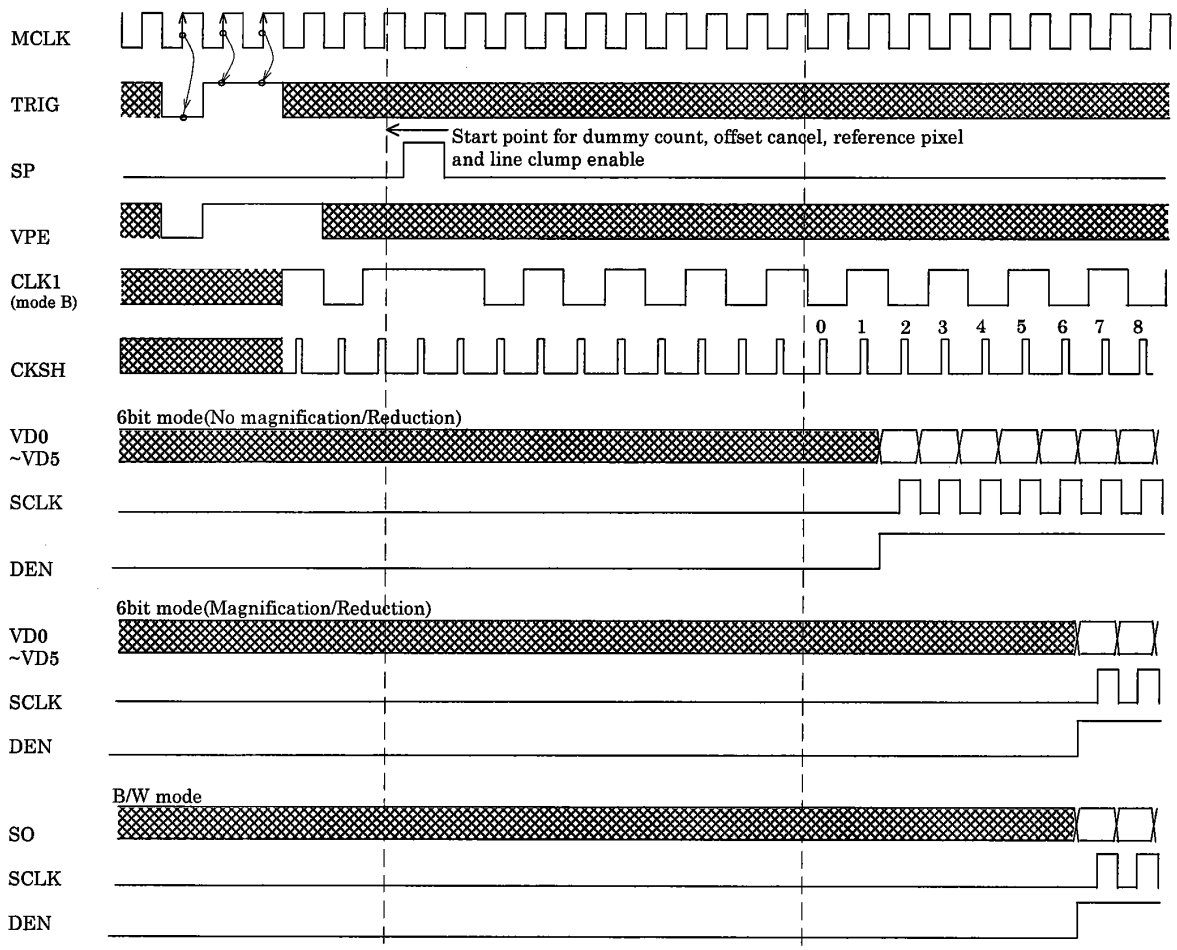
This signal is the clump enable width in a line in the line clump mode, which can be set by every 1 pixel by the control register.
It should be set in dummy pixels.

□Black reference pixel enable (BOFFEN)

This signal is used to determine the black reference pixel when offset cancel mode, which can be set by every 16 pixels by control register.
It can be set either in the dummy pixels or the effective pixels.

□Output data enable DEN

This signal shows the data valid period in a line.
This signal becomes active only at the lines, which is indicated as an enabled line by VPE=1.
VPE is sampled at the beginning of the line.


MCLK
TRIG
Start point for dummy count, offset cancel, reference pixel
and line clump enable
SP
VPE
CLK1
(mode B)
0 1 2 3 4 5 6 7 8
CKSH
6bit mode(No magnification/Reduction)
VD0
~VD5
SCLK
DEN
6bit mode(Magnification/Reduction)
VD0
~VD5
SCLK
DEN
B/W mode
SO
SCLK
DEN

■CLUMP signal control

In line clump mode, AK8414 is able to control the clump signal falling and rising edge timing by register setting. Relationship among MCLK,TRIG,CKSH,SP and CLUMP signals shows below figure A and B.

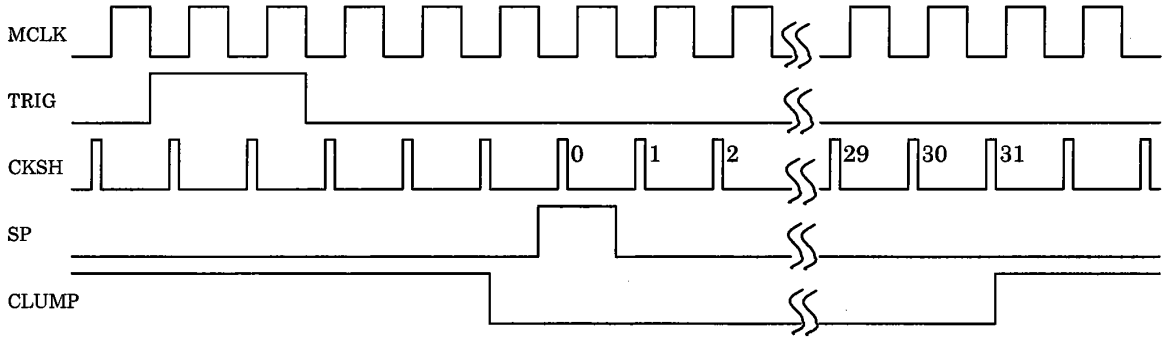


Figure A: The clump signal falling and rising edge timing
Sensor pixel count is 32.
Dummy pixel count is 0.
Line clump enable 1 setting is 0.
Line clump enable 2 setting is 0.

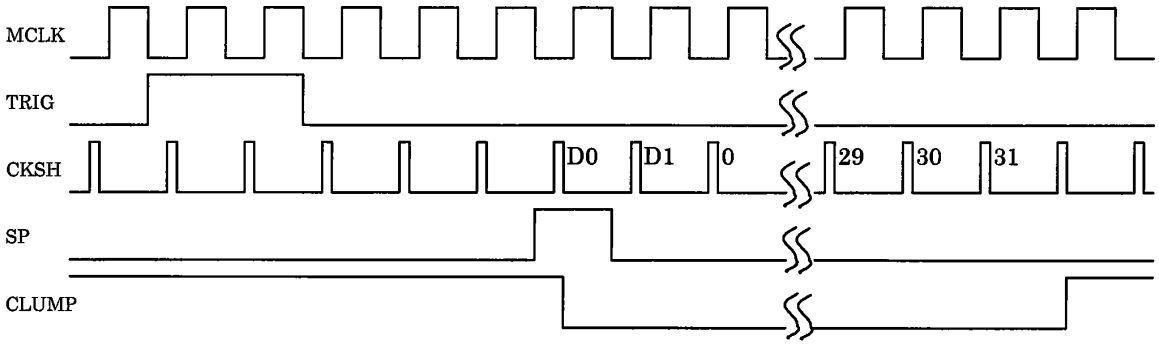


Figure B: The clump signal falling and rising edge timing
Sensor pixel count is 32.
Dummy pixel count is 2.
Line clump enable 1 setting is 1.
Line clump enable 2 setting is 1.

Compared to figure A,
the clump signal falling edge timing is delayed for (line clump enable 1) clocks.
the clump signal rising edge timing is delayed for (line clump enable 2) clocks.
The clump signal should be set to fall in dummy pixels.

■Image processing

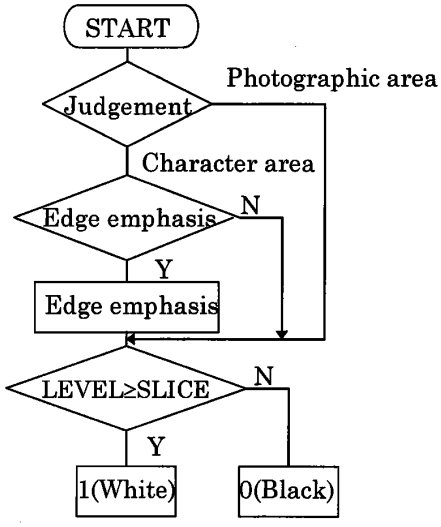
□Image processing mode

AK8414 supports 3 types of image processing mode. Each image processing mode is shown in the following flow chart.

(1)Bi-level processing

Character area is by bi-level processing(with edge emphasis), and photographic area is by simple bi-level processing(without edge emphasis).

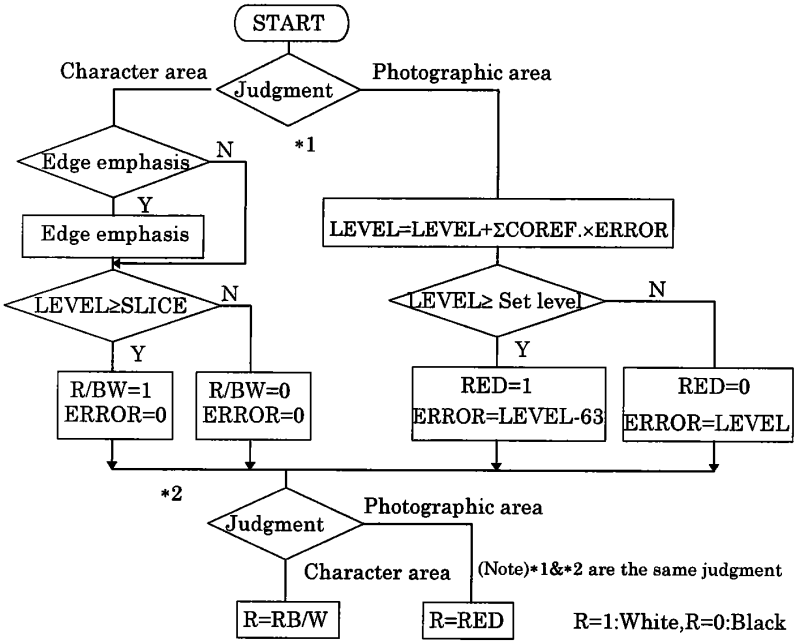
Enable of edge emphasis for character area is set by a control register.



SLICE is determined by the automatically changing level following to the background density.

(2)Error diffusion A

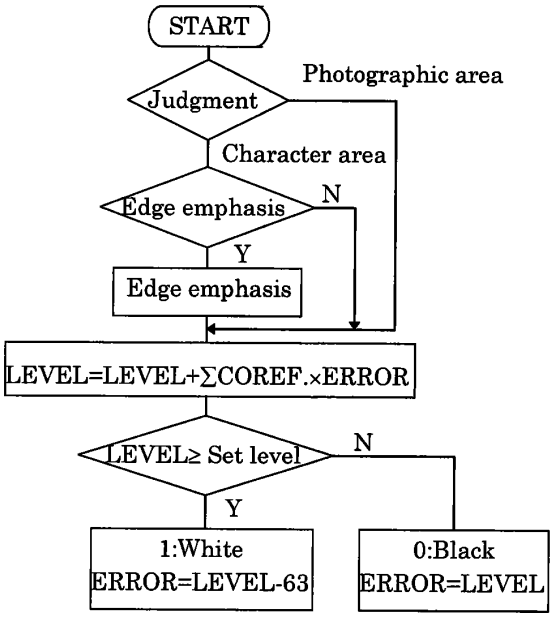
Character area is by bi-level processing, and photographic area is processed by error diffusion. Enable of edge emphasis for character area is set by a control register.



(3)Error diffusion B

All area is by error diffusion.

Edge emphasis for character area is set by a control register.



(4)Line memory for the image processing

AK8414 has 4 banks of on-chip line memory (2,592×4×6=62,208bits).
If the sensor pixel count equals or less than 2,592, an external line memory is not necessary. Otherwise, an external line memory is necessary, which AK8414 controls. The contents of this memory is as the below table, depending on the image processing mode or other conditions.

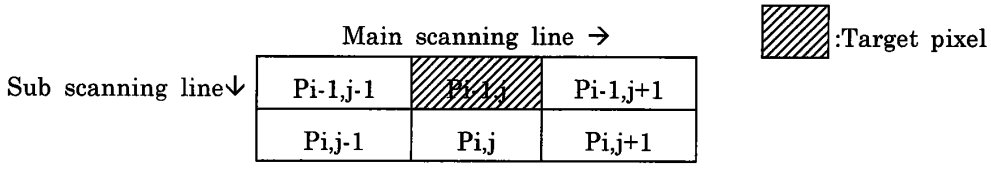
	Image processing mode	Image processing window	Black shading correction	Contents
Bank0	Bi-level	X	X	Black shading data
	Error diffusion	3×2	X	Black shading data
		3×3	Pixel to pixel	Black shading data
			offset cancel	6bit image data for the line before the previous one
Bank1	X	X	X	6bit image data for the previous line
Bank2	X	X	X	White shading data
Bank3	Bi-level	X	X	6bit image data for the line before the previous one
	Error diffusion	X	X	Error data

As shown in the above table, when pixel to pixel type black correction, and error diffusion 3×3 window is selected at the same time, the black correction mode set is superior than the window set. As that result, when these parameters are set, image processing window is automatically set to 3×2, and the contents of the bank0 memory should be the black shading data.

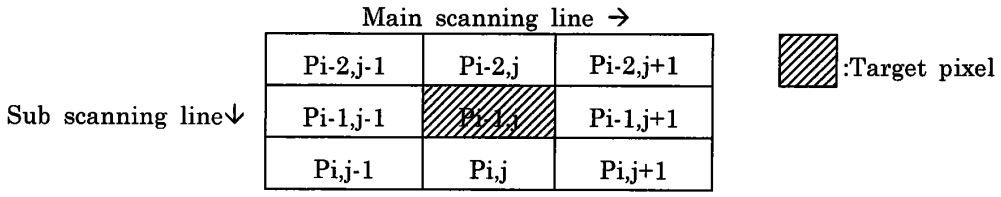
□Photographic area judgment

Photographic area judgment is performed by comparing target pixel level, and differential component between target pixel level and surrounding pixels' one (3×2 or 3×3 window) with the each threshold parameter.
Three parameters can be set by the control registers.

(1)3×2 window



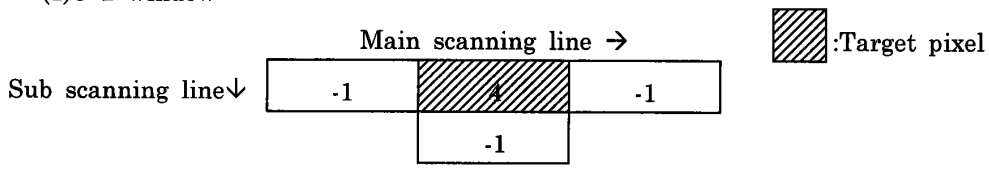
(2)3×3 window



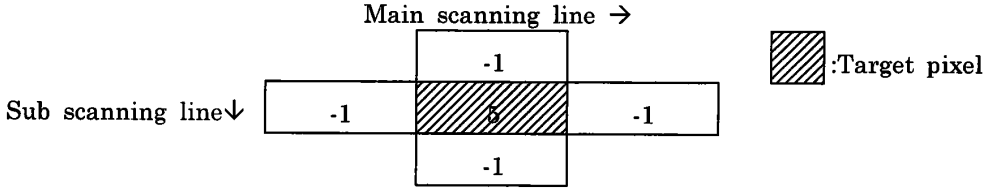
□MTF correction

MTF correction is performed by the following window.
Coefficients and window are fixed.

(1)3×2 window



(2)3×3 window



□Error diffusion

AK8414 executes error diffusion according to the window and coefficients shown below and threshold which is set register.

Main scanning line →

Sub scanning line↓

A1=1	A2=2	A3=4	A4=2	A5=1	*:Target pixel
A6=2	A7=4	*			

$$\tilde{P}*=P+1/16\times\Sigma(Ai\times ERRi)$$

SLED: Threshold

Target pixel level ≥ SLED White : 1

ERR* = ~P* - 63

Target pixel level < SLED Black : 0

ERR* = ~P*

ERR*, ERRi: signed 7bit data

SLED: 24,28,32,36,40,44,48,52 (Selectable)

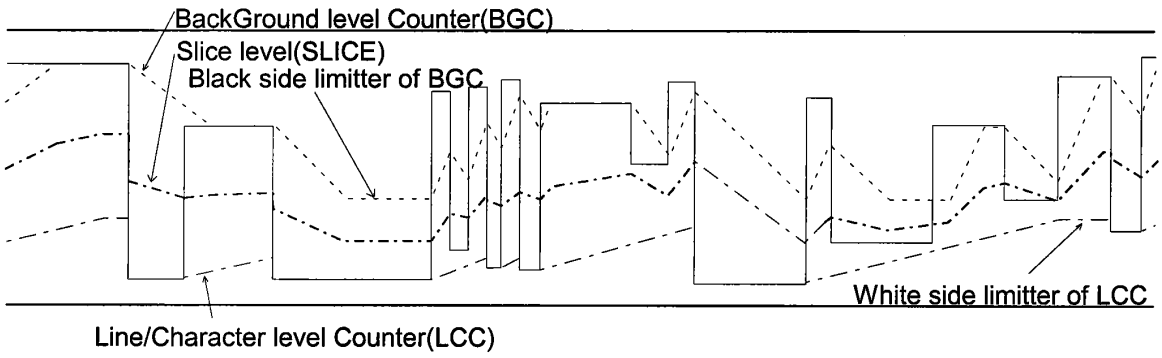
NOTE :In case of the pixel is judged as white background, black background or character, ERR*=0.

□Automatical changing slice-level function

AK8414 uses the windows shown in below(3×3 or 3×2) and controls BGC(BackGround level Counter) and LCC(Line/Character level Counter) for this function.
A general idea is shown the below figure.
The BGC is updated by the maximum value among pixels in the window pixel by pixel, and the LCC is updated by minimum value among pixels in the window pixel by pixel.
As a result, slice level is automatically updated by BGC contents and LCC contents pixel by pixel. There are two limitters(Black side / White side), which restrict the following range to be programmed by registers.

Pi-1,j-1	Pi-1,j	Pi-1,j+1
Pi,j-1	Pi,j	Pi,j+1

Pi-2,j-1	Pi-2,j	Pi-2,j+1
Pi-1,j-1	Pi-1,j	Pi-1,j+1
Pi,j-1	Pi,j	Pi,j+1



□γ correction

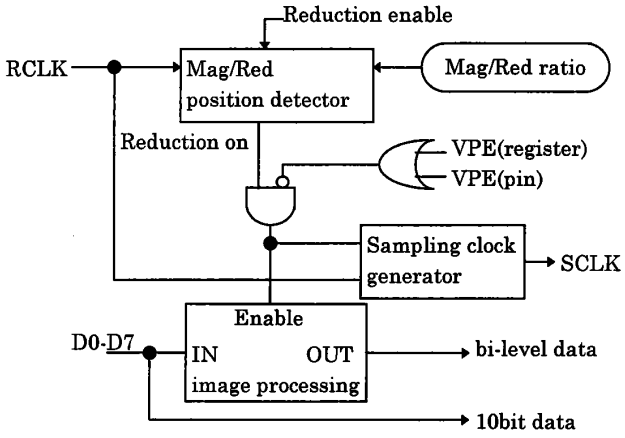
AK8414 performs γ correction by setting data into the internal RAM.

(Example)

Input data (address)	RAM table	Output data (γ correction)
0	0	0
1	0	0
2	1	1
3	1	1
62	63	63
63	63	63

□Magnification/Reduction

AK8414 supports reduction from 1% to 99% (1% step) and magnification 101% to 200% (1% step). In case of reduction mode, image processing is done similarly to that 6bit video data is reduced before binary processing. And in case of magnification mode, binary processed data output twice.
In reduction mode, image processing enable/disable is controlled by magnification/ reduction position detector. At the position which is judged as a reduction point, image processing is automatically disabled.
In magnification mode, 6bit or bi-level data output twice when judged magnification position. Magnification/reduction position detector works for the left end pixel of line not to be lost.



■Output data format

□Serial output

AK8414 outputs 6bit data through VD bus(VD0 ~ VD5) and bi-level data through SO pin. in both case, basic sampling clock is SCLK. In the reduction mode, some portion of SCLK are skipped, and in the magnification mode, some clocks are inserted.
MCLK also can be used as the sampling clock only in the cases without reduction/ magnification.

□Parallel output (DMA interface)

AK8414 supports DMA interface. Both of 6bit data or bi-level data which is set to a 8bit parallel data, is able to be read through the system bus(D0~D7).
When DMA controller receives AK8414 /DREQ signal, it can read out that data by /DACK = L and /RD = L.

□SCLK, /DREQ

In case of serial / parallel interface, SCLK and /DREQ clock count are shown below.

(1)Without magnification / reduction
N: pixel number (multiple of 32)

$n_{SCLK} = n_{DREQ}(6) = N$
$n_{DREQ}(2) = N / 8$

(2)With magnification / reduction
N: pixel number (multiple of 32)
K: Magnification / Reduction ratio
[M]: Minimum integer which are not smaller than M

$n_{SCLK} = n_{DREQ}(6) = [N \times K]$
$n_{DREQ}(2) = [[N \times K] / 8]$

(Example 1) N = 1728 , K = 0.71
$n_{SCLK} = n_{DREQ}(6) = [1728 \times 0.71] = [1266.88] = 1267$
$n_{DREQ}(2) = [[1728 \times 0.71] / 8] = [[1266.88] / 8]$
$= [1267 / 8] = [158.375] = 159$

(Example 2) N = 1728 , K = 1.15
$n_{SCLK} = n_{DREQ}(6) = [1728 \times 1.15] = [1987.2] = 1988$
$n_{DREQ}(2) = [[1728 \times 1.15] / 8] = [[1987.2] / 8]$
$= [1988 / 8] = [248.5] = 249$

In case of bi-level parallel interface, the last data which falls short of 8bit is filled by '0'.
Please note that in the magnification mode, SCLK and /DREQ clock rate becomes faster. For example, in case of magnification ratio is 200%, SCLK and /DREQ clock rate becomes twice.

■Operation control

□Pre-processing stage

Before scanning the document, it is needed to detect shading data of the image sensor. Basic operation sequence of the pre-processing stage is

(1) Initial parameters set
(2) Black shading detect
(3) Peak detect
(4) White shading detect

After these operations are finished, shading data or peak value are stored in the internal/ external RAM or in the internal register.

When executing each pre-processing mode, set OPERATION MODE bits and OPERATION ENABLE bit. These command becomes valid at the first TRIG after it is issued.
Waiting defined time, and check BUSY flag to confirm that executing each processing mode is finished. The OPERATION ENABLE bit is automatically cleared, and AK8414 goes to idle state.
Necessary time for black shading detection and, for white shading detection it is 1 line time, and for peak detection it is 2 line time.

□Scanning stage

In the scanning mode, set VIDEO PROCESSING ENABLE bit or VPE pin, and PAGE START bit to 'H' level, in addition to OPERATION ENABLE bit and OPERATION MODE bits.

Command becomes valid at the first TRIG after it is issued. After scanned 2 lines, PAGE START bit is automatically cleared. Image data and sampling clock(SCLK), DMA request (/DREQ) begins to output.
Because of 1 line output delay for image processing, the extra 1 line image processing is necessary to send out all data.

Reduction of sub-scan axis should be done by skipping line, or paper feed speed control etc. externally. In the case of skipping line method, reset VIDEO PROCESSING ENABLE bit or VPE pin into 'L' level at the line start.

□Line memory access

It is possible to access internal RAM (γ correction table RAM) or internal/external line memory through AK8414. In this mode, reset VIDEO PROCESSING ENABLE bit and VPE pin to 'L' level, and set LINE MEMORY ACCESS ENABLE bit to 'L' level, and after that, to 'H' level.
After that, you can read/write line memory through the window register sequentially.
Bank select of black/white shading data, image data for the previous line, image data for the line before the previous one, and error data, can be set by control registers.

Register

Address (HEX)	init.	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	00h	W (R)	Operation Enable (BUSY)	Page start	LEDC	Video Proc.Ena (VPE)	Memory Access Enable	ABC Enable	Operation Enable	
1	04h	W	Mag./ Reduct. Enable	Memory Mode	BCC, LCC Enable	PLL Clock Stop	ABC Time Constant		White Limitter Enable	ABC Mode
2	04h	W	X	γ Correct. Enable	MTF Correct. Enable	Image Processing Mode		Slice Level		
3	00h	W	X	Output Data Polarity	Image Proc. Window	Bi-level / 6bit Select	Black Correct. Type	RAM Bank Select		
4	40h	W	Error Diffusion Threshold			Clump Mode	Sensor Clock Select 2	SP clock Polarity Select	Line Clump Pulse	Sensor Clock Select 1
			ERRS2	ERRS1	ERRS0					
5	XXh	W	ABC White side limitter				ABC Black side limitter			
			AWL3	AWL2	AWL1	AWL0	ABL3	ABL2	ABL1	ABL0
6	XXh	W	X	X	X	Photographic Area Separation Param.(lower)				
						PBL4	PBL3	PBL2	PBL1	PBL0
7	XXh	W	X	X	X	Photographic Area Separation Param.(upper)				
						PWL4	PWL3	PWL2	PWL1	PWL0
8	XXh	W	X	X	X	Photographic Area Separation Param.(differ)				
						PD4	PD3	PD2	PD1	PD0
9	XXh	W	Magnification / Reduction Ratio							
			RED7	RED6	RED5	RED4	RED3	RED2	RED1	RED0
A	00h	W	X	Line Clump Enable 1						
				CLPA6	CLPA5	CLPA4	CLPA3	CLPA2	CLPA1	CLPA0
B	00h	W	X	Line Clump Enable 2						
				CLPB6	CLPB5	CLPB4	CLPB3	CLPB2	CLPB1	CLPB0
C	XXh	R	X	Peak Detection Counter Monitor						
				PEAK6	PEAK5	PEAK4	PEAK3	PEAK2	PEAK1	PEAK0
D	40h	R/W	X	Peak Hold Data						
				PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
E	00h	W	White Reference Voltage				Black Reference Voltage			
			VWHT3	VWHT2	VWHT1	VWHT0	VBLK3	VBLK2	VBLK1	VBLK0
F	XXh	W	Sensor Pixel Count							
			PIX7	PIX6	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
10	XXh	W	X	Dummy Pixel Count						
				DUM6	DUM5	DUM4	DUM3	DUM2	DUM1	DUM0
11	XXh	W	Peak Detection Width (end)				Peak Detection Width (start)			
			PKE3	PKE2	PKE1	PKE0	PKS3	PKS2	PKS1	PKS0
12	XXh	R/W	X	X	Access widow					
					WIN5	WIN4	WIN3	WIN2	WIN1	WIN0

Address (HEX)	init.	R/W	D7	D6	D5	D4	D3	D2	D1	D0
13	00h	R/W	Offset cancel ref. Pixel			Peak detection circuit calibration value				
			REF2	REF1	REF0	PCAL4	PCAL3	PCAL2	PCAL1	PCAL0
14	00h	R/W	X	X	Offset Correction					
					OF5	OF4	OF3	OF2	OF1	OF0
15	2Ah	W	X	BGC Down Speed		LCC Up Speed			BGC Up Speed	
16	24h	W	X	X	BGC Black Side Limitter					
17	1Ch	W	X	X	LCC White Side Limitter					
18	XXh	W	DEN start position (for windowing the picture)							
			CUTS7	CUTS6	CUTS5	CUTS4	CUTS3	CUTS2	CUTS1	CUTS0
19	XXh	W	DEN end position (for windowing the picture)							
			CUTE7	CUTE6	CUTE5	CUTE4	CUTE3	CUTE2	CUTE1	CUTE0

DMA register	XXh	R	Image signal data							
			0	0	VD5	VD4	VD3	VD2	VD1	VD0
			VD_{N-7}	VD_{N-6}	VD_{N-5}	VD_{N-4}	VD_{N-3}	VD_{N-2}	VD_{N-1}	VD_N

1. ☐ is reset by /RESET

2. ▒ is enabled by the first TRIG↑ after the data/command being written.

3. R14 register cannot be accessed during the execution of the black shading detect mode.

4. RC register cannot be accessed during the execution of the peak detect and the white shading detect modes. The accessible period during the scanning mode is limited from 5 clocks after DEN↓ till the next TRIG↑.
   Generally, RD register read is recommended for the peak value read.

5. RD register cannot be accessed during the execution of the peak detect and the white shading detect modes.
   Set value of this register becomes valid after DEN↓.
   Be careful that this register must be set to 40H before the execution of the black shading detect mode.

6. RE register(D0~D3) contents is valid unless the new data is written.
   But the DAC output changes according to this value by the operation enable(R0/D7) and scanning mode(R0/D0~D1) set.

7. When reading internal/external RAM through R12 register, one dummy read cycle before reading the valid data is necessary.

(1)R0 register

1.D0~D1 : Operation mode

D1	D0	
0	0	: Scanning mode (after reset)
0	1	: Black shading mode
1	0	: White shading mode
1	1	: Peak detect mode

When R0/D7=1, operation will start in the first TRIG↑ after the command is issued.

2.D2 : ABC enable

0 : ABC disable (after reset)
1 : ABC enable

When R0/D7=1, operation will start in the first TRIG↑ after the command is issued.

3.D3 : Memory access enable

It is possible to access sequentially to the line memory (internal or external) which selected by R3/D0~D2. In this mode, R0/D7 must be disabled.

0 : Disable (after reset)
1 : Enable

4.D4 : Video processing enable

0 : Disable (after reset)
1 : Enable

This register has the same function as the VPE pin.

5.D5 : LEDC port control

0 : LEDC = 0 (after reset)
1 : LEDC = 1

6.D6 : Page start

0 : Normal operation (after reset)
1 : Page start

7.D7 : Operation Enable (Read possible)

0 : Disable (after reset)
1 : Enable

(2)R1 register

1.D0 : ABC mode

0 : ABC mode (after reset)
1 : AGC mode

2.D1 : White side limitter enable

ABC white side limitter is enabled by this register.
0 : Disable (after reset)
1 : Enable

3.D2~D3 : ABC time constant

D3	D2	
0	0	: 1/4 LSB
0	1	: 1/2 LSB (after reset)
1	0	: 1 LSB
1	1	: 2 LSB

4.D4 : PLL clock enable

This register enables the PLL operation.
0 : On (after reset)
1 : Off

5.D5 : Automatical changing slice-level function(BGC,LCC) enable

This register enable Automatical changing slice-level function(BGC and LCC counter).
0 : Disable (after reset)
1 : Enable

6.D6 : Memory mode
This register select internal line memory or external line memory.
0 : Internal (after reset)
1 : External

7.D7 : Magnification/Reduction enable

0 : Disable (after reset)
1 : Enable

(3) R2 register

1.D0~D2 : Slice level

Relationship between set value(N) and actual slice level of Ns is shown below.

$$Ns = LCC + N / 8 \times (BGC - LCC)$$

Besides,
Ns : Bi-level slice level
N : Parameter (N=1~7 , after reset N=4)
BGC : BackGround level Counter
LCC : Line/Character level Counter

In case of R1/D6=0 or after reset, BGC and LCC are automatically set. (BGC=48 , LCC=16)

2.D3~D4 : Image processing mode

D4	D3	Image processing mode
0	X	Bi-level (after reset)
1	0	Error diffusion A mode (char:bi-level , photo:error diff)
1	1	Error diffusion B mode (error diffusion)

MTF correction enable for character area is enabled by R2/D5.

3.D5 : MTF correction enable

0 : Disable (after reset)
1 : Enable

4.D6 : γ correction enable

0 : Disable (after reset)
1 : Enable

(4)R3 register

1.D0~D2 : RAM bank select

Line mem/ RAM	R3/ D2	R3/ D1	R3/ D0	R2/ D4	R3/ D5	R3/ D3	Contents	BA1	BA0
Line Memory	0	0	0	0	X	X	Black shading data	0	0
				1	0	X	Black shading data		
					1	0	Black shading data		
						1	Image data for the line before the previous one		
		0	1	X	X	X	Image data for the previous line	0	1
		1	0	X	X	X	White shading data	1	0
		1	1	0	X	X	Image data for the line before the previous one	1	1
				1	X	X	Error data		
	1	X	X	X	X	X	γ correction table	-	-

In case of line memory access mode, it is possible to control BA0~BA1 addresses directly. Note that the accessible RAM bank is changed according to the image processing mode.
Internal γ correction table is able to be accessed sequentially in ADC code upwards orders. (N=0,1,···,63)
Note that in this case, one dummy read cycle is necessary.

2.D3 : Black correction type

0 : All pixel mode (after reset)
1 : Offset cancel mode

3.D4 : Bi-level data / 6bit data select

0 : Bi-level mode (after reset)
1 : 6bit mode

4.D5 : Image processing window

0 : 3×2 (after reset)
1 : 3×3

5.D6 : Output data polarity

0 : Bi-level data(0:Black , 1:White), 6bit data(0:Black → 3FH:White) (after reset)
1 : Bi-level data(0:White , 1:Black), 6bit data(0:White → 3FH:Black)

(5)R4 register

1.D0 : Sensor clock select 1

0 : CIS mode (after reset)
1 : CCD mode

2.D1 : Line clump pulse select

0 : Mode A (after reset)
1 : Mode B
This bit is effective when R4/D4=0.

3.D2 : SP clock porality select

0 : Active high (after reset)
1 : Active low

4.D3 : Sensor clock select 2

Sensor clock rate can be selected in CCD mode (R4/D0=1).
0 : Mode A (after reset) Data rate
1 : Mode B Data rate / 2

5.D4 :Clump mode

0 : Line clump (after reset)
1 : Bit clump

6.D5~D7 : Error diffusion threshold

D7	D6	D5		
0	0	0	: 24	
0	0	1	: 28	
0	1	0	: 32	(after reset)
0	1	1	: 36	
1	0	0	: 40	
1	0	1	: 44	
1	1	0	: 48	
1	1	1	: 52	

(6)R5 register

1.D0~D3 : ABC black side limitter

Relationship between set value(N) and actual limitter value of N_{LB} is shown below.
$N_{LB}=8\times N$ (N=0~15)

2.D4~D7 : ABC white side limitter

Relationship between set value(N) and actual limitter value of N_{LW} is shown below.
$N_{LW}=8\times N+7$ (N=0~15) > N_{LB}

(7)R6 register

1.D0~D4 : Photographic area separation parameter (lower)

Relationship between set value(N) and actual parameter (N_{PB}) is shown below.
$N_{PB}=N$ (N=0~31)
If the concerning pixel level is less than N_{PB}, this pixel is judged as black background.

(8)R7 register

1.D0~D4 : Photographic area separation parameter (upper)

Relationship between set value(N) and actual parameter (N_{PW}) is shown below.
$N_{PW}=N+32$ (N=0~31)
If the concerning pixel level is more than N_{PW}, this pixel is judged as white background.

(9)R8 register

1.D0~D4 : Photographic area separation parameter (differential)

Relationship between set value(N) and actual parameter (N_{PD}) is shown below.
$N_{PD}=N$ (N=0~31)
If at least one difference component among all of the differences with surrounding cells is more than N_{PD}, this pixel is judged as character area.

(10)R9 register

1.D0~D7 : Magnification/Reduction ratio set (1/100 ~ 200/100)

Set numerator value in magnification/reduction mode.

(11)RA register

1.D0~D6 : Line clump enable 1

Set line clump enable falling edge timing in line clump mode.
Relationship between set value(N) and actual falling edge CLP (CLP↓) is shown below.
CLP↓ = N (N=0~127, after reset N=0)

(12)RB register

1.D0~D6 : Line clump enable 2

Set line clump enable rising edge timing in line clump mode.
Relationship between set value (N) and actual rising edge CLP (CLP↑) is shown below.
CLP↑ = N + (pixel number + dummy pixel number) (N=0~127, after reset N=0)

(13)RC register

1.D0~D7 : Peak detection counter monitor register

It is possible to read peak detection counter value.

(14)RD register

1.D0~D6 : Peak hold data

The present peak value can be read, and a new value can be re-write through this register.

(15)RE register

1.D0~D3 : Black reference voltage
2.D4~D7 : White reference voltage

Set white reference voltage(VWHT) and black reference voltage(VBLK).
Resolution is 0.25/15 of (V_{PEAK}-V_{CLP}), and actual value of coefficient(α,β) is as the below table. VWHT and VBLK are calculated by the following way.
These set values are available in read mode.

V_{WHT} = V_{CLP} (1.3V typ.) + α× (V_{PEAK}-V_{CLP})
V_{BLK} = V_{CLP} (1.3V typ.) + β× (V_{PEAK}-V_{CLP})
V_{CLP} : Clump Voltage, V_{PEAK}: Signal peak voltage

Set Value	α	β
0	1.000	0.000
1	0.983	0.017
2	0.967	0.033
3	0.950	0.050
4	0.933	0.067
5	0.917	0.083
6	0.900	0.100
7	0.883	0.117
8	0.867	0.133
9	0.850	0.150
A	0.833	0.167
B	0.817	0.183
C	0.800	0.200
D	0.783	0.217
E	0.767	0.233
F	0.750	0.250

(16)RF register

1.D0~D7 : Sensor pixel count

Set available sensor pixel count by 32 pixel unit. It doesn't include dummy pixel.
Maximum value is 8192 pixel.
Relationship between set value(N) and available pixel number(S) is shown below.

$S = 32 \times (N + 1)$ (N = 0 ~ 255)

(17)R10 register

1.D0~D6 : Dummy pixel count

Set pre-dummy pixel count of sensor by 1 pixel unit.
Relationship between set value(N) and actual dummy pixel count(D) is shown below.

$D = N$ (N = 0 ~ 127)

(18)R11 register

1.D0~D3 : Peak detection width set (START)

Set peak detection width(PHEW). Starting pixel position is set by 256 pixel unit. It doesn't include dummy pixel.
Relationship between set value(N) and actual starting pixel position(PS) is shown below.

if pixel count < 4096 PS = 256 × N (N = 0 ~ 15)
if pixel count ≥ 4096 PS = 512 × N (N = 0 ~ 15)

2.D4~D7 : Peak detection width set (END)

Set peak detection width(PHEW). Ending pixel position is set by 256 pixel unit. It doesn't include dummy pixel.
Relationship between set value(N) and actual ending pixel position(PE) is shown below.

if pixel count < 4096 S ≥ PE = 256 × (N + 1) > PS (N = 0 ~ 15)
if pixel count ≥ 4096 S ≥ PE = 512 × (N + 1) > PS (N = 0 ~ 15)

(19)R12 register

1.D0~D5 : Line memory / internal RAM access window

It is possible to access to line memory or internal RAM through this register.

(20)R13 register

1.D0~D4 : Peak detection circuit calibration value

After black shading detect, the offset calibration value for peak detection related circuit is stored to this register.
It is possible to read/write this register.

2.D5~D7 : Offset cancel reference pixel

In case of offset cancel mode in black shading detect, set reference pixel to take correction data. It is possible to set by 16pixels unit.
Relationship between set value(N) and actual reference pixel position(B) is shown below.

B = 16 × (N + 1) (N = 0 ~ 7)

As it is counted by an another counter from the dummy pixel counter, the reference pixel ca n be set in the dummy pixels or the effective pixels.

(21)R14 register

1.D0~D5 : Offset correction

In case of the offset cancel mode, black correction data which is correspond with the reference pixel is stored after executing the black distortion detection mode.

(22)R15 register

1.D0~D1 : BGC up speed

Set BackGround Counter (BGC) up speed.

D1	D0	
0	0	: 1/2LSB
0	1	: 1LSB
1	0	: 2LSB (after reset)
1	1	: 4LSB

2.D2~D4 : LCC up speed

Set Line/Character Counter (LCC) up speed.

D4	D3	D2	
0	0	0	: 1/4LSB
0	0	1	: 1/2LSB
0	1	0	: 1LSB (after reset)
0	1	1	: 2LSB
1	X	X	: 4LSB

3.D5~D6 : BGC down speed

Set background counter (BGC) down speed.

D6	D5	
0	0	: 1/4LSB
0	1	: 1/2LSB (after reset)
1	0	: 1LSB
1	1	: 2LSB

(23)R16 register

1.D0~D5 : BGC black side limitter (after reset BGC=24H)

(24)R17 register

1.D0~D5 : LCC white side limitter (after reset LCC=1CH)

(25) R18 register

1.D0~D7 : DEN start position (for windowing the picture)

Set the left end position of the capturing picture.
It is possible to set by 16 pixels unit.
Relationship between set value(N) and actual start pixel position(S) is shown below.

if pixel count < 4096 $S = 16 \times N$ (N = 0 ~ 255)
if pixel count ≥ 4096 $S = 32 \times N$ (N = 0 ~ 255)

(26) R19 register

1.D0~D7 : DEN end position (for windowing the picture)

Set the right end position of the capturing picture.
It is possible to set by 16 pixels unit.
Relationship between set value(N) and actual end pixel position(E) is shown below.

if pixel count < 4096 $E = 16 \times N$ (N = 0 ~ 255)
if pixel count ≥ 4096 $E = 32 \times N$ (N = 0 ~ 255)

(27)DMA register

In case of getting image processed data through system bus, read this register.
In case of binary mode, the oldest data is stored in MSB and the latest data is stored in LSB. 6bit data is able to be read through this register too.
It is needed to use DMA controller in 1-byte transfer mode.

Absolute maximum ratings

Parameters	Sym	min.	max.	Unit	Remarks
Supply voltage					VA≥VD,VA
Digital	VD	-0.3	6.5	V	must rise up
Analog	VA	-0.3	6.5	V	faster than VD.
Digital applied voltage	V_{TD}	-0.3	VD+0.3	V	
Analog applied voltage	V_{TA}	-0.3	VA+0.3	V	
Storage Temperature	T_{STG}	-55	125	°C	
Soldering Temperature and time	T_{SOL}	260°C,10sec		-	

All voltage defined to their corresponding ground: AVSS,DVSS=0V

Recommended operating Conditions

Parameters	Sym	min.	typ.	max.	Unit	Remarks
Supply voltage						
Digital	VD	4.75	5.0	5.25	V	
Analog	VA	4.75	5.0	5.25	V	
Operating Temperature	Ta	0		70	°C	

All voltage defined to their corresponding ground: AVSS,DVSS=0V

Electrical specifications

■DC Characteristics

(Unless otherwise specified,VD,VA=5V±5%,Ta=0~70°C)

Parameters	Sym	Pins	min.	typ.	max.	Unit	Conditions
Supply current Digital (include RAM) Analog	 ID IA				 65 30	 mA mA	 MCLK=2.0MHz No load
High level Input Voltage	V_{IH}	Input I/O	2.6	-	-	V	
Low level Input Voltage	V_{IL}		-	-	0.8	V	
High level Output Voltage	V_{OH}	Output I/O	4.0			V	I_{OH}=-1mA
Low level Output Voltage	V_{OL}				0.4	V	I_{OL}=4mA
Leakage current	I_L	Input I/O	-10		10	μA	V_I=DVDD V_I=DVSS

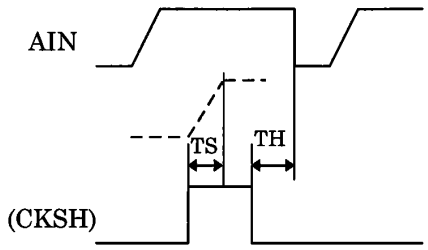
■Analog characteristics

(Unless otherwise specified,VD,VA=5V±5%,Ta=0~70°C)

Parameters	Sym	min.	typ.	max.	Unit	Remarks
Analog input						
Maximum signal input level	V_{MAX}	1.2	1.3	1.4	V_{p-p}	AIN
Sampling rate	S_{FRQ}			2.0	M_{pix}/S	AIN
Input registance	R_{IN}		1		MΩ	AIN
Input capacitance	C_{IN}		20		pF	AIN
Voltage reference						
Clump voltage	V_{CLP}		1.3		V	AIN
VREF voltage	V_{REF}		2.6		V	VREF
Black shading detect/correction circuit						
Minimum range	RG_{BC}	V_{CLP}-230		V_{CLP}+190	mV	
Resolution	RL_{BC}		8		mV	
Correction accuracy	AC_{BC}			±3	LSB	Video ADC equivalent V_{WHT}-V_{BLK}=0.8V MCLK=2.0MHz
Peak detect/hold circuit						
Maximum detect voltage	V_{MAX}	1.2	1.3	1.4	V	High voltage side than V_{CLP} is positive
Resolution	RSL		7		BIT	
Peak hold settling time	T1			1.0	mS	64LSB changing C_L=1μF
	T2			100	μS	2LSB changing C_L=1μF

(Unless otherwise specified,VD,VA=5V±5%,Ta=0~70°C)

Parameters	Sym	min.	typ.	max.	Unit	Remarks
Clump circuit						
Switch ON resistance	R_{ON}			60	Ω	AIN=1.35V include OP-amp impedance
Sample hold circuit						
Analog input settling time	T_S			30	nS	0.1%
Analog input hold time	T_H			0	nS	
White shading detect/correction circuit						
Resolution	RSL		5		bit	
Correction range	RNG		60		%	Ratio to (V_{PEAK}-V_{CLP})
Correction accuracy	ACR			±4	LSB	Scanning ADC equivalent V_{WHT}-V_{BLK}=1.2V
DACs for reference voltage generation of scanning use ADC						
Voltage accuracy	ACR			±1	%	
ADC for scanning						
Resolution	RSL		6		bit	No code missing V_{WHT}-V_{BLK}=0.8V



■Digital AC Specifications

(Unless otherwise specified,VD,VA=5V±5%,Ta=70°C)

No.	Parameters	Pins	min.	typ.	max.	Unit	Condition
1	MCLK cycle Time(T)	MCLK	500		2222	nS	
2	MCLK High level width	MCLK	30%		70%	T	
3	MCLK Low level width	MCLK	30%		70%	T	
4	TRIG set up time (to MCLK↑)	TRIG	20			nS	
5	TRIG hold time (to MCLK↑)	TRIG	20			nS	
6	VPE set up time (to MCLK↑)	VPE	20			nS	(Note)
7	VPE hold time (to MCLK↑)	VPE	5T/32 +20			nS	(Note)
8	/RESET pulse width	/RESET	20			nS	
9	CLK1↑,CLK2↑ delay time (MODE B) (to MCLK↑)	CLK1 CLK2			T/2 +30	nS	C=20pF
10	CLK1↓,CLK2↓ delay time (MODE B) (to MCLK↑)	CLK1 CLK2			T/2 +30	nS	C=20pF
11	CLK1,CLK2 High level width (MODE B)	CLK1 CLK2		1		T	
12	CLK1,CLK2 Low level width (MODE B)	CLK1 CLK2		1		T	
13	CLK1,CLK2 cycle time (MODE B)	CLK1 CLK2		2		T	
14	CLK3↑ delay time (MODE A,B) (to MCLK↑)	CLK3			T/16 +25	nS	C=20pF
15	CLK3 High level width (MODE A,B)	CLK3		1/8		T	
16	CLK3 Low level width (MODE A,B)	CLK3		7/8		T	
17	CLK3 cycle time (MODE A,B)	CLK3		1		T	
18	SP↑ delay time (to MCLK↑)	SP			T/2 +30	nS	C=20pF
19	SP↓ delay time (to MCLK↑)	SP			T/2 +30	nS	C=20pF
20	SP pulse width	SP		1		T	
21	(CKSH) delay time (to MCLK↑)	(CKSH)			27T/32 +25	nS	C=20pF
22	(CKSH) High level width	(CKSH)		1/8		T	
23	(CKSH) Low level width	(CKSH)		7/8		T	
24	(CKSH) cycle time	(CKSH)		1		T	
25	CLUMP delay time (to MCLK↑)	CLUMP			T/16 +25	nS	C=20pF
26	CLUMP High level width	CLUMP		1/8		T	
27	CLUMP Low level width	CLUMP		7/8		T	
28	CLUMP cycle time	CLUMP		1		T	
29	CLK1 delay time (MODE A,CIS)(to MCLK↑)	CLK1			30	nS	C=20pF

(Note) One for 2nd. MCLK after TRIG enabled

(Unless otherwise specified,VD,VA=5V±5%,Ta=70°C)

No.	Parameter	Pins	min.	typ.	max.	Unit	Condition
30	CLK1,CLK2 High level width (MODE A,CIS)	CLK1 CLK2		1/2		T	
31	CLK1,CLK2 Low level width (MODE A,CIS)	CLK1 CLK2		1/2		T	
32	CLK1,CLK2 cycle time (MODE A,CIS)	CLK1 CLK2		1		T	
33	CLK2↑ delay time (MODE A,CIS)(to MCLK↑)	CLK2			30	nS	C=20pF
34	CLK3 delay time (MODECIS) (to MCLK↑)	CLK3			25	nS	C=20pF
35	CLK3 High level width (MODE CIS)	CLK3		1/4		T	
36	CLK3 Low level width (MODE CIS)	CLK3		3/4		T	
37	CLK3 cycle time (MODECIS)	CLK3		1		T	
38	CLK3↑ delay time (CIS) (to MCLK↑)	CLK3	T/32 -5			nS	C=20pF
39	VD5~0 delay time (to MCLK↑)	VD5~0			11T/32 +33	nS	C=20pF
40	SO,VD5~0 set up time (to MCLK↑)	SO, VD5~0	T/2-15			nS	C=20pF,Normal
			T/4-10			nS	C=20pF, Magnification
41	SO,VD5~0 hold time (to MCLK↑)	SO, VD5~0	T/2-5			nS	C=20pF, Normal
			T/4-10			nS	C=20pF, Magnification
42	SO delay time (to MCLK↑)	SO			11T/32 +30	nS	C=20pF
43	SCLK delay time (to MCLK↑)	SCLK			27T/32 +25	nS	C=20pF, Normal
					3T/32 +25	nS	C=20pF, Magnification
44	SCLK High level width	SCLK		1/2		T	Normal
				1/4		T	Magnification
45	SCLK Low level width	SCLK		1/2		T	Normal
				1/4		T	Magnification
46	SCLK cycle time	SCLK		1		T	Normal
				1/2		T	Magnification
47	DEN delay time	DEN			11T/32 +25	nS	C=20pF
48	DEN set up time (to SCLK↑)	DEN	T/2-10			nS	C=20pF,Normal
			T/4-10			nS	C=20pF, Magnification
49	DEN hold time (to SCLK↑)	DEN	T/2-10			nS	C=20pF,Normal
			T/4-10			nS	C=20pF, Magnification
50	LA12~0 set up time (to /LWR↓)	LA12~0	T/16 -13			nS	C=20pF
51	LA12~0 hold time (to /LWR↑)	LA12~0	0			nS	C=20pF

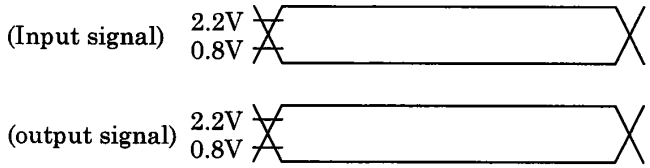
(Unless otherwise specified,VD,VA=5V±5%,Ta=70°C)

No.	Parameters	Pins	min.	typ.	max.	Unit	Condition
52	BA1~0 set up time (to /LWR↓)	BA1~0	T/16 -13			nS	C=20pF
53	BA1~0 hold time (to /LWR↑)	BA1~0	0			nS	C=20pF
54	/LWR minimum cycle time	/LWR		1/8		T	C=20pF
55	/LWR pulse width	/LWR		1/16		T	C=20pF
56	LD5~0 set up time (to /LWR↑)	LD5~0	T/16-5			nS	C=20pF
57	LD5~0 hold time (to /LWR↑)	LD5~0	0			nS	C=20pF
58	LD5~0 acceptable delay time (to LA12~0)	LD5~0			T/8-27	nS	C=20pF
59	LD5~0 acceptable delay time (to BA1~0)	LD5~0			T/8-27	nS	C=20pF
60	LA12~0 hold time (to /LRD↑)	LA12~0	0			nS	C=20pF
61	BA1~0 hold time (to /LRD↑)	BA1~0	0			nS	C=20pF
62	LD5~0 acceptable delay time (to /LRD↓)	LD5~0			T/8-27	nS	C=20pF
63	/LRD pulse width	/LRD		1/8		T	
64	/LRD minimum cycle time	/LRD		1/8		T	
65	LD5~0 hold time (to /LRD↑)	LD5~0	0			nS	C=20pF
66	LD5~0→Hi-Z acceptable delay time				T/16-5	nS	C=20pF
67	/CS set up time (to /WR↓)	/CS	20			nS	
68	/CS hold time (to /WR↑)	/CS	0			nS	
69	RA4~0 set up time (to /WR↓)	RA4~0	20			nS	
70	RA4~0 hold time (to /WR↑)	RA4~0	0			nS	
71	/WR Low level width	/WR	20			nS	
72	/WR minimum cycle time	/WR	1			T	
73	D7~0 acceptable delay time (to /WR↓)	D7~0			5T/16 -20	T	
74	D7~0 set up time (to /WR↑)	D7~0	20			nS	
75	D7~0 hold time (to /WR↑)	D7~0	0			nS	
76	/LWR↓ delay time (to /WR↓)	/LWR			25	nS	C=20pF
77	/LWR↑ delay time (to /WR↑)	/LWR			25	nS	C=20pF
78	LD5~0 active delay time (to /WR↓)	LD5~0			25	nS	C=20pF
79	LD5~0 delay time (to D5~0)	LD5~0			25	nS	C=20pF

(Unless otherwise specified,VD,VA=5V±5%,Ta=70°C)

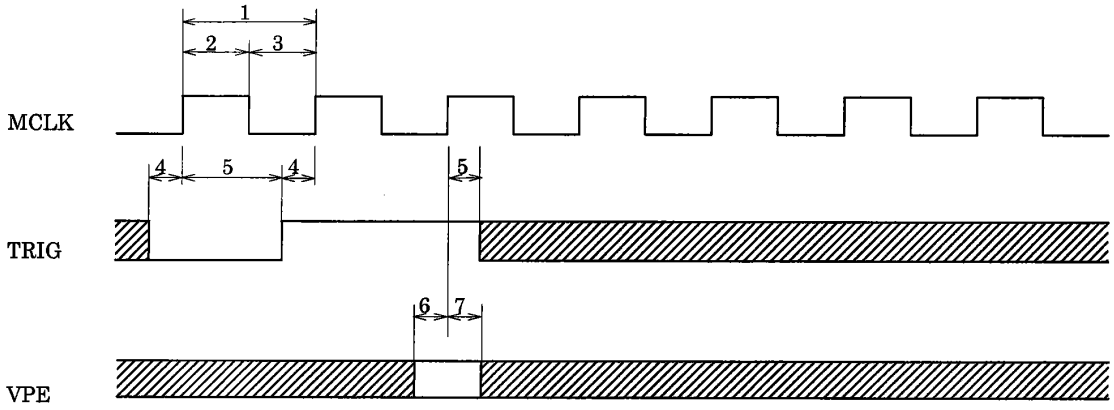
No.	Parameters	Pins	min.	typ.	max.	Unit	Condition
80	LD5~0 hold time (to /LWR↑)	LD5~0	0			nS	C=20pF
81	LA12~0 hold time (to /LWR↑)	LA12~0	0			nS	C=20pF
82	/RD Low level width	/RD	20			nS	
83	/RD minimum cycle time	/RD	1			T	
84	LA12~0 hold time (to /RD↓)	D7~0			30	nS	C=50pF
85	D7~0 hold time (to /RD↑)	D7~0	0			nS	C=50pF
86	D7~0 delay time (to LD5~0)	D7~0			30	nS	C=50pF
87	/LRD↓ delay time (to /RD↓)	/LRD			25	nS	C=20pF
88	/LRD↑ delay time (to /RD↑)	/LRD			25	nS	C=20pF
89	LD5~0 hold time (to /LRD↑)	LD5~0	0			nS	
90	LA12~0 hold time (to /LRD↑)	LA12~0	0			nS	C=20pF
91	LEDC hold time (to /WR↓)	LEDC	0			nS	C=50pF
92	LEDC delay time (to D7~0)	LEDC			30	nS	C=50pF
93	/DREQ↓ delay time (to MCLK↑)	/DREQ			11T/32 +35	nS	C=20pF Bi-level mode
					27T/32 +30	nS	C=20pF 6bit mode
94	/DREQ↑ delay time (to /RD↓)	/DREQ			25	nS	C=20pF
95	/DACK↓ set up time (to /RD↓)	/DACK	0			nS	
96	/DACK↑ hold time (to /RD↑)	/DACK	0			nS	
97	/RD↓ response time (to /DREQ↓)	/RD	0		31T/8 -25	nS	C=20pF Bi-level mode
			0		3T/8 -25	nS	C=20pF 6bit mode
98	/RD↑ acceptable delay time (to /DREQ↓)	/RD			4T-30	nS	C=20pF Bi-level mode
					T/2-30	nS	C=20pF 6bit mode

■Measurement Conditions

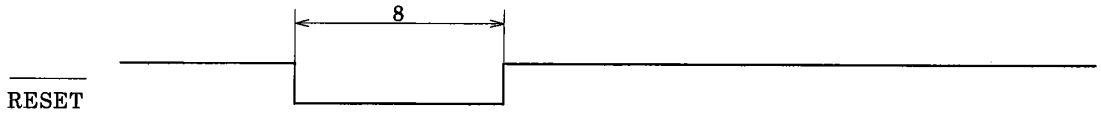


■Timing specification

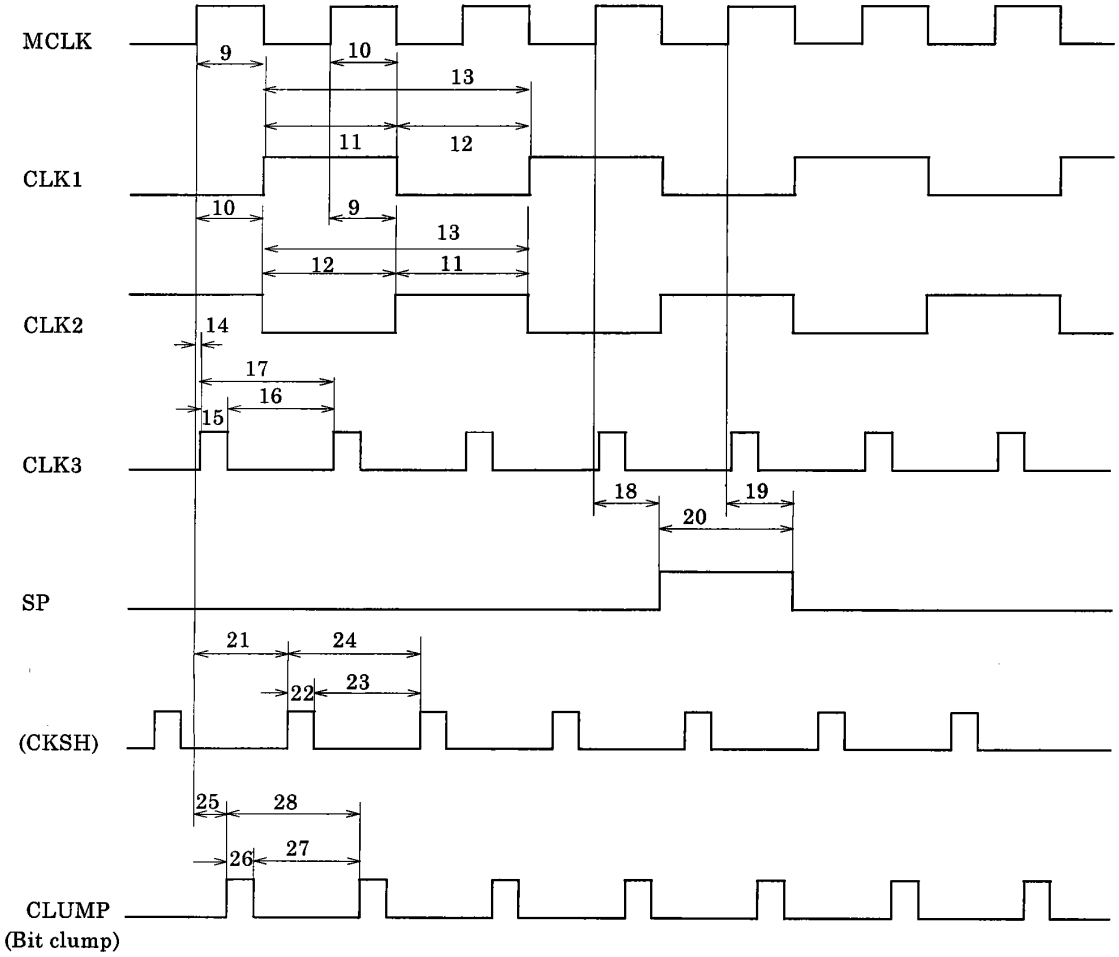
(1)Clock signals



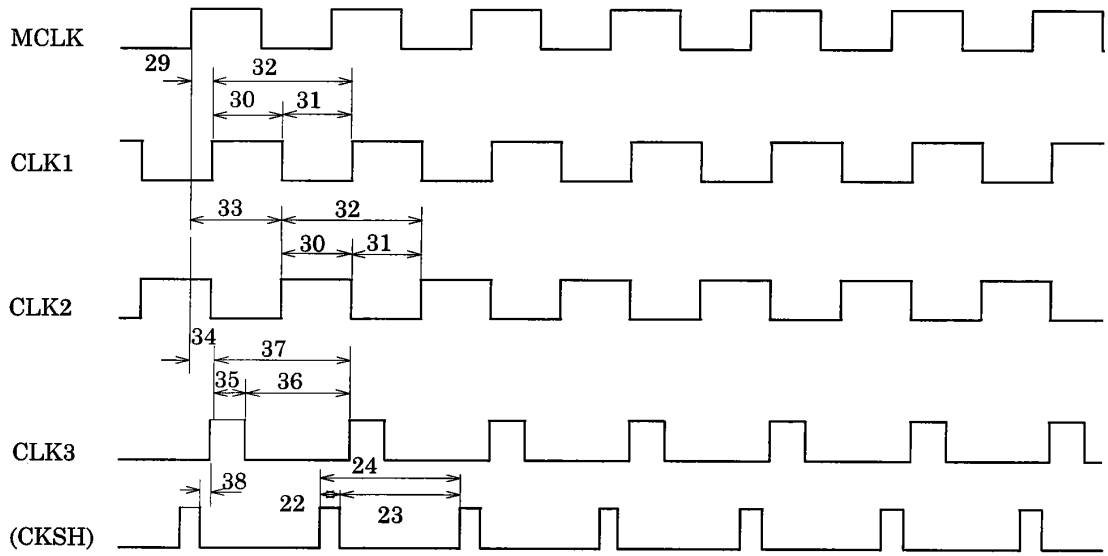
(2)Reset



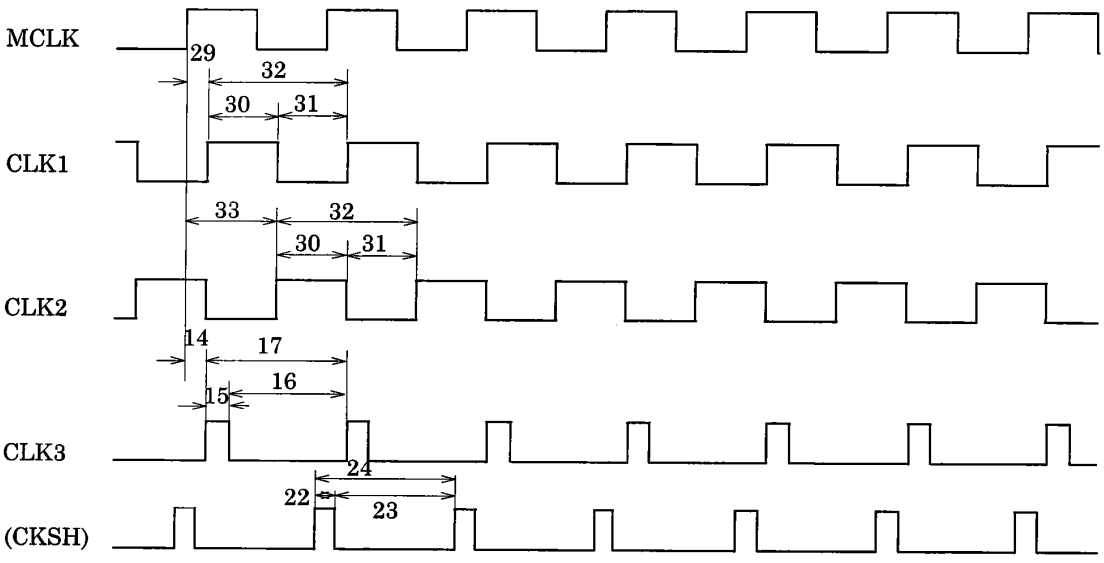
(3)Sensor clocks (CCD mode B)



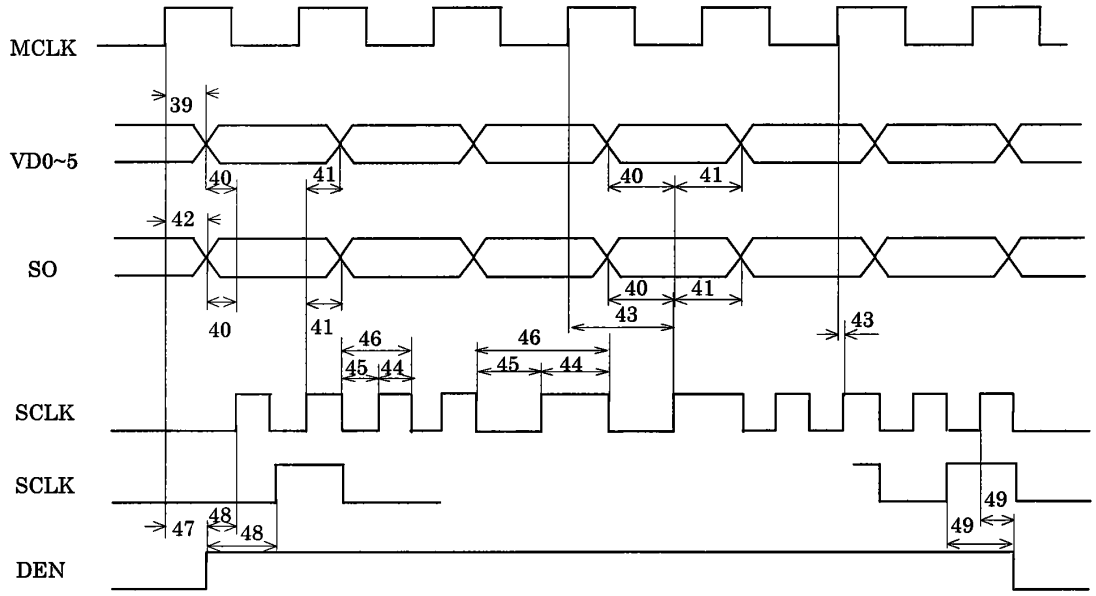
(4)Sensor clocks (CIS mode)



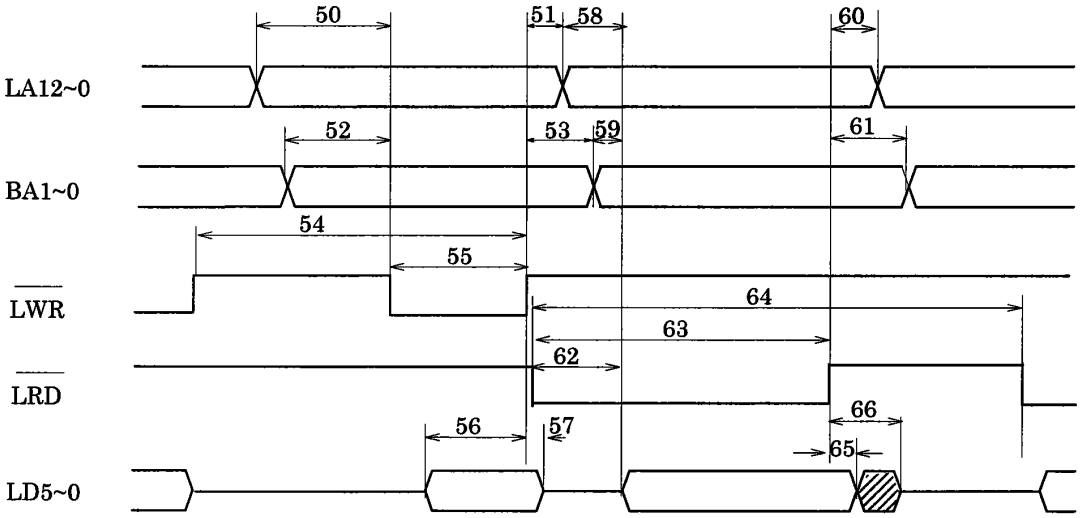
(5)Sensor clocks (CCD mode A)



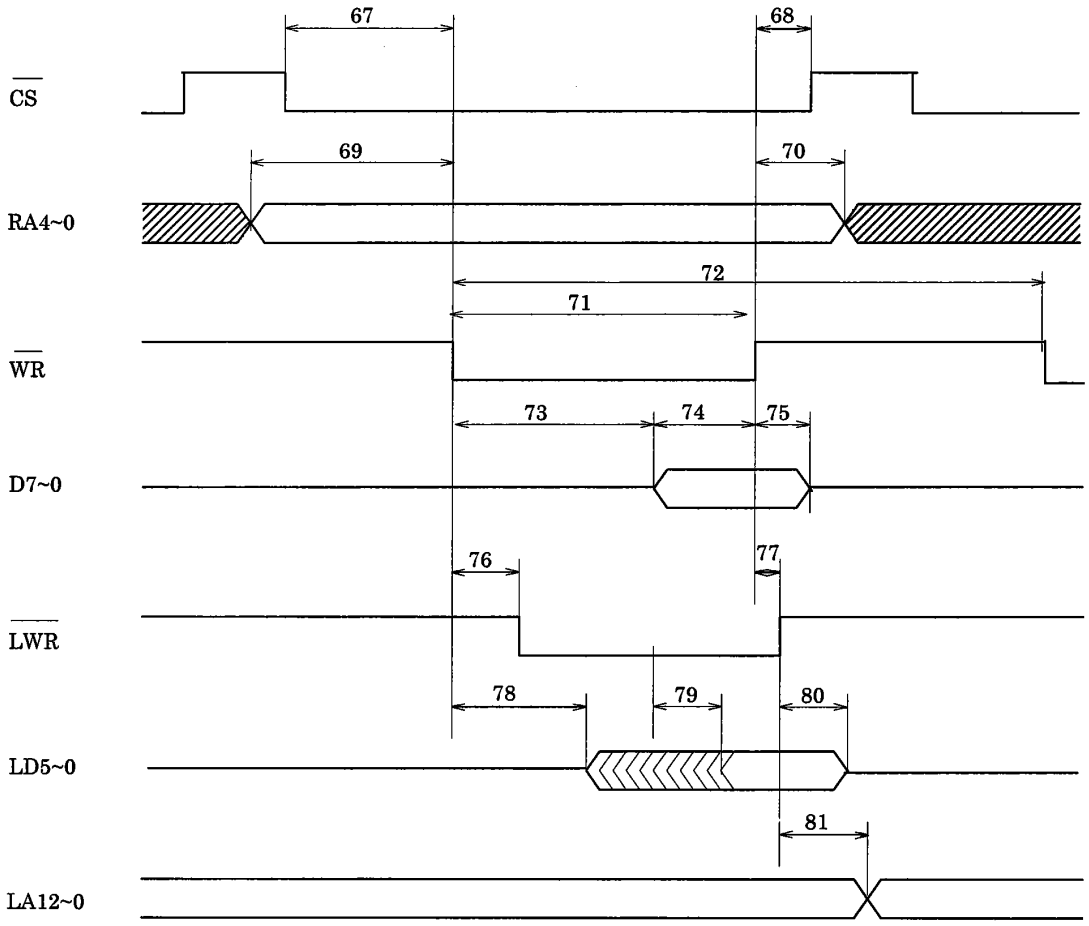
(6)Video memory I/F



(7)Memory access (operation enabled)

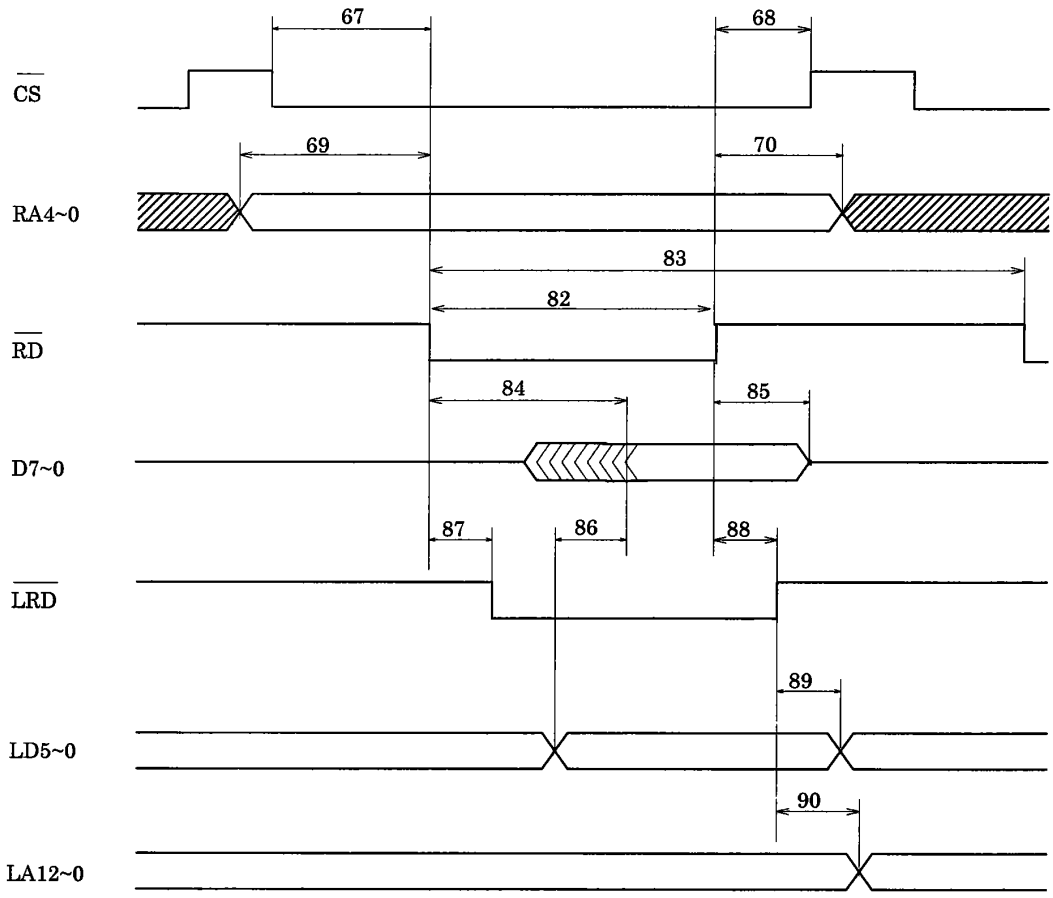


(8)Memory access (internal/external RAM access)
Write

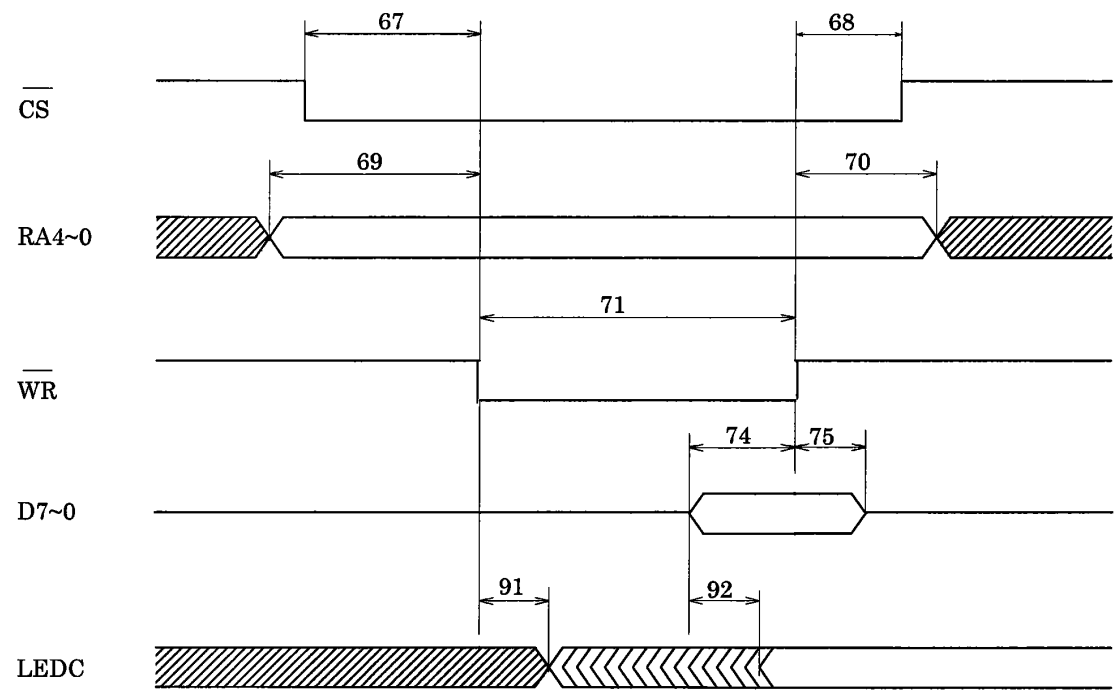


(9)Memory access (internal/external RAM access)

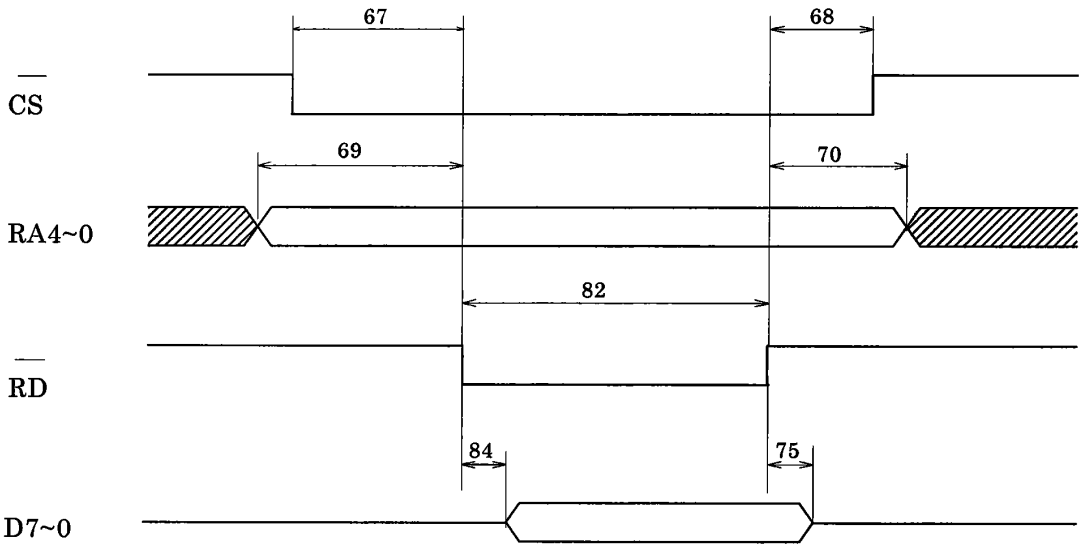
Read



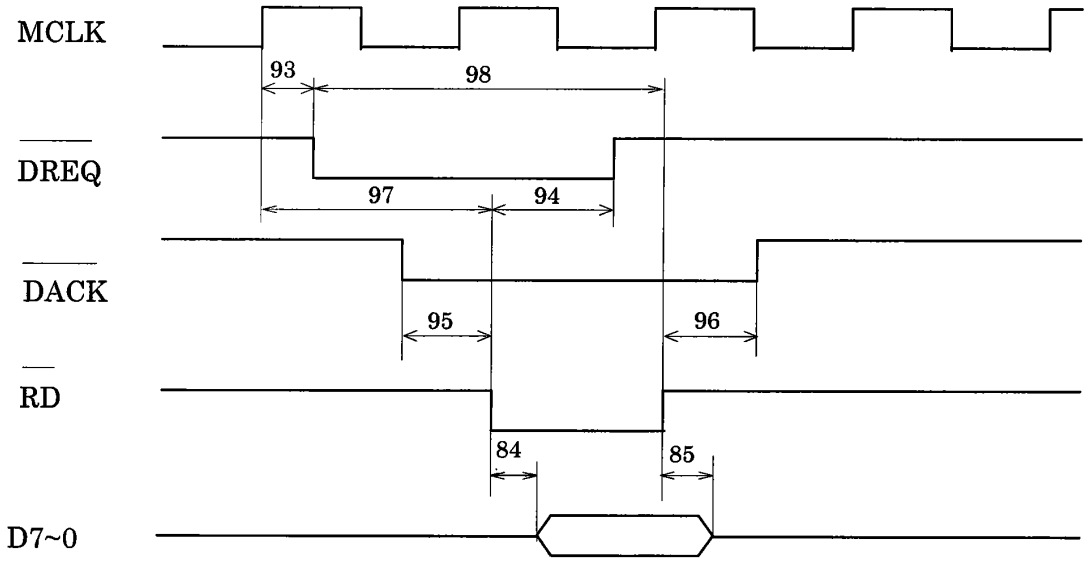
(10)μC I/F
Write



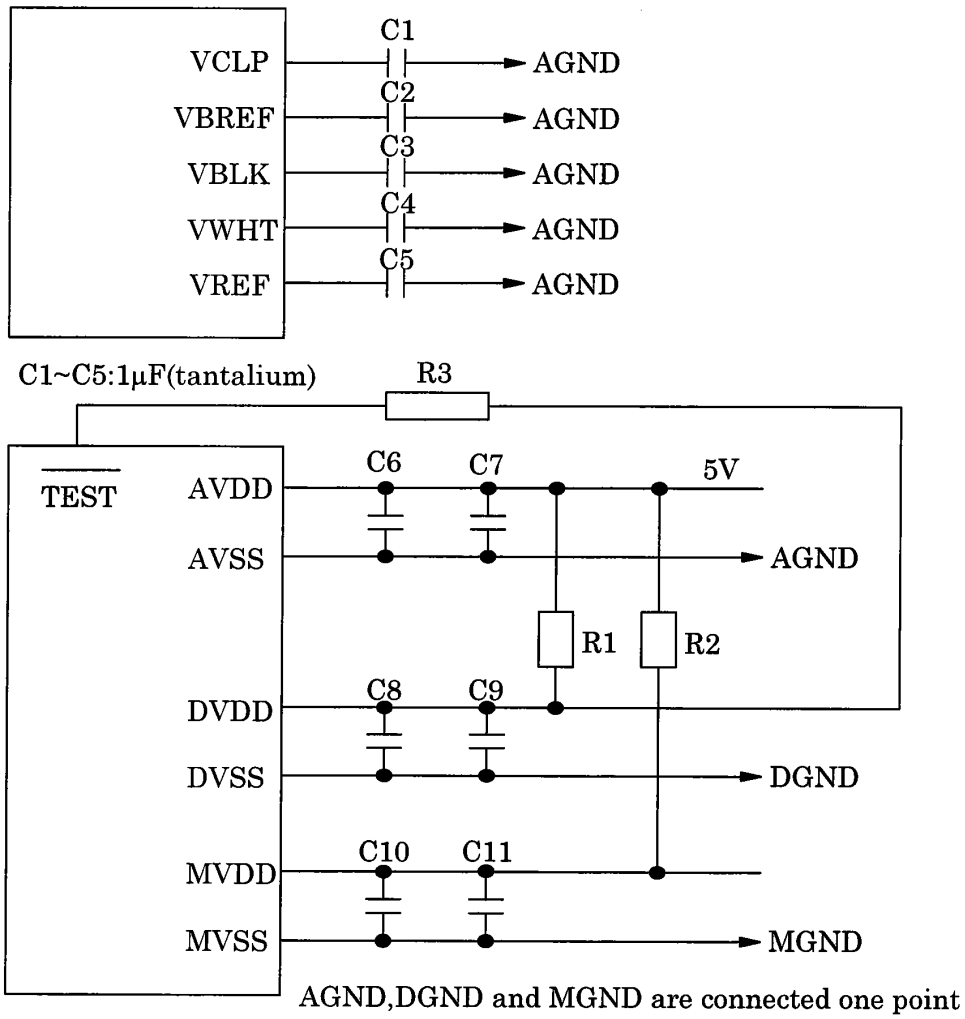
(11)μC I/F
Read



(12)DMA I/F



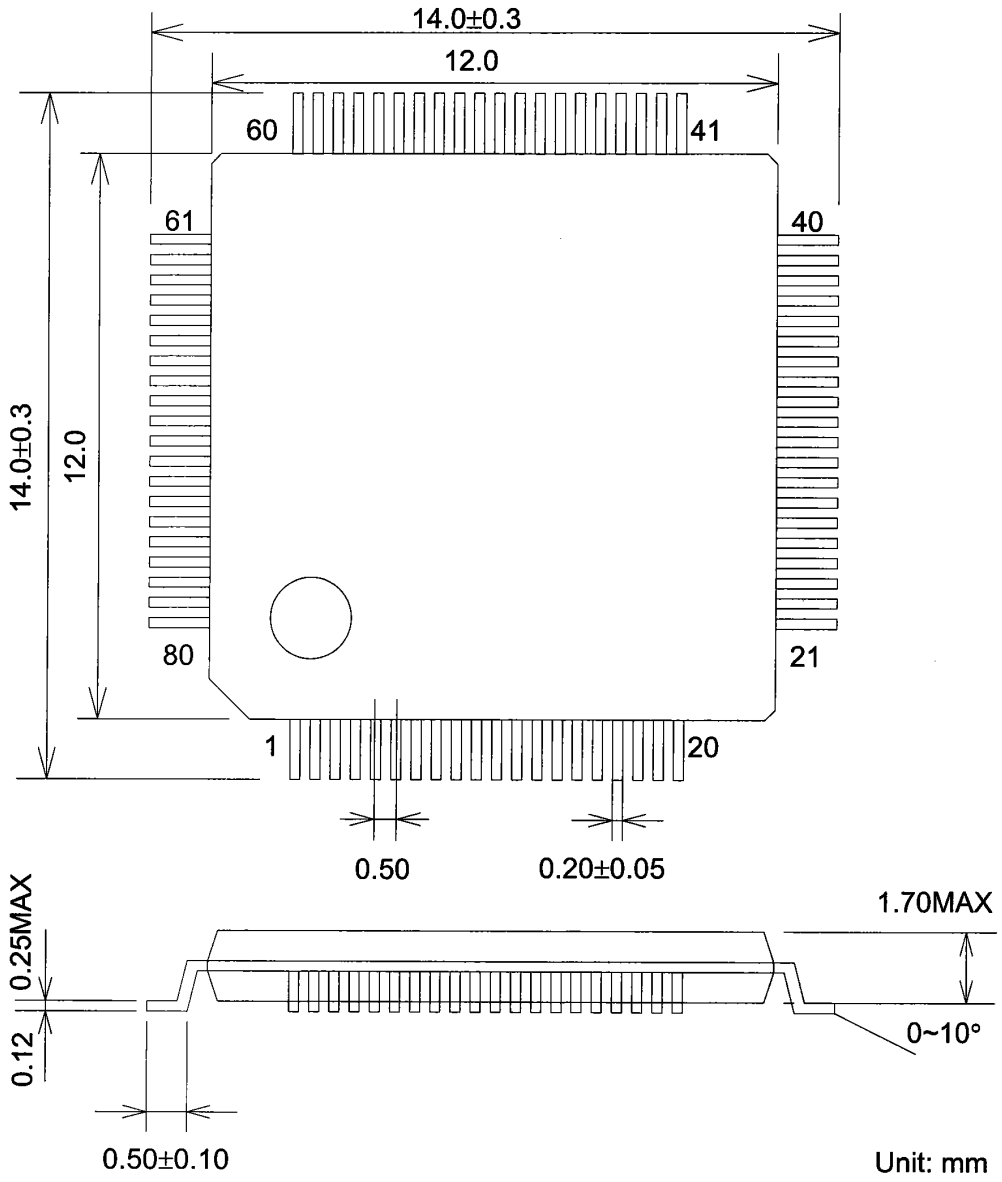
Recommended external circuit



AGND,DGND and MGND are connected one point

C6,C8,C10:22μF(Tantalium)
C7,C9,C11:0.1μF(Ceramic)
R1,R2 :2Ω
R3 :10kΩ

Package


14.0±0.3
12.0
60
41
61
40
14.0±0.3
12.0
80
21
1
20
0.50
0.20±0.05
1.70MAX
0.25MAX
0.12
0~10°
0.50±0.10
Unit: mm

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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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