AK8441

6 Channel 10 Bit 35MSPS/ch AFE for Linear CCD

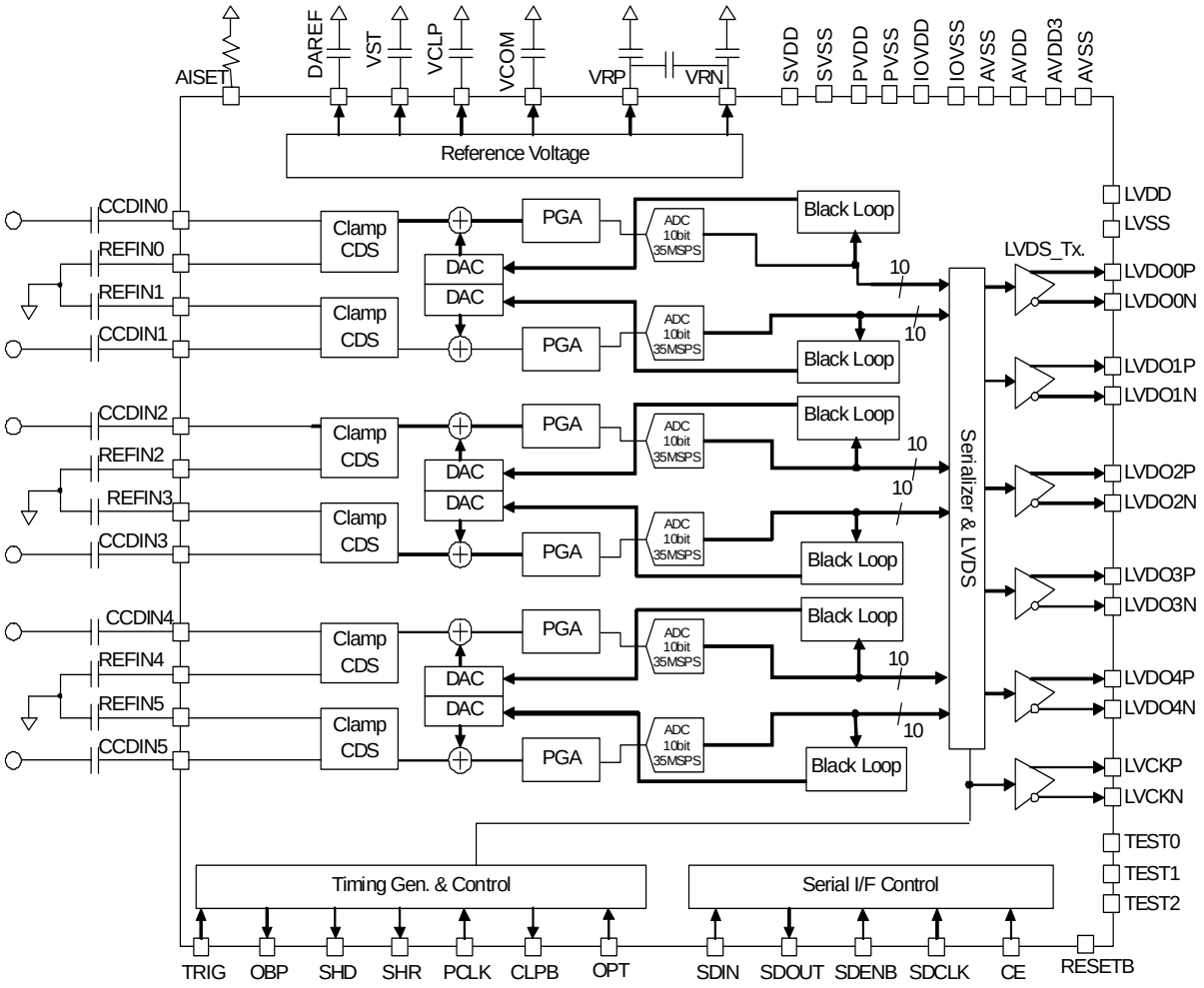
Device Outline

The AK8441 is a +3.3 V CMOS, 6 Channels 10 Bit 10M~35MSPS/ch ADC which integrates on-chip Offset Adjust DAC, Gain Adjust PGA and CDS circuit. The device is optimized for Flatbed Scanner applications etc.

Features

- ☐ Maximum conversion rate : 35MSPS / ch.
- ☐ Input range : 1.26Vpp(typ.)@CDS mode/ 1.2V(typ.)@Clamp mode
- ☐ Input polarity : Negative polarity only
- ☐ 6ch. sampling : CDS circuit (Correlated Double Sampling)
- ☐ Offset DAC : Separate 6 channel 8bit DAC with automatic black offset loop.
- ☐ PGA : Gain range 0dB~18dB , 6bit, 6 channel
- ☐ Linearity : DNL = −1LSB(min.), +1LSB(max.) Monotone guarantee
- ☐ LVDS output : 5LVDS-Data+LVDS-Clock
- ☐ Timing Generator : Generate internal drive pulses(SHR,SHD,ADCK,OBP,CLPB)
- ☐ 4 line serial register : Write and read-back available , Single access mode / Continuous access mode
- ☐ Power supplies : AVDD:1.7~2.0V/AVDD3,PVDD,SVDD,LVDD:3.0~3.6V, IOVDD: 1.7~3.6V
- ☐ Operation Temperature: 0°C~70°C
- ☐ Power consumption : 661mW (typ.)@6ch.mode, 35MSPS / channel
- ☐ Package: 80 pin LQFP ,Pin Pitch 0.5mm, Mold Size 12mm×12mm

Circuit Block



AK8441 Block Diagram

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