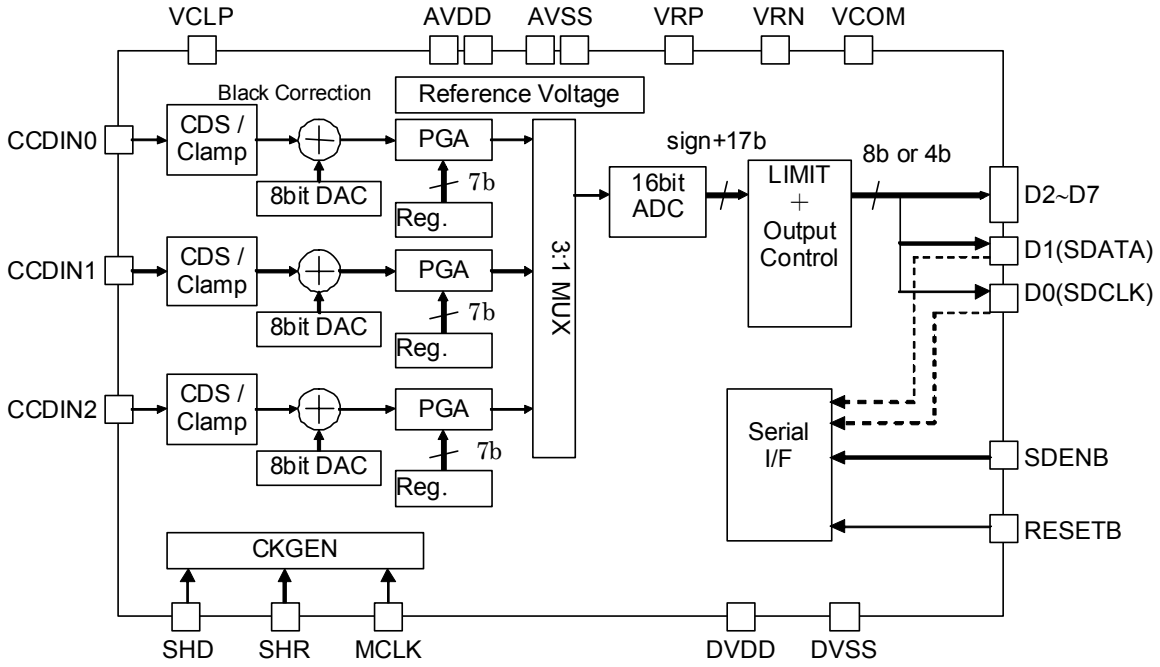
AK8443

16bit 30MSPS video ADC with CCD/CIS interface

Features

- ☐ CCD I/F
  - Channel number: 3ch (2ch.)
  - D-Range: 1.764Vpp / 2.341Vpp (typ.)
  - CDS circuit: Pos. /Neg. polarity
- ☐ ADC
  - Max. Conversion Rate: 30MSPS (10MSPS/ch)
  - Resolution: 16bit (straight binary code)
- ☐ Offset DAC
  - Range: ±321mV (normal input range)
  - Resolution: 8bit
- ☐ PGA
  - Range: 0dB~22dB
  - Resolution: 7bit
- ☐ Output format: 8bit x 2 → 16bit or 4bit x 4 → 16bit
- ☐ Power supply: 3.3V±0.3V
- ☐ CPU I/F: 3 Wire Serial Interface
- ☐ Power consumption: 365 mW (typ.)
- ☐ Operation Temperature: 0°C~70°C
- ☐ Package: 28pin QFN with radiation PAD in solder side



Circuit Block

■ Clamp, CDS Block

The clamp circuit and correlated double sample circuits are provided for CCD output signal. In CDS mode, the difference between the feed threw level of signal and the data level is sampled. In clamp mode, the difference between the internal reference VCLP and the data level of signal is sampled. Clamp pull the feed threw level into VCLP level when SHR is high.

■ Black Correction

Circuit to add an offset voltage to the sampled signal level. Voltage range of DAC which generates Offset is ±321 mV(typ.) and its resolution is 8 bit.

■ MUX Block

MUX is a select switch that selects one signal from three ADC output signals sequentially. The AK8443 has 2-channel mode and 3-channel mode. Each mode is selected by control register.

■ ADC Block

The ADC coverts PGA output signal to digital data. The resolution is 16-bit and the maximum conversion rate is 30MSPS. The output code is straight binary. The output data corresponding to black is 0000h, and the data corresponding to white is FFFFh.

■ Output Control Block

The output control multiplexes a 16-bit word ADC data into two cycle 8-bit word data or four cycle 4-bit word data.

■ Reference Voltage Gen1erator Block

All reference voltage is generated internally.

Pin descriptions

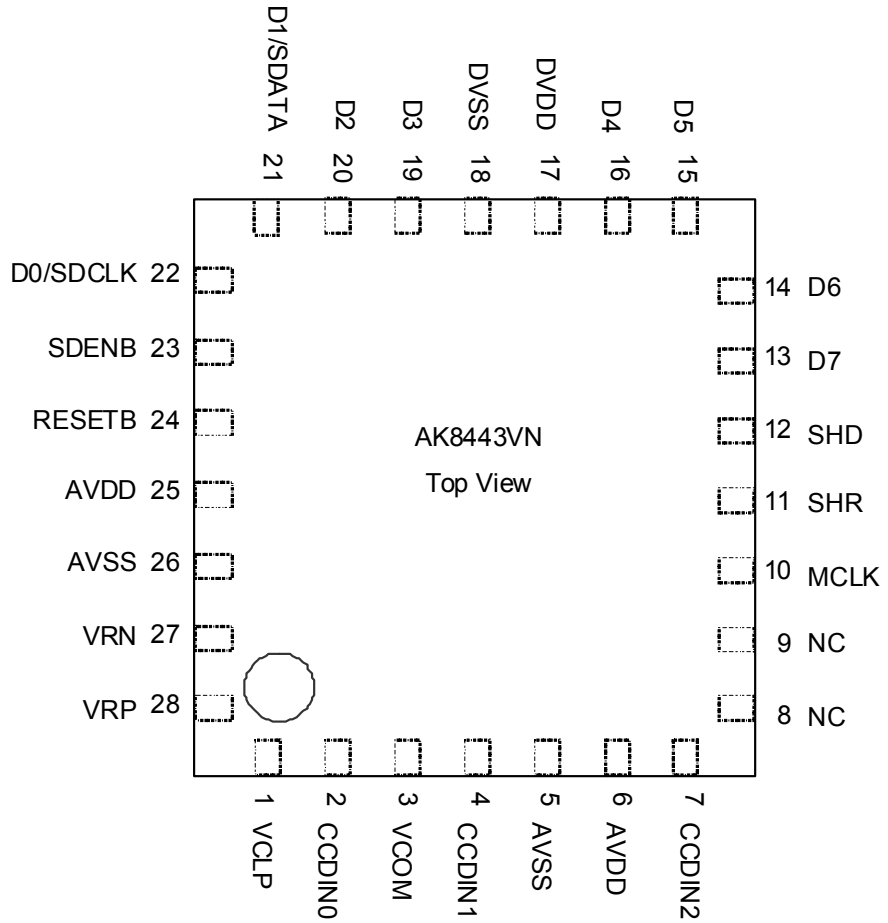
No.	Name	IO	@PD	Description
1	VCLP	I/O	VSS (note1)	CDS, Clamp mode: Clamp Voltage output, Connect capacitor0.1uF between AVSS and this pin. DC direct mode: sensor reference voltage input
2	CCDIN0	I		Sensor signal input
3	VCOM	O	Hi-Z	ADC reference voltage. Connect capacitor0.1uF between AVSS and this pin.
4	CCDIN1	I		Sensor signal input
5	AVSS	P		Analog ground
6	AVDD	P		Analog VDD
7	CCDIN2	I		Sensor signal input
8	NC	-		No connection(note 2)
9	NC	-		No connection(note 2)
10	MCLK	I		Main clock
11	SHR	I		Reference level sampling clock
12	SHD	I		Data level sampling clock
13	D7	O	Low	Data output (MSB)
14	D6	O	Low	Data output
15	D5	O	Low	Data output
16	D4	O	Low	Data output
17	DVDD	P		Digital VDD
18	DVSS	P		Digital Ground
19	D3	O	Low	Data output
20	D2	O	Low	Data output
21	D1/SDATA	I/O	Low (note 3)	Data output / Serial I/F Data input
22	D0/SDCLK	I/O	Low (note 3)	Data output (LSB) / Serial I/F Clock input
23	SDENB	I		Serial I/F Enable.
24	RESETB	I		Reset input. Pull-up 100kΩ to AVDD.
25	AVDD	P		Analog VDD
26	AVSS	P		Analog ground
27	VRN	O	VSS	ADC reference voltage; Negative side. Connect capacitor0.1uF between AVSS and this pin. And connect capacitor 1uF between VRP and this pin.
28	VRP	O	VSS	ADC reference voltage; Positive side. Connect capacitor0.1uF between AVSS and this pin. And connect capacitor 1uF between VRN and this pin.

(note1) It is connect with VSS via internal resistance by CDS, Clamp mode or DC direct mode

(note2) Do not connect it anywhere.

(note3) When SDENB is Hi, it will be output condition as VSS. When SDENB is Low, it will be input condition.

Pin Layout



Absolute Maximum Ratings

All voltage defined to their corresponding ground. AVSS=DVSS==0V

Item	Symbol	Min.	Max.	Unit	Remarks
Analog Supply	AVDD	−0.3	4.6	V	
Digital Supply	DVDD	−0.3	4.6	V	
Input Voltage	VINA	−0.3	AVDD+0.3	V	
Storage Temperature	Tstg	−65	150	°C	

Stress above these ratings may cause permanent damage to the device. Functional operation of the device at these ratings is not implied.

Recommended Operating Conditions

All voltage defined to their corresponding ground, AVSS=DRVSS=0V

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Analog Supply	AVDD	3.0	3.3	3.6	V	
Digital Supply	DVDD	3.0	3.3	3.6	V	
Operating Temperature	Ta	0		70	°C	

**At the power up, the device must be reset once by RESETB pin.

**When power on AVDD, please set up the same time with DVDD or DVDD first.

**When power down AVDD, please set up the same time with DVDD or before DVDD.

**| AVDD-DVDD | < = 0.3V

Electrical Characteristics

Analog Characteristics (AVDD=DVDD=3.3V, Ta= 25°C, MCLK=30MHz unless otherwise specified)

Item	Symbol	Condition	min	typ	max	Unit
Reference Voltage Block						
Clamp voltage	VCLP	Negative, Normal range	2.2	2.3	2.4	V
		Negative, Large range	2.5	2.6	2.7	V
		Positive, Normal range	0.7	0.8	0.9	V
		Positive, Large range	0.5	0.6	0.7	V
DC direct reference level	VCLP	External input	0.94	1.1	1.26	V
Common voltage	VCOM		1.15	1.25	1.35	V
ADC positive reference voltage	VRP		1.7	1.8	1.9	V
ADC negative reference voltage	VRN		0.6	0.7	0.8	V
Clamp and CDS Block						
Input range (*note 1)	VI	PGA gain=0dB setting				
		Normal range	1.56	1.764		Vpp
		Large range	2.07	2.341		Vpp
		DC direct mode		1.1		Vpp
CDS effect (note 2)	CDS	noise 100mVpp 0.5MHz Signal 1.6Vpp 2MHz		-30		dB
Clamp bandwidth	CLPBW	(Design target value) External cap=0.1uF		2080		usec

These characteristics are a value at the time of the external part value which was shown in the external-circuit instance.

(note 1) Be careful an input signal which doesn't cross a power supply voltage in case of the positive-polarity and large-range. DC direct mode only use normal range, when input is 1.1Vpp, PGA is 30H setting, it will be full scale. (@VCLP voltage=1.1V)

(note 2) When SHR width is minimum.

(AVDD=DVDD=3.3V, Ta= 25°C, MCLK=30MHz unless otherwise specified)

Item	Symbol	Condition	min	typ	max	Unit
Offset DAC						
Resolution	DRES			8		bit
Range (note 1)	DRNG	Input conversion value Positive Negative	 271 -373.5	 321 -323.5	 371 -273.5	 mV mV
Range2 (note 2)	DRNG2	Input conversion value Positive Negative		 350.7 -353.5		 mV mV
Range3 (note 3)	DRNG3	Input conversion value Positive Negative		 307 -309.4		 mV mV
Differential nonlinearity	DNL	The Monotonicity guarantee	-1.0		+1.0	LSB

These characteristics are a value at the time of the external part value which was shown in the external-circuit instance.

(note 1) Normal range input.
(note 2) Large range input.
(note 3) DC direct mode.

(AVDD=DVDD=3.3V, Ta= 25°C, MCLK=30MHz unless otherwise specified.)

Item	Symbol	Condition	min	typ	max	Unit
PGA						
Maximum gain	GMAX	CCDIN~ADC Relative value to 0dB setting	20.3	21.3	22.3	dB
Step width	GSTA	The Monotonicity guarantee	0.001	0.06		dB
ADC						
Resolution	RES				16	bit
Differential nonlinearity	DNL	CCDIN~ADC 12bit accuracy No missing code	−16		+16	LSB
Noise, Internal offset, Crosstalk						
No input noise (note 1)	NI	PGA gain=0dB PGA gain=21.3dB		9 65		LSB_{rms}
Offset voltage (note 2)	VOFST	CDS, Clamp(normal input) CDS, Clamp(Large input) DC Direct PGA gain=0dB	−120 −145 −100		120 145 100	mV
Crosstalk	XTALK1	(note 3)		128		LSB
	XTALK2	(note 4)		64		LSB
Power consumption						
Normal operation	AVDD DVDD	(note 5) (note 6)		97.1 13.4	123 27.5	mA
Power down	IPD				0.1	mA

These characteristics are a value at the time of the external part value which was shown in the external-circuit instance.

(note 1) This is defined as sigma of the ADC output cord scattering at no input.

(note 2) Definition is that the Offset DAC setting value in no input signal condition exists between Offset DAC setting values, (equivalent to an input-referred – 120mV) and (equivalent to an input-referred + 120mV) where ADC output code changes from 000h to 001h. Since a total adjustable range of Offset Adjust DAC includes this internal Offset adjust range, a practical adjustable range of input signal is reduced by the internal Offset amount.

(note 3) Definition at MCLK=30MHz, 3ch, CDS mode. PGA gain of the channel to be measured is set at its maximum value, all other channels' PGA gains are set at minimum values. Then measure how much the output code of the target channel to be measured fluctuates when input to the measures channel is fixed and a full-scale minus 1 dB step signal is input on all other channels.

(note 4) Definition at MCLK=30MHz, 3ch, CDS mode. All channels' PGA gains at minimum values. Then measure how much the output code of the target channel to be measured fluctuates when input to the measures channel is fixed and a full-scale minus 1 dB step signal is input on all other channels.

(note 5) At MCLK=30MHz, and 1.569 Vpp, 1MHz sine-wave signal fed on all 3 channel.

(note 6) At the capacitive load is 20pF.

2) Digital DC Characteristics

(AVDD=DVDD=3.0V～3.6V,Ta= 0~70°C)

Item	Symbol	Pin	Min.	Max.	Unit	Remark
High level input voltage	VIH	**1	0.7*AVDD		V	
Low level input voltage	VIL	**1		0.3*AVDD	V	
High level output voltage	VOH	**2	0.8*DVDD		V	IOH=－1mA
Low level output voltage	VOL	**2		0.2*DVDD	V	IOL=1mA
Input leakage current	ILIKG	**1	−10	10	μA	

**1 MCLK, SHR, SHD,D0(SDCLK), D1(SDATA), SDENB, RESETB

**2 D0~D7

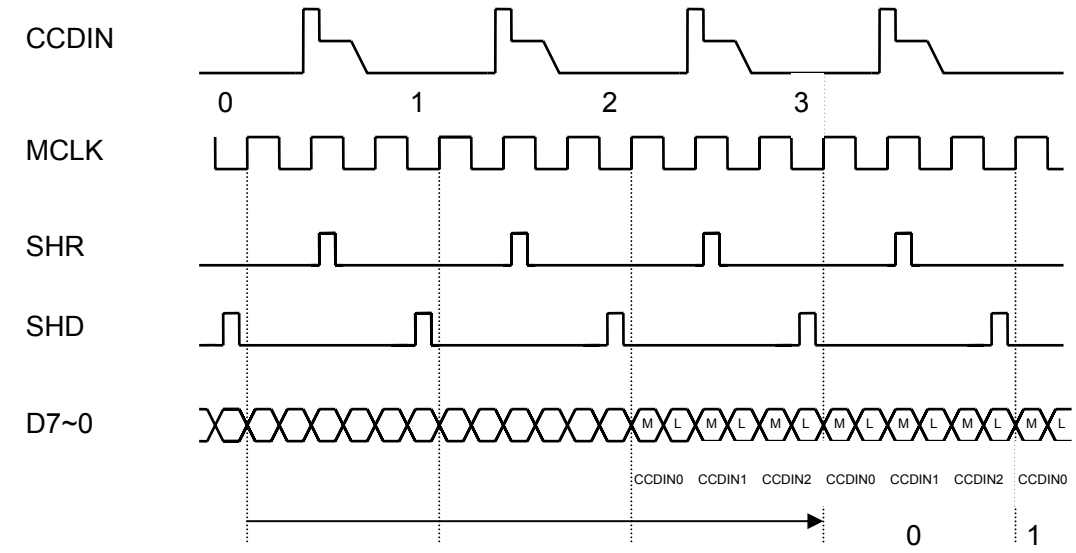
■ Switching characteristics

(AVDD=DVDD=3.0V～3.6V,Ta=0～70°C, 8bit bus, unless otherwise specified)

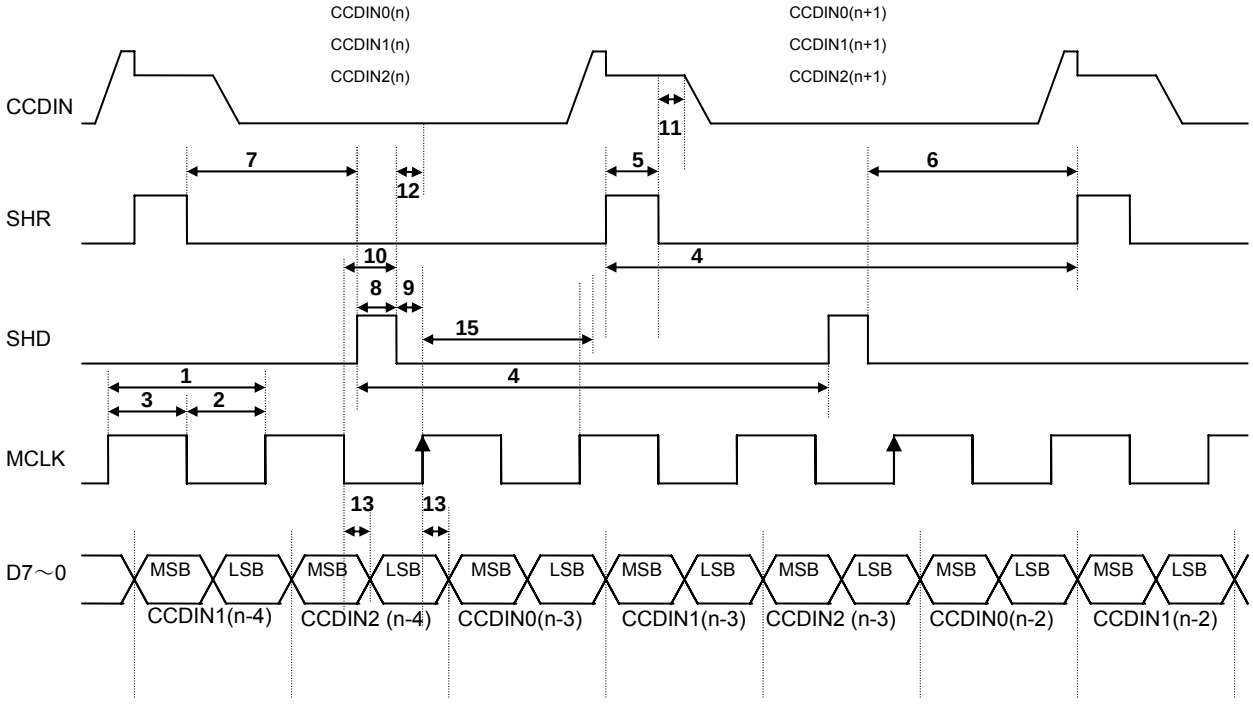
No.	Item	Pin	Min.	Typ.	Max.	Unit	Condition
1	MCLK cycle time(T)	MCLK	33.3		2000	ns	
2	MCLK Low width	MCLK	15			ns	
3	MCLK High width	MCLK	15			ns	
4	SHR,SHD cycle time	SHR SHD	100 66.7	3T 2T	6000 4000	ns	3ch 2ch
5	SHR pulse width	SHR	8			ns	
6	SHR delay （referenced to SHD↓）	SHR	2			ns	
7	SHD↑delay （referenced to SHR↓）	SHD	2			ns	
8	SHD pulse width	SHD	8			ns	
9	SHD setup time （referenced to MCLK↑）	SHD	0			ns	
10	SHD delay （referenced to MCLK↓）	SHD	10			ns	
11	SHR aperture delay	SHR		2		ns	
12	SHD aperture delay	SHD		2		ns	
13	D0～7 output delay （ referenced to MCLK↑or MCLK↓）	D7～D0	2		12	ns	Hold setup C=20pF
14	Pipeline delay (SHD conversion)	D7～D0		3 4		clock	3ch mode 2ch mode
15	SHD=”H” inhibition period （ After referenced to SHD↓, first MCLK↑）	SHD	T+10			ns	3ch mode 2ch mode

(AVDD=DVDD=3.0V～3.6V,Ta=0～70°C, 4 bit bus, unless otherwise specified)

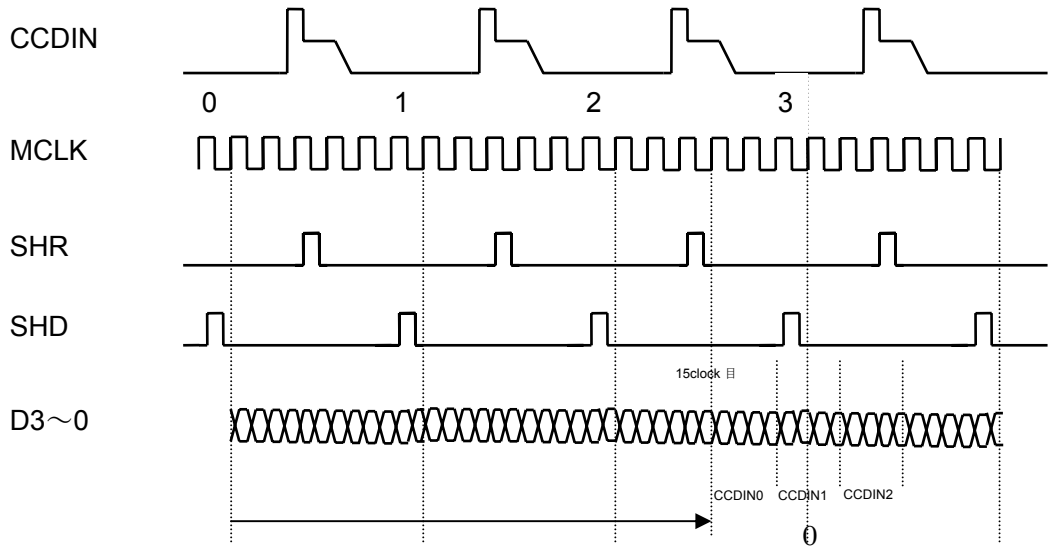
No.	Item	Pin	Min.	Typ.	Max.	Unit	Condition
1	MCLK cycle time (T)	MCLK	33.3		2000	ns	
2	MCLK Low width	MCLK	15			ns	
3	MCLK High width	MCLK	15			ns	
4	SHR,SHD cycle time	SHR SHD	199.8 133.2	6T 4T	12000 8000	ns	3ch 2ch
5	SHR pulse width	SHR	8			ns	
6	SHR delay （referenced to SHD↓）	SHR	2			ns	
7	SHD↑ delay （referenced to SHR↓）	SHD	2			ns	
8	SHD pulse width	SHD	8			ns	
9	SHD setup time （referenced to MCLK↑）	SHD	0			ns	
10	SHD delay time （referenced to MCLK↑）	SHD	10			ns	
11	SHR aperture delay	SHR		2		ns	
12	SHD aperture delay	SHD		2		ns	
13	D0～7 delay time （reference to MCLK ↑or MCLK ↓）	D3～D0	2		12	ns	hold setup C=20pF
14	Pipeline delay (MCLK conversion)	D3～D0		15		clock	3ch mode 2ch mode
15	SHD=”H” inhibition period （ After referenced to SHD↓, first MCLK↑）	SHD	2T+10			ns	3ch mode 2ch mode



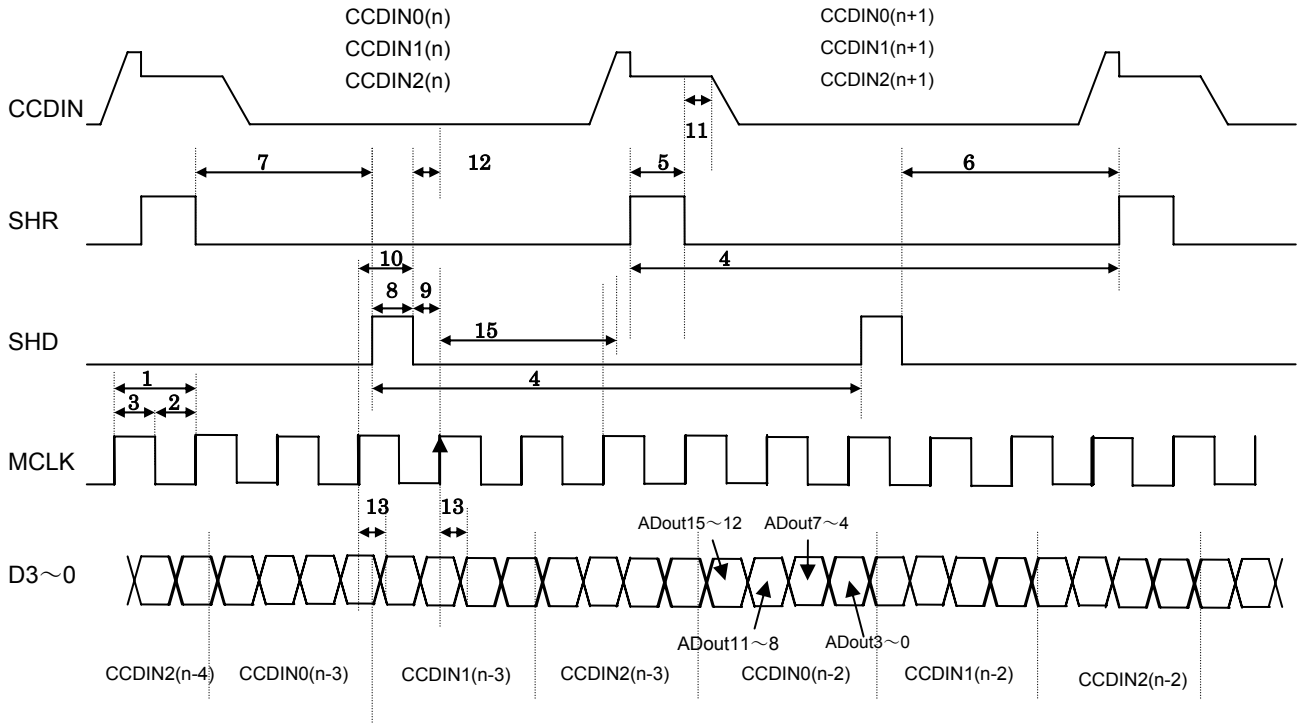
L among D7 to D0 indicates LSB data, and M indicates MSB data.



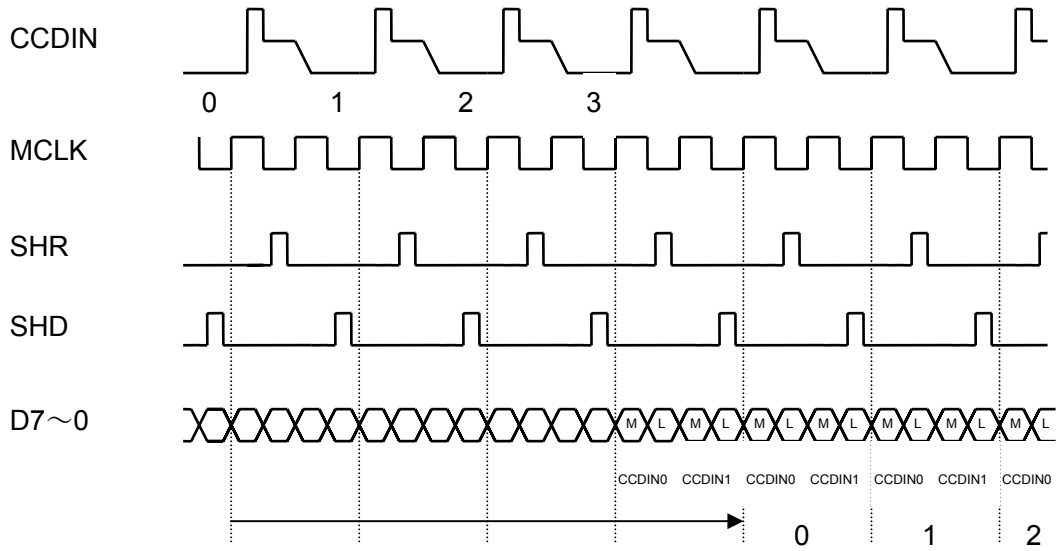
3ch and 8bit bus mode



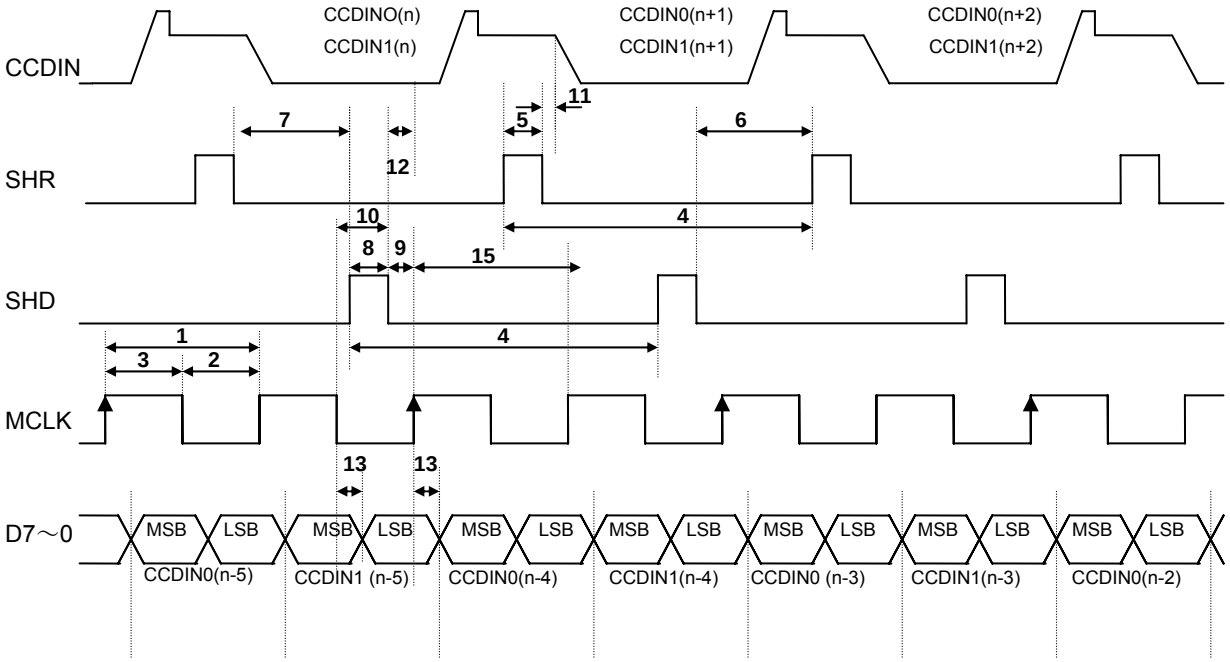
D3 ~ D0 output order is ADout[15:12]→ADout[11:8]→ADout[7:4]→ADout[3:0].



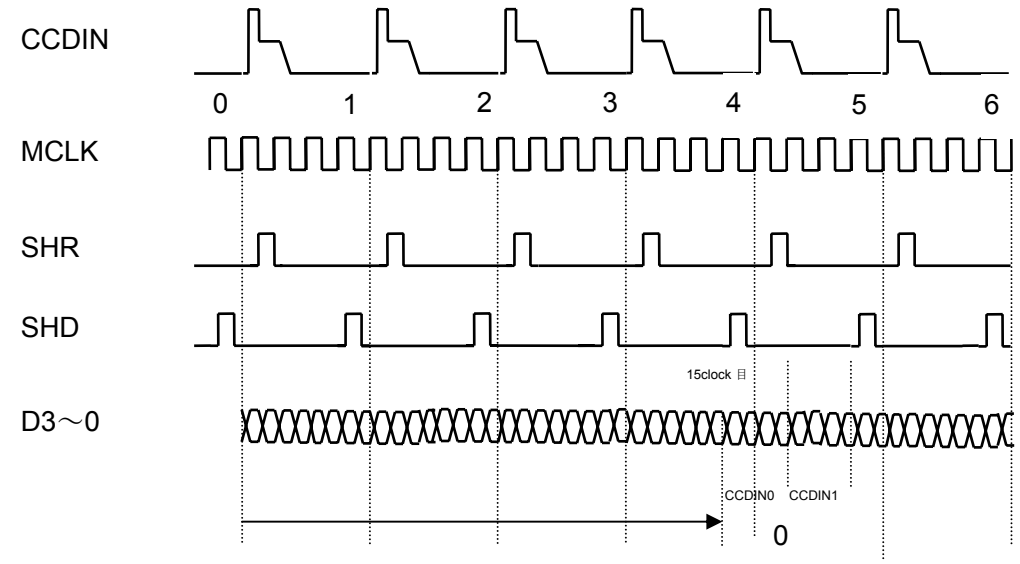
3ch and 4bit bus mode



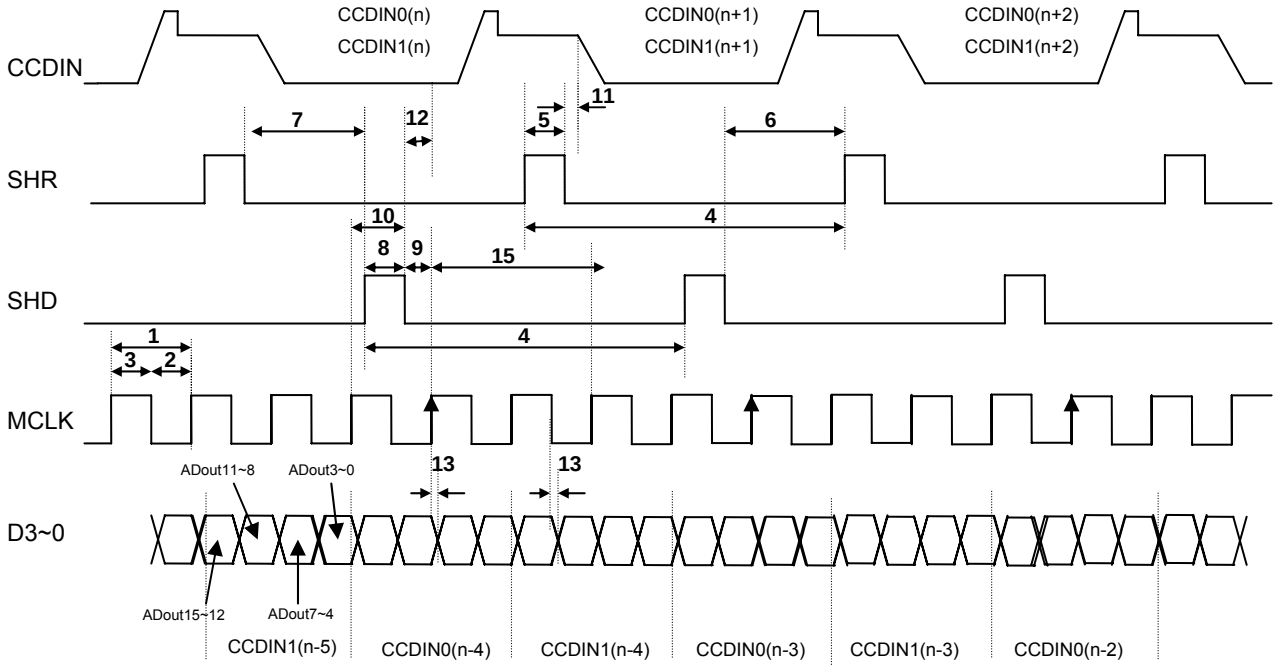
L among D7 to D0 indicates LSB data, and M indicates MSB data.



2ch and 8 bit bus mode



D3 ~ D0 output order is ADout[15:12]→ADout[11:8]→ADout[7:4]→ADout[3:0].

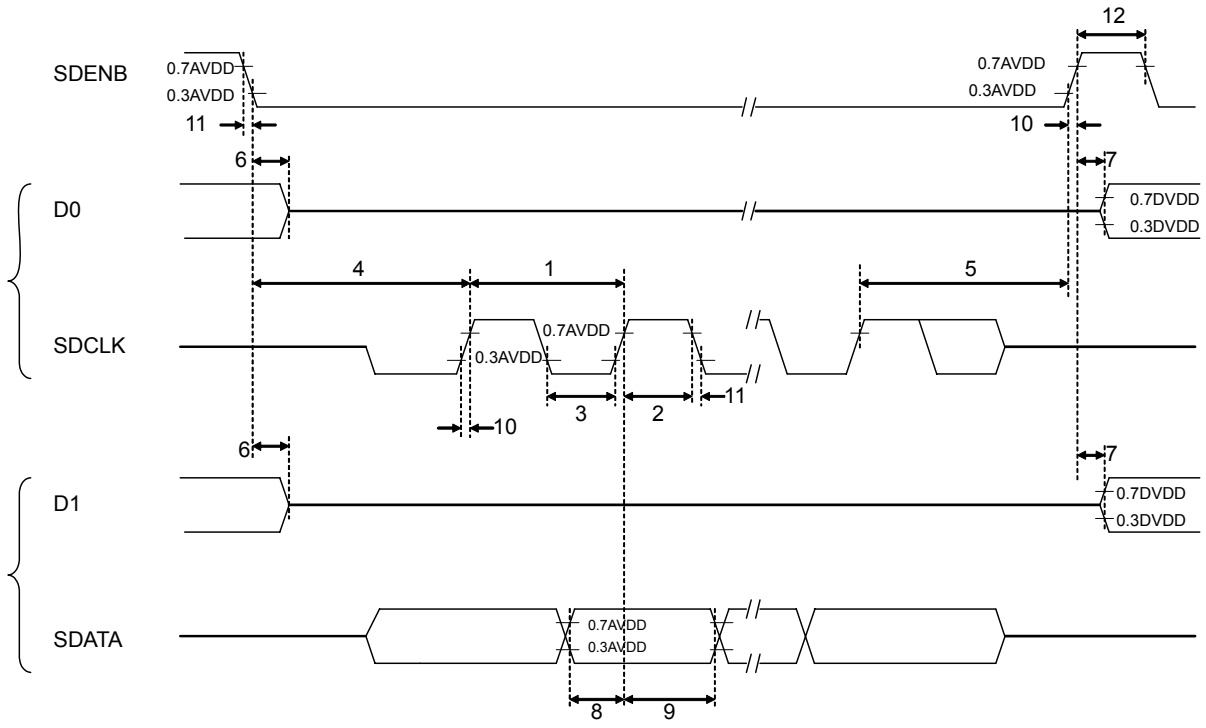


2ch and 4bit bus mode

■ Serial Interface switching characteristics

(AVDD=3.0~3.6V, DVDD=3.0~3.6V ,Ta= 0~70°C unless otherwise specified.)

No.	Item	Pin	Min.	Typ.	Max.	Unit	Condition
1	Clock cycle	SDCLK	0.1		10	MHz	
2	Clock pulse width(High)	SDCLK	40			ns	
3	Clock pulse width(Low)	SDCLK	40			ns	
4	SDENB setup time (to SDCLK rising↑)	SDENB	80			ns	
5	SDENB hold time (from SDCLK rising↑)	SDENB	80			ns	
6	Data High-Z delay (from SDENB falling↓)	D0, D1	0		40	ns	
7	Data enable delay (to SDENB rising↑)	D0, D1	0		40	ns	
8	SDATA setup time (to SDCLK rising↑)	SDATA	40			ns	
9	SDATA hold time (from SDCLK rising↑)	SDATA SDENB	40			ns	
10	SDCLK,SDENB rising time	SDCLK SDENB			6	ns	
11	SDCLK,SDENB falling time	SDCLK SDENB			6	ns	
12	SDENB High level width	SDENB	40			ns	

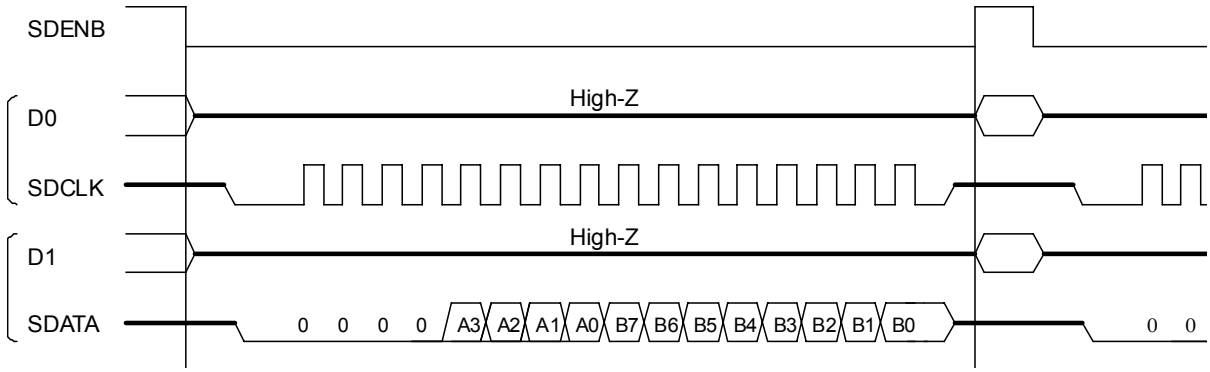


Serial interface write timing

Clock Input pin SDCLK and Data Input pin SDATA for Serial Interface are shared with A/D Data Output pins, D0 and D1 respectively. When SDENB becomes low, D0 and D1 are put into High-Z conditions and it is enabled to input SDCLK and SDATA. SDATA is captured at the rising edge of SDCLK. SDATA is 16 Bit long. Write “zeros“ from first Bit to 4th Bit. 5th ~8th Bits are assigned for Register Address where the 5th Bit is MSB and the 8th Bit is LSB. 9th~ 16th Bits are assigned for Data where the 9th Bit is MSB and the 16th Bit is LSB.

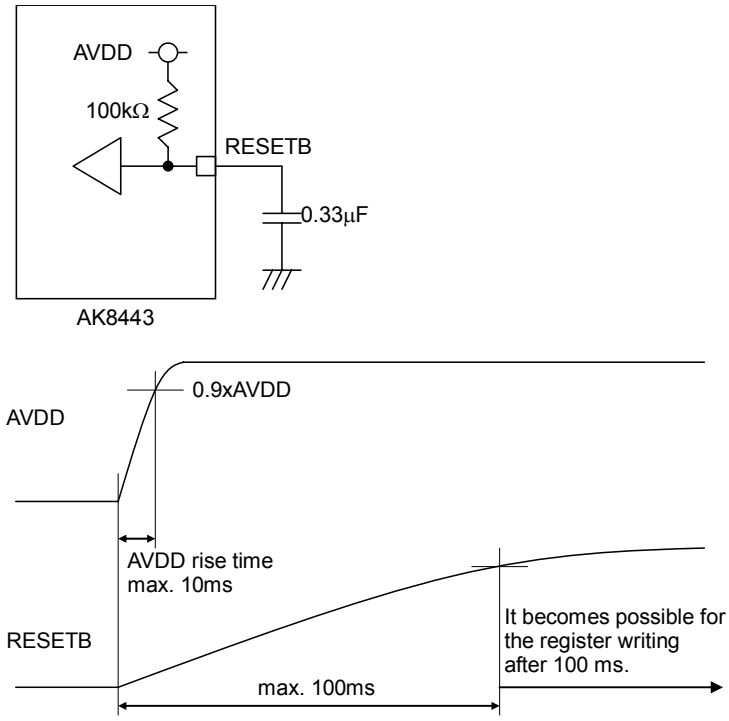
16 and more rising edges of SDCLK are required while SDENB is low, from the time to fall to the time to rise. When it is less than 16 rises, registers will not be written properly.

If it is more than 16 rises while SDENB is low, from falling to rising, the last 16 edges become effective. There is a possibility that an erroneous data will be written into registers if noises occur on D0 Output / SDCLK input pin and D1 Output / SDATA input pin when these pins are at High-Z conditions. To avoid this, resistors should be connected between D0 / SDCLK pin, D1 / SDATA pin and AVSS respectively to pull-down these pins.



Wright Register

- Power on reset



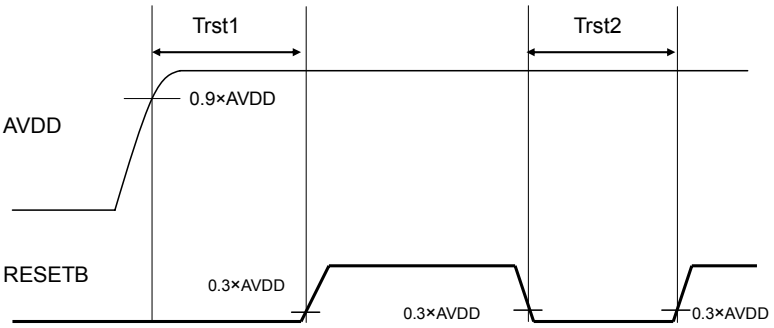
Power on reset

At the power-on, Power-On-Reset must be executed by using RESETB pin. When a 0.33 μF external capacitor on RESETB pin is used, the rise time of AVDD must be shorter than 10 ms in order to assure proper Power-On-Reset operation. Maximum time from AVDD power-on to the release from Power-On-Reset is 100 ms. Registers should be written after waiting for longer than 100 ms after AVDD power-on.

As electric charge is retained in the external capacitor even after AVDD is made to 0V, voltage on RESETB pin does not go to 0V immediately. If AVDD is powered-up again before RESETB pin returns to 0V, a proper Power-On-Reset operation is not made. In order to assure proper Power-On-Reset operation when to power-up AVDD again, it is required that AVDD time to be kept at 0V is longer than 300 ms. If the 300 ms AVDD time to be kept at 0V, is not obtainable, the device must be reset by applying a low pulse externally on RESETB pin.

When the condition doesn't fill above, please make the RESETB high after power supply start-up, Without CAP connect to RESETB pin.

In RESETB pin use



（AVDD=DVDD=3.0~3.6V、Ta=0~70□）

Item	Symbol	Pin	min	typ	max	Unit	Condition
Reset period 1	Trst1	RESETB	100			ns	
Reset period 2	Trst2	RESETB	100			ns	

Register map

Sub Adrs	Bits	Default Value	Register Name	Function
0H	6	*0******	TEST	Test register
	5	**0*****	BUS	Output bus setting
	4	***0****	INPUTRANG	Input range setting
	3	****0***	REVERSE	Input inverted setting
	2:0	*****000	MODE	Operation mode setting
1H	7:0	00000000	OFF0	CCDIN0 offset setting
2H	7:0	00000000	OFF1	CCDIN1 offset setting
3H	7:0	00000000	OFF2	CCDIN2 offset setting
4H	6:0	*0000000	GAIN0	CCDIN0 gain setting
5H	6:0	*0000000	GAIN1	CCDIN1 gain setting
6H	6:0	*0000000	GAIN2	CCDIN2 gain setting
7H	1:0	******00	DIRECT	DC direct mode setting register

Address “08H”~”0EH” is test register. Please do not access the test register.

Operation mode setting（Address “00H”） Reset *000 0000

Please set “0” to test register

Output mode setting register

BUS	Output mode
0	8bit bus mode
1	4bit bus mode

Input range change register

Input Range	Input range
0	1.764V
1	2.341V

Input inverted mode register

Reverse	Input mode
0	Input downstream from VCLP
1	Input upstream from VCLP

Operation mode setting

MODE	Operation mode
000	Power down
100	3ch
101	2ch（0, 1ch active）
110	2ch（1, 2ch active）
111	2ch（0, 1ch active）
Other	Inhibition

(*) Unused input pin be Hi-z by 2ch mode.

Offset setting（Address “01H”～ “03H”） Reset 0000 0000

01H CCDIN0 offset setting

02H CCDIN1 offset setting

03H CCDIN2 offset setting

OFF*[7:0]	Offset
	Normal range
0111 1111	＋321.0mV
0111 1110	＋318.5mV
・・・	・・・
0000 0001	＋2. 5mV
0000 0000	0
1111 1111	－2. 5mV
・・・	・・・
1000 0001	－321.0mV
1000 0000	－323.5mV

Note1) At an offset of +2.5 mV, the signal fraction is corrected toward 2.5 mV subtraction.

Note2) The value for the normal range input.

By large range, 1.093 times x normal range.

By DC direct mode, 0.956 times x normal range.

Gain setting（Address “04H”～ “06H”） Reset *000 0000

04H CCDIN0 gain setting

05H CCDIN1 gain setting

06H CCDIN2 gain setting

GAIN*	gain
000 0000	0
000 0001	0. 06 dB
000 0010	0. 13 dB
・・・	・・・
111 1110	20. 58 dB
111 1111	21. 28 dB

Note) Gain is expressed by the following equations.

This value is relative gain from “000 0000” setting

$$Vout = \frac{204}{12 + (127 - x)} \times Vin$$ （$x = 0$ ～ 127） Input range＝1. 764V

$$Vout = \frac{168}{12 + (127 - x)} \times Vin$$ （$x = 0$ ～ 127） Input range＝2. 341V

Operation mode setting 2（Address “07H”） Reset **** **00

DC direct mode setting register

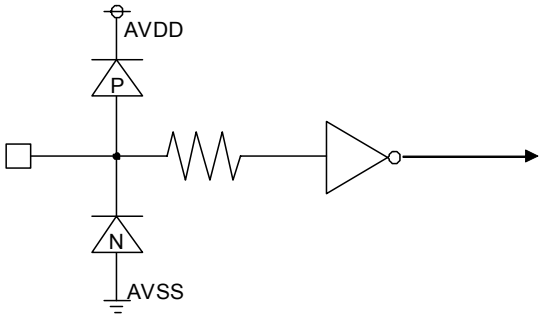
DIRECT	
00	CDS mode, Clamp mode
11	DC direct mode

When DC direct mode setting, internal VCLP pin connect GND via 12kΩ.

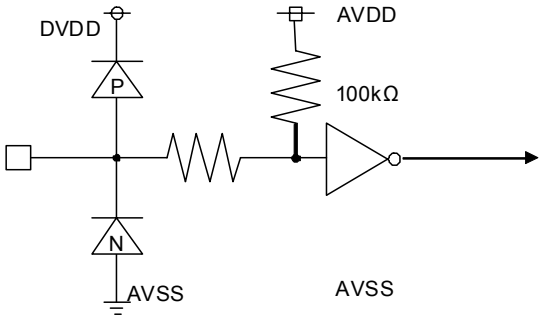
IO Pin Connection Information

Input Output equivalent circuit

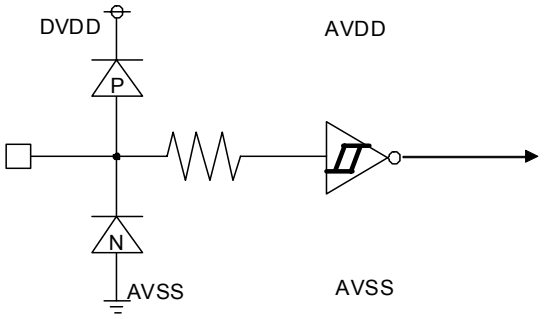
SHR, SHD, MCLK



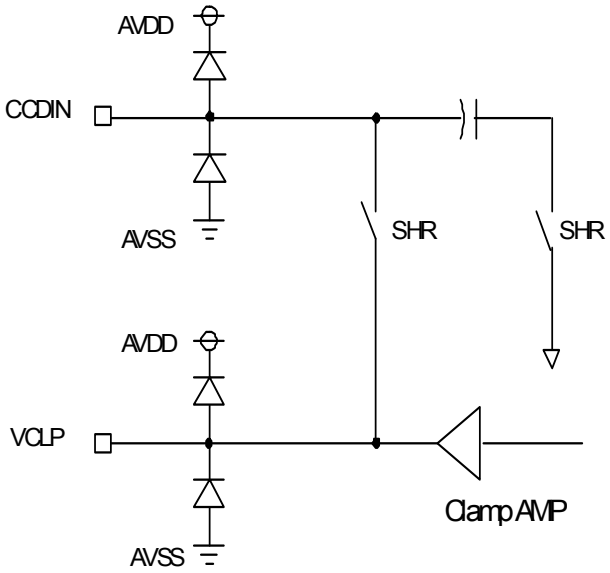
RESETB



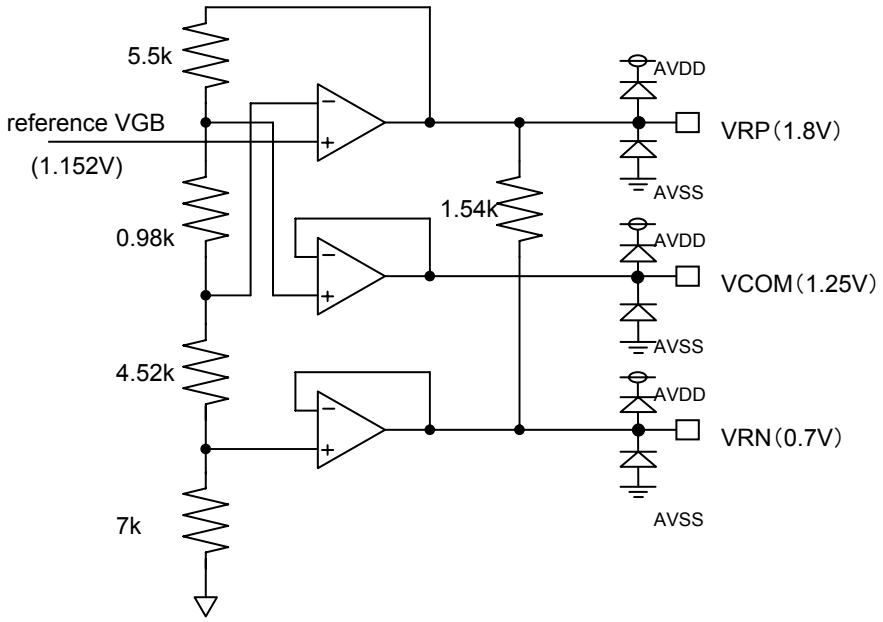
SDENB



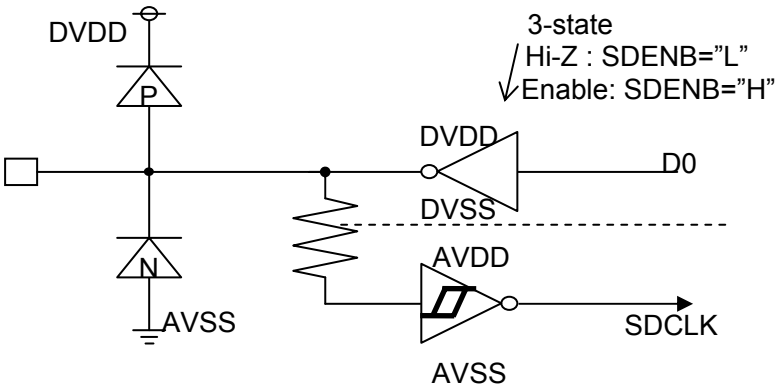
CCDIN, VCLP



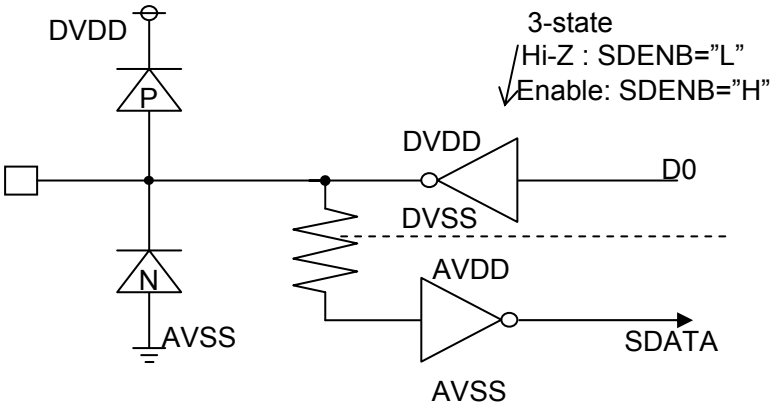
VRP, VCOM, VRN



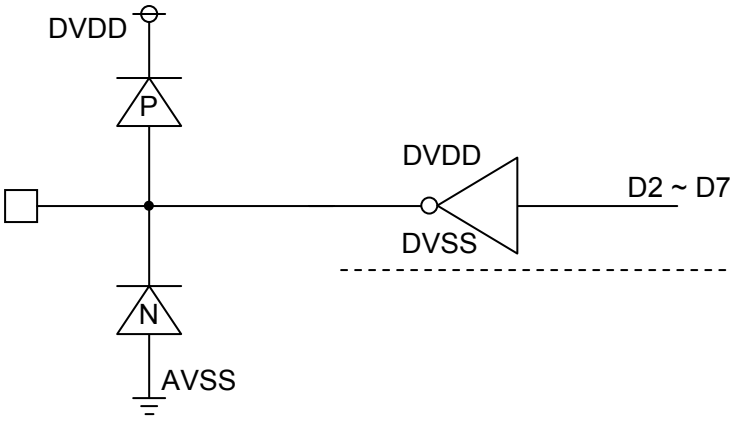
D0



D1

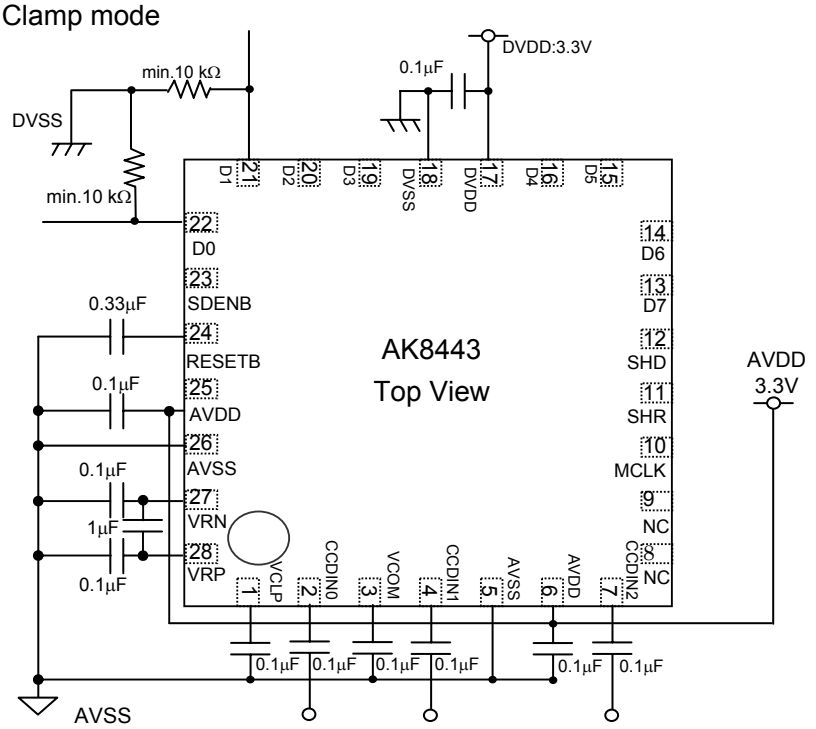


D2 ~ D7

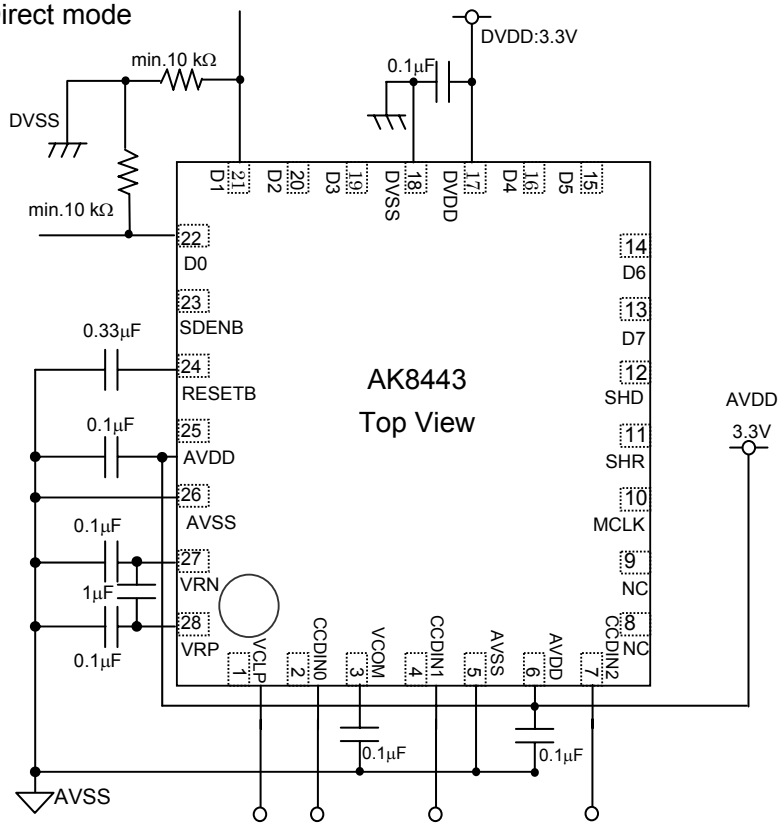


External circuit example

CDS, Clamp mode



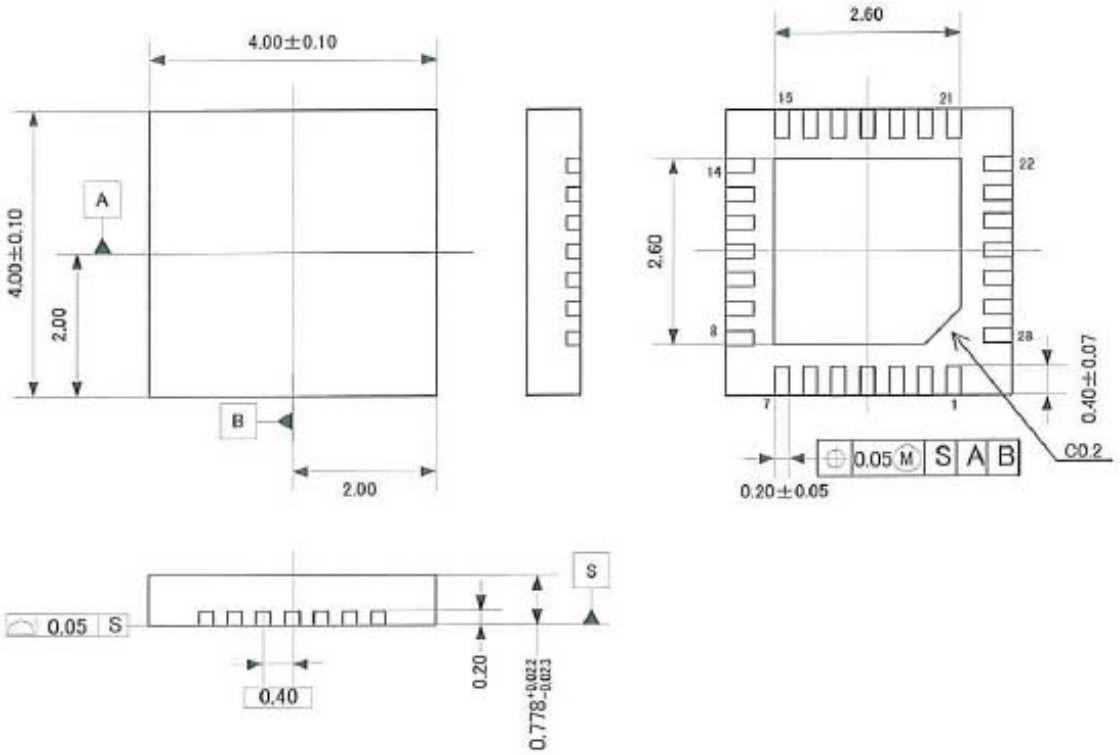
DC Direct mode



* The radiation PAD on the package solder side connects with analog ground (AVSS).

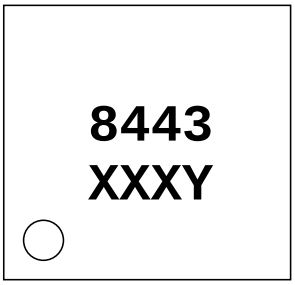
Package

■ Package dimension unit [mm]



■ Marking

1. Marketing code :8443
2. Date code :XXX Week code
   :Y The company management code



Marking

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