AsahiKASEI
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AK8451

1 channel-input 16 bit 6MSPS ADC

Device Outline

■AFE Block

The AK8451 is a +3.3 V, Two Channel 16 Bit 6MSPS ADC which integrates on-chip Offset Adjust DAC, Gain Adjust PGA, CDS circuit and <4.5~5.7V> 3 channel LED Drivers.

■ LED Driver Block

This product is the 3 channel LED driver who drives the LED of the anode common in the constant current. The current to pass for each channel can be adjusted by the external resistance and the register setting. Also, it has the control pins which turn on or off the current.

Features

■AFE Block

- ☐ CCD I/F
  - Number of Channels: 1 channel
  - Range: 1.98 Vpp (typ.)
  - Signal Input Range: 0~3.3V @ DC Direct Coupled input mode at AVDD = 3.3 V
  - Integrated On-chip CDS circuit
  - Compatible with both Positive and Negative signal polarities
- ☐ ADC
  - Maximum Conversion Rate: 6 MSPS
  - Resolution: 16 Bit (Straight Binary Code)
- ☐ Black Level Correction DAC
  - Correctable Range: ± 240 mV (typ.)
  - Resolution: 8 Bit
- ☐ Gain Adjust
  - Adjustable Range: 0 dB ~ +13.9 dB (typ.) (1.0× ~ 4.9×)
  - Resolution: 6 Bit
- ☐ Total Performance (Input ~ Video ADC)
  - Output Noise: 5 LSBs rms (typ.) @ PGA Gain = 0 dB setting
- ☐ Data Output: 2 bit wide or 4bit wide
- ☐ Power Supplies
  - Analog part: +3.3V ±5 % / Digital Output part: +3.3V ±0.3V
- ☐ CPU I/F: 3-Wire Serial Interface (Write Only)
  - Clock, Data are commonly shared with A/D Data Output pins
- ☐ Power Dissipation
  - 132mW (typ.) with DC Direct Coupled input mode at AVDD= 3.3V
- ☐ Operating Temperature Range: 0 °C ~ +70 °C
- ☐ Package: 28 Pin QFN
  - Pin pitch: 0.4 mm, Mold size: 4 mm × 4 mm
- ☐ VREF Output for CCD: 1.1V±100mV。10mAmax.

■ LED Driver Block

☐ Operation Voltage(LVDD)	4.5V~5.7V
☐ Absolute Maximum Voltage	6.5V
☐ Operating Temperature Range	0 ~ 70°C
☐ LED driver current	RED：60mA(Adjustment external resister:20m~60mA) GREEN: (Programmable: RED-29% ; 4.17% step) BLUE: (Programmable: RED-29% ; 4.17% step) Usable Vf range of the LED is from 1.5V to <LVDD-0.5V>. The resistance for the current regulation is usable in 1/16W -type. The number of channels of applying an current to the LED is at the same time to one or two. When the external resistance value becomes the assumption outside, it has the protection circuit which doesn't make the electric current which flows through the LED equal to or more than 150mA±30%.
☐Rch Current Accuracy	53 ~ 67mA(at 60mA setting)
☐LED Current rise / fall time	less than 10μs (10%←→90%)
☐LED Vf Range	<1.5V>(min.) ～ <LVDD-0.5V>(max.)
☐Application	A light source driver for CIS module of MFP

Block Diagram

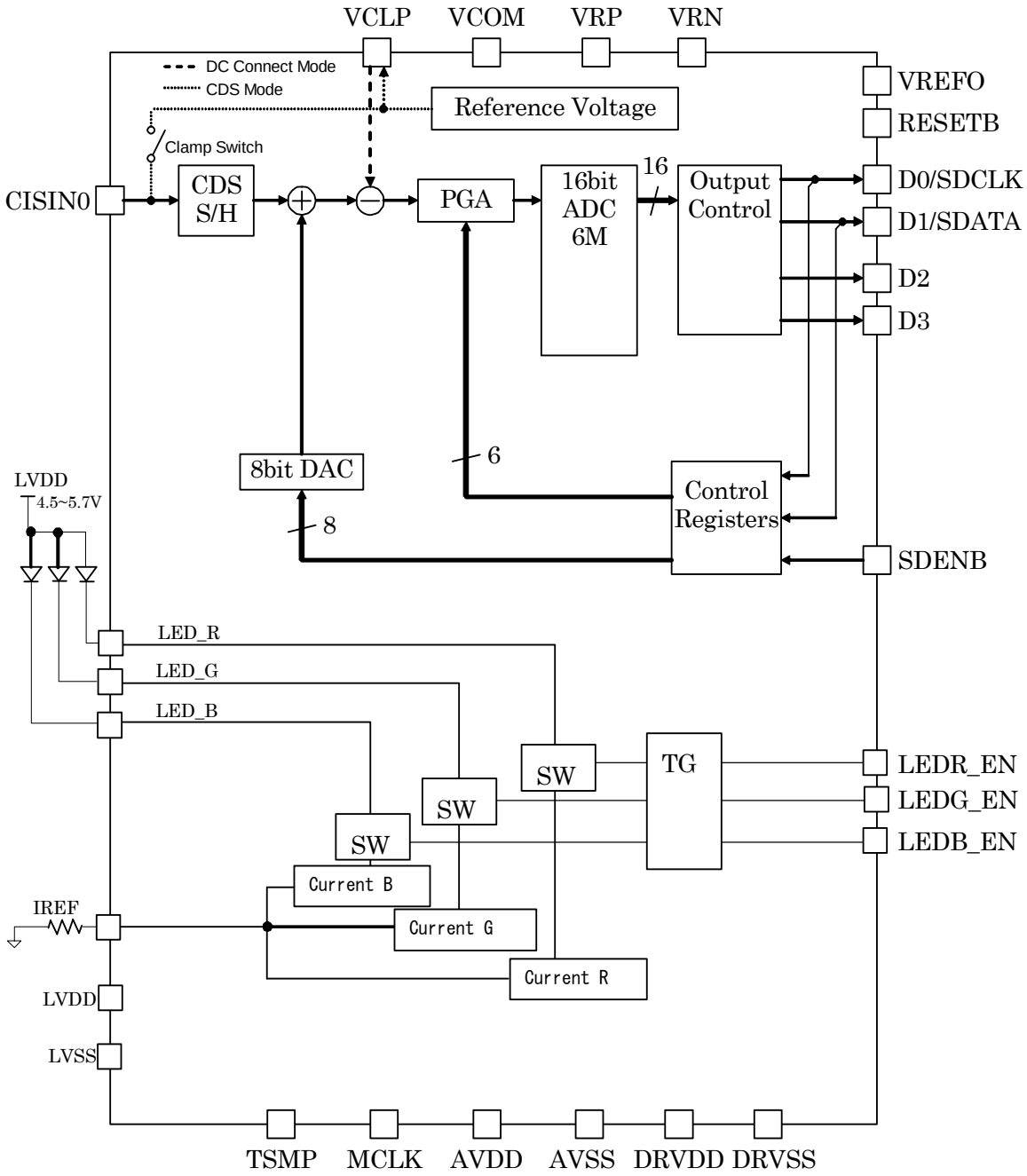


Fig. 1 Block diagram

Pin Functions

No.	Name	IO	PD	Description
1	IREF	I		LED current setting external resister pin
2	VREFO	O	Hi-Z	Reference voltage output :1.1V External capacitor : 0.33μF
3	CISIN0	I		Sensor Signal input
4	VCLP	IO	(note 2)	Sensor Reference Level input at DC Direct Coupled mode Clamp Level output at CDS mode (external Cap.: 0.1μF)
5	NC	-		Unused(note 1)
6	AVSS	PWR		Analog ground
7	AVDD	PWR		Analog power supply
8	LED_R	O	Hi-Z	LED output pin R
9	LVDD	PWR		LED power supply
10	LVSS	PWR		LED ground
11	LED_G	O	Hi-Z	LED output pin G
12	LED_B	O	Hi-Z	LED output pin B
13	LEDR_EN	I		LED control input R
14	LEDG_EN	I		LED control input G
15	LEDB_EN	I		LED control input B
16	D0/SDCLK	IO	(note 3)	SDENB=High ; A/D Data output : Lower Bit (D0) SDENB=Low ; Serial Interface Clock input
17	D1/SDATA	IO	(note 3)	SDENB=High ; A/D Data output : Lower Bit (D1) SDENB=Low ; Serial Interface Data input
18	DRVSS	PWR		A/D Output buffer ground
19	DRVDD	PWR		A/D Output buffer power supply
20	D2	O	H or L (note4)	A/D Data output : D2 Bit
21	D3	O	H or L (note4)	A/D Data output : Upper Bit (D3)
22	SDENB	I		Serial Interface Enable
23	MCLK	I		Main Clock
24	TSMP	I		Sampling Timing
25	RESETB	I		Reset pin : Active Low, on chip pull-up resister : 100kΩ (typ.)
26	VCOM	O	Hi-Z	Internal Reference Voltage : external capacitor 0.1μF
27	VRN	O	L (note 5)	ADC Negative Reference Voltage : external capacitor 0.1μF
28	VRP	O	L (note 5)	ADC Positive Reference Voltage : external capacitor 0.1μF

I: input , O: output , PWR: power/ground pin

(note 1)Please connect it with analog ground on the board.

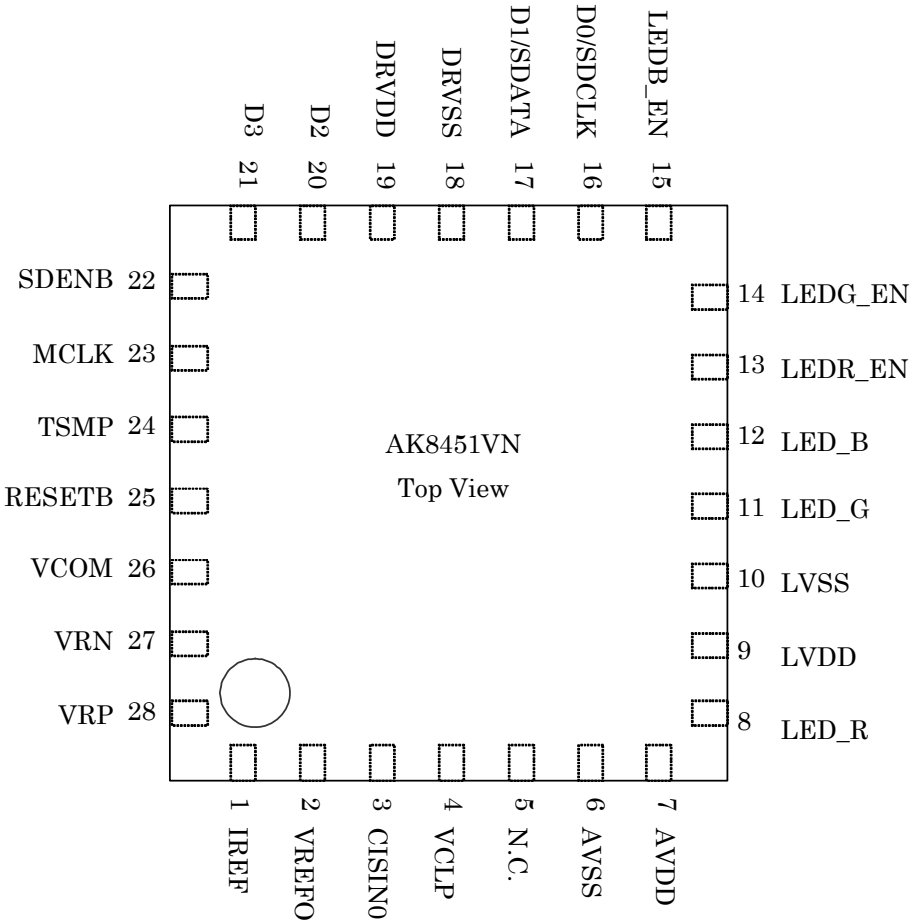
(note 2)It will be input on DC mode, be Hi-Z on CCD mode.

(note 3)Please be input state.

(note 4)It will be H or L since PD mode.

(note 5)It is connect with AVSS via internal resistance.

Pin Allocation



Circuit Block Description

■ Sensor Interface Part

Circuit to sample & hold input signal which is fed on CISIN0 pin. Signal input range is 1.98V (typ.). There are two input modes, DC Direct Coupled Mode and CDS Mode. In DC Direct Coupled Mode, Positive polarity signal is handled. In CDS Mode, Negative polarity signal is handled. Signal Reference Voltage should be input on VCLP pin in DC Direct Coupled mode. In CDS mode, Voltage level to clamp signal is internally generated and it is output on VCLP pin.

■ Black Level Correction Circuit

Circuit to add an offset voltage to the sampled signal level. Voltage range of DAC which generates Offset is ±240 mV (typ.) and its resolution is 8 Bit.

■ PGA Part

Circuit to adjust signal amplitude, prior to AD conversion. Adjustable gain range is from 0dB to 13.9dB (typ.) (1.0× ~ 4.9×) and its resolution is 6 Bit.

■ ADC Part

AD conversion circuit to convert into Digital data an Analog signal after both Black level correction and Gain adjustment are made. Its resolution is 16 Bit with its maximum conversion rate of 6MSPS. Data output is in a straight Binary code. 0000h is output at Black level input (0Vpp input) and FFFFh is output at White level input (maximum input).

■ Output Control Part

A 16 Bit-wide × 1ch ADC output data is re-arranged into 2 Bit × 8 cycle×1ch or 4Bit × 4cycle×1ch stream at this part. In Single Edge Mode operation, Data is output at the rising edge of MCLK. In Double Edge Mode operation, it is output at both rising and falling edges of MCLK. Output mode is 2bit or 4bit by single mode, only 2bit on double mode. Particulars is on P34 & P35.

■ Reference Voltage Generator

Circuit to generate internal reference voltages. Clamp Reference Voltage VCLP, internal common voltage VCOM and ADC reference voltages VRP and VRN are generated. Each reference voltage is output on respective device pins. For voltage stabilization, capacitors should be connected between respective pins and AVSS.

■ LED Driver Part

This product generates has 3 channel LED driver to drive RGB constant current. Use the ON/ OFF digital terminal to control the constant current.

■ Serial Interface Part

A 3-Wire Interface circuit to access setting-registers. SDCLK (clock) and SDATA (data) pins are shared with D0 and D1 pins of ADC Data Output. When SDENB pin is at low, D0 and D1pins function as SDCLK and SDATA input pins. In order to avoid both SDCLK and SDATA pins to become floating condition, proper pull-down resistors should be connected between D0 / SDCLK pin, D1 / SDATA pin and AVSS respectively.

Absolute Maximum Ratings

Voltages are referenced to corresponding ground level. AVSS = DRVSS = 0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supplies					
Analog power supply	AVDD	–0.3	4.5	V	
Output buffer power supply	DRVDD	–0.3	4.5	V	
LEDD power supply	LVDD	–0.3	6.5	V	
Digital Input Voltage	VTD	–0.3	AVDD+0.3	V	
Analog Input Voltage	VTA	–0.3	AVDD+0.3	V	
Storage temperature	Tstg	–65	150	°C	

Operation under a condition exceeding above limits may cause permanent damage to the device. Normal operation is not guaranteed under the above extreme conditions.

Recommended Operating Conditions

Voltages are referenced to corresponding ground level. AVSS = DRVSS = 0V

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supplies						
Analog power supply	AVDD	3.135	3.3	3.465	V	
Output buffer power supply	DRVDD	3.0	3.3	3.6	V	
LEDD power supply	LVDD	4.5	5.5	5.7		
Operating temperature	Ta	0		70	°C	

Please power on AVDD and LVDD the same time or AVDD first.

Electrical Characteristics

■ DC characteristics

(AVDD=3.135~3.465V, DRVDD=3.0~3.6V, Ta=0~70°C, unless otherwise specified)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Remarks
H level input voltage	VIH	Note 1,2 Note 4,5	0.7× AVDD			V	
L level input voltage	VIL	Note 1,2 Note 4,5			0.3× AVDD	V	
H level output voltage	VOH	Note 3	0.7× DRVDD			V	IOH= –2mA
L level output voltage	VOL	Note 3			0.3× DRVDD	V	IOL=2mA
Input leakage current 1	IL1	Note 1,5	–10		10	μA	
Input leakage current 2	IL2	Note 2	–69.3		10	μA	apply 0V ~ AVDD
High-Z leakage current	ILZ	Note 4	–10		10	μA	
Pull-up resistor	RPU	Note 2	50	100	150	kΩ	

(Note 1) TSMP, MCLK, SDENB
(Note 2) RESETB
(Note 3) D0, D1 (at SDENB=High), D2, D3
(Note 4) SDATA, SDCLK (at SDENB = Low)
(Note 5) LEDR_EN, LEDG_EN, LEDB_EN

■ AFE block, Analog characteristics

(AVDD=3.3V, DRVDD=3.3V, MCLK=40MHz,Single Edge Mode, Ta=25°C, unless otherwise specified)

Item	Min.	Typ.	Max.	Unit	Remarks
Reference voltage					
VCOM voltage	1.4	1.5	1.6	V	
VRP voltage	1.9	2.0	2.1	V	
VRN voltage	0.9	1.0	1.1	V	
VREF voltage	1.0	1.1	1.2	V	Band Gap error
at current sink error			+0.1	V	@ I=10mA (diff. @I=0mA)
at current source error	-0.1			V	@ I=-10mA(diff. @I=0mA)
Analog input					
Maximum signal input level		1.98		$V_{p\text{-}p}$	
Absolute gain	–0.7	0	0.7	dB	At DC mode (Note 1)
	–1.50	–0.60	0.30	dB	At CDS mode (Note 1)
Sampling rate	1		6	MSPS	
Input reference level	0	1.1	1.5	V	At DC mode
VCLP input resistence	10	60		kΩ	At DC mode
Input signal range	0		AVDD	V	At DC mode (Note 2)
Clamp level (VCLP voltage)	1.98	2.08	2.18	V	At CDS mode
Clamp resister		7	10	kΩ	At CDS mode
CDS advantage		-40		dB	(note 11)
Black level correction DAC					
Resolution		8		bit	(Note 3)
Correctable range	±215	±240	±265	mV	(Note 4)
Internal offset voltage	–50		50	mV	(Note 5)
PGA(Programmable Gain Amp.) circuit					
Resolution		6		bit	
Min. gain		0		dB	
Max. gain	13.3	13.9	14.5	dB	(Note 7)
Video ADC					
Resolution		16		bit	
DNL	–16		+16	LSB	
INL	-96	±32	+96	LSB	
Noise					
Output noise		6		LSB_{rms}	PGA min.
		16		LSB_{rms}	PGA max.
Power Consumption					
Analog part power dissipations		31.5.	47	mA	At DC mode (Note 7)
		35.5	52	mA	At CDS mode (Note 7)
			0.1	mA	At power down (Note 8)
Digital output driver power dissipation		3	6	mA	(Note 9)

(Note 1) 0dB is defined at the gain where ADC output reaches its full-scale when 1.98Vpp signal is input with PGA setting at 00h.

(Note 2) At 2 bit bus mode.

(Note 3) CISIN0 input signal must be in this range which is referenced to AVSS.

(Note 4) Monotonicity guaranteed.

(Note 5) ±50 mV of the total correctable range is used for internal offset adjustment.

(Note 6) It defines that a boundary point of ADC output codes between 0000h and 0001h exists within ±50mV range of the offset adjustment DAC setting when 1.1V is fed on CISIN & VCLP pins in DC Direct Coupled mode, and when PGA gain is set to 0dB.

(Note 7) Relative value to the gain at PGA setting is 00h.

(Note 8) A full-scale minus 2 dB, 1 MHz sine-wave signal is input. (@ 4bit bus)

(Note 9) A clock supply to MCLK is stopped.

(Note 10) At the capacitive load is 20pF.

(Note 11) Condition: Input signal frequency : 1MHz, Noise frequency : 0.1MHz, Signal : Noise = 10:1.No shipping inspection.

■ LEDD block, Analog characteristics

(AVDD=3.3V, LVDD=5.5, MCLK=40MHz, Single Edge Mode, Ta=25°C, unless otherwise specified)

Item	Min.	Typ.	Max.	Unit	Remarks
LED drive current range	20		60	mA	
The LED protection circuit activation current	105	150	195	mA	
LED current (Including resistance accuracy) (RED)	53	60	67	mA	← There is possibility to adjust the typical value after ES evaluation. It adjusts together with the Min./Max. value. IREF resister =4.7k±1% LED pin voltage =2.0V(Note 1)
LED current					IREF resister =4.7k±1%
Red		100		%	LED pin voltage =2.0V
Green	95		105	%	
Blue	95		105	%	
LED current accuracy					LED pin voltage =0.5V
(GREEN,BLUE)		100		%	000
	94.8	95.8	96.8	%	001
	90.7	91.7	92.7	%	010
	86.5	87.5	88.5	%	011
	82.3	83.3	84.3	%	100
	78.2	79.2	80.2	%	101
	74.0	75.0	76.0	%	110
	69.8	70.8	71.8	%	111
LED current LED pin voltage dependence	-2.5		2.5	%	LED pin voltage =2.0V reference
LVDD power consumption		0.6	1.5	mA	Except LED drive current

(Note 1) IREF resister(kΩ) = 60 ÷ [RED LED current(mA)] × 4.7(kΩ) . And [RED LED current] can be set within the range of 20mA～60mA .

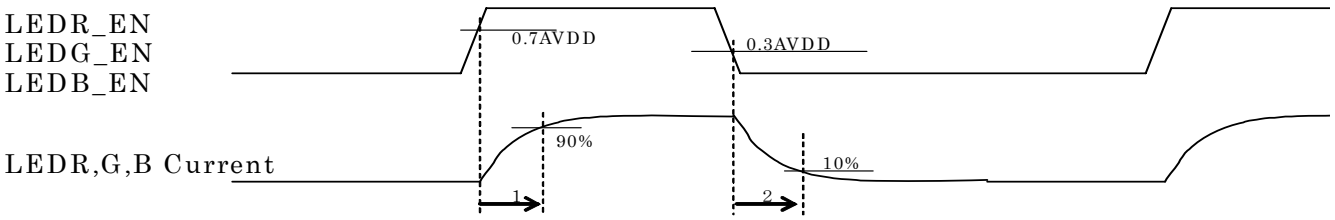
(AVDD=3.135~3.465V, LVDD= 4.5~5.7 V, Ta=0~70°C, unless otherwise specified)

Item	Min.	Typ.	Max.	Unit	Remarks
LED pin voltage	0.5			V	
LED Vf	1.5		4.8	V	When LVDD<5.3V case, Vf(max.)=LVDD-0.5V

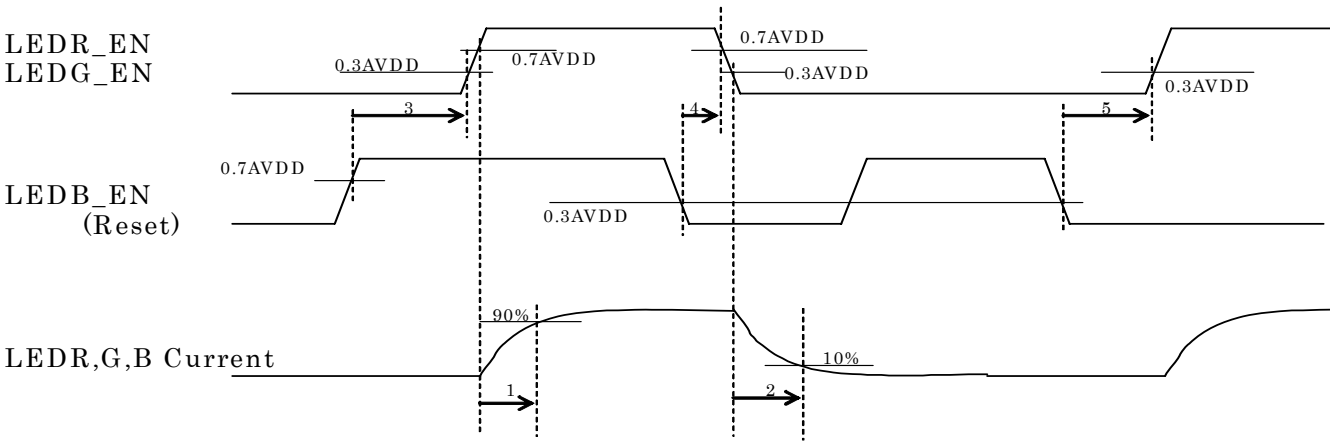
■ LEDD block, Switching characteristics

(AVDD=3.135~3.465V, LVDD= 4.5~5.7 V, Ta=0~70°C, unless otherwise specified)

No.	Item	min.	typ.	max.	Unit	Condition
1	LED current rise time			10	μsec	
2	LED current fall time			10	μsec	
3	Reset valid setup time LEDB_EN(0.7AVDD):base position	0.1			μsec	LEDB_EN(0.7AVDD) To LEDR_EN(0.3AVDD) LEDG_EN(0.3AVDD)
4	Count up setup time LEDB_EN(0.3AVDD):base position	0.1			μsec	LEDB_EN(0.3AVDD) To LEDR_EN(0.7AVDD) LEDG_EN(0.7AVDD)
5	Reset invalid setup time LEDB_EN(0.3AVDD):base position	0.1			μsec	LEDB_EN(0.3AVDD) To LEDR_EN(0.3AVDD) LEDG_EN(0.3AVDD)



- LED*_EN through mode



- Except the through mode

■ AFE block, Switching characteristics

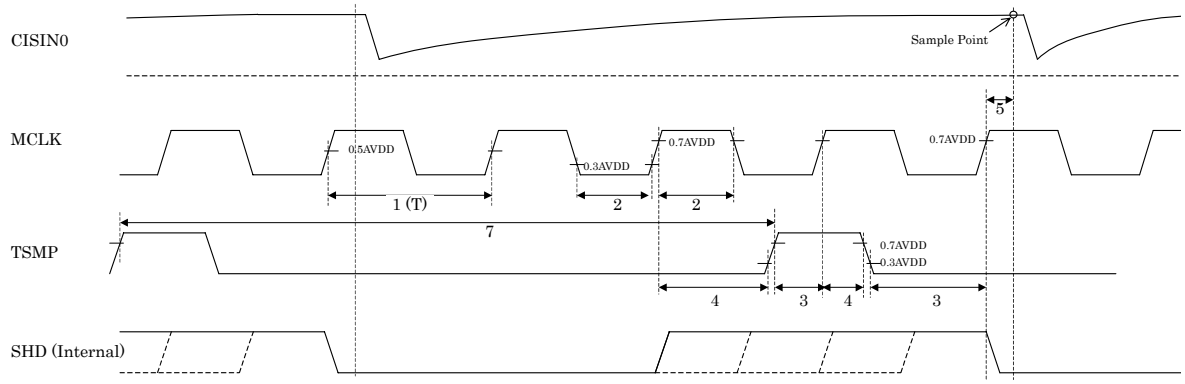
(AVDD=3.135~3.465V, DRVDD=3.0~3.6V, Ta=0~70°C , unless otherwise specified)

No.	Item	pin	min.	typ.	max.	unit	Condition
1	MCLK cycle time (T)	MCLK	41.6		250	ns	mode 1(note 2)
			20.8		125		mode 2(note 2)
			41.6		250		mode 3(note 2)
2	MCLK H / L width	MCLK	20.8			ns	mode 1(note 2)
			10.4				mode 2(note 2)
			20.8				mode 3(note 2)
3	TSMP setup time (referenced to MCLK↑)	TSMP	5			ns	Note 1
4	TSMP hold time (referenced to MCLK↑)	TSMP	5			ns	Note 1
5	Aperture delay (referenced to MCLK↑)	CISIN		2		ns	Data level
6	Aperture delay (referenced to MCLK↑)	CISIN		2		ns	Reference level
7	TSMP cycle (MCLK period-unit)	TSMP		4T			mode 1(note 2)
				8T			mode 2(note 2)
				4T			mode 3(note 2)
8	Data output delay (referenced to MCLK↑)	D0, D1,D2,D3					At load: 20pF Drivability
			2		25	ns	: normal mode
			2		20	ns	: x2 mode
9	Pipeline delay (SMP period-unit)	D0, D1,D2,D3		6			At 4bit bus
				5			At 2bit bus
10	Reset pulse width	RESETB	50			ns	

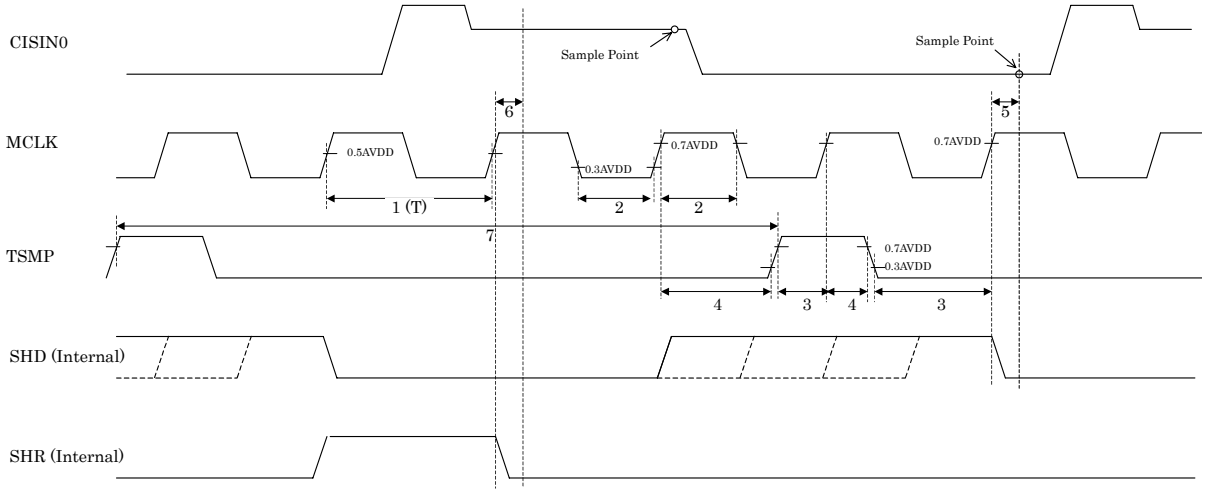
Note 1) Number of MCLK rising edges during TSMP = H duration is allowed to be 1 to 3 times in Single Edge, 2bit bus Mode operation, and only a single edge is allowed in the other mode operation.

Note 2) mode 1 ~ mode 3 explanation

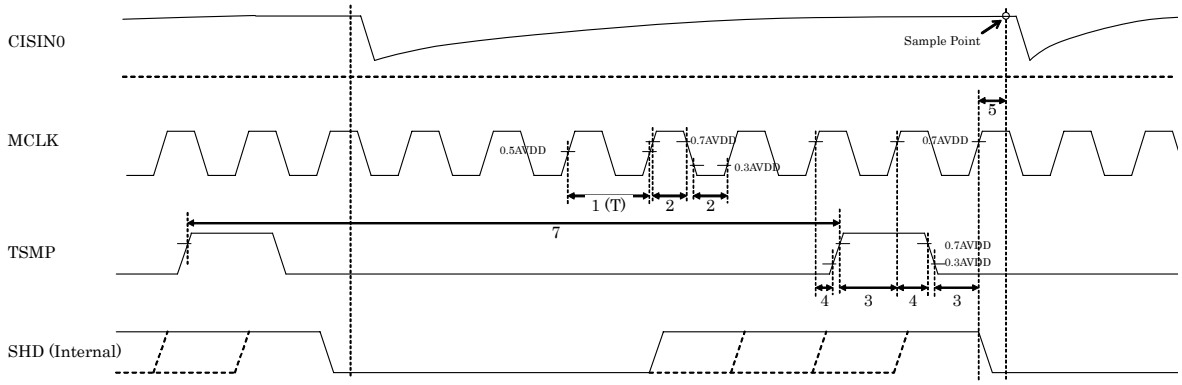
mode 1 : single edge/ 4bit bus mode
mode 2 : single edge/ 2bit bus mode
mode 3 : double edge/ 2bit bus mode



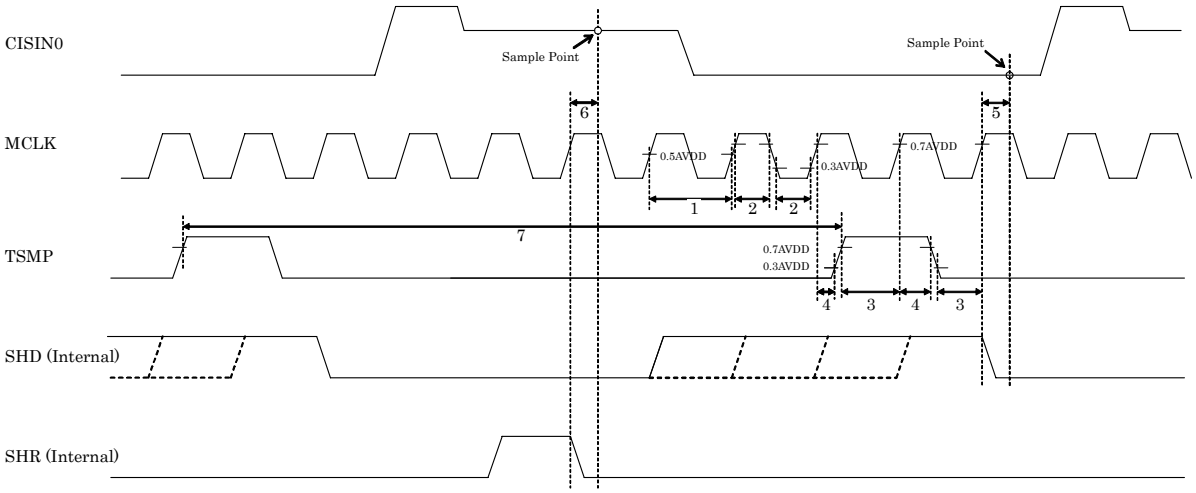
Sampling timing (DC mode, AFE 1ch, Single edge, 4 bit bus mode)



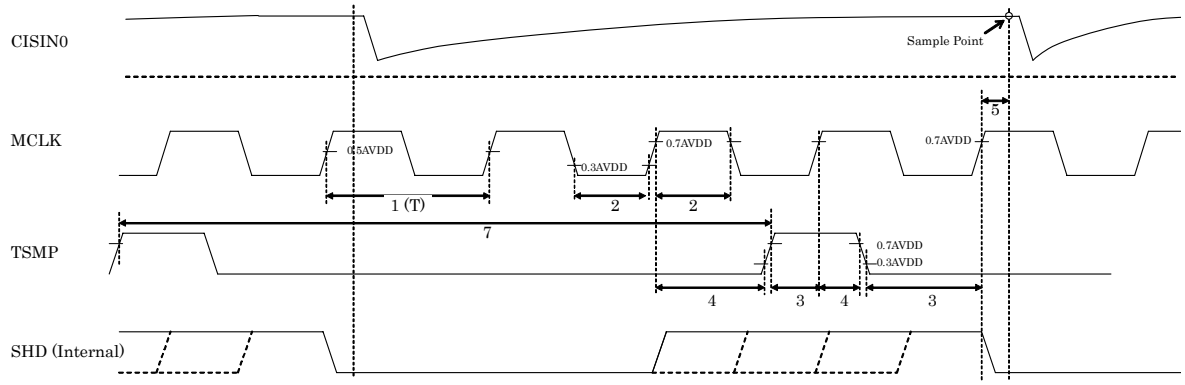
Sampling timing (CDS mode, AFE 1ch, Single edge, 4 bit bus mode)



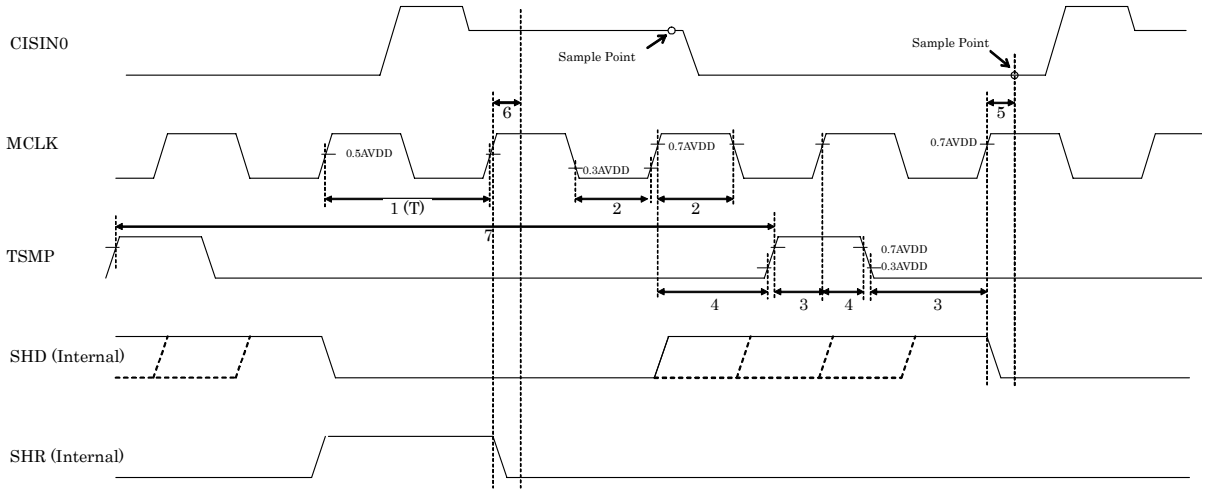
Sampling timing (DC mode, AFE 1ch, Single edge, 2 bit bus mode)



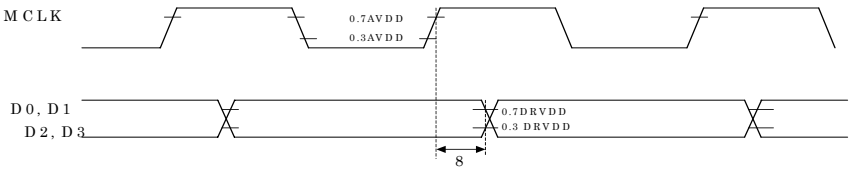
Sampling timing (CDS mode, AFE 1ch, Single edge, 2 bit bus mode)



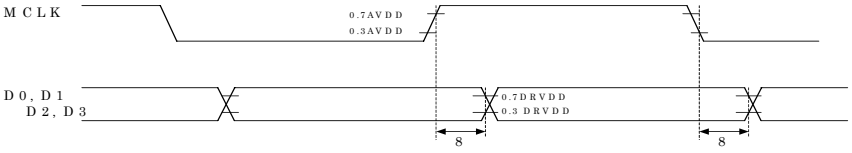
Sampling timing (DC mode, AFE 1ch, Double edge, 2 bit bus mode)



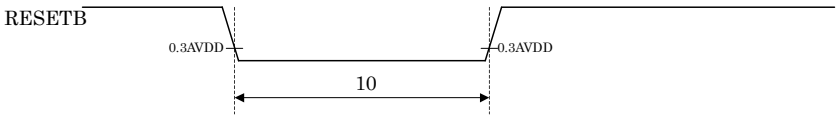
Sampling timing (CDS mode, AFE 1ch, Double edge, 2 bit bus mode)



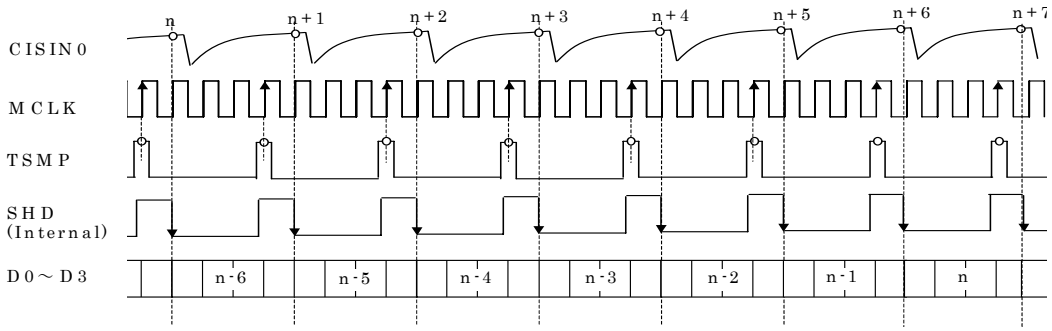
Data output timing (Single edge mode)



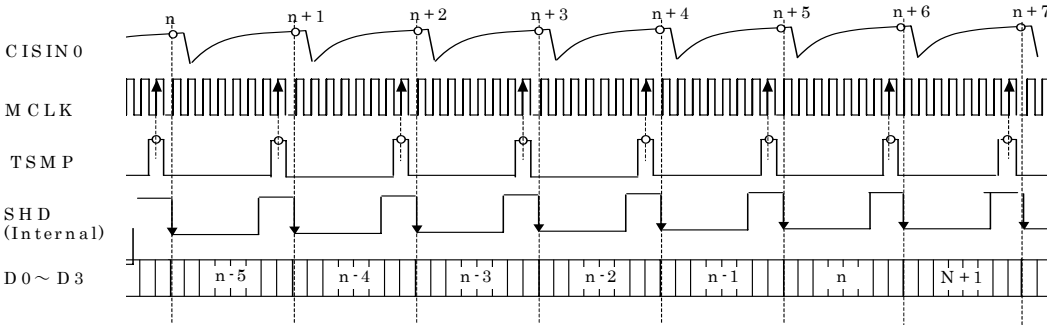
Data output timing (Double edge mode)



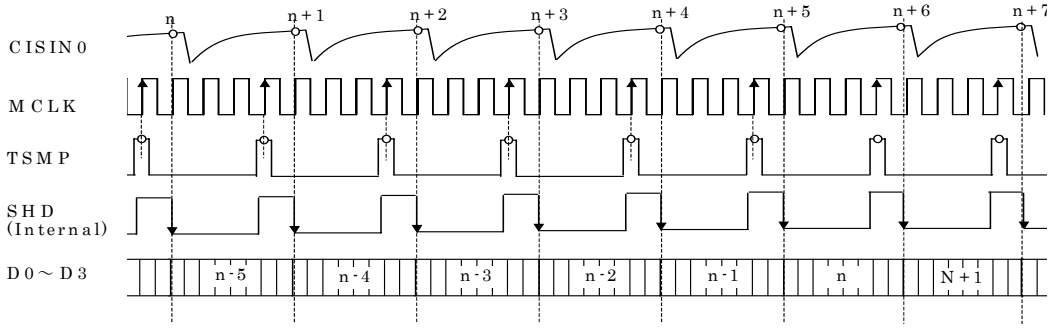
Reset pulse width



Pipeline delay (AFE 1ch, Single edge, 4 bit bus mode)



Pipeline delay (AFE1ch, Single edge, 2 bit bus mode)

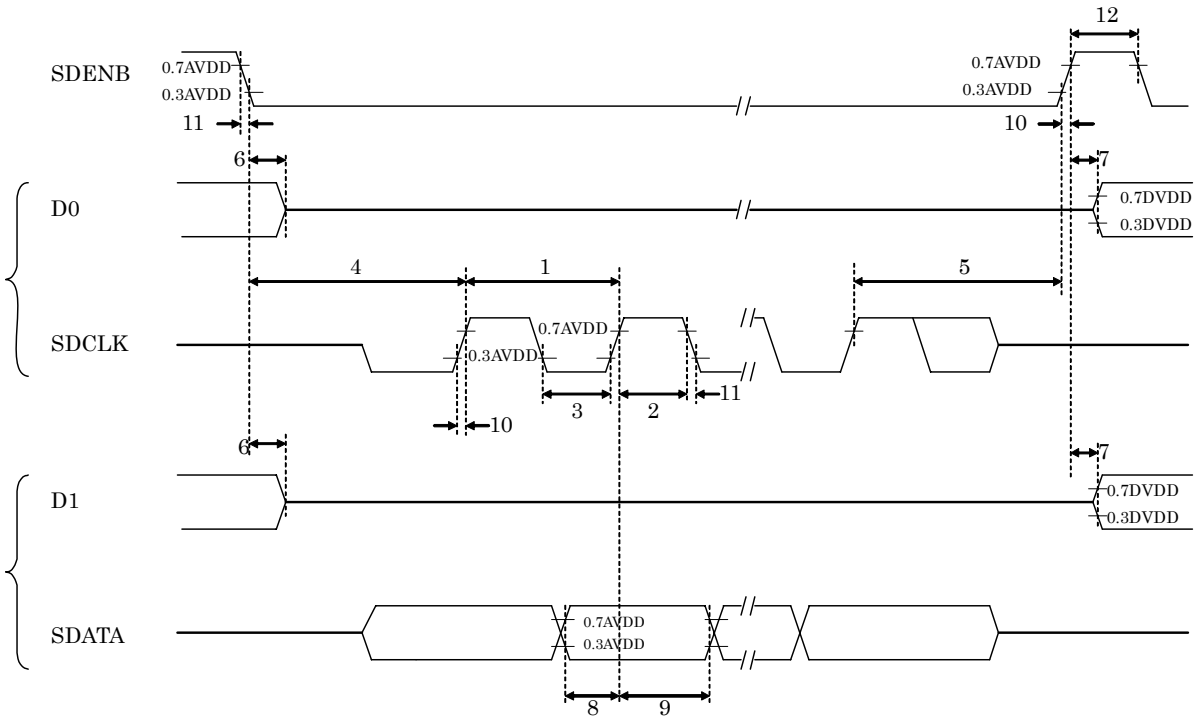


Pipeline delay (AFE1ch, Double edge, 2 bit bus mode)

■ Serial interface: Switching characteristics

(AVDD=3.135~3.465V, DRVDD=3.0~3.6V ,Ta= 0~70°C , unless otherwise specified)

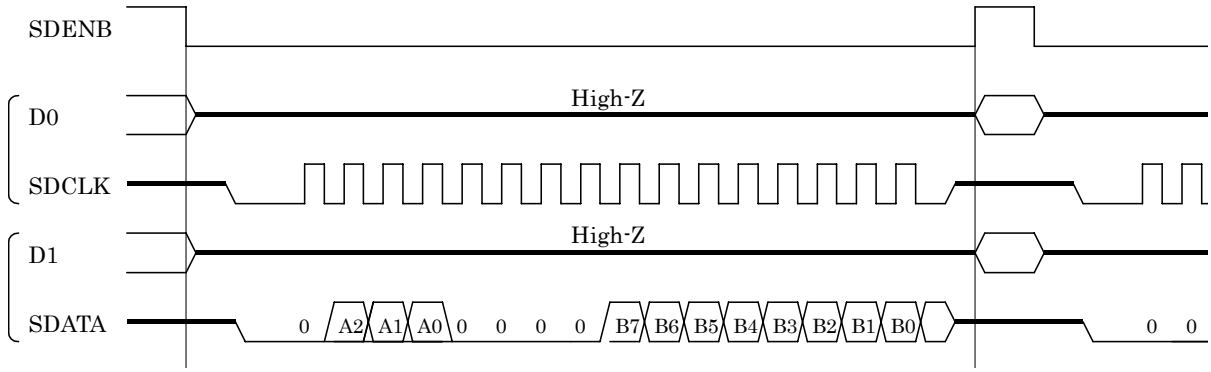
No.	Item	pin	Min.	Typ.	Max.	unit	Condition
1	Clock Period	SDCLK	0.1		10	MHz	
2	Clock Pulse Width (H duration)	SDCLK	40			ns	
3	Clock Pulse Width (L duration)	SDCLK	40			ns	
4	SDENB setup time (to SDCLK rising edge↑)	SDENB	80			ns	
5	SDENB hold time (from SDCLK rising edge↑)	SDENB	80			ns	
6	Data High-Z delay (from SDENB falling edge↓)	D0, D1	0		40	ns	
7	Data Enable delay (from SDENB rising edge↑)	D0, D1	0		40	ns	
8	SDATA setup time (to SDCLK rising edge↑)	SDATA	40			ns	
9	SDATA hold time (from SDCLK rising edge↑)	SDATA SDENB	40			ns	
10	SDCLK,SDENB Rise time	SDCLK SDENB			6	ns	
11	SDCLK,SDENB Fall time	SDCLK SDENB			6	ns	
12	SDENB High level pulse width	SDENB	40			ns	



Serial interface timing

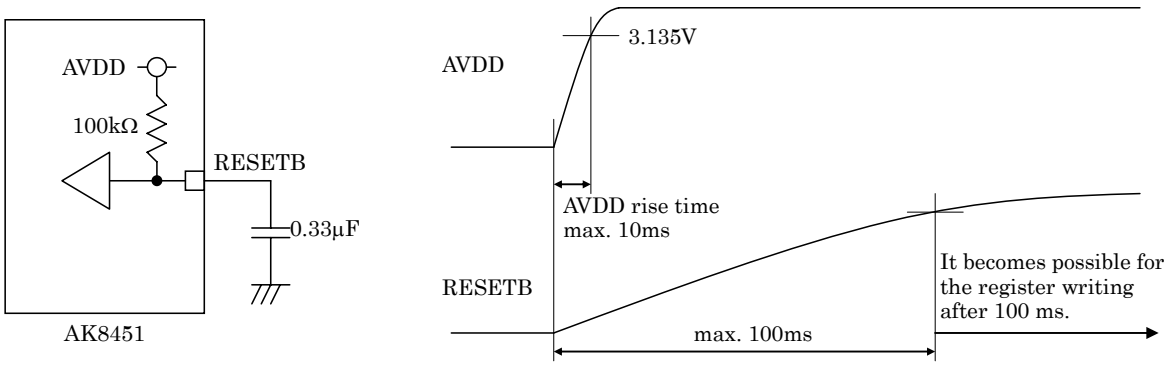
Clock Input pin SDCLK and Data Input pin SDATA for Serial Interface are shared with A/D Data Output pins, D0 and D1 respectively. When SDENB becomes low, D0 and D1 are put into High-Z conditions and it is enabled to input SDCLK and SDATA. SDATA is captured at the rising edge of SDCLK. SDATA is 16 Bit long. Write "zeros" first bit and from the 5th Bit to the 5th

Bit. 2nd~4th Bits are assigned for Register Address where the 2nd Bit is MSB and the 4th Bit is LSB. 9th~ 16th Bits are assigned for Data where the 9th Bit is MSB and the 16th Bit is LSB.
16 and more rising edges of SDCLK are required while SDENB is low, from the time to fall to the time to rise. When it is less than 16 rises, registers will not be written properly.
If it is more than 16 rises while SDENB is low, from falling to rising, the last 16 edges become effective. There is a possibility that an erroneous data will be written into registers if noises occur on D0 Output / SDCLK input pin and D1 Output / SDATA input pin when these pins are at High-Z conditions. To avoid this, resistors should be connected between D0 / SDCLK pin, D1 / SDATA pin and AVSS respectively to pull-down these pins.



Register Write

- Power on reset



Power on reset

At the power-on, Power-On-Reset must be executed by using RESETB pin. When a 0.33 uF external capacitor on RESETB pin is used, the rise time of AVDD must be shorter than 10 ms in order to assure proper Power-On-Reset operation. Maximum time from AVDD power-on to the release from Power-On-Reset is 100 ms. Registers should be written after waiting for longer than 100 ms after AVDD power-on.

As electric charge is retained in the external capacitor even after AVDD is made to 0V, voltage on RESETB pin does not go to 0V immediately. If AVDD is powered-up again before RESETB pin returns to 0V, a proper Power-On-Reset operation is not made. In order to assure proper Power-On-Reset operation when to power-up AVDD again, it is required that AVDD time to be kept at 0V is longer than 300 ms. If the 300 ms AVDD time to be kept at 0V, is not obtainable, the device must be reset by applying a low pulse externally on RESETB pin.

-Register Map

Sub Adrs	Bits	Default Value	Register Name	Function
0H	7	0*******	RST	Register reset
	6	*0******	Reserved 1	Reserved 1
	5	**0*****	OUT_DR	Output buffer drivability
	4	***0****	MD_CCD	Input mode, CDS mode / DC mode
	3:2	****00**	TMG_SHR	Reference level sampling timing
	1	******0*	MD_DBLEGG	Clock mode select
	0	*******0	NPD	Power down mode
1H	7:0	10000000	DAC0	Offset DAC0 setting
2H	5:0	**000000	PGA0	PGA0 Gain setting
3H	7:6	00******	LEDSPEED	TSMP frequency selection
	5:3	**000***	SHDSET	SHD timing setting
	2	*****0**	OUT_BS	Output bus select
	1	******0*	OEN	Output buffer enable
	0	*******0	TEST_O	Output order select
4H	7:0	********	Reserved 2	Reserved 2
5H	5:0	********	Reserved 3	Reserved 3
6H	6	*0******	HALF	LED current half mode
	5:3	**000***	G_CURRENT	G current setting
	2:0	*****000	B_CURRENT	B current setting
7H	7:6	00******	A_CONT	Lower address access control
	3:2	****00**	TGMODE	TGMODE register
	1:0	******00	TGCSEL	TGCSEL register

Operation mode setting register 1 (Address "0000", Reset "0000 0000")

RST:D7	Register reset
0	Register reset (At reset)
1	release from Reset

When this bit is set to "1", all other registers are set to initial values, except for this bit.
When this bit is "1", write operation into all other registers except for this bit is ignored.

Reserved 1:D6	
0	Normal mode
1	Prohibited

OUT_DR:D5	Output Buffer Drivability
0	Normal (at reset)
1	2× (Double)

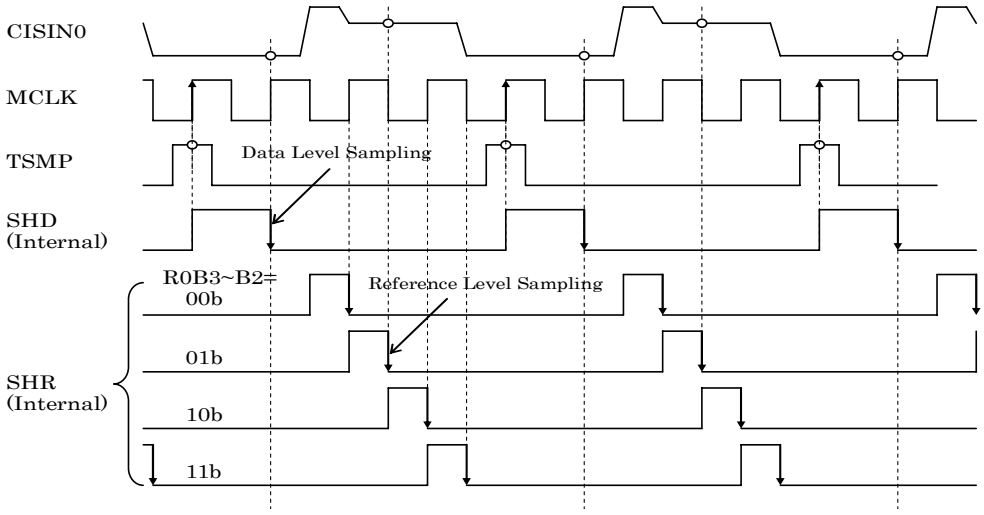
When Output Buffer Drivability is set to "2×", maximum output current of the output buffers increases. This selection is used when the Data Output Delay which is referenced to Data Capture clock becomes too large, due to capacitive loading.

MD_CCD:D4	Input mode
0	DC Direct-Coupled mode
1	CDS mode

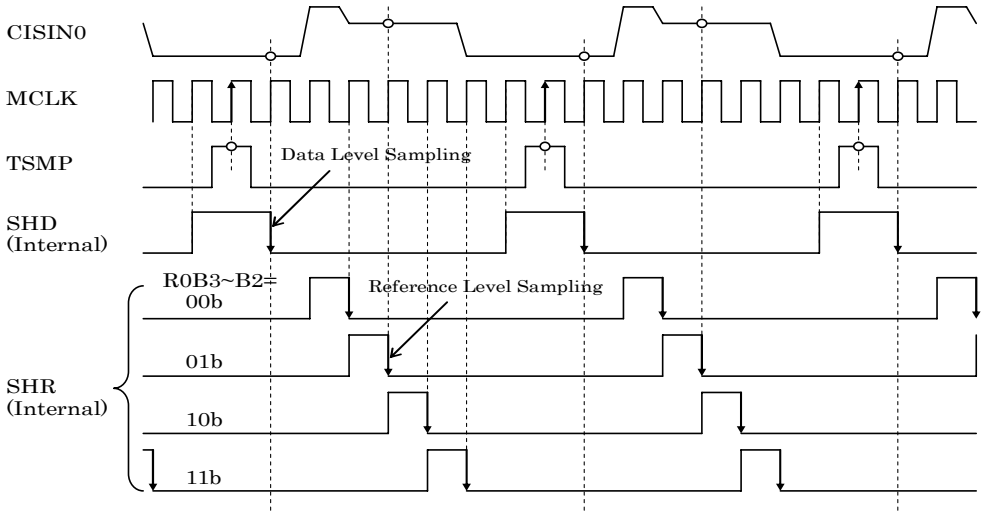
Signal Polarity which can be processed by the AK8451 is determined by the type of Input Modes. In DC Direct-Coupled Mode, it handles Positive polarity (signal is output toward higher voltage than reference level: VCLP) and in CDS Mode, it handles Negative polarity (signal is output toward lower voltage than reference level).

TMG_SHR:D[3:2]	Feed-Through Level Sampling Pulse (SHR) Position
00	2×MCLK(1×) delay from the Data Level Sampling position
01	3×MCLK(1.5×) delay from the Data Level Sampling position
10	4×MCLK(2×) delay from the Data Level Sampling position
11	5×MCLK(2.5×) delay from the Data Level Sampling position

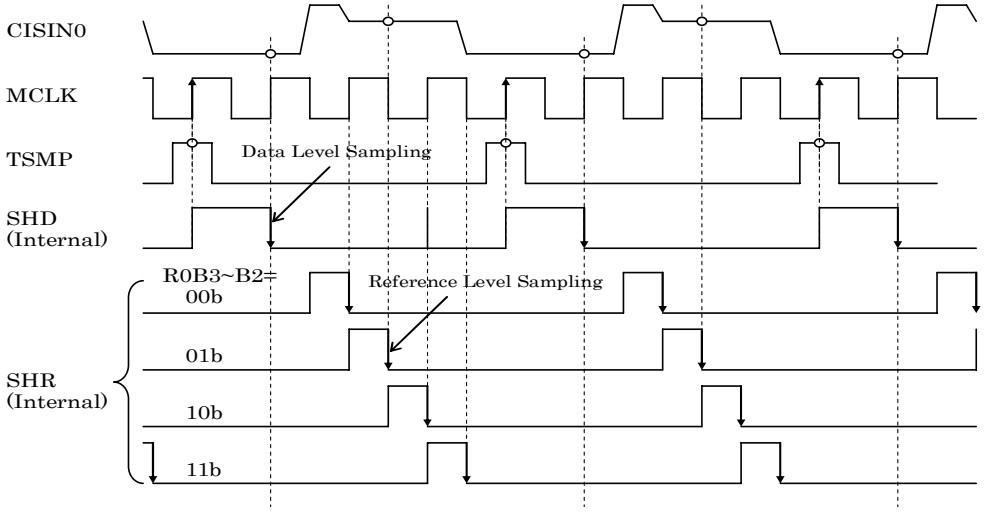
Note) In the brackets (value), it is the value when the operation frequency= 4×MCLK.



AFE 1ch/ Single edge/ 4 bit bus mode input output timing



AFE 1ch/ Single edge/ 2 bit bus mode input output timing



AFE 1ch/ Double edge/ 2 bit bus mode input output timing

MD_DBLEGG:D1	Clock mode select
0	Single edge mode
1	Double edge mode

NPD:D0	Power Down Setting
0	Power Down
1	Normal

In the power down, regardless of the condition of SDENB, the logic of the following pin is as follows.

D0/SDCLK	Input
D1/SDATA	Input
D2	H or L; Fixed level (High or Low depends on the previous condition.)
D3	H or L; Fixed level (High or Low depends on the previous condition.)

The table of each setting

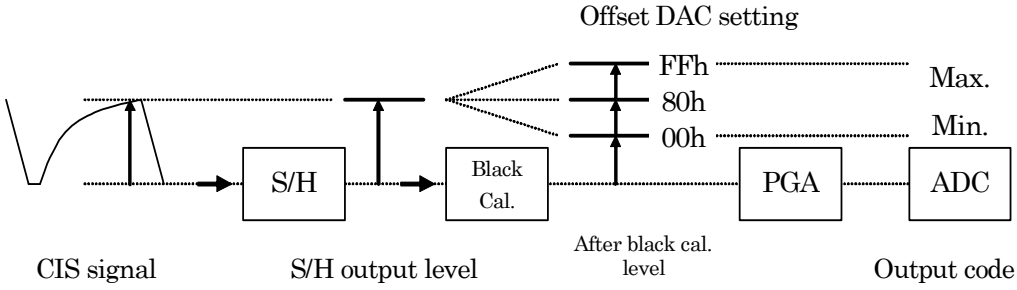
Clock mode	Output bus sel.	Compatible / not
Single edge	4 bit bus	○
	2 bit bus	○
Double edge	4 bit bus	×
	2 bit bus	○

Offset DAC0 data setting (Address “0001”, reset “1000 0000”)

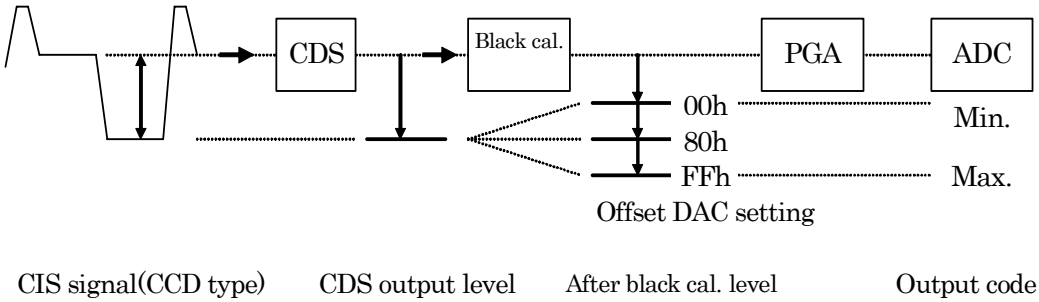
register	DAC output
00000000	-240.0mV
00000001	-238.1mV
00000010	-236.2mV
•	•
•	•
01111110	-3.8mV
01111111	-1.9 mV
10000000	**0 mV**
10000001	+1.9mV
10000010	+3.8mV
•	•
•	•
11111101	+234.4mV
11111110	+236.3mV
11111111	+238.1mV

$$Offset(x) = -240 + 480/256 \times x[\mathrm{mV}]$$; *x is setting value*

@ reset x=128, Offset(128)=0mV



The change of the level by the offset setting (DC direct mode = pos. polarity)



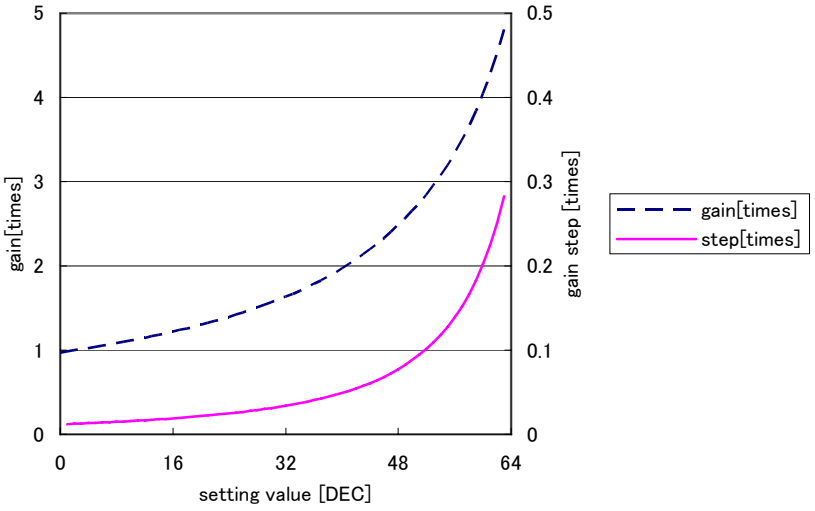
The change of the level by the offset setting (CDS mode = neg. polarity)

PGA0 gain setting (address “0010”, reset “xx00 0000”)

register	Gain [times]
000000	**1.000**
000001	1.015
000010	1.029
000011	1.042
:	:
:	:
111100	4.168
111101	4.400
111110	4.659
111111	4.950

$$Gain(x) = \frac{1.98}{2.0} \times \frac{80}{16 + (63 - x)} [times] \qquad ; x \text{ is setting value}$$

@ reset x=0, Gain(0)=1.003 times

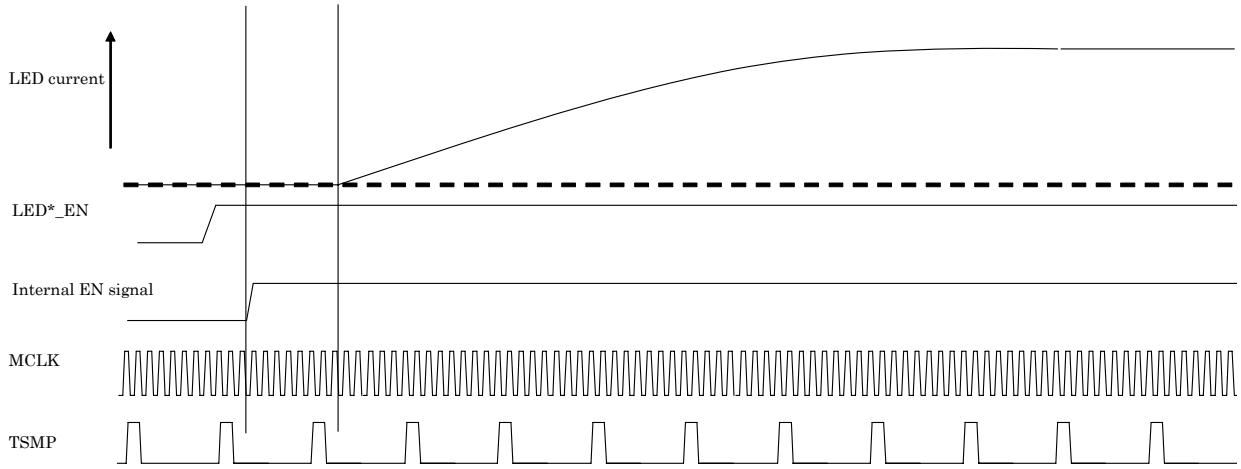


gain curve (theoretical figure)

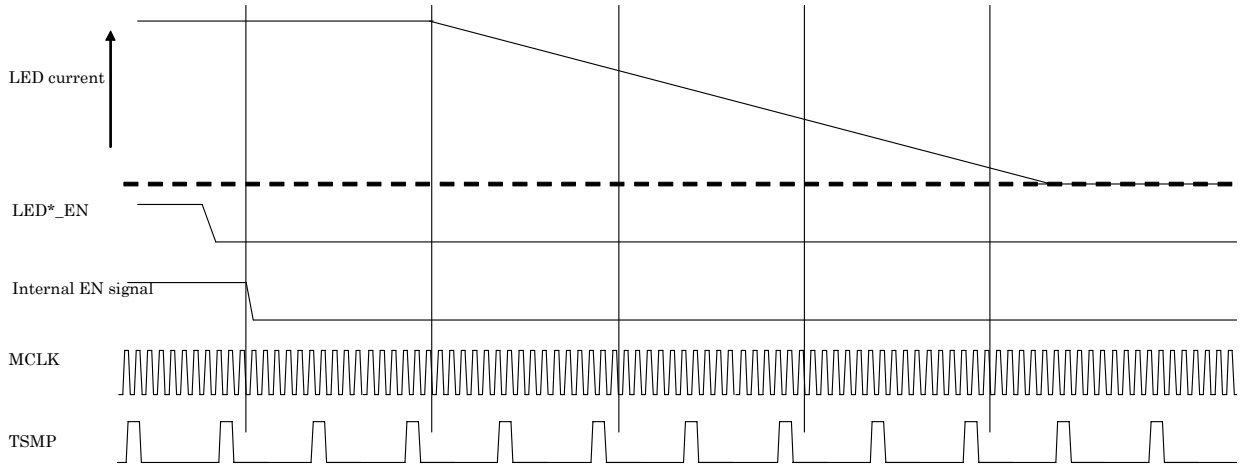
** The definition with the above PGA gain is the value of PGA simple substance. In DC direct mode, (the positive-polarity) is gained < PGA gain's being duple > after offset adjustment in the voltage of the difference between the reference voltage which is inputted to the VCLP terminal and the signal level (the part of SHD). In CDS mode , (the negative electrode), the voltage of the difference between the reference level (the part of SHR) and the signal level (the part of SHD) is gained absolute gain duple(-0.6dB typ.) and it is < PGA gain's being duple > after offset adjustment.

Operation setting 2 (address “0011”, reset “0000 0000”)

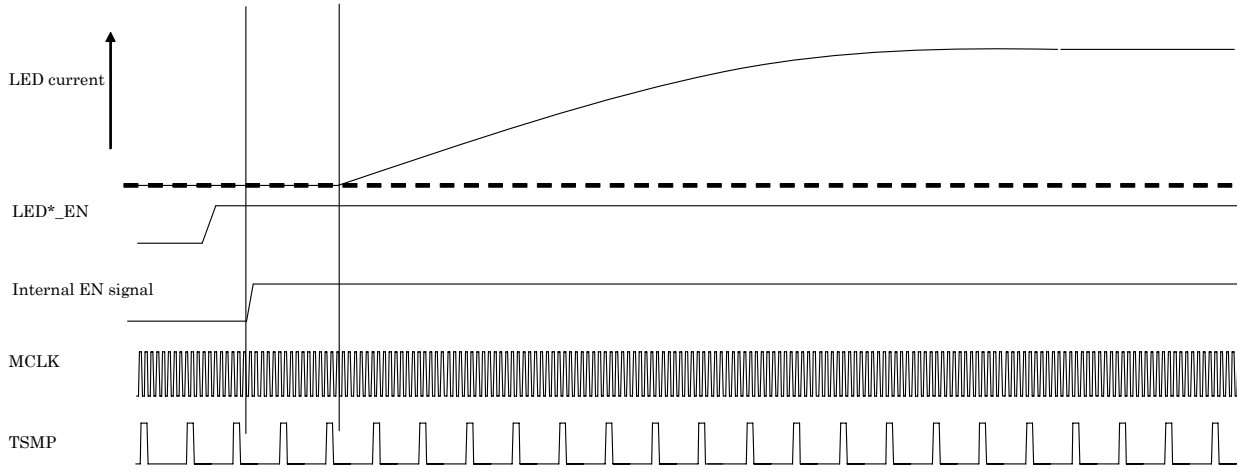
LEDSPEED:D[7:6]	TSMP frequency select for adjust LED timing
00	LED timing frequency diving ratio = 1 (1MHz <=TSMP frequency < 2MHz)
01	LED timing frequency diving ratio = 1/2 (2MHz <=TSMP frequency < 4.4MHz)
10	LED timing frequency diving ratio = 1/4 (TSMP frequency >=4MHz)
11	Inhibition



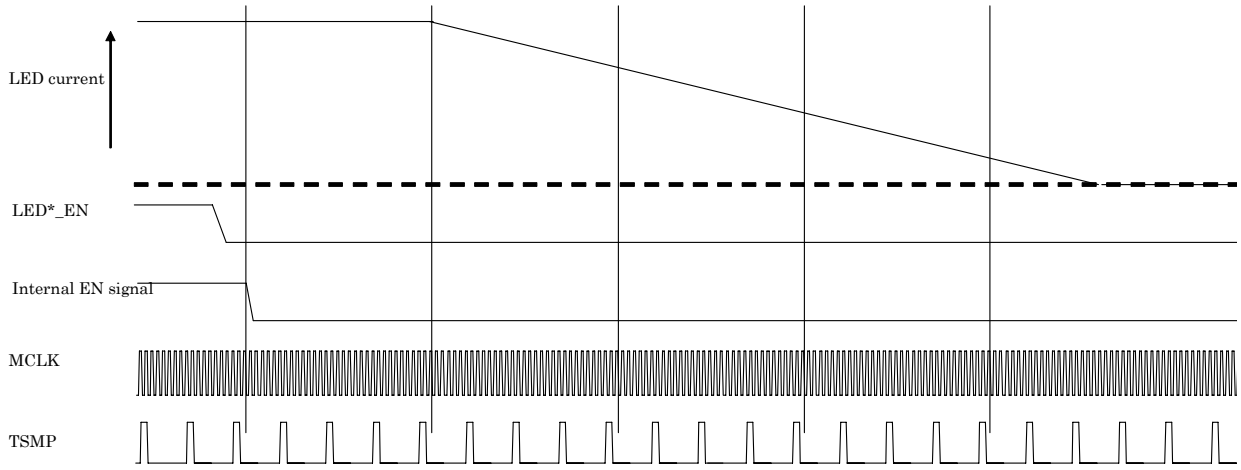
** By 00 setting LED＊_EN OFF to ON timing（Single edge mode/2 bit output）



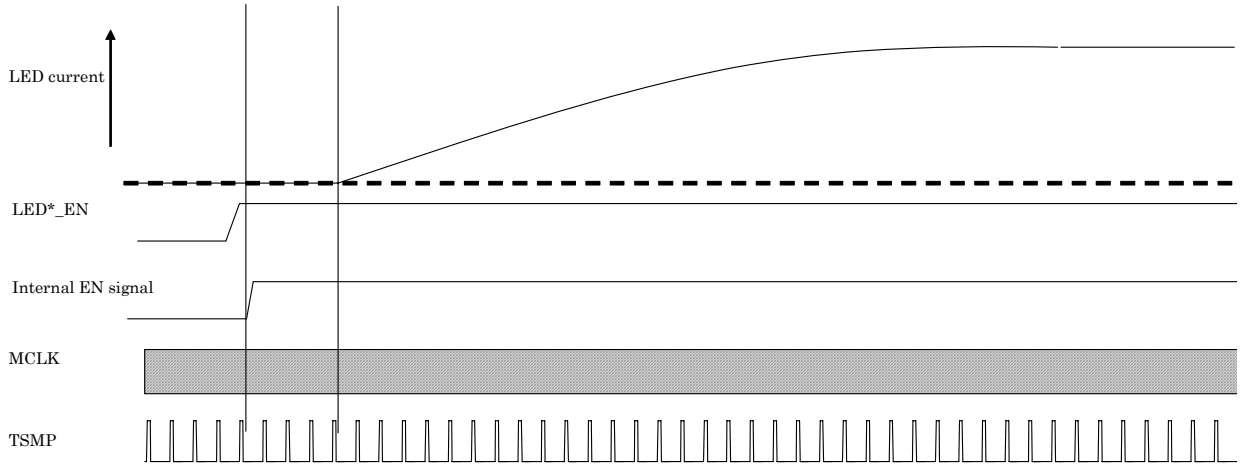
** By 00 setting LED＊_EN ON to OFF（Single edge mode/2 bit output）



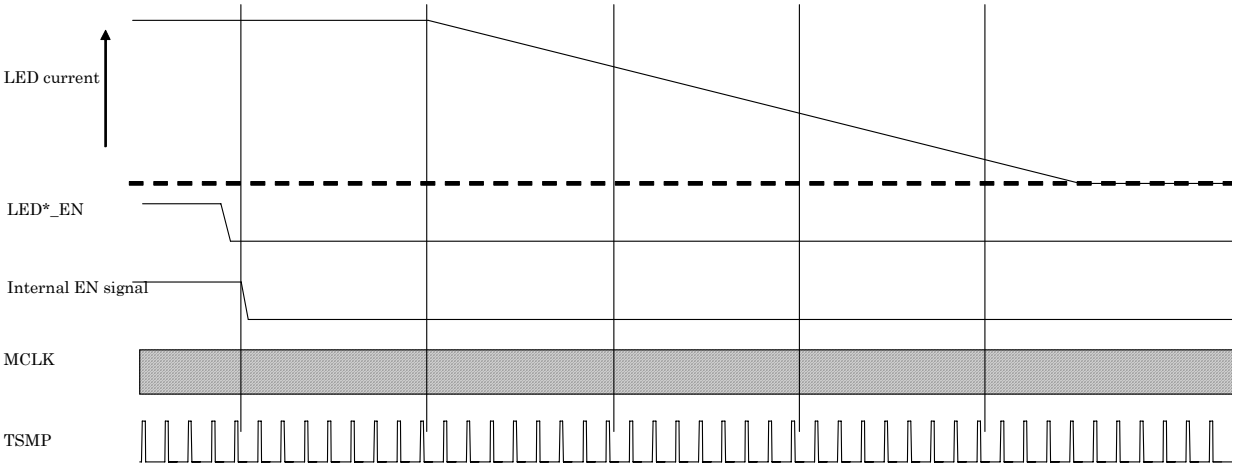
** By 01 setting LED＊_EN OFF to ON（Single edge mode/2 bit output）



** By 01 setting LED＊_EN ON to OFF（Single edge mode/2 bit output）

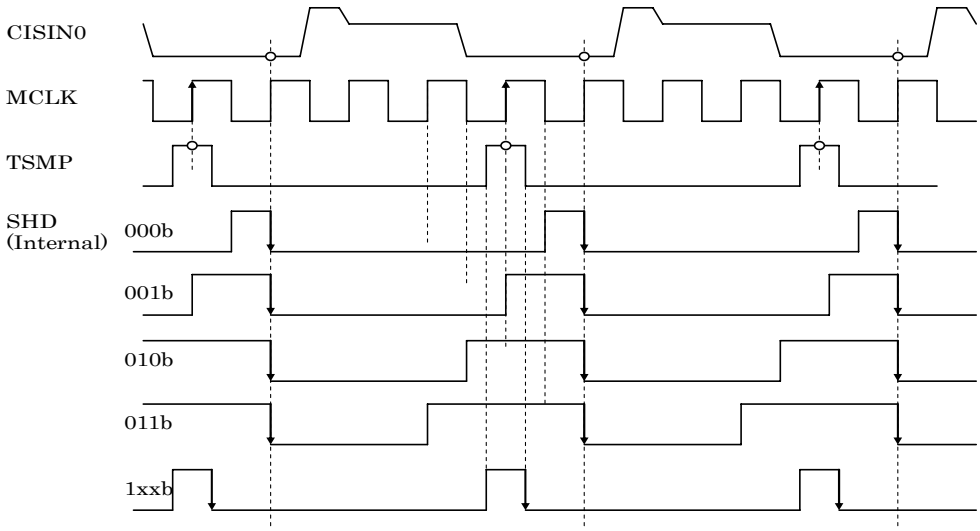


** By 10 setting LED＊_EN OFF to ON（Single edge mode/2 bit output）

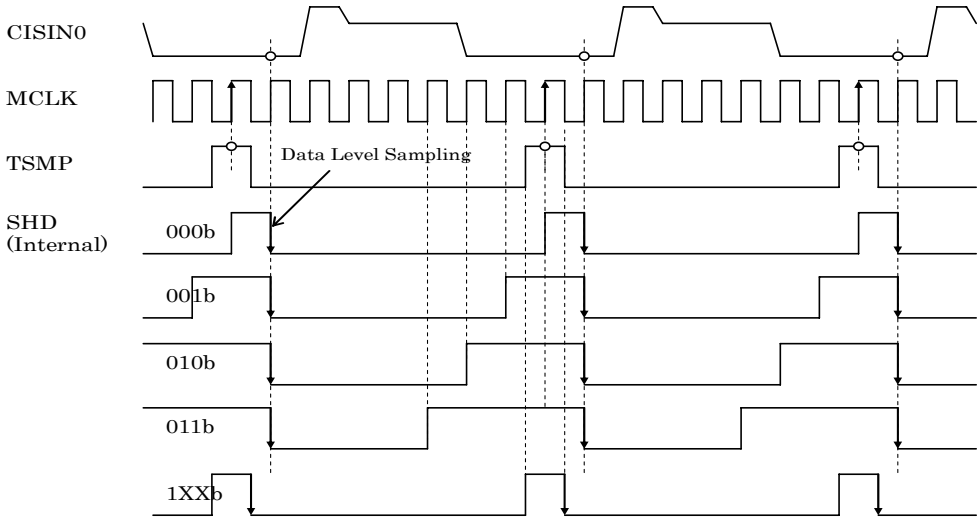


** By 10 setting LED＊_EN ON to OFF（Single edge mode/2 bit output）

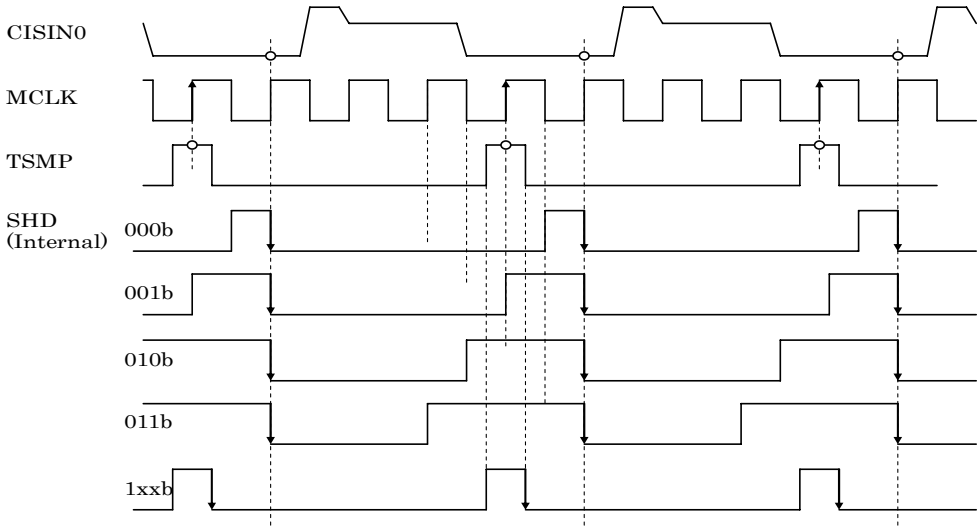
SHDSET：D[5:3]	SHD timing
000	It is delayed for 7(3.5) clocks than a data sampling position.
001	It is delayed for 6(3) clocks than a data sampling position.
010	It is delayed for 5(2.5) clocks than a data sampling position.
011	It is delayed for 4(2) clocks than a data sampling position.
1XX	SHD (input clock) = TSMP



AFE1ch / single edge mode / 4 bit bus mode IO timing



AFE1ch / single edge / 2 bit bus mode IO timing

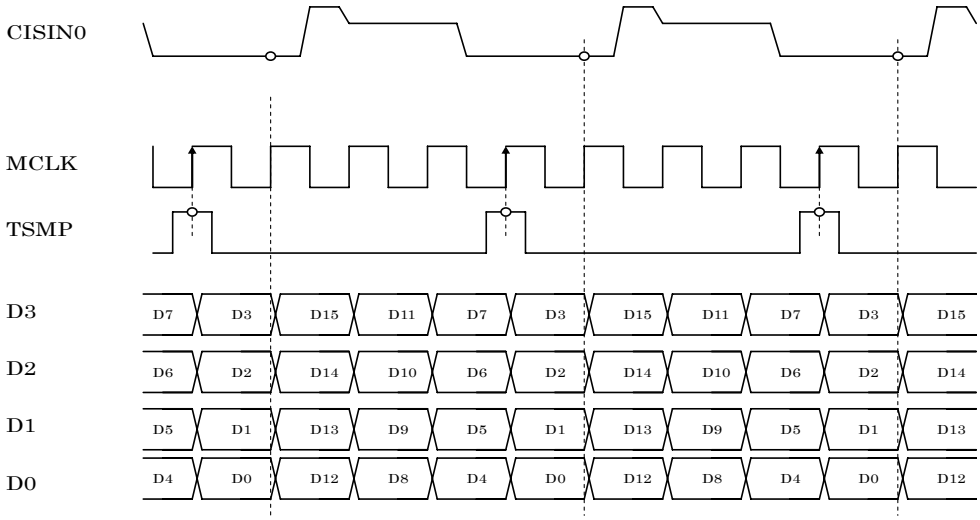


AFE1ch / double edge / 2 bit bus mode IO timing

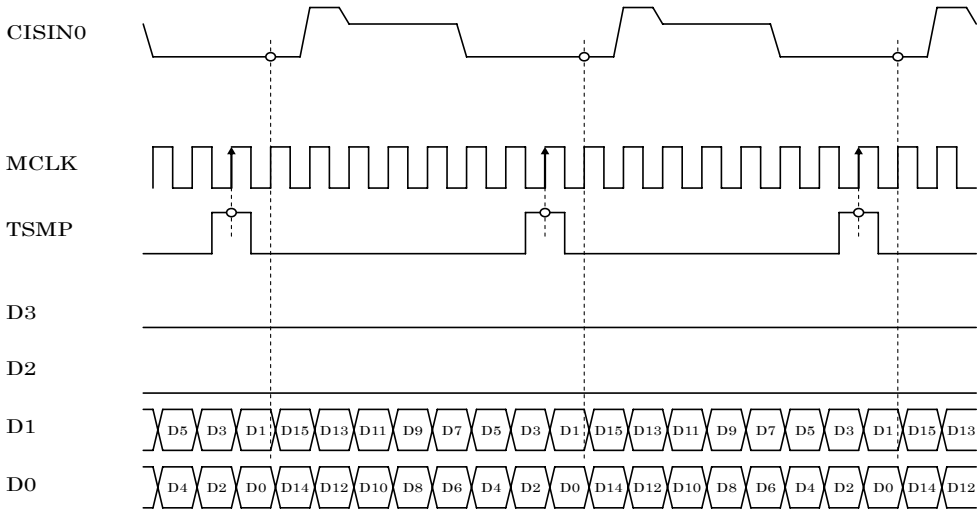
OUT_BS:D2	Output bus size mode
0	2 bit bus mode
1	4 bit bus mode

The table of each setting

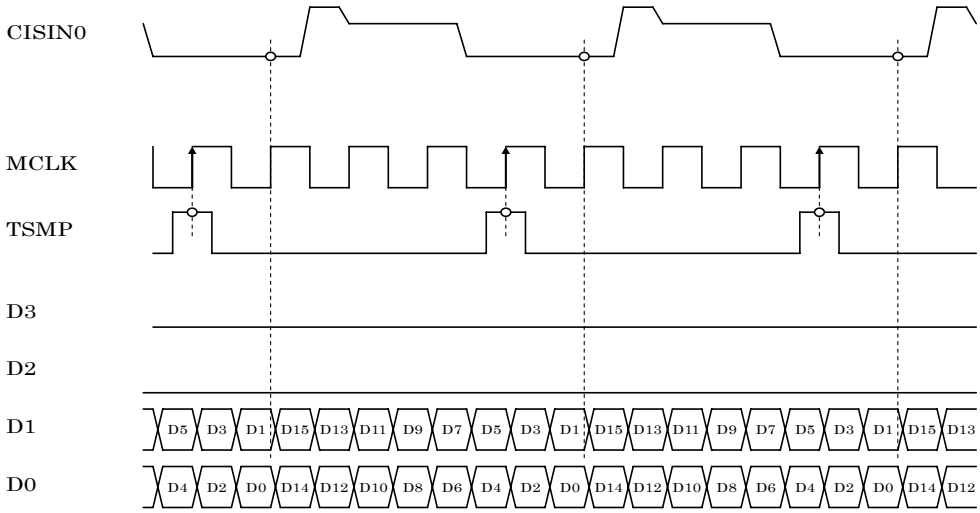
Clock mode	Output bus sel.	Compatible / not
Single edge	4 bit bus	○
	2 bit bus	○
Double edge	4 bit bus	×
	2 bit bus	○



AFE1ch / single edge / 4 bit bus mode IO timing



AFE1ch / single edge / 2 bit bus mode IO timing

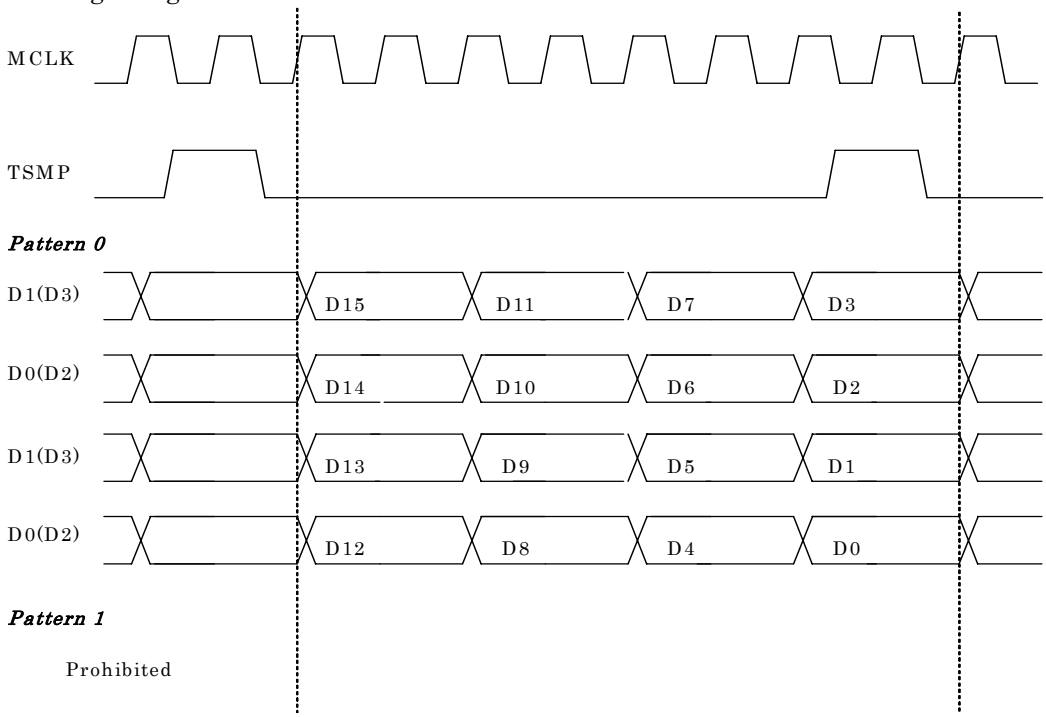


AFE1ch / double edge / 2 bit bus mode IO timing

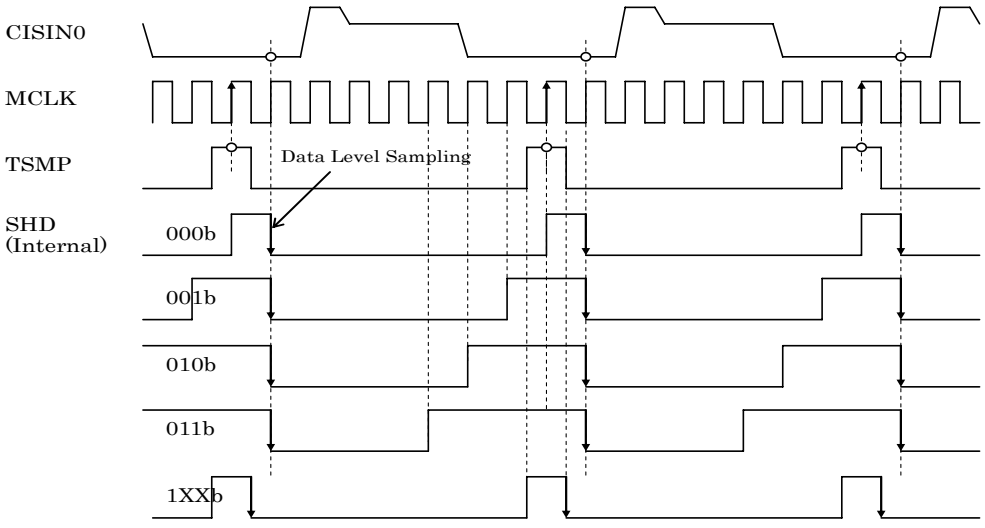
OEN:D1	Output buffer enable
0	enable
1	Hi-z

TEST_O:D0	Output order select
0	Pattern 0
1	Pattern 1

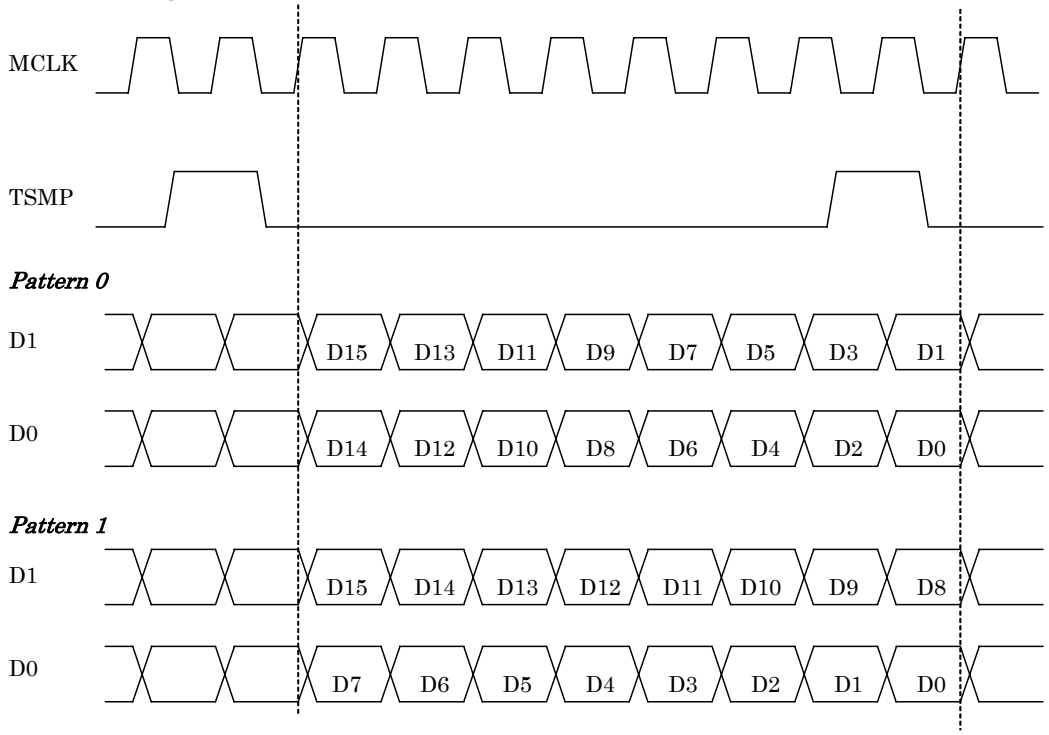
AFE1ch / single edge / 4 bit bus mode format



AFE1ch / single edge / 2 bit bus mode



AFE1ch / double edge / 2 bit bus mode format



LED setting 1 (address “0110”, reset “X0000000”)

HALF:D6	LED current half mode
0	Normal mode
1	The LED output current value becomes 1/2.

G_CURRENT: D[5:3]	Green current setting [%] This value is a ratio with the red LED.
000	100
001	95.8
010	91.7
011	87.5
100	83.3
101	79.2
110	75
111	70.8

B_CURRENT: D[2:0]	Blue current setting [%] This value is a ratio with the red LED.
000	100
001	95.8
010	91.7
011	87.5
100	83.3
101	79.2
110	75
111	70.8

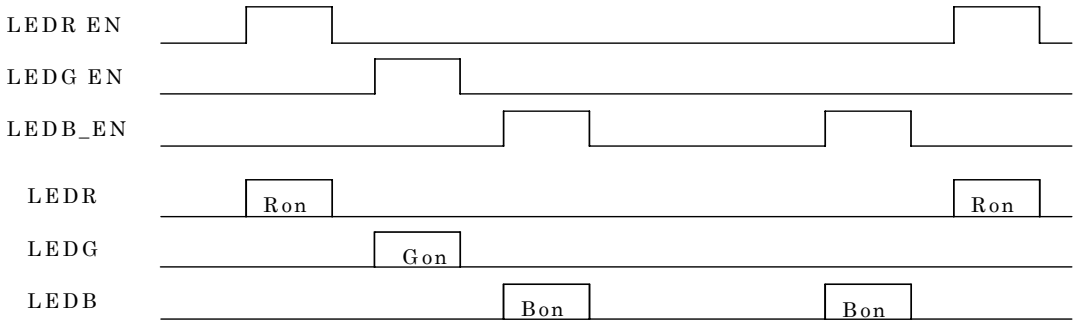
LED setting 2 （address “0111”, reset “00XX 0000”）

A_CONT : D[7:6]	Lower address (00H ~ 06H) access control
00	Access enable (Normal Operation ）
01	Access disable
10	Access disable
11	Access disable

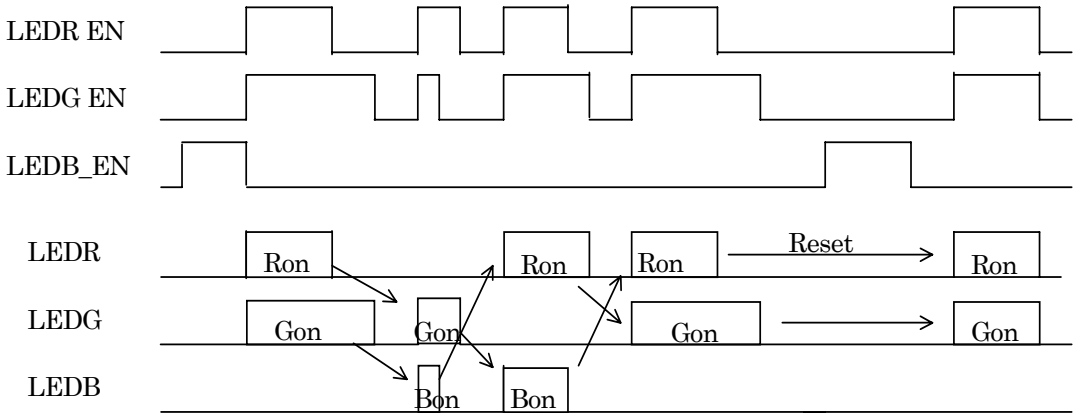
It becomes impossible in writing a thing except "00" in D:[7:6] to write notes in lower-address (00H-06H). Write "00" in D:[7:6] and use to be general.

TGMODE : D[3:2]	Operation
00	LED*_EN through mode
01	<TG mode a> LEDR_EN : R→off→G→off→B→off : LED switch order LEDG_EN : G→off→B→off→R→off : LED switch order LEDB_EN : LED counter reset
10	<TG mode b> LEDR_EN : G→off →B→off →R→off : LED switch order LEDG_EN : B→off→R→off→G→off : LED switch order LEDB_EN : LED counter reset
11	<TG mode c> LEDR_EN : B→off →R→off →G→off : LED switch order LEDG_EN : R→off→G→off→B→off : LED switch order LEDB_EN : LED counter reset

At LED*_EN through mode function



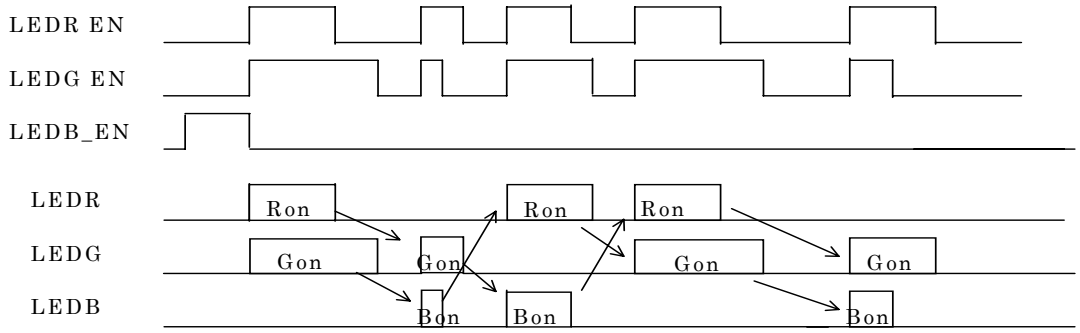
At TG mode function (Following figure is example of TGMODE =01 setting)



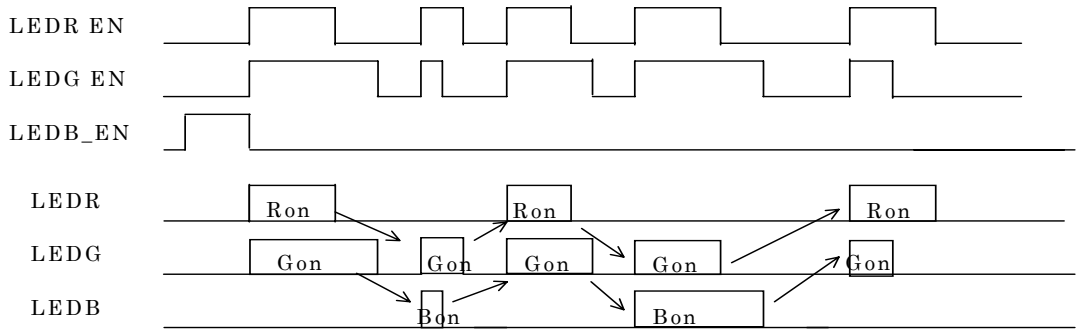
TGCSEL : D[1:0]	Operation
00	When TGMODE≠"00" ; The LED repeats on/off of 3 color in turn.
01	When TGMODE≠"00" ; The LED repeats on/off, that the first only 2 color is alternate.
10	When TGMODE≠"00" ; Only the first color LED repeats on/off.
11	Prohibited

TGMODE =01 setting example

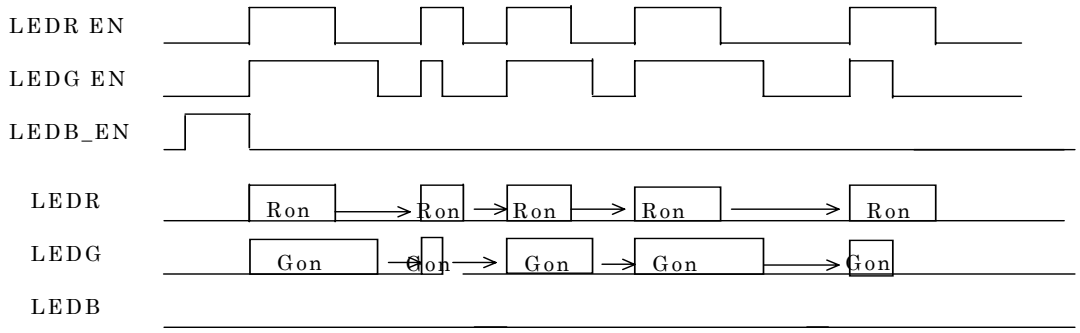
TGCSEL= 00



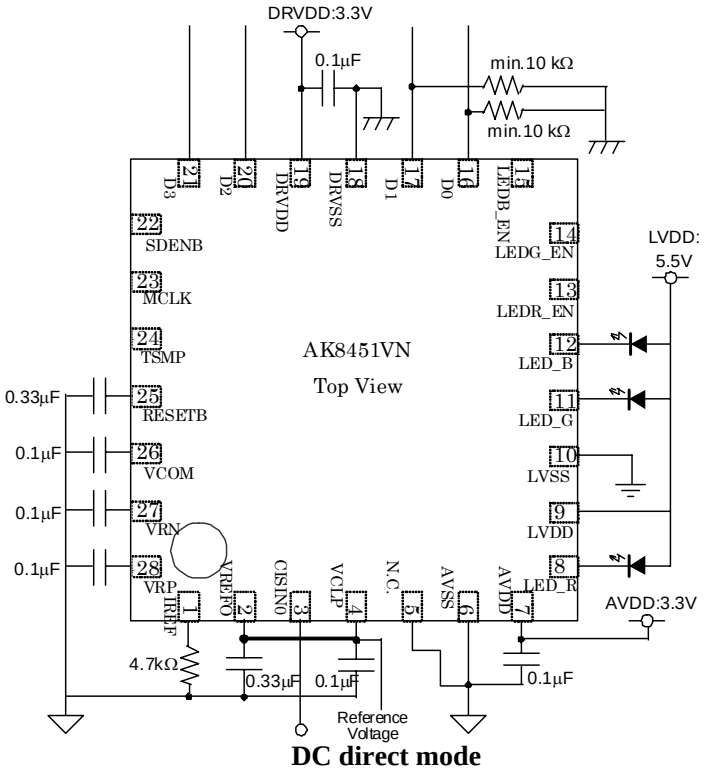
TGCSEL = 01



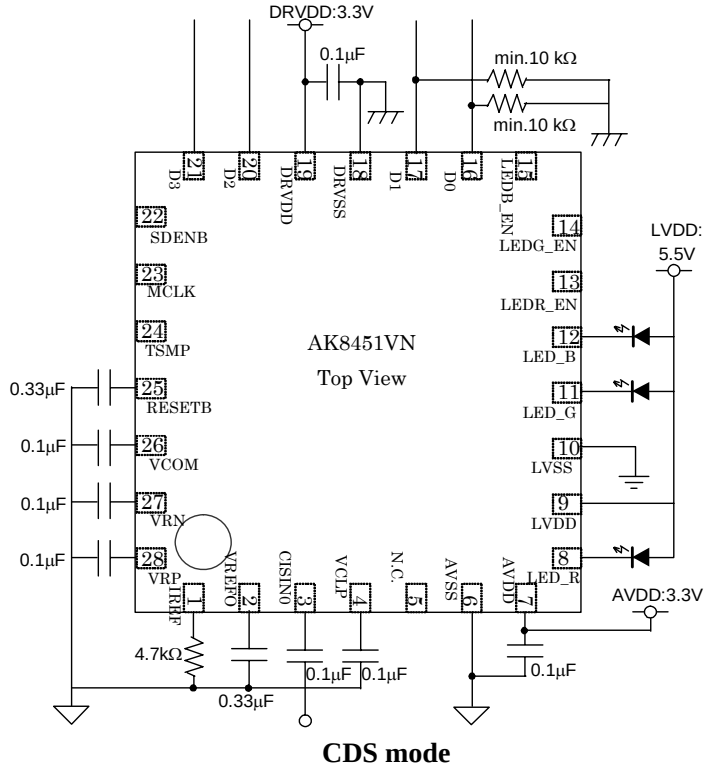
TGCSEL = 10



External circuit example



DC direct mode

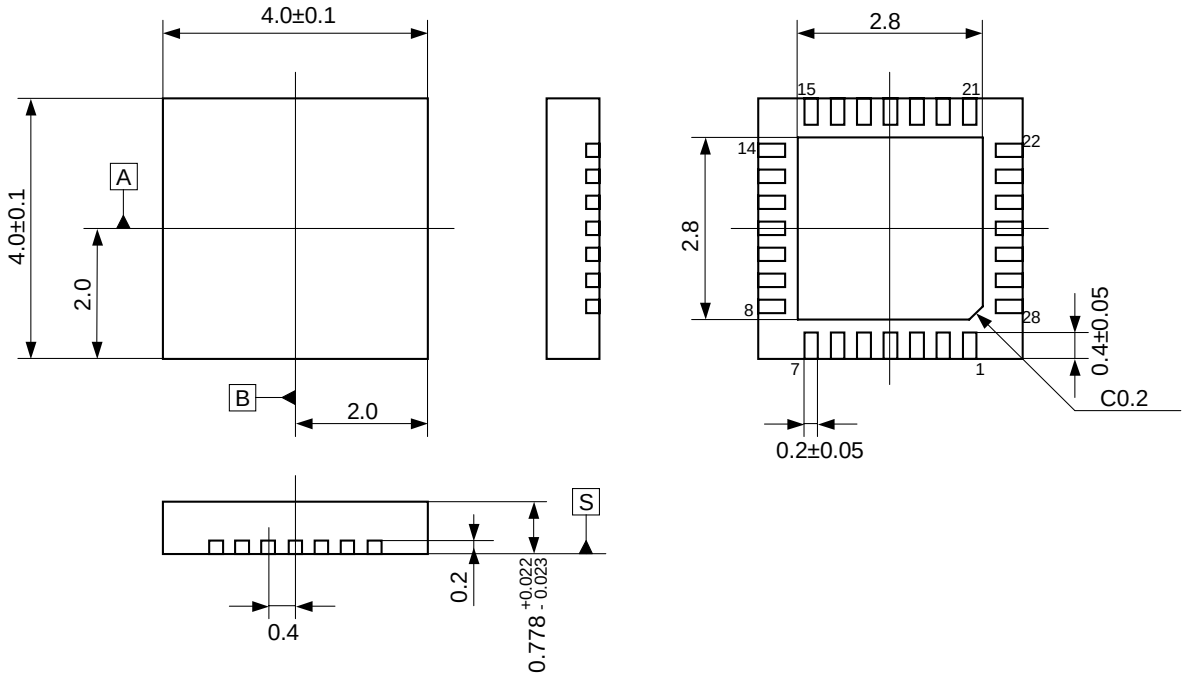


CDS mode

* The radiation PAD on the package solder side connect with analog ground (AVSS).

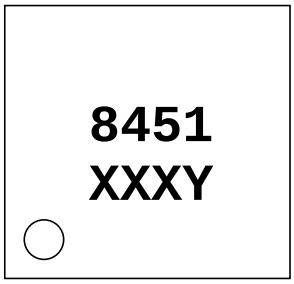
Package

■ Package dimension unit [mm]



■ Marking

1. Marketing code :8451
2. Date code :XXX Week code
   :Y The company management code



Marking

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  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei EMD Corporation (AKEMD) or authorized distributors as to current status of the products.
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  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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