

AsahiKASEI

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AK8826VN**HD/SD Multi Format Video Encoder with 3ch DAC****General Description**

The AK8826 is a HD/SD TV Video Encoder with onchip 3-channel 10bit DAC.

As input data, in SDTV encoder mode, SMT E-125M / IT UR-R.BT601, 656 compatible Y/Cb/Cr 4:2:2 formats (8bit) are accepted and in HDTV encoder mode, SMPT E-274M (1080i), SMPT E296M (720p) compatible Y/Cb/Cr 4:2:2 formats (8bit x 2) are accepted.

As input data capture method, either a Synchronous mode to be made by detecting encoded EAV signal or a mode to synchronize with externally-fed H/V SYNC signal is selectable.

Outputs of CVBS / SDY / SDC and HDY / HDPB / HDPR and R / G / B analog signal can be output exclusively.

VBI signal can be also superimposed on output in addition to Video signals by register setting.

AK8826 supports I2C compatible interface as Micro-Processor interface.

Features**Component Video Encoder**

- Compatible Input Data
 - SMPTE125M-1995 / ITU-R BT601 (525i/625i)
 - SMPTE293M-1996 / ITU-R BT1358 (525p/625p)
 - SMPT E274M-1998 (1080i)
 - SMPT E296M-2001 (720p)
- Input Signal Format (525i / 625i, 525p / 625p, 1080i, 720P)
 - Y/Cb/Cr 4:2:2 (8bit x 1: 525i/625i)
 - Y/Cb/Cr 4:2:2 (8bit x 2: 525p/625p/1080i/720p)
- RGB 6:6:6
- RGB 5:6:5
- Input Clock
 - 27MHz (525i / 625i / 525p / 625p) / 74.25MHz (1080i/720p)
- Output Signals
 - Y/Pb/Pr Interlace
 - Y/Pb/Pr Progressive
 - (EIA 770.2, EAI 770.3)
- Input Signal Synchronization
 - ITU-R.BT 656 I/F (EAV Decode)
 - Slave operation by HSYNC / VSYNC
 - (525i: ITU-R. BT601 Compatible 625i / 525p / 625p / 1080i / 720p; CEA-861-D Compatible)
- VBID (CGMS-A), CC/XDS, WSS, CEA-805-B (Type A/B)
- Internal Color bar Generator
- Internal Black Burst Generator
- Adjustable Y / Pb / Pr Delay Function

NTSC / PAL Composite Video Encoder

- NTSC-M, PAL-B, D, G, H, I, M, N Encoding
- Composite Video Output / S-Video Output
- Compatible Input Data
 - SMPTE125M-1995 / ITU-R BT601(525i/625i) Y/Cb/Cr 4:2:2 (8bit x 1)
- RGB 6:6:6
- RGB 5:6:5
- Input Signal Synchronization
 - ITU-R.BT 656 I/F (EAV Decode)
 - Slave operation by HSYNC / VSYNC
 - (525i / 625i: ITU-R. BT601 Compatible)
- Input Clock
 - 27MHz
- VBID(CGMS-A), CC/XDS, WSS



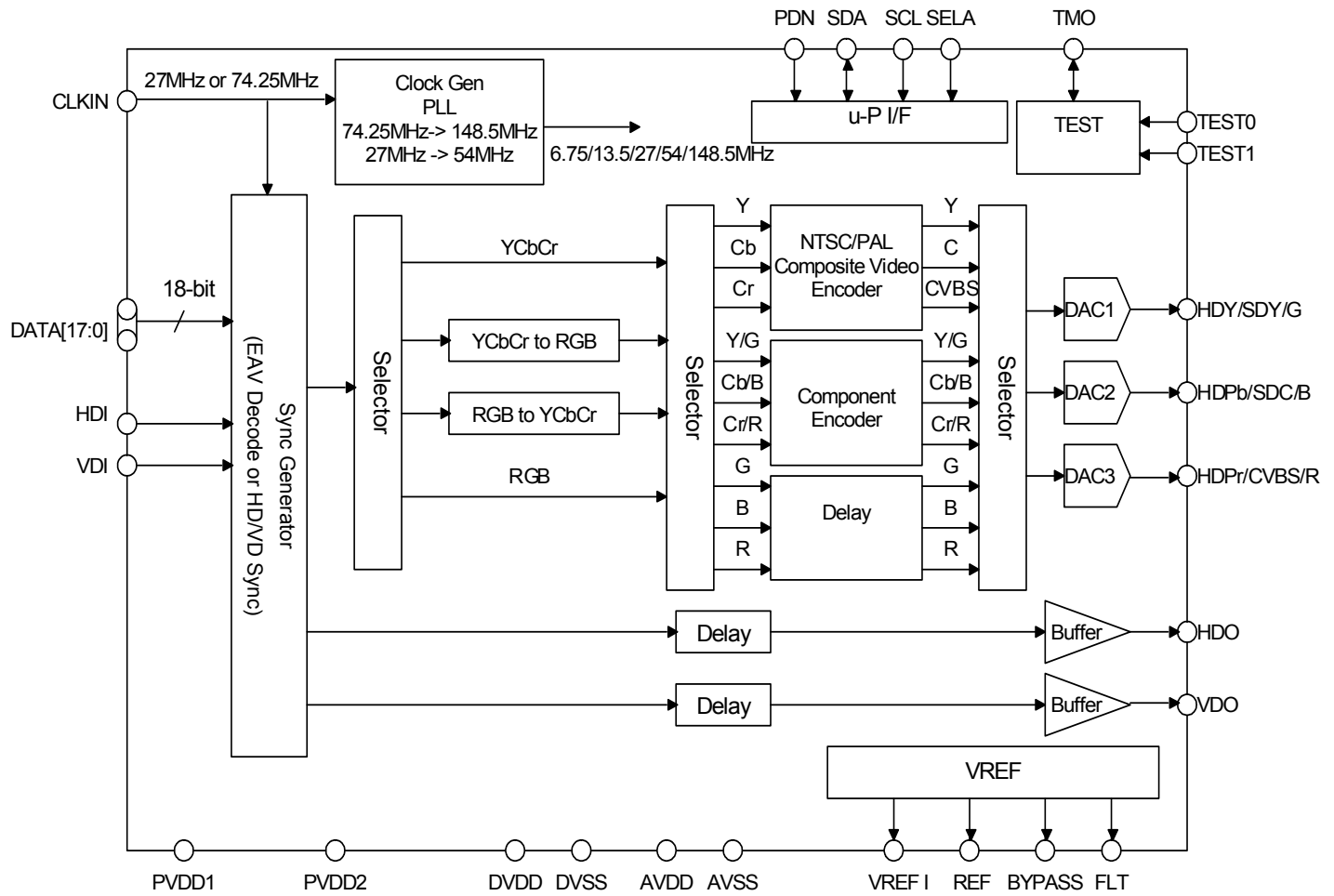
RGB Video DAC

- RGB output
- Input Data Format
 - RGB 6:6:6
 - RGB 5:6:5
- Input Clock
 - 54MHz (max)

Common Specification

- 10bit DAC x 3ch (max operating speed 150MHz)
- I²C BUS I/F (400kHz) compatible
- Power Down mode
- Internal VREF Circuit
- 3.0V / 1.8V VCC
- 48pin QFN (7.2mm x 7.2mm)

1. Block Diagram

**Fig. 1 Block Diagram**

With Register setting, AK8826 works as

- Multi-Format Component Video Encoder (Component Video Encoder)
- NTSC/PAL Composite Video Encoder (Composite Video Encoder)
- High Speed Video DAC

1-1. Component Video Encoder Block

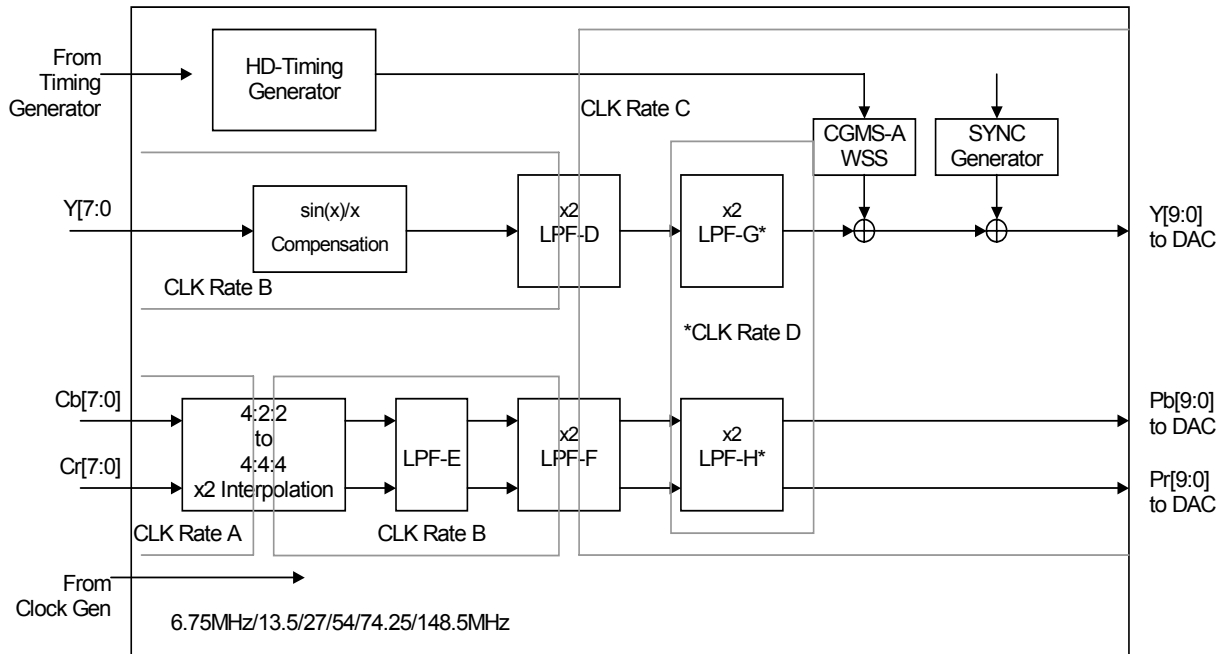


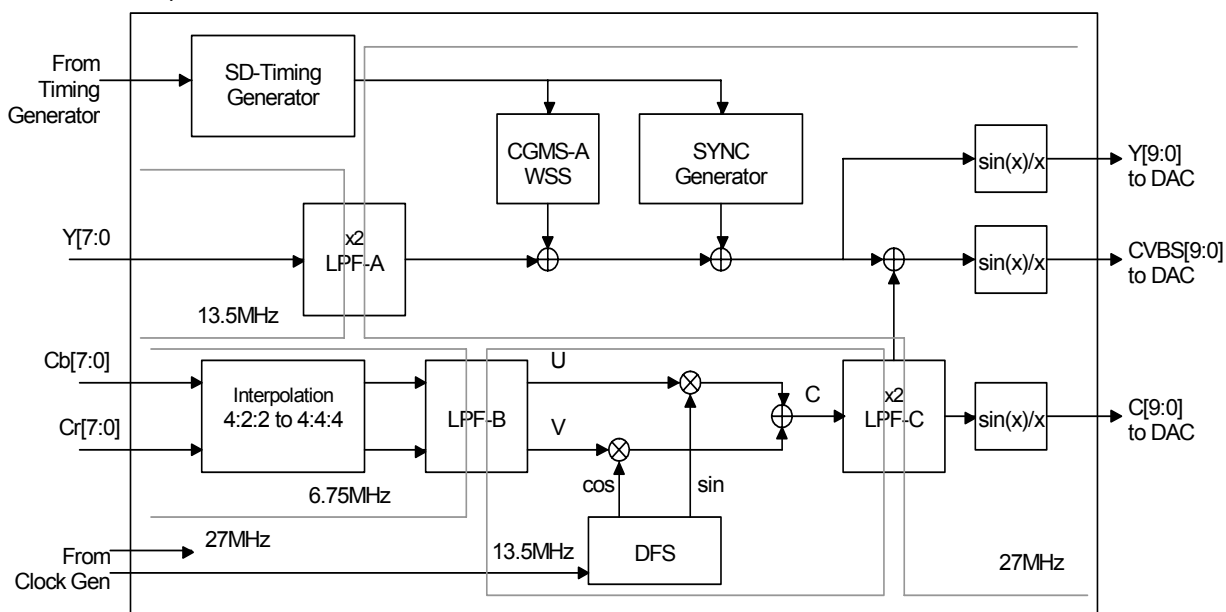
Fig. 2 Component Video Encoder Block

This Block described as Component Video Encoder Block in this datasheet.
CLK Rate D is only a case of D1(525i/625i) mode.

Clock Rate

	D1(525i /625i)	D2(525P / 625P)	D3/D4(1080i/720P)
CLK Rate A	6.75MHz	13.5MHz	37.125MHz
CLK Rate B	13.5MHz	27MHz	74.25MHz
CLK Rate C	27MHz	54MHz	148.5MHz
CLK Rate D	54MHz	-	-

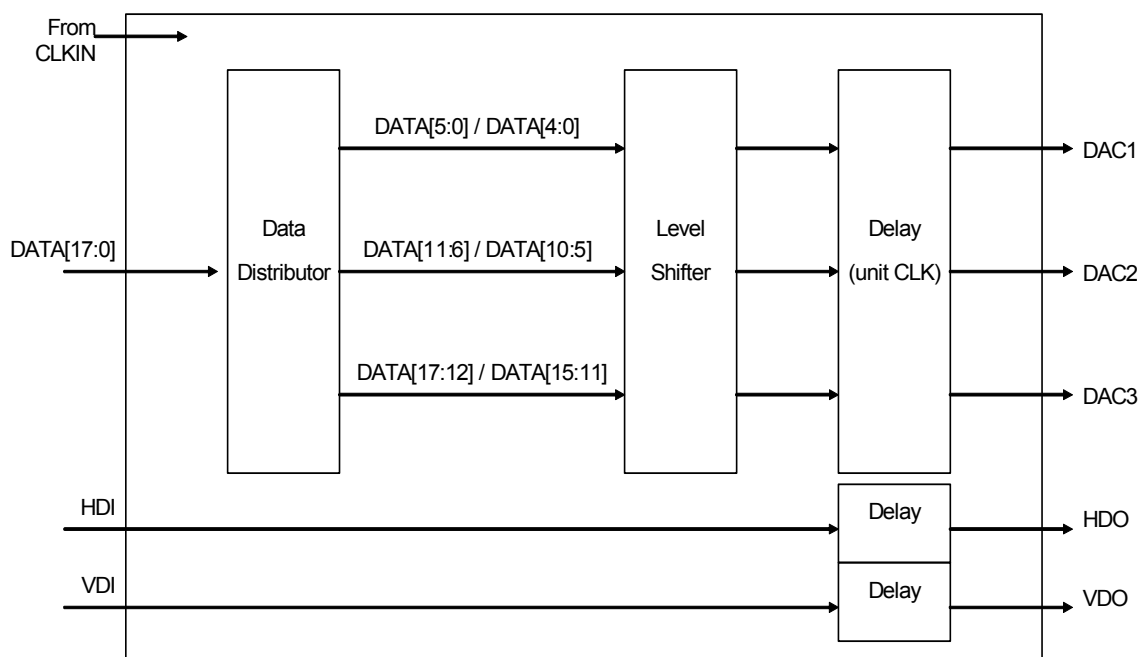
1-2. NTSC/PAL Composite Video Encoder Block

**Fig. 3 Composite Video Encoder Block**

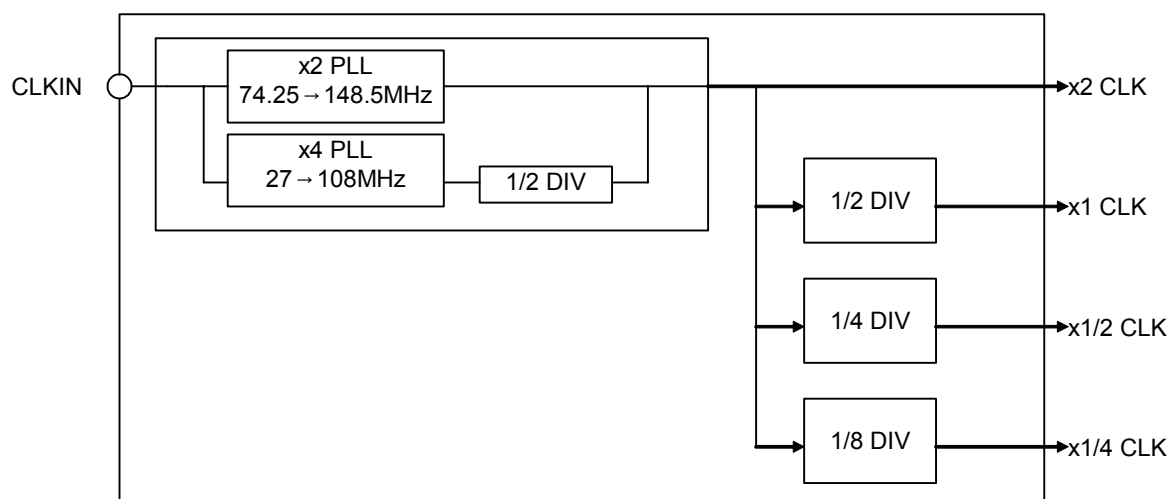
This Block described as Composite Video Encoder Block in this datasheet.

1-3 High Speed Video DAC mode

AK8826 can be used as High Speed Video DAC. This mode is described as Video DAC mode in this datasheet.

**Fig. 4 High Speed Video ADC Block**

1-4. CLK Gen Block

**Fig. 5 CLK Gen Block**

Clock Rate

	D1(525i /625i)	D2(525P / 625P)	D3/D4(1080i/720P)
x1/4 CLK	6.75MHz	-	-
x1/2 CLK	13.5MHz	13.5MHz	37.125MHz
x1 CLK	27MHz	27MHz	74.25MHz
x2 CLK	54MHz	54MHz	148.5MHz

Notice Information

In this document, relations of the word are shown as following table

Number of Lines in Frame	Description in this datasheet
525 Interlace	525i or 480i or D1
625 Interlace	625i or 576i or D1
525 Progressive	525p or 480p or D2
625 Progressive	625p or 576p or D2
1125 Interlace	1125i or 1080i or D3
750 Progressive	750p or 720p or D4

2. Ordering Guide

AK8826VN 48 pin QFN

3. Pin Assignment

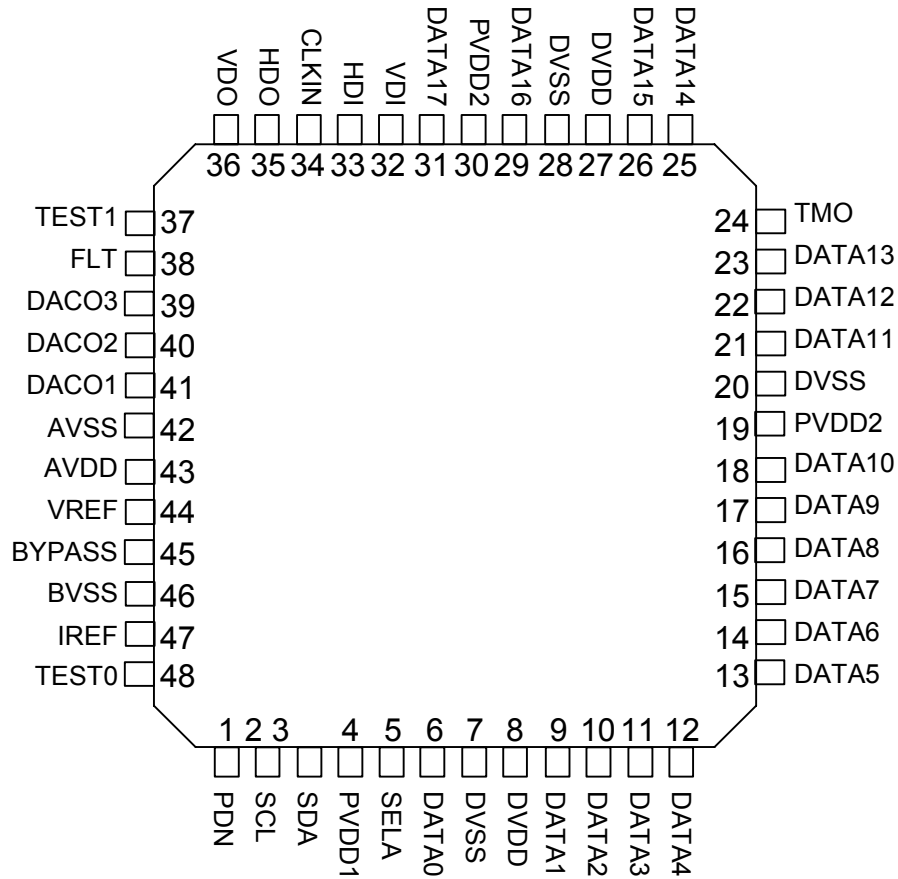


Fig. 6 Pin Layout (TopView)

4. Function of Pins

pin#	Pin Name	power	I/O	Function
1 PDN		P1	I	Control Pin for Power Down and Reset. AK8826 is initialized with PDN = Low. AK8826 becomes Power down states during PDN=Low Normal operation mode, PDN pin should be High. This pin is Prohibited to be Hi-z States
2 SCL		P1	I	I2C BUS clock input pin. Pulled up externally.
3 SDA		P1	I/O	I2C Bus Data Input Pin. Pulled up externally.
4	PVDD1	P1	P	Power supply pin for I/O(PDN, SDA, SCL, SELA)
5 SELA		P1	I	I2C BUS Address select pin. Fixed to PVSS1 or PVDD1.
6 DAT	A0	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
7	DVSS	D	G	Ground pins for Digital.
8	DVDD	D	P	Power supply pins for Digital.
9 DAT	A1	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
10 DAT	A2	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
11 DAT	A3	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
12 DAT	A4	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
13 DAT	A5	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
14 DAT	A6	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
15 DAT	A7	P2	I	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
16 DAT	A8	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
17 DAT	A9	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
18 DAT	A10	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
19	PVDD2	P2	P	Power supply pins for I/O(CLKIN, DATA[17:0], HDI, VDI)
20	DVSS	D	G	Ground pins for Digital.
21 DAT	A11	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
22 DAT	A12	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
23 DAT	A13	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
24 T	MO	I/O	P2	TEST pin. Leave open. (Internally Pull-down with approx. 100k-ohm)
25 DAT	A14	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
26 DAT	A15	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
27	DVDD	D	P	Power supply pins for Digital.

28	DVSS	D	G	Ground pins for Digital.
29	DAT A16	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
30	PVDD2	P2	P	Power supply pins for I/O(CLKIN, DATA[17:0], HDI, VDI)
31	DAT A17	P2	I/O	Data Input pin Refer "Data input Format". In case of PDN pin = Low, Hi-z states is possible.
32	VDI	P2	I/O	In case of slave Synchronization operation mode, Vertical Sync timing should be input. In case of PDN pin = Low, Hi-z states is possible.
33	HDI	P2	I/O	In case of slave Synchronization operation mode, Horizontal Sync timing should be input. In case of PDN pin = Low, Hi-z states is possible.
34	CLKIN	P2	I	Clock Input Pin Composite Video Encoder Mode: Input 27MHz Clock. Component Video Encoder Mode: Either 27MHz or 74.25MHz clock is input. (Depending on Input Video Format) High Speed Video DAC Mode: Max input clock is 54MHz. Prohibited Hi-z States
35	HDO	P2	O	Horizontal Sync Timing signal output pin. In case of PDN pin = Low, this pin outputs Low.
36	VDO	P2	O	Vertical Sync Timing signal output pin. In case of PDN Pin = Low, this pin outputs Low.
37	T EST1	I	P2	TEST pin. Connect to DVSS. (Internally Pull-down with approx. 100k-ohm)
38	F LT	A	O	Filter Pin for PLL. 4.7nF capacitor and 820-ohm resistor should be connected as shown in "11. SYSTEM CONNECTION EXAMPLE"
39	DACO3	A	O	DAC3 output pin. Output signal is set by register Composite Video Encoder mode: Pr or R Component Video Encoder mode: CVBS High Speed Video DAC mode: Depending on Input data. Load resistor is 300-ohm
40	DACO2	A	O	DAC2 output pin. Output signal is set by register Composite Video Encoder mode: Pb or B Component Video Encoder mode: C High Speed Video DAC mode: Depending on Input data. Load resistor is 300-ohm
41	DACO1	A	O	DAC1 output pin. Output signal is set by register Composite Video Encoder mode: Y or CVBS Component Video Encoder mode: Y or G High Speed Video DAC mode: Depending on Input data. Load resistor is 300-ohm
42	AVSS	A	G	Ground pin for Analog
43	AVDD	A	P	Power supply pin for Analog.
44	VREF	A	I	to be connected to AVDD via a 0.1 uF capacitor
45	BYPASS	A	O	Output pin to output On-Chip VREF voltage. Should be connected to AVSS via a larger-than 0.1 uF capacitor.
46	BVSS	A	G	Ground pin for Substrate. Connect to AVSS.
47	IREF	A	O	Reference Current Output pin for DAC Should be connected to AVSS via a 3.3 K ohm (+/- 1 %) resistor.
48	T EST0	I	P1	TEST pin. Connect to DVSS. (Internally Pull-down with approx. 100k-ohm)

Power A: AVDD D: DVDD P1: PVDD1 P2: PVDD2

I/O: Input/Output pin I : Input pin O: Output pin G: Ground pin P: Power Supply pin



Pull Up / Down Pins

Pin Name	Pull-up/Down	Pull-Up/Down Resistor
TEST0	Pull Down	Approx. 100k-ohm
TEST1	Pull Down	Approx. 100k-ohm
TMO	Pull Down	Approx. 100k-ohm

5. Electrical Characteristics

- Absolute Maximum Ratings (* Power supply voltages are values where each ground pin(DVSS=AVSS) is at 0V)

Parameter	Min.	Max.	Unit
Power Supply (VDD)			
AVDD (DAC, PLL, VREF)		4.2	
DVDD (Digital Core)	-0.3	2.2	V
PDVD1(Digital I/O)		4.2	
PVDD2 (Digital I/O)		4.2	
Input Voltage (VIN)	-0.3	PVDD1 + 0.3 PVDD2 + 0.3	V
Input Current (IIN)		+/- 10	mA
Storage temperature	-40	125	°C

* All power supply ground pins (DVSS, AVSS) should be at the same potential.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
No normal Operating Specifications are not guaranteed at these extremes.

- Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Power Supply (VDD)				
AVDD	2.7	3.0	3.6	
DVDD	1.65	1.8	2.0	V
PVDD1	DVDD	1.8	3.6	
PVDD2	DVDD	1.8	3.6	
Operating Temperature (TA)	-40		85	°C

- Analog Characteristics and Power Dissipation (operating voltage AVDD3.0V, DVDD 1.8V Temperature 25°C)

Parameter	Min	Typ.	Max.	Unit	Condition
DAC Resolution		10		bit	
Integral Non-Linearity Error INL		+/- 0.6	+/- 2.0	LSB	Note 1)
Differential Non-Linearity Error DNL		+/- 0.4	+/- 1.0	LSB	Note 1)
Output Full Scale Voltage	1.15	1.28	1.41	V	Load Resistor 300Ω
DAC SNR		54		dB	Note 2)
Output Bandwidth		+/- 1		dB	Note 3)
Unbalances between DACs		1.5	3	%	Note 4)
Internal Reference Voltage		1.43		V	
Internal Reference Drift		60		ppm/°C	
Current Consumption of Analog part		30	40	mA	Note 5)
Current Consumption of Digital part					
Component Encoder mode		35	70	mA	Note 6)
Composite Encoder mode		8	16	No	
DAC mode		8	16		
Current Consumption of Sleep mode		1		mA	
Current Consumption of Power down		10	300	uA	PDN=Low

Note 1. DAC: 148MHz Operation

Note 2. 2MHz Sin-wave input. (Noise Band-Width 0 – 30MHz)

Note 3. Output Bandwidth 30MHz: at 148MHz Operation DAC1 (Load Resistor 300ohm) Channel Only External Load Capacitor 10 pF (SubAddress[0x0A] HDAFLT[1:0]=11)

Note 4. Variation when a 700 mV equivalent code is input on DACs.

Note 5. DAC 3ch ON fs=74MHz / Component mode (Y: 30MHz Sin wave, CbCr: 15MHz Sin wave)

Note 6: Clock-rate and Input data is

Composite Video Encoder mode: 515i (27MHz) Internal Color Bar

Component Video Encoder mode: 1080i (74MHz) Y: 30MHz Sin wave, CbCr: 15MHz Sin wave)

High Speed DAC mode: 54MHz Clock 20MHz Sin wave Data input.

■ Digital Input / Output DC Characteristics

(AVDD=2.7-3.6V, DVDD=1.65-2.0V, PVDD1= 1.65-3.6V, PVDD2 = 1.65-3.6V Ta= -40-85°C)

Parameter	Symbol	MIN	TYP	MAX	unit	Condition
High Level Input Voltage 1	VIH1	0.70 PVDD1			V	Note. 1
High Level Input Voltage 2	VIH2	0.70 PVDD2			V	Note. 2
Low Level Input Voltage 1	VIL1			0.30 PVDD1	V	Note. 1
Low Level Input Voltage 2	VIL2			0.30 PVDD2	V	Note. 2
High Level Output Voltage	VOH	0.80 PVDD2			V	Note. 3 IOH = -600 uA
Low Level Output Voltage	VOL			0.20 PVDD2	V	Note. 3 IOL = 1.4 mA
Input pin Leakage Current	ILIKG			±10	uA	Note. 4
I2C High Level Input Voltage	VIHC	0.77PVDD1			V	Note. 5
I2C Low Level Input Voltage	VILC			0.21PVDD1	V	Note. 5
I2C Low Level Output Voltage	VOL2			0.4	V	Note. 6 IOLC=3mA

Note. 1. PDN pin.

Note. 2. CLKIN, DATA[17:0], HDI, VDI pins

Note. 3. HDO, VDO pins

Note. 4. CLKIN, DATA[17:0], HDI, VDI, PDN, SELA, SDA, SCL pins

Note. 5. SELA, SDA, SCL pins

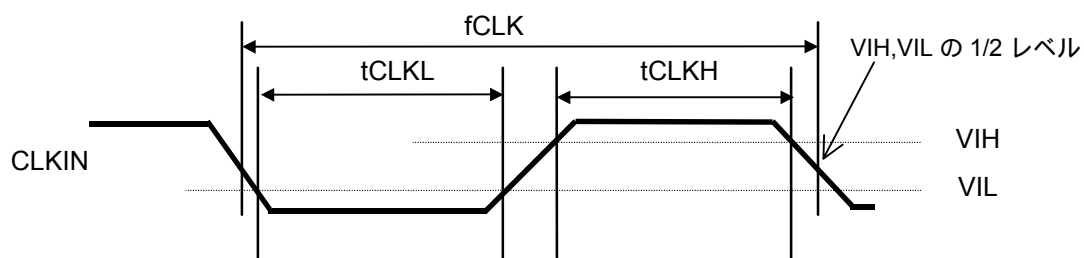
Note. 6. SDA pin

■ AC Timing

(AVDD=2.7-3.6V, DVDD=1.65-2.0V, PVDD1 = DVDD-3.6V, PVDD2 = DVDD-3.6V Ta: -40□-85°C)

(1) CLKIN

(1-1) Component Video Encoder / Composite Video Encoder mode

**Fig. 7**

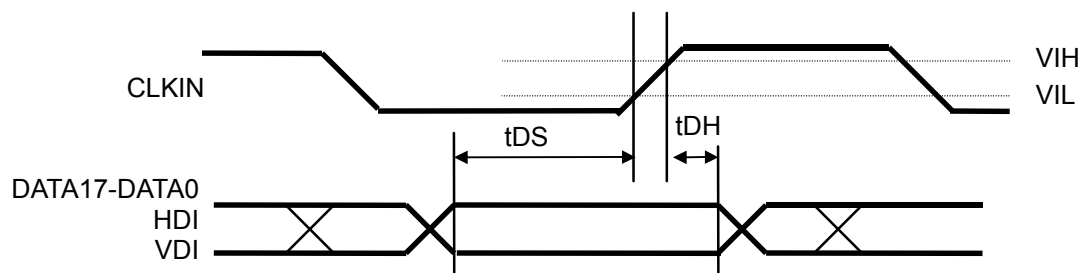
parameter	Symbol	min	Typ	max	unit	Note
CLKIN fCLK			74.25 27		MHz	74.25 / 74.175MHz 27MHz(*)
CLKIN Pulse Width H	tCLKH	4.04 15.0			nsec	74.25/74.175MHz 27MHz
CLKIN Pulse Width L	tCLKL	4.04 15.0			nsec	74.25 / 74.175MHz 27MHz

(*) Accuracy of frequency may affect to color display.

(1-2) Video DAC mode

parameter	Symbol	min	typ	max	unit	Note
CLKIN f	CLK	6		54	MHz	
CLKIN Pulse Width H	tCLKH	7.4			nsec	
CLKIN Pulse Width L	tCLKL	7.4			nsec	

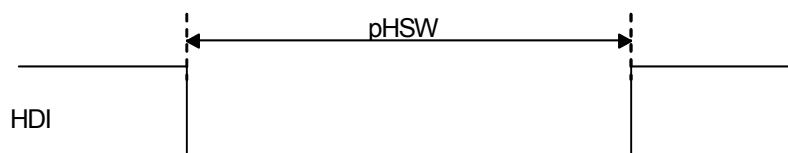
(2) Pixel Data Input Timing

**Fig. 8**

parameter	Symbol	min	typ	max	unit
Data Setup Time	tDS_HD	3.3			nsec
Data Hold Time	tDH_HD	3.3			nsec

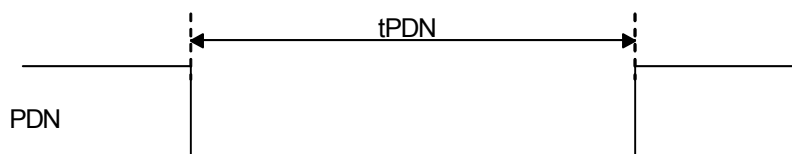
Note) DATA17:DATA0, HDI, VDI can be captured inverted clock edge by register setting

(3) HSYNC Pulse Width

**Fig. 9**

parameter	Symbol	min	typ	max	unit	Note
HSYNC Pulse Width	pHSW	15	128		CLKs	D1 Video 27MHz
		15	64			D2 Video 27MHz
		15	272			D3, D4 Video 74.25MHz

(4) PDN Pulse Width

**Fig. 10**

Parameter	Synbol	min	typ	max	unit	備考
PDN Pulse Width	tPDN	100			ns	

(5) Power Up sequence

There are no order restriction to make power up, AVDD, DVDD, PVDD1, PVDD2.

Clock input is not necessary to write register.

(5-1) The sequence for power down mode after power-up.

Clock input to the CLKIN pin is necessary to guarantee "Current Consumption of Power down"

(r) : Register-bit

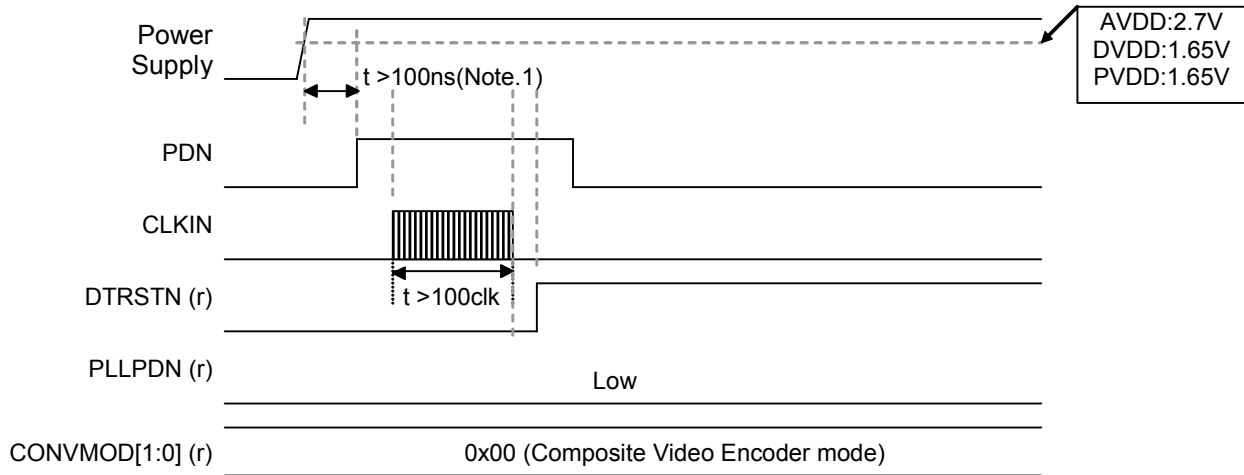


Fig. 11 Power-Up sequence (To make Power down state after power-up)

Note.1) Please wait 100ns for make PDN pin low after the Voltage of Power Supply becomes stable enough,

(5-2) Setting to Composite Video Encoder mode after power-up

After initializing with PDN-pin = Low, AK8826 is Composite Video Encoder mode.

(r) : Register-bit

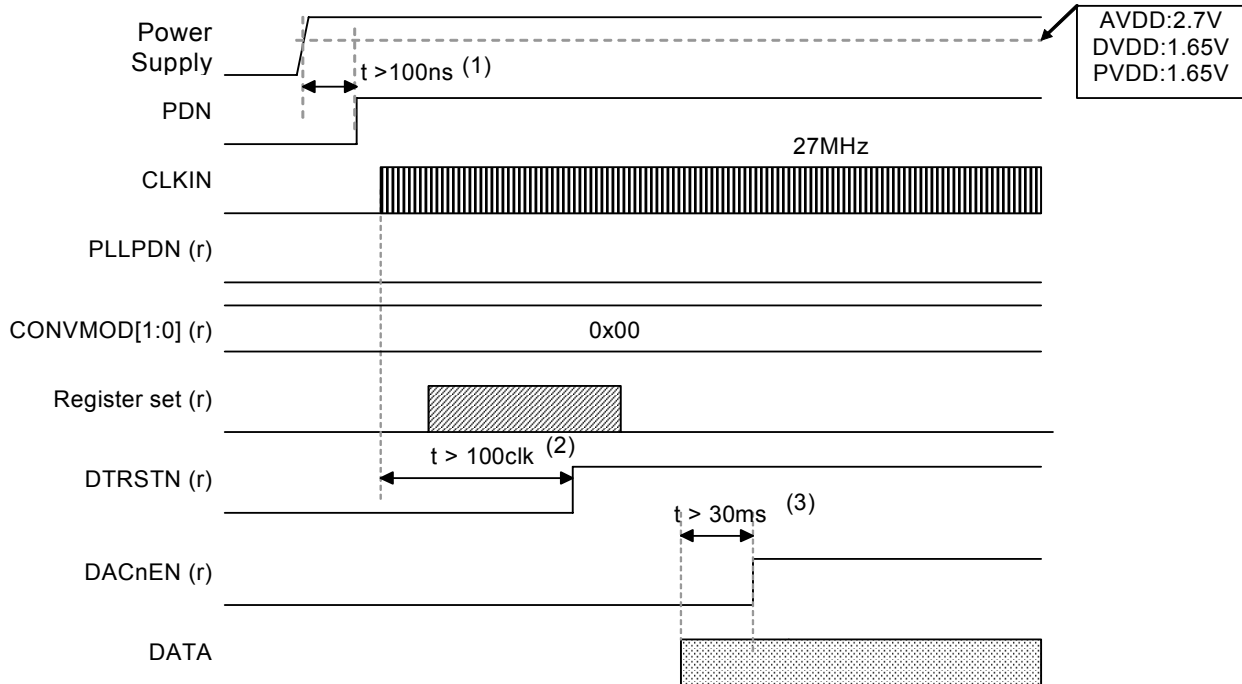


Fig. 12 Power-Up sequence (To set Composite Video Encoder mode after power-up)

- (1) PDN-pin should be Low states more than 100ns after power-up.
- (2) To initialize in Composite Video Encoder Block. Clock input is necessary to CLKIN-pin. DTRSTN-bit should be 0 more than 100clock count.
- (3) BT656 Interface mode operation, it is more than 1-Frame periode to synchronize with input data. To avoid displaying noise etc, DAC should be ON after synchronization.

(5-3) Setting to Component Video Encoder mode after power-up

After initializing with PDN-pin = Low, AK8826 is Composite Video Encoder mode.

Set to Component Video Encoder mode by register setting. (Set CONVMOD[1:0]-bit = [01])

(r) Shows Register-bit

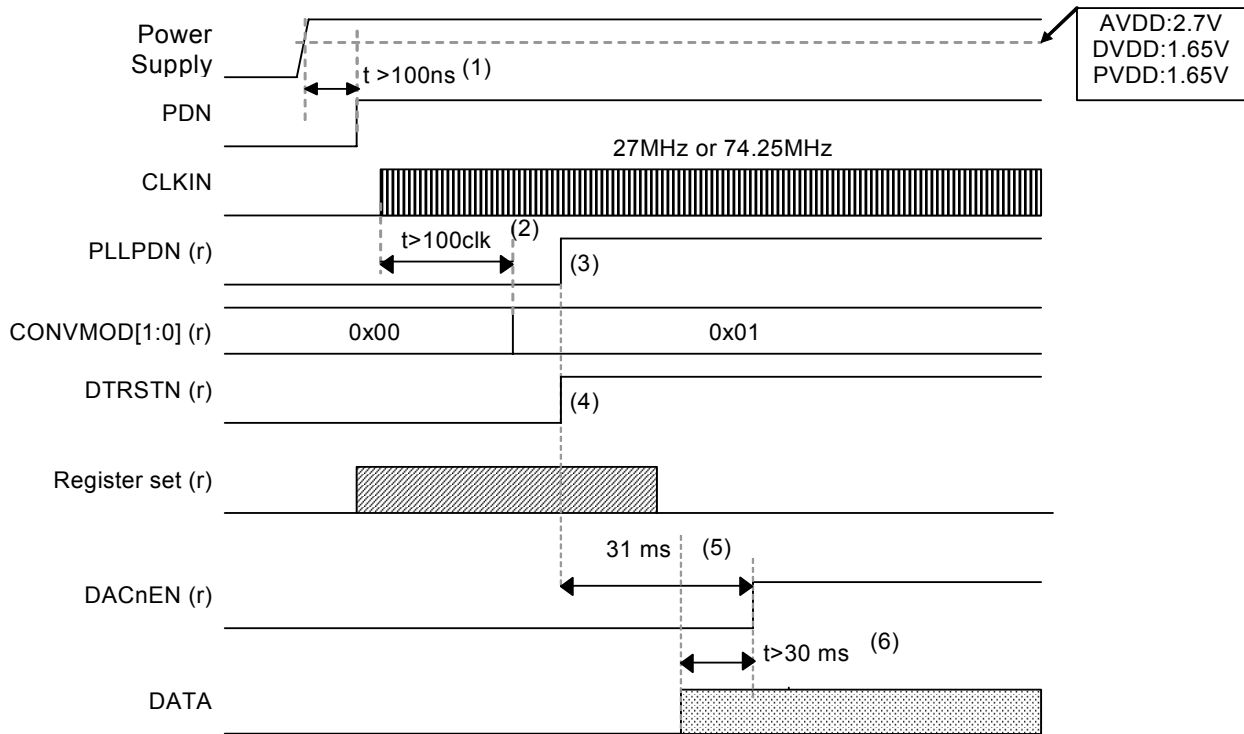


Fig. 13 Power-Up sequence (To set Component Video Encoder mode after power-up)

- (1) PDN-pin should be Low states more than 100ns after power-up.
- (2) Set to Component Video Encoder mode after 100clock count with Clock Input to CLKIN-pin.
- (3) PLLPDN-bit should be set to High after setting Component Video Encoder mode.
- (4) DTRSTN-bit should be set to High after setting component Video Encoder mode.
- (5)(6) After setting PLLPDN -bit = High, wait more than 31ms, then set DAC ON.

(5-4) Setting to High Speed Video DAC mode after power-up

After initializing with PDN-pin = Low, AK8826 is Composite Video Encoder mode.

Set to Component Video Encoder mode by register setting. (Set CONVMOD[1:0]-bit = [10])

(r) shows Register-bit

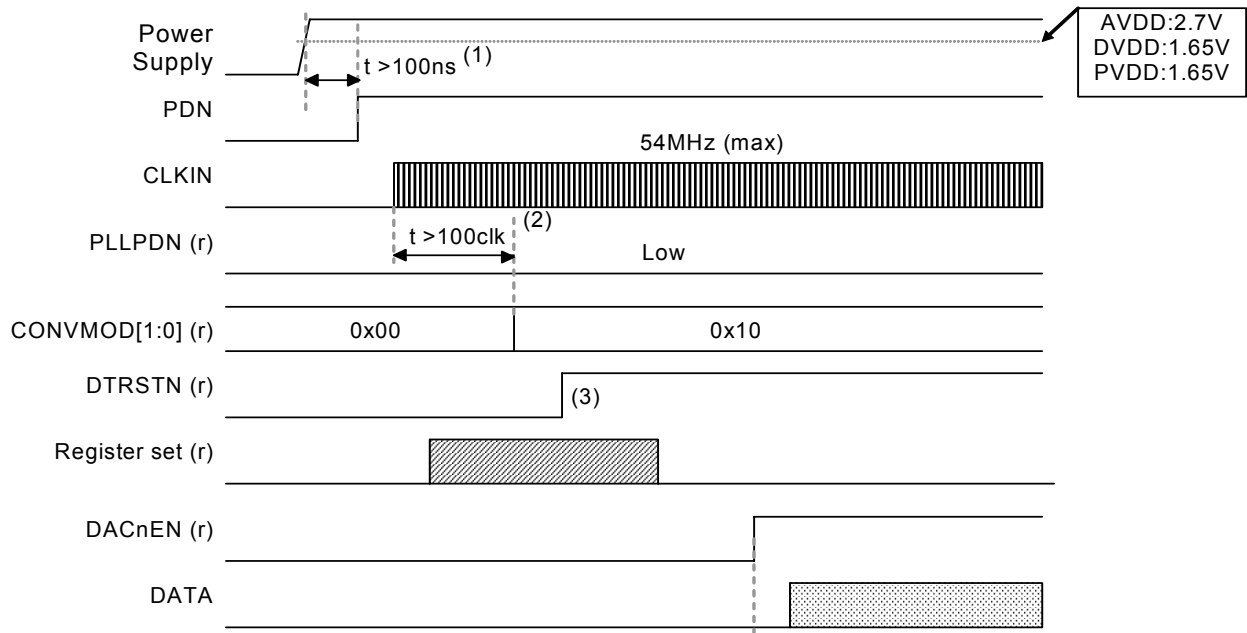


Fig. 14 Power-Up sequence (To set High Speed Video DAC mode after power-up)

- (1) PDN-pin should be Low states more than 100ns after power-up.
- (2) Set to High Speed DAC mode after 100clock count with Clock Input to CLKIN-pin.
- (3) Set to DTRSTN-bit should be High after setting High Speed Video DAC mode

(6) Power-Down Sequence and reset sequence after power-down release

Before setting to PDN=LOW, DTRSTN(r) should be Low to initialize.

After power-down release (PDN =LOW -> High), wait for 10ms for Analog Reference Voltage / Current becomes stable.

During PDN=Low (Power down States), either with clock-in or clock-not in is

During PDN = Low, AVDD / DVDD can be power-off.

Power down sequence is shown as Fig. 16. (r) means Register-bit.

PDN = Low makes AK8826 initialize condition, so that after power-down release, make sure register setting.

(6-1) Power-Down and power-down release Sequence from Composite Video Encoder mode

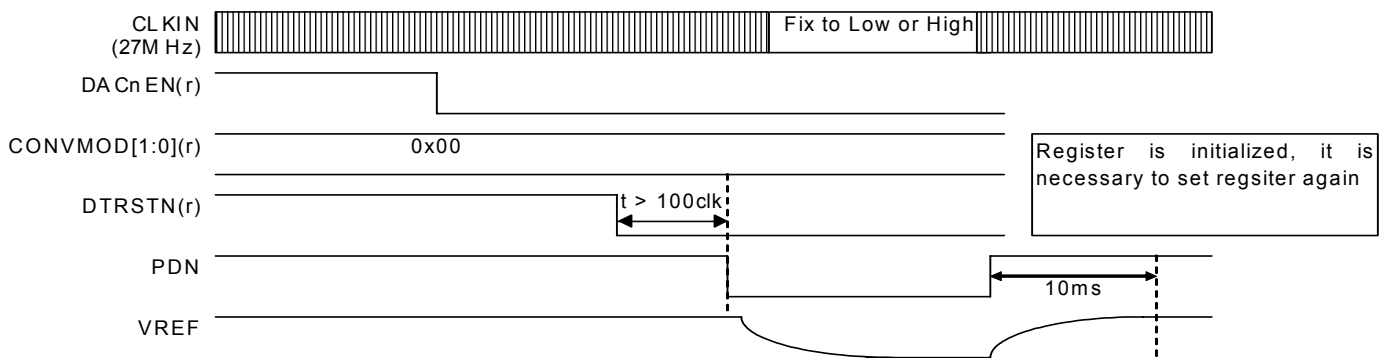
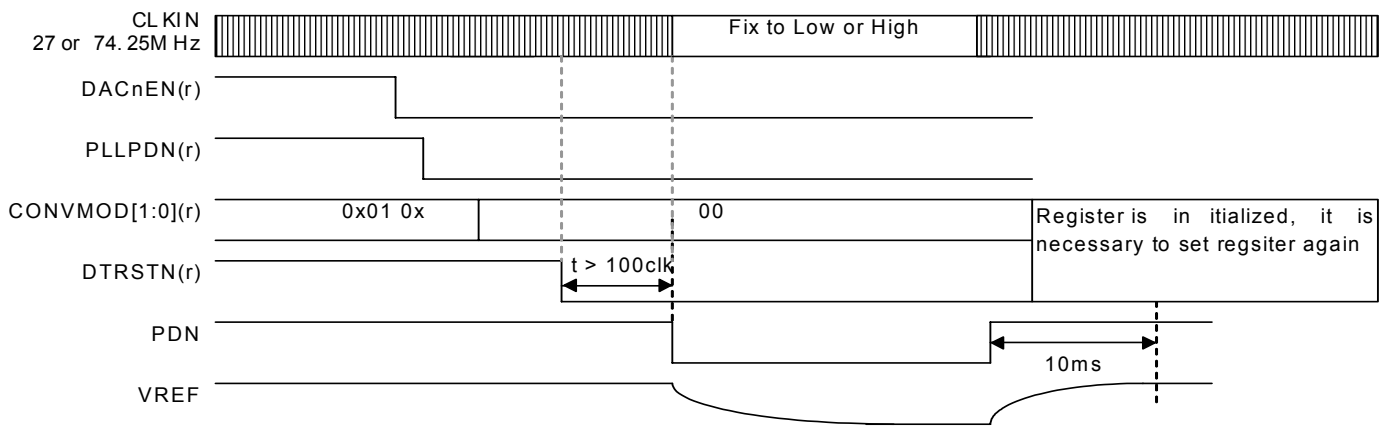
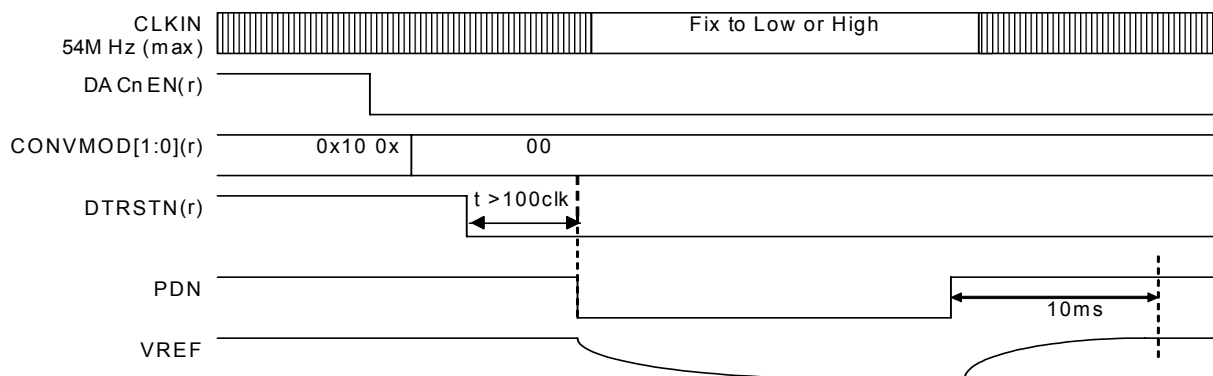


Fig. 15 Power-Down and power-down release Sequence from Composite Video Encoder mode

(6-2) Power-Down and power-down release Sequence from Component Video Encoder mode

**Fig. 16 Power-Down and power-down release Sequence from Component Video Encoder mode**

(6-3) Power-Down and power-down release Sequence from High Speed Video DAC mode

**Fig. 17 Power-Down and power-down release Sequence from Component Video Encoder mode**

(7) I²C Timing
(7-1) Timing 1

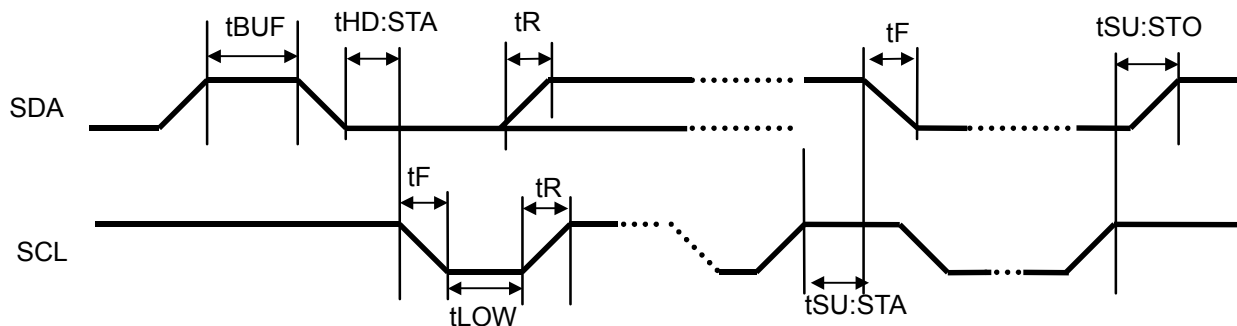


Fig. 18 I²C Timing 1

parameter	symbol	min	max	unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

The above I2C Bus related timings are I2C Bus specifications, and they are not the device limits. For details, refer to I2C Bus Specifications.

(7-2) Timing 2

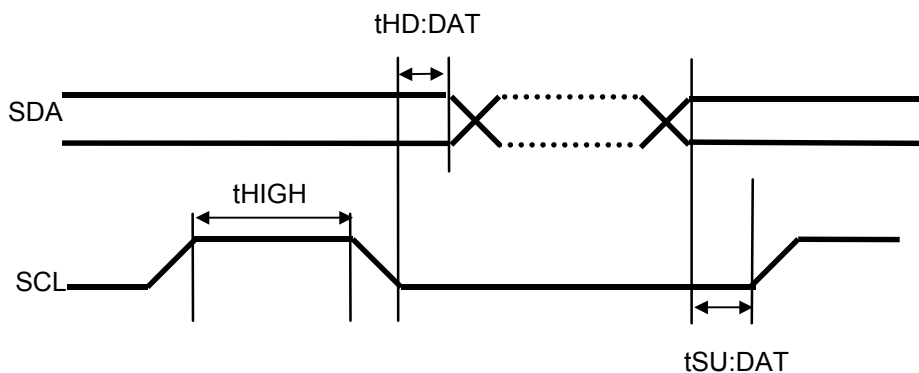


Fig. 19 I²C Timing 2

parameter	symbol	min	max	unit
Data Setup Time	tSU:DAT	100 (note1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (note2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

note 1 : when to use in I2C Bus Standard mode, tSU : DAT ≥ 250 nsec must be satisfied.

note 2 : when the AK8826 is used on not-extended tLOW Bus (used at tLOW = minimum specification), this condition must be satisfied.

R/W operation to the register is possible without Clock input to CLKIN-pin.

6. Common Function Specification

This section describes common function specifications among Composite Video Encoder, Component Video Encoder, High Speed Video DAC function Block.

■ Device Control Interface

The AK8826 is controlled via I2C Bus Control Interface.

[I2C Bus Slave Address]

I2C Slave Address is selectable to be either 0x40 or 0x42 by SELA pin setting.

SELA -pin		SLAVE Address
Low	(PVSS1)	0x40
High	(PVDD1)	0x42

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	0 0		0	0	SELA	

[I2C Control Sequence]

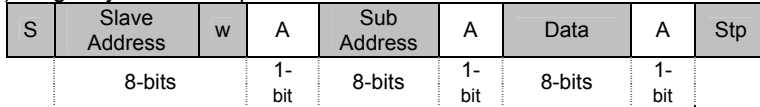
(1) Write Sequence

When the Slave Address of the AK8826 Write mode is received at the first byte, Sub-Address at the second byte and Data at the third & succeeding bytes are received.

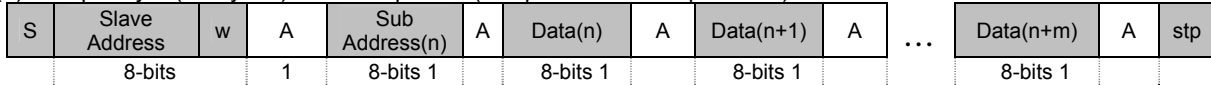
There are 2 operations in Write sequence—

A sequence to write at every single byte, and a sequential write operation to write multiple bytes successively.

(a) Single byte Write sequence

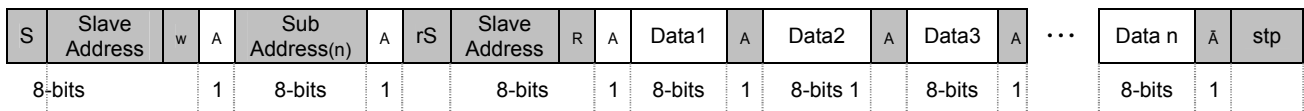


(b) Multiple Byte (m-bytes) Write Sequence (Sequential Write Operation)



(2) Read Sequence

When the Slave Address of the AK8826 Read Mode is received at the first byte, data at the second and succeeding bytes are transmitted from the AK8826.



Abbreviated Terms listed above mean :

S, rS : Start Condition
A : Acknowledge (SDA low)
 $\bar{A}$: Not Acknowledged (SDA high)
Stp : Stop Condition
R / W : 1 : Read, 0 : Write

: to be controlled by the Master Device. To be output by micro-computer normally.

: to be controlled by the Slave Device. To be output by the AK8826.

Note: At the MultipleByte Read/Write Sequence, read or write register operation cannot be done at one-time.

Add[0x00] - Add[0x35] operation is done, then Add[0x36] - Add[0x3F] should be done.

To read or to write Test Register, 1 Byte Read/Write sequence should be done.

■ Mode Select

AK8826 has 3-function block as Composite Video Encoder, Component Video Encoder and High Speed Video DAC. These functions are selected by CONVMOD[1:0]-bit of **I/O Data Format Register (R/W) [Sub Address 0x0B]**.

At mode change timing, CONVMOD[1:0]-bit and DACnEN-bit of **DAC Control Register(R/W) [Sub Address 0x0D]** and PLLPDN-bit of **Powerdown Mode Register (R/W) [Sub Address 0x06]** should be taken care.

I/O Data Format Register

Sub Address 0x0B

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDSDMASE	YC2RGB	Reserved	DTFMT	CONVMOD1	CONVMOD0	INPFMT1	INPFMT0

CONVMOD[1:0]-bit	Mode	Note
00	Composite Video Encoder mode	Component Video Encoder Block becomes power down state automatically. PLL Block is still working, PLLPDN-bit can make PLL block to power down state.
01	Component Video Encoder mode	Composite Video Encoder Block becomes Power down states automatically. PLLPDN-bit should be set to "1" for this mode.
10	High Speed Video DAC mode	Composite/Component Video Encoder Block become power down state automatically. PLLPDN-bit should be set to "0" .
11	Reserved	Reserve set

DAC Control Register

Sub Address 0x0D

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	OLVL	DTRSTN	CVBSSEL DA	C3EN	DAC2EN	DAC1EN

Output signal from DAC1/2/3 with setting DACnEN-bit =1 (n=1,2,3)

	CONVMOD[1:0]-bit			condition
	00		01	
	CVBSSEL=0	CVBSSEL=1		
DAC1 output	Y	CVBS	Y	DAC1EN=1
DAC2 output	C	-	Pb	In CVBSSEL=1 case, DAC2EN -bit and DAC3EN-bit should be set 0. (Output signal from DAC2, DAC3 is 0)
DAC3 output	CVBS	-	Pr	

Powerdown Mode Register

Sub Address 0x06 < HD Block >

Default Value 0x00

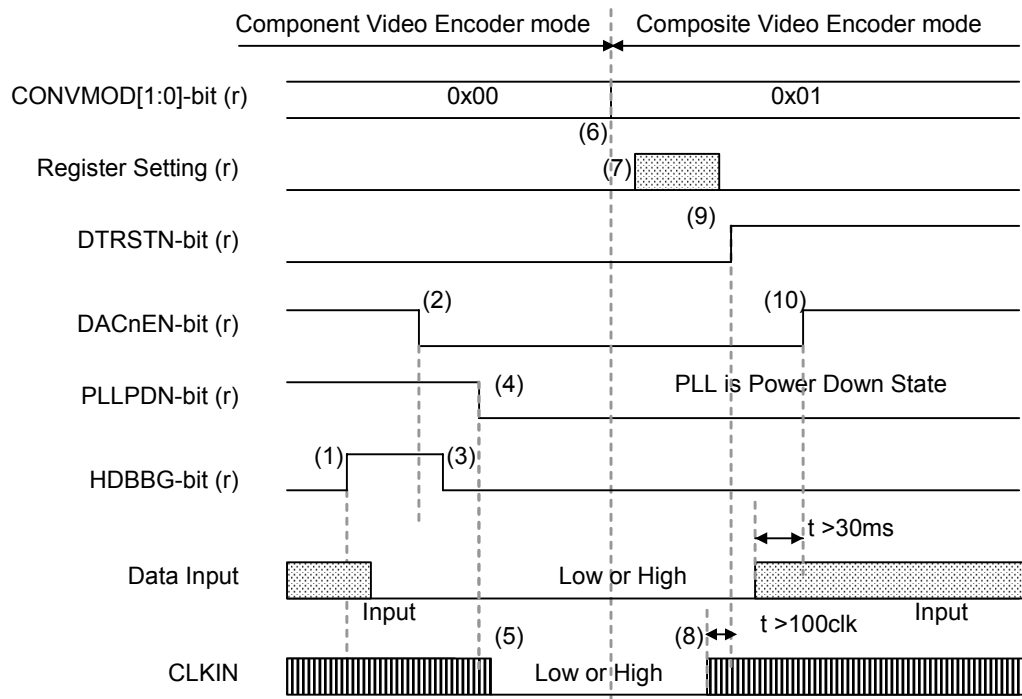
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	PLLPDN	SLPEN1	SLPEN0

When setting to Component mode, PLLPDN-bit should be set to "1" since x2 PLL is necessary to work for Component Video Encoder mode.

PLLPDN-bit	Operation
0	PLL is power down states
1	PLL is working. Component Video Encoder mode, this bit should be set 1.

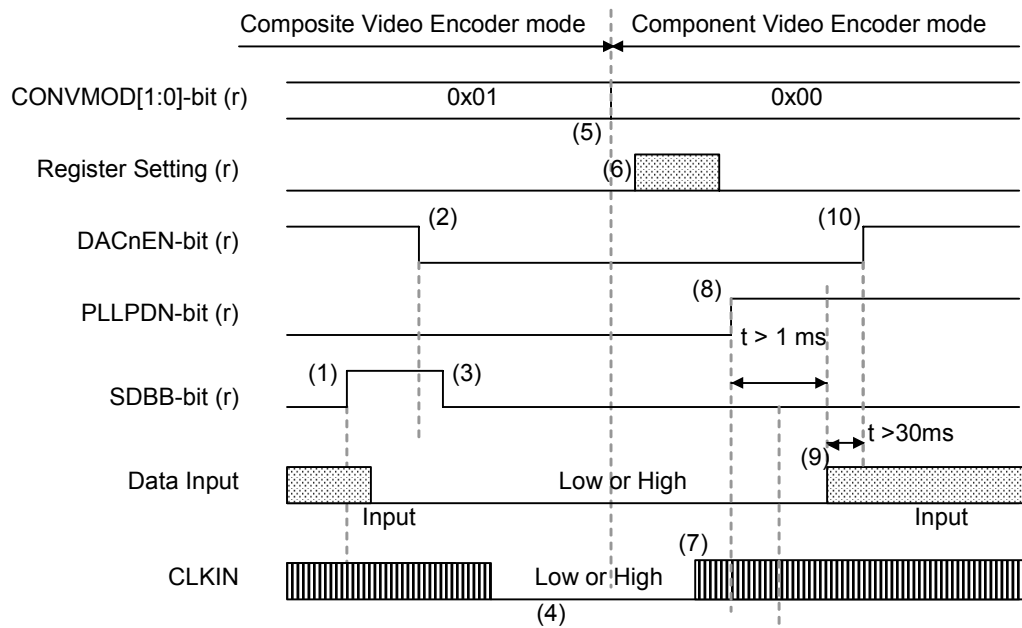
Mode switching sequence

(1) Component Video Encoder mode to Composite Video Encoder mode

**Fig. 20 Mode Switching sequence (Component Video Encoder mode to Composite Video Encoder mode)**

- (1) To avoid making noise, Black Burst Generator is On, then stop inputting data.
- (2) Turn Off DACs.
- (3) Black Burst Generator OFF.
- (4) Set PLLPDN-bit = 0 (PLL Block becomes Power Down States)
- (5) Stop Clock Input to CLKIN pin.
- (6) Mode Change from Component Video Encoder mode to Composite Video Encoder mode.
- (7) Set Sync-mode, Output Signal etc.
- (8) Change clock, if necessary.
It is allowed that changing clock without stopping clock input, however Process(6), (7) should be done before clock change.
- (9) Set DTRSTN=1 after DTRSTN-bit =0.
DTRSTN-bit =0 period should be more than 100-clk counts with clock input.
- (10) Turn On DACs after more than 30ms later

(2) Composite Video Encoder mode to Component Video Encoder mode

**Fig. 21 Mode Switching sequence (Composite Video Encoder mode to Component Video Encoder mode)**

- (1) To avoid making noise, Black Burst Generator is On, then stop inputting data.
- (2) Turns OFF DACs.
- (3) Black Burst Generator OFF.
- (4) Stop Clock Input to CLKIN pin.
- (5) Mode Change from Composite Video Encoder mode to Component Video Encoder mode.
- (6) Set Sync-mode, Output Signal etc.
- (7) Change clock, if necessary.
It is allowed that changing clock without stopping clock input, however Process (6), (7) should be done before clock change.
- (8) After Input Clock becomes stable, Internal PLL makes power-up. (PLLPDN-bit = 1)
- (9) After PLL becomes stable, starting input video data.
- (10) Turn ON DACs after more than 30ms later

(3) Clock rate change in Component Video Encoder mode

Fig.23 shows the sequence of Clock rate is changed from 27MHz to 74.25MHz or 74.25MHz to 27MHz.

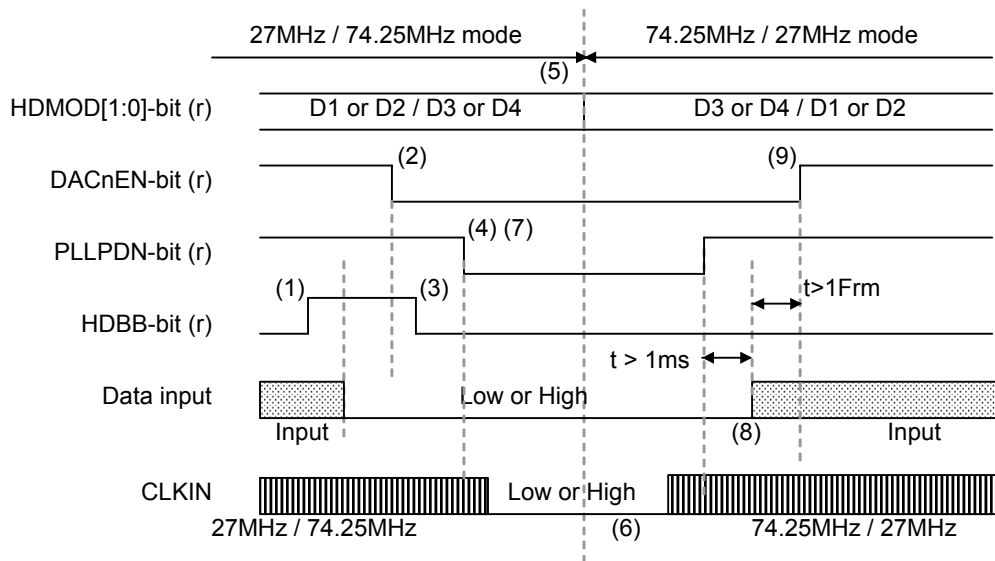


Fig. 22 Clock rate change in Component Video Encoder mode

- (1) To avoid making noise, Black Burst Generator is On, then stop inputting data.
- (2) Turns Off DACs
- (3) Black Burst Generator OFF.
- (4) Set PLLPDN-bit = 0 (PLL Block becomes Power Down States)
- (5) Mode Change, for example, from D1 to D3.
- (6) Change clock
It is allowed that changing clock without stopping clock input, however, PLLPDN-bit should be 0.
- (7) Turning on PLL (Set PLLPDN-bit = 1)
- (8) After PLL becomes stable, starting input video data.
- (9) Turn ON DACs after more than 30ms later

■ Clock

Input Clock is determined by output signal. The relation between input Clock and the output signal is defined as following table.

Input Clock

	NTSC/PAL Composite Video Encoder mode	Component Video Encoder mode		High Speed Video DAC mode
		D1, D2	D3, D4	
Input Clock to CLKIN pin	27MHz	27MHz	74.25MHz	54MHz (max)
DAC operation clock rate	27MHz	54MHz	148.5MHz	Clock to CLKIN pin
Internal PLL status	OFF	ON	ON	OFF

D1 = 480i/576i(525i/625i), D2 = 480p/576p (525p/625p), D3 = 1080i (1125i), D4 = 720p (750p)

In case of switching clock, PLLPDN-bit of Powerdown Mode Register (R/W) [Sub Address 0x06] should be "0".

■ Internal PLL

AK8826 has x2 PLL.

In case of Component Video Encoder mode, PLL should be on.

In time to switch clock rate, PLLPDN-bit should be "0".

Powerdown Mode Register

Sub Address 0x06 < HD Block >

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	PLLPDN	SLPEN1	SLPEN0

PLLPDN	Function
0	PLL is Power Down
1	PLL is working. Set PLLPDN=1, in case of Component Video Encoder mode.

■ Reset

(1) Component Video Encoder Block and High Speed DAC Block, and Serial Interface Block are reset with making PDN-pin = Low. It is not necessary to input clock to CLKIN pin.

(2) Composite Video Encoder Block.

Composite Video Encoder Block is reset under the condition of DTRSTN-bit = "0" of **DAC Control Register(R/W) [Sub Address 0x0D]** with clock input to CLKIN-pin. It should be keep DTSTN-bit = "0" at least 100 clock count.

DAC Control Register

Sub Address 0x0D

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	OLVL	DTRSTN	CVBSSEL	DAC3EN	DAC2EN	DAC1EN

After Reset all register values become default value, and Video DAC output pins become Hi-z.

■ Power Down

It is possible to make AK8826 power down states with PDN-pin = Low. Power down sequence is defined section (6) Power-Down Sequence and reset sequence after power-down release of AC Timing definition.
After releasing PDN-Pin =Low, all register values become default values, It is necessary to set the register again.
During PDN pin =Low, AVDD and DVDD can be power-off with PVDD1and PVDD2=ON.

■ Sleep Mode

To set SLPEN[1:0]-bit of **Powerdown Mode Register (R/W) [Sub Address 0x06]** =[11], AK8826 becomes sleep mode. In this mode, all blocks except serial I/F block become power down mode. To save power consumption much less, use the PDN-pin.

Sub Address 0x06 < HD Block >						Default Value 0x00	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	PLLPDN	SLPEN1	SLPEN0

■ Data Input Format

AK8826 supports 4 kinds of Data Input Format such as 8-bit YCbCr / 16-bit YCbCr / 18bit RGB / 16-bit RGB formats. Data Input Format can be defined by INPFMT[1:0]-bit and DTFMT-bit of **I/O Data Format Register (R/W)**.

I/O Data Format Register

Sub Address 0x0B

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDSDMASE	YC2RGB	Reserved	DTFMT	CONVMOD1	CONVMOD0	INPFMT1	INPFMT0

INPFMT[1:0] -bits defines bit width. Detailed setting is shown in following table

INPFMT[1:0]-bit	Input Data Format (width)	Note
00	8-bit Data input	
01	16-bit Data Input	
10	18-bit Data Input	
11	Reserve	

DTFMT -bit defines Data format.

DTFMT -bit	Input Data Format
0	YCbCr Data format
1	RGB Data Format In case of CONVMOD[1:0]=[00] or [01], internal RGB to YCbCr convertor works*

* In case of RGB Input mode, AK8826 doesn't support Rec.656 I/F mode.

* 525i/625i/525P/625P composite, component encode only.

CONVMOD[1:0] -bits define encoder mode show as following table.

CONVMOD[1:0] -bit	mode
00	Composite Video Encoder mode
01	Component Video Encoder mode
10	High Speed DAC mode
11	Prohibited to set

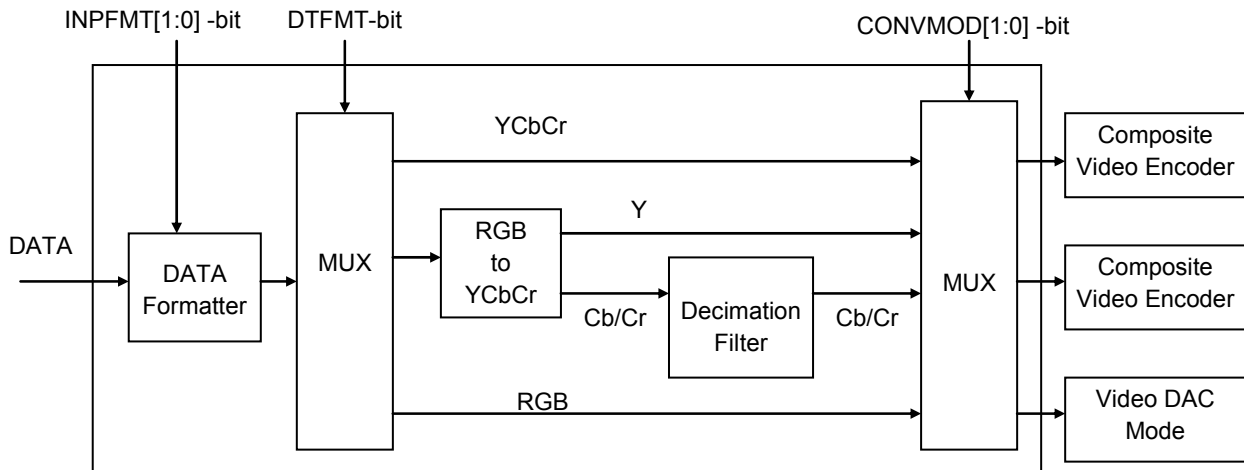


Fig. 23 Data Interface block outline

(2) YCbCr 16bit Data Input Format

In case of 525i / 625i / 525P / 625P / 1080i / 720P Data input, this format is used.

The relation between input data format and Input clock rate to CLKIN pin are relation as follows,

525i / 625i / 525p / 625p : 27MHz

1080i / 720p / : 74.25MHz

DATA15-DATA0 pins are used as Data Input pins.

Y_n / Cb_n / Cr_n means $Y[n]$ / $Cb[n]$ / $Cr[n]$ in following table.

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	Cb7 Cr7	Cb6 Cr6	Cb5 Cr5	Cb4 Cr4	Cb3 Cr3	Cb2 Cr2	Cb1 Cr1	Cb0 Cr0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

D17 - D0 corresponds to DATA17 - DATA0 pins

The Register setting is defined as following table.

[I/O Data Format Register] Setting

INPFMT[1:0]-bit	DTFMT-bit	Note
01	0	16bit YCbCr Data Input

Output signal is set CONVMOD[1:0]-bit of I/O Data Format Register (R/W) [Sub Address 0x0B] and HD Mode Register (R/W) [Sub Address 0x00] or SD Block Control Register (R/W) [Sub Address 0x11]

(2-1) 525i / 625i Data input

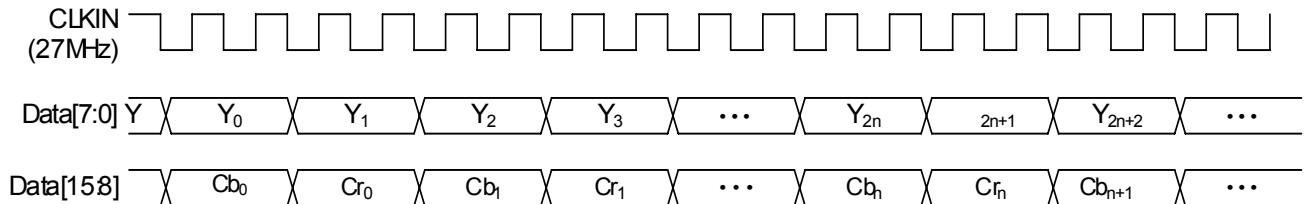


Fig. 25

(2-2) 525P / 625P / 1080i / 720P Data input

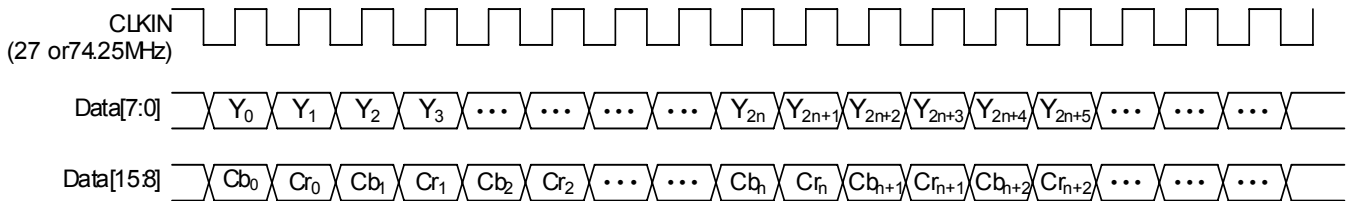


Fig. 26

(3) RGB 8bit Data Input Format (RGB5:6:5)

In case of to encode NTSC/PAL composite Video signal or YPbPr component Video signal from RGB data, this mode is used. Clock rate to CLKIN pin is 27MHz.

DATA7-DATA0 pins are used as Data Input pins. Input data format is RG[7:0] / GB[7:0] shown as following table.

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2			D1	D0
-	-	-					-	-	-	R4 G2	R3 G1	R2 G0	R1 B4	R0 B3	G5 B2	G4 B1	G3 B0		

D17 - D0 corresponds to DATA17 - DATA0 pins

RG Data = [R4, R3, R2, R1, R0, G5, G4, G3]

GB Data = [G2, G1, G0, B4, B3, B2, B1, B0]

The Register setting is defined as following table.

[I/O Data Format Register] Setting

INPFMT[1:0]-bit	DTFMT-bit	Note
00	1	8bit RGB Data Input

Output signal is set CONVMOD[1:0]-bit of **I/O Data Format Register (R/W) [Sub Address 0x0B]** and **HD Mode Register (R/W) [Sub Address 0x00]** or **SD Block Control Register (R/W) [Sub Address 0x11]**

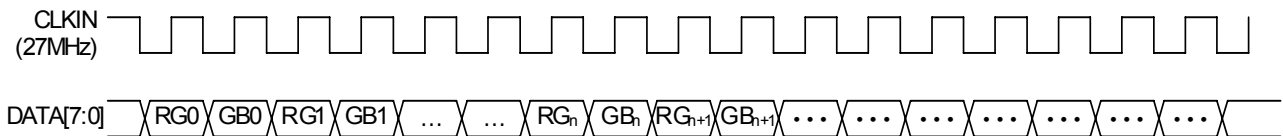


Fig. 27

(4) RGB 16bit Data Input Format (RGB 5:6:5)

In case of encoding NTSC/PAL / 525i/625i , 525p/625p component signal, Clock rate to CLKIN pin 27MHz..

Using as High Speed DAC mode, the maximum conversion rate is 54MHz.

DATA15 - DATA0 pins are used as Data Input pins.

D17	D16	D15	D14	D13	D12	D11		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-	-	R4	R3	R2	R1	R0		G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

The Register setting is defined as following table.

[I/O Data Format Register] Setting

INPFMT[1:0]-bit	DTFMT-bit	Note
01	1	16bit RGB Input

Output signal is set CONVMOD[1:0]-bit of **I/O Data Format Register (R/W) [Sub Address 0x0B]** and **HD Mode Register (R/W) [Sub Address 0x00]** or **SD Block Control Register (R/W) [Sub Address 0x11]**

(4-1) 525i / 625i data input case

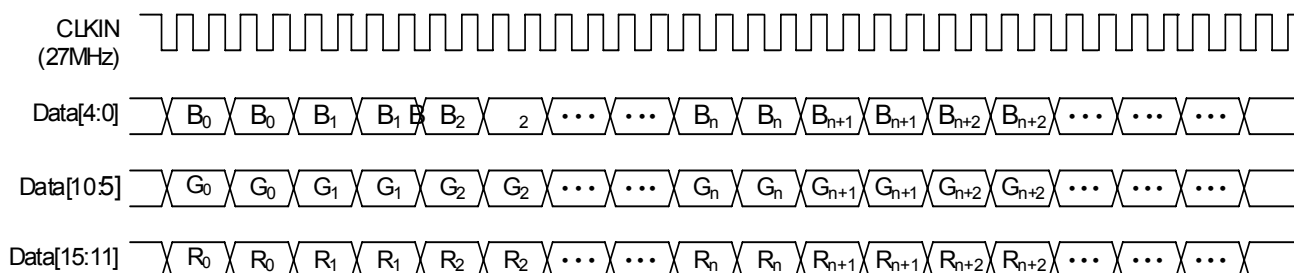


Fig. 28

(4-2) 525P / 625P data input case

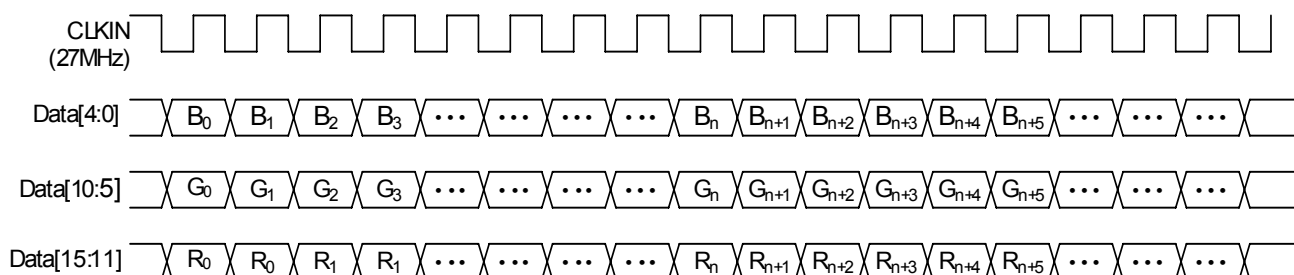


Fig. 29

(5) RGB 18bit Data Input Format (RGB 6:6:6)

In case of encoding NTSC/PAL / 525i/625i , 525p/625p component signal, Clock rate to CLKIN pin 27MHz..

Using as High Speed DAC mode, the maximum conversion rate is 54MHz.

DATA17 - DATA0 pins are used as Data Input pins.

D17	D16	D15	D14	D13	D12	D11		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0		G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

The Register setting is defined as following table.

[I/O Data Format Register] Setting

INPFMT[1:0]-bit	DTFMT-bit	Note
10	1	18bit RGB Input

Output signal is set CONVMOD[1:0]-bit of **I/O Data Format Register (R/W) [Sub Address 0x0B]** and **HD Mode Register (R/W) [Sub Address 0x00]** or **SD Block Control Register (R/W) [Sub Address 0x11]**

(5-1) 525i / 625i data input case

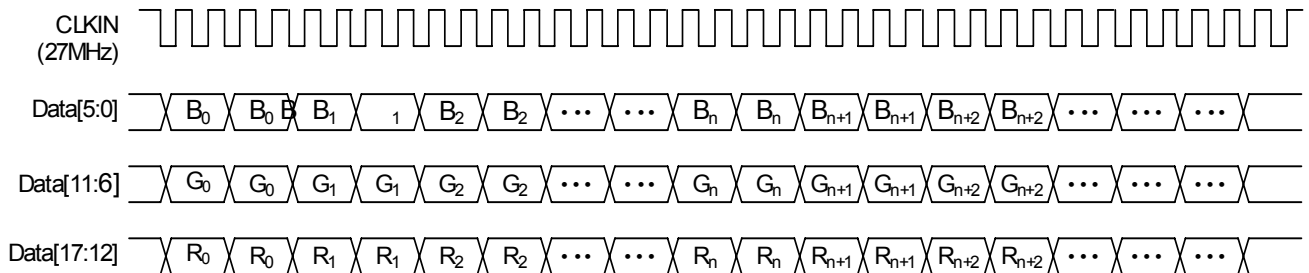


Fig. 30

(5-2) 525P / 625P data input case

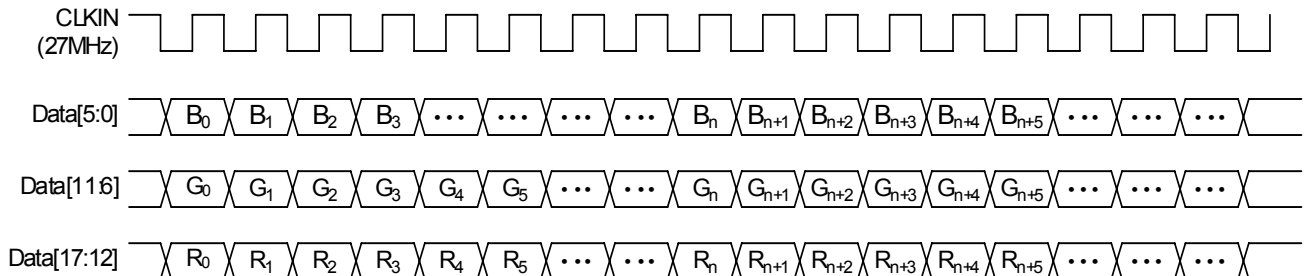


Fig. 31

■ On chip out-put limiter

Limiter function is performed on signals which exceed Pedestal Level.
Limiter Levels are set at “no limiter”, “- 1.5IRE”, “- 7IRE”.

The limit level is set with HDCLPLVL[1:0]-bit of HD VBI & Clip Level Control Register (R/W) [Sub Address 0x01] in Component Video Encoder mode and SDCLPLVL[1:0]-bit of SD Block Delay Register (R/W) [Sub Address 0x13] in Composite Video Encoder mode.

HD VBI & Clip Level Control Register

Sub Address 0x01

default Value 0x04

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCLPLVL1	HDCLPLVL0	Reserved	Reserved	Reserved	HDVUNMSK	HDVL1	HDVL0

SD Block Delay Register

Sub Address 0x13

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDCLPLVL1	SDCLPLVL0	SYD2	SYD1	SYD0	Reserved	Reserved	Reserved

The Limit level defined as this table.

HDCLPLVL[1:0]-bit SDCLPLVL[1:0]-bit	Under-shoot Limit Level
00 no	Clipping
01	Clipped at -7.0 IRE Level
10	Clipped at -1.5 IRE Level
11	Reserved

■ Black Burst Signal Generation Function

The AK8826 can output Black Burst Signal (Black Level Output).

When HDBBG-bit of **HD Mode Register (R/W) [Sub Address 0x00]** in Component Video Encoder mode, SDBBG-bit of **SD Block Control Register (R/W) [Sub Address 0x11]** is set to “1”, same operation is processed as in the case when the fixed-16 Luminance signal and the fixed-Cb/Cr signal outputs are input. In this case when setup-bit is “ON”, set-up process is done and when it is “OFF”, no set-up process is made.

HD Mode Register

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG	HDBBG	HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH

SD Block Control Register

Sub Address 0x11

Default Value 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG	SDCBG	SDSETUP	SCR	SDVM3	SDVM2	SDVM1	SDVM0

■ Color Bar Signal Generation Function

The AK8826 can output 100% Color Bar Signal. Color Bar Signal is output by setting HDCBG-bit of **HD Mode Register (R/W) [Sub Address 0x00]** in Component Video Encoder mode and SDCBG-bit of **SD Block Control Register (R/W) [Sub Address 0x11]** in Composite Video Encoder mode to "1".

HD Mode Register

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG	HDBBG	HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH

SD Block Control Register

Sub Address 0x11

Default Value 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG	SDCBG	SDSETUP	SCR	SDVM3	SDVM2	SDVM1	SDVM0

■ Setup Process Function

In the AK8826, a 7.5% set-up can be added by Register.

In Component Video Encoder mode, HDSETUP-bit of HD Mode Register (R/W) [Sub Address 0x00] is the control bit of this function and, in composite Video Encoder mode, SDSETUP-bit of SD Block Control Register (R/W) [Sub Address 0x11] is the control bit of this function

This bit is enabled at Color-bar Generator mode and Black Burst Generator mode.

HD Mode Register

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG	HDBBG	HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH

SD Block Control Register

Sub Address 0x11

Default Value 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG	SDCBG	SDSETUP	SCR	SDVM3	SDVM2	SDVM1	SDVM0

■ Closed Caption

The AK8826 has encoding function of the Closed Captioning and Extended Data.

ON/OFF control of these functions and its data are in accordance with **SD/HD V-Blanking Control Register (R/W) [Sub Address 0x12]** setting. Data occupies a consecutive 2Byte Register area

Closed Caption Data 1 Register (R/W) [Sub Address 0x26]

Closed Caption Data 2 Register (R/W) [Sub Address 0x27]

for Closed Caption data and

CC Extended Data 1 Register (R/W) [Sub Address 0x28]

CC Extended Data 2 Register (R/W) [Sub Address 0x29]

for Extended data.

Data is written at 0x26/0x28(closed caption / extended data) first, then 0x27/0x29 in this order

Data is judged to be updated when data at 0x27 is written.

When data is updated, it is encoded on a coming thereafter, pre-scribed Line.

When no data updating is made, ASCII Null code is output.

Each data is assumed with ODD parity + 7 bit US ASCII code. Parity is processed at the Host side.

* Closed Caption Data is encoded on the following Lines.

	D1/60 System (SMPTE)	625/50 System (ITU-R)
Closed Caption	21 Line default	22 Line default
Extended Data	284 Line default	335 Line default

RGB output mode doesn't support closed caption encoding function.

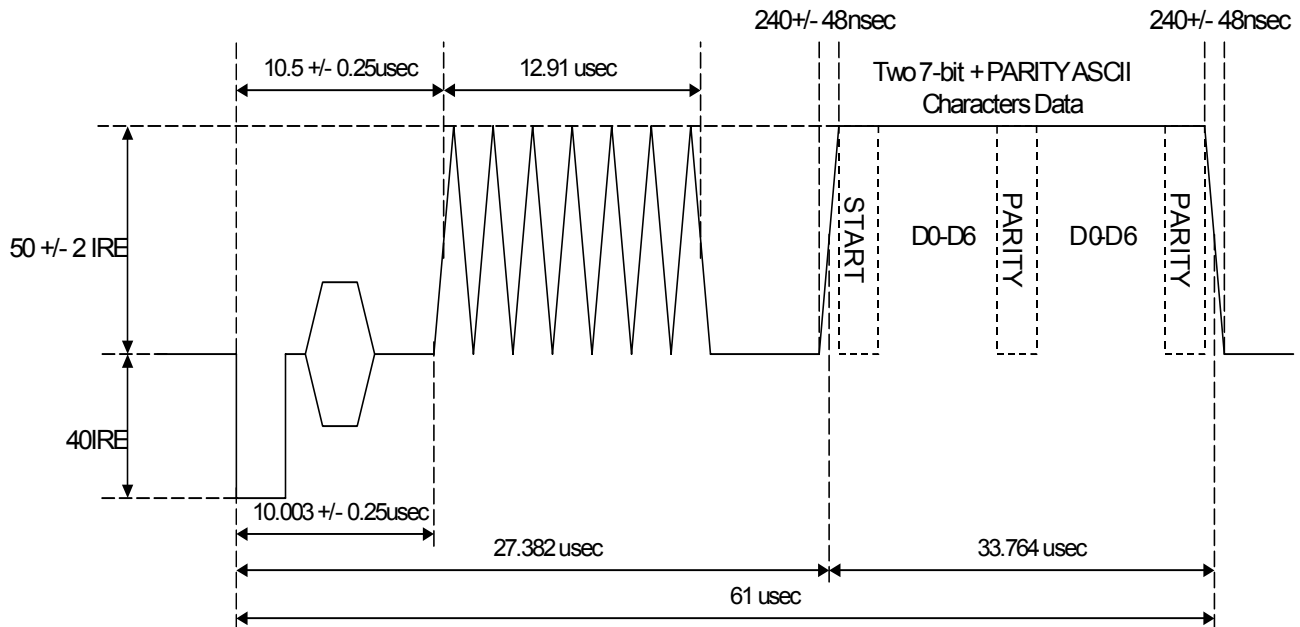


Fig. 32

■ WSS

The AK8826 supports to encode WSS (ITU-R. Bt1119), IEC62375 which distinguish the Aspect Ratio etc. Turning “ON/OFF” of this function is controlled by WSEN-bit of **SD/HD V-Blanking Control Register (R/W) [Sub Address 0x12]** at Composite Video Encoder mode, HDWSS-bit of **HD Block Control Register (R/W)[Sub Address 0x07]**.

Setting data is set to **SD WSS Data 1/2 Register(R/W) [Sub Address 0x18 / 0x19]** at composite Video Encoder mode, and **HD WSS Data 1/2 Register (R/W) [Sub Address 0x08/0x09]** at Component Video Encoder mode.

SD/HD V-Blanking Control Register

Sub Address 0x12

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	SDWSS	SDHDCC284	SDHDCC21	SDVBID

HD Block Control Register

Sub Address 0x07

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDWSS	HDCFLT1	HDCFLT0	HDYFLT1	HDYFLT0	Reserved	COLSNCEN	HDVRATIO

WSS Data Up-date Timing

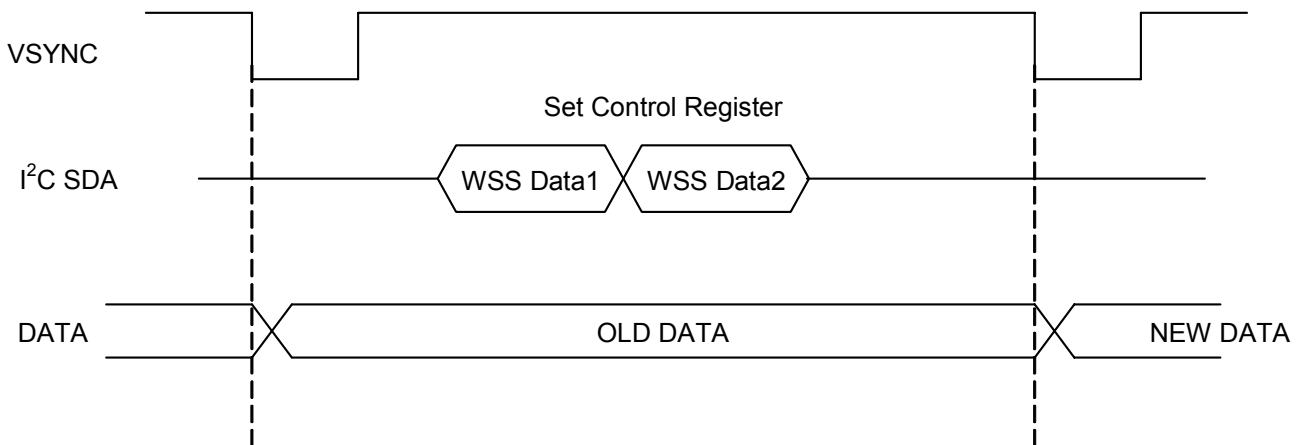


Fig. 33

WSS Data1: Composite Video Encoder mode SubAddress 0x18 / Component Video Encoder mode 0x08

WSS Data2: Composite Video Encoder mode SubAddress 0x19 / Component Video Encoder mode 0x09

WSS Waveform

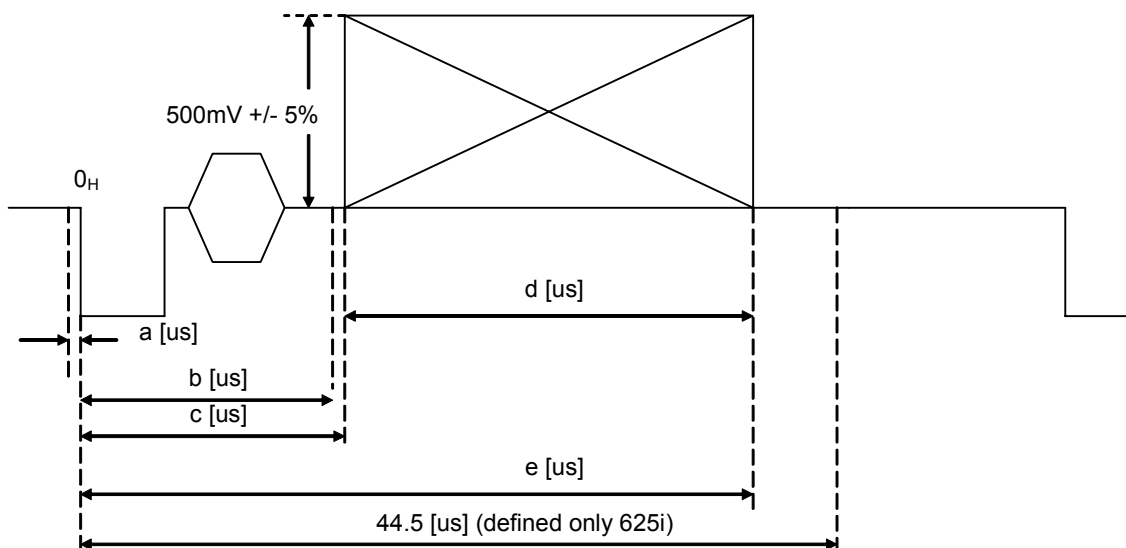


Fig. 34

Encode	Line	Encode Clock	c d		e
625i /50Hz (ITU-R.Bt.1119)	23	5MHz (Ts=200ns)	11.0 +/- 0.25	27.4	38.4
625p /50Hz (IEC 62375)	43	10MHz +/- 1kHz (Ts = 100ns)	5.5 +/- 0.125	13.7	19.2

Encode Line: 625i/50 23-Line / 625p/50 43-Line

The input video data is not encoded on the WSS encoded line.

Coding: bi-phase modulation coding

Run-in St	art code	Group 1 Aspect ratio	Group 2 Enhanced Services	Group 3 Subtitles	Group4 Others
29 elements	24 elements	24 elements	24 elements	18 elements	18 elements
		Bit numbering 0 1 2 3 LSB M SB	Bit numbering 4 5 6 7 LSB M SB	Bit numbering 8 9 10 LSB MSB	Bit numbering 11 12 13 LSB MSB
		0 : 000111 1 : 111000	0 : 000111 1 : 111000	0 : 000111 1 : 111000	0 : 000111 1 : 111000
0x1F1C71C7 0x1E3C1F					

■ Video DAC

The AK8826 has 10-bit resolution, discrete 3 channel current DACs which run at 150MHz.

These DACs are designed to output 1.28V_{o-p} Full Scale with load resistors of 300-ohm(+/-1.0%) when a 3.9k-ohm(+/-1.0%) resistor is connected between IREF pin and AVSS.

VREF pin should be connected to AVDD via 0.1uF or more capacitor, and BYPASS pin should be connected to AVSS via 0.1uF or more capacitor. (Refer to System Connection example.)

Each DAC's "ON/OFF" can be individually controlled by DACnEN-bit (n=1,2,3) of DAC Control Register [SubAddress0x0D]. At the time of DAC-OFF state, the output DAC is Hi-z.

DAC Control Register

Sub Address 0x0D

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	OLVL	DTRSTN	CVBSSEL	DAC3EN	DAC2EN	DAC1EN

The relation between DACnEN-bit (n=1,2,3) and DAC output are shown in following table.

DAC1EN -bit		DAC2EN -bit		DAC3EN -bit	
0	1	0	1	0	1
DAC1=OFF	DAC1=ON	DAC2=OFF	DAC2=ON	DAC3=OFF	DAC3=ON

■ DAC Setting

CVBSSEL-bit of **DAC Control Register(R/W) [Sub Address 0x0D]** sets the output signal from DAC1 and DAC3. Following table shows the output signal and CVBSSEL-bit.

DAC Control Register

Sub Address 0x0D

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	OLVL	DTRSTN	CVBSSEL	DAC3EN	DAC2EN	DAC1EN

	SD-YC output CONVMOD[1:0]=00	SD-CVBS output CONVMOD[1:0]=00	HD output CONVMOD[1:0]=01	Video DAC mode CONVMOD[1:0]=10
CVBSSEL-bit	0	1	0	-
DAC1	Y	CVBS	Y	G
DAC2 C		0-code output	Pb	B
DAC3 CVBS		0-code output	Pr	R

HD output: Output signal from Component Video Encoder Block

SD-YC output and SD-CVBS output: Output signal from Composite Video Encoder Block

The operation clock of DACs is

Composite Video Encoder mode:

Component Video Encoder mode:

High Speed Video DAC mode:

Same clock-rate as the clock fed into CLKIN-pin.

x2 clock rate of the clock fed into CLKIN-pin

Same clock-rate as the clock fed into CLKIN-pin.

7. Multi-Format Component Video Encoder Block

■ Block Diagram

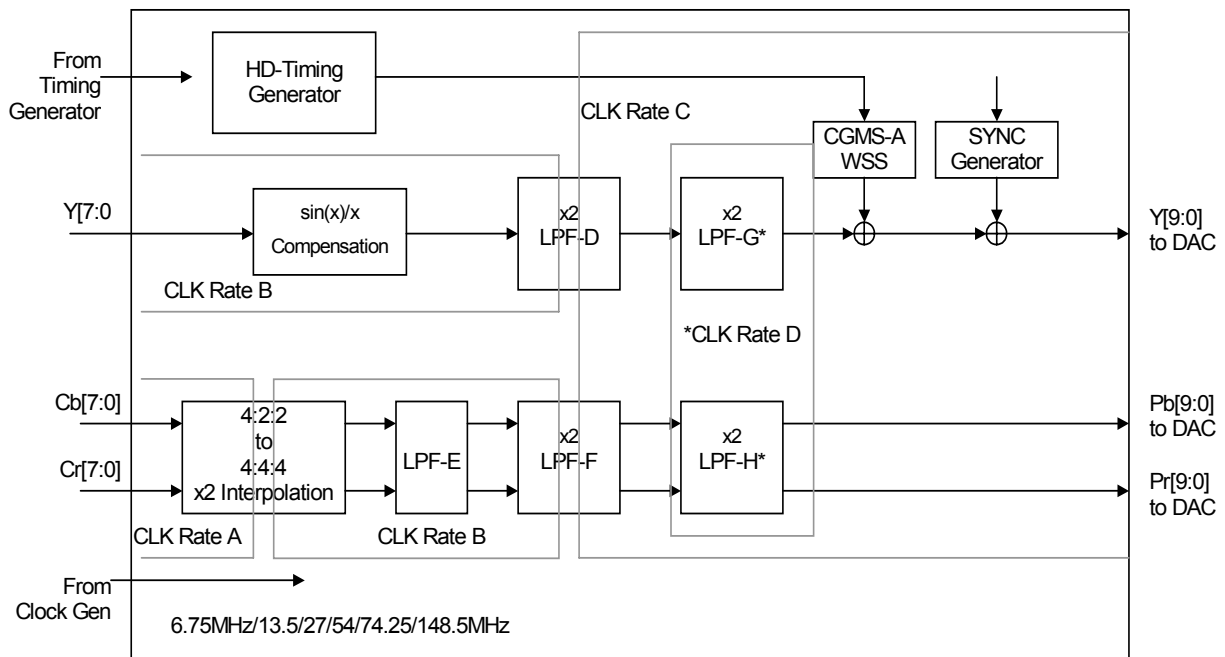


Fig. 35 Component Video Encoder Block

■ Signal Process (Data Path)

The output signal can be set with HDRFRSH-bit, HDMODE[1:0]-bit of **HD Mode Register [Sub Address 0x00]**.

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG HDBBG		HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH

The output signals are defined as following table.

Output signal	HDMODE[1:0] -bit	HDRFRSH -bit	Note
525i 00		0	D1/60
625i 00		1	D1/50
525p 01		0	D2/60
625p 01		1	D2/50
1080i / 60	10	0	D3/60
1080i / 50	10	1	D3/50
720p / 60	11	0	D4/60
720p / 50	11	1	D4/50

(1) Case of 525i /625i Data Input

Y/Cb/Cr multiplexed data synchronized to 27MHz clock fed into CLKIN-pin are input.

When EAV-Decoding mode, the timing signal is extracted from data stream. After extracting sync-timing, the Y/Cb/Cr data are proceeded into Y-process block and Cb/Cr -process block. In case of H/V Slave operation mode, it is same way as EAV sync mode.

As shown in the block diagram,

Y data proceeded by x4 over-sampling filter is added the Sync-timing signal after passing through the delay adjustment block. Cb/Cr data proceeded by x8 over-sampling filter are processed by delay adjustment block. These data are passed to the DAC with 54MHz Clock rate.

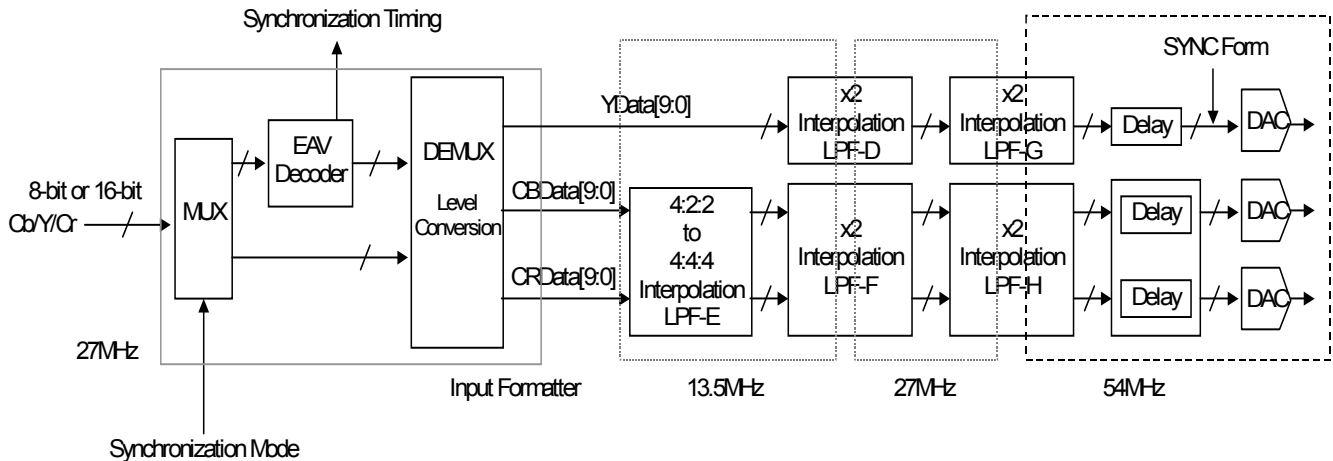


Fig. 36 525i/625i mode Block Diagram

x4 Over-sampling Filter for Y-data (Luminance Data)

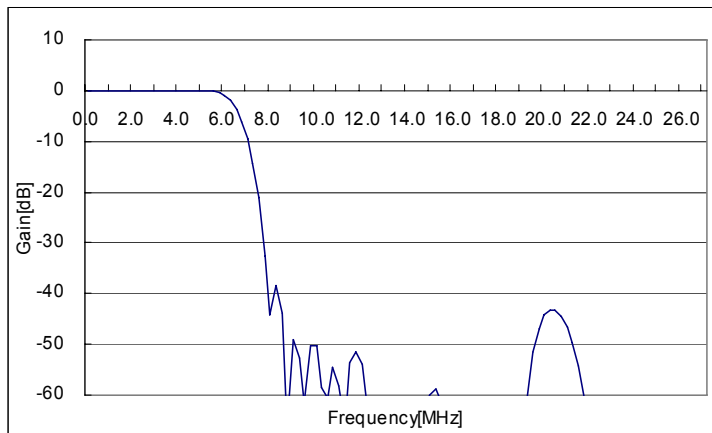


Fig. 37

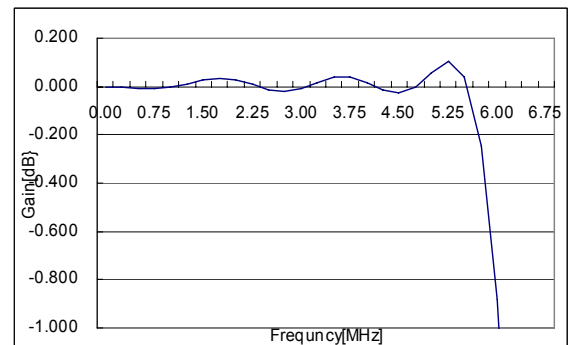


Fig. 38

x8 Over-Sampling Filter for Cb/Cr-Data (Color Data)

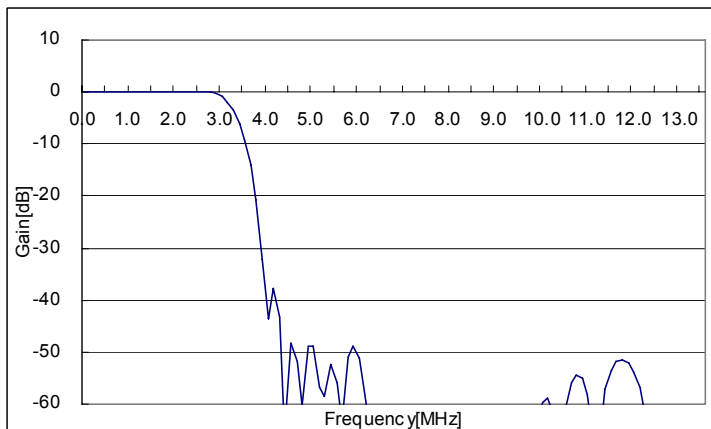


Fig. 39

(2) Case of 525P/625P Data Input

Y/Cb/Cr data should be input with 16-bit width at 27MHz clock-rate.

x2 Over-sampling filter for Y-data and x4 Over-sampling filter for Cb/Cr data is equipped.

The block diagram is shown as follows,

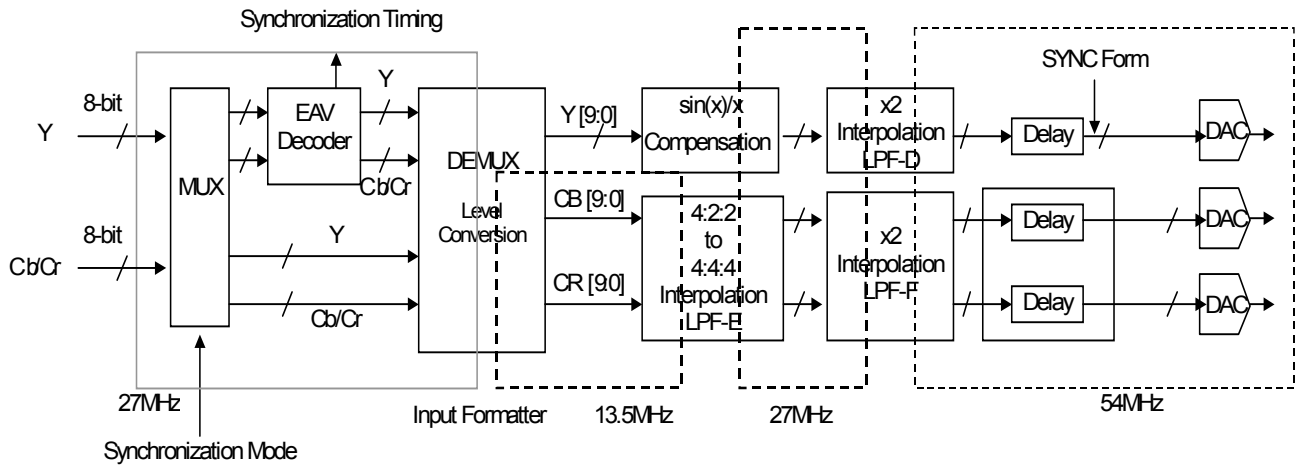


Fig. 40 525P/625P mode Block Diagram

Over-sampling filter with aperture-effect compensation for Luminance (525P/625P)

AK8826 equips the aperture-effect compensation filter for Luminance Signal.

This filter can be set with HDAFT [1:0]-bit of **HD Block Miscellaneous Control Register [Sub Address 0x0A]**. Compensation degree can be set with this register-bit. "Mode 0" is less compensation and "Mode 3" is more compensation.

HD Block Miscellaneous Control Register

Sub Address 0x0A

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	STD770_2C	HDCEA805B	CCWSSSUE	Reserved	HDAFLT1	HDAFLT0
Default Value							
0	0	0	0	0	0	0	0

HDAFLT[1:0]-bit	Filter mode	Note
00	MODE0	less
01	MODE1	
10 MODE2		
11 MODE3		more

x2 Over-sampling Filter for Y-data

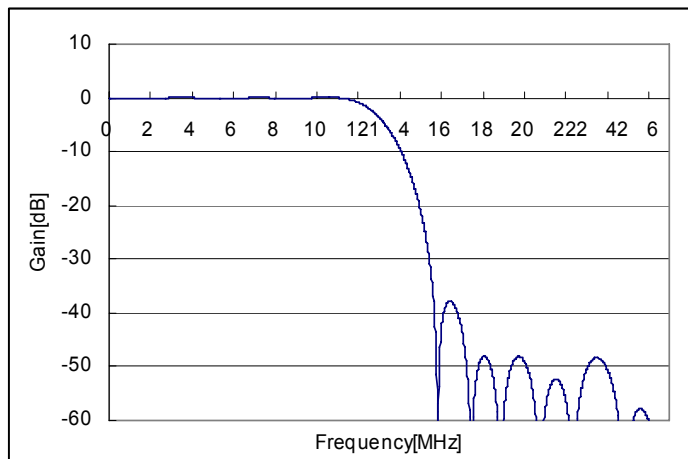


Fig. 42 x2 Over-sampling filter for 525p/625p

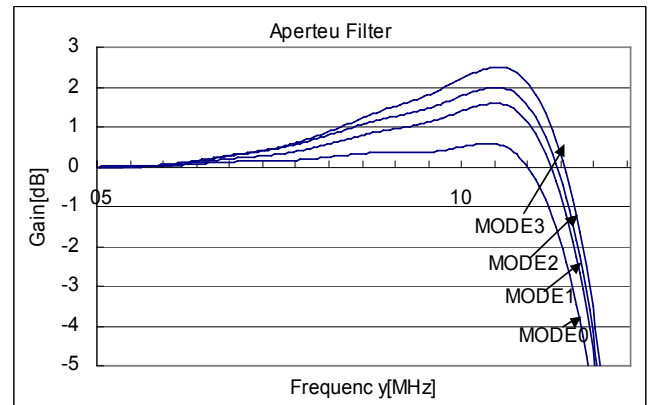


Fig. 41 Aperture Filter

x4 Over-sampling Filter for Cb/Cr

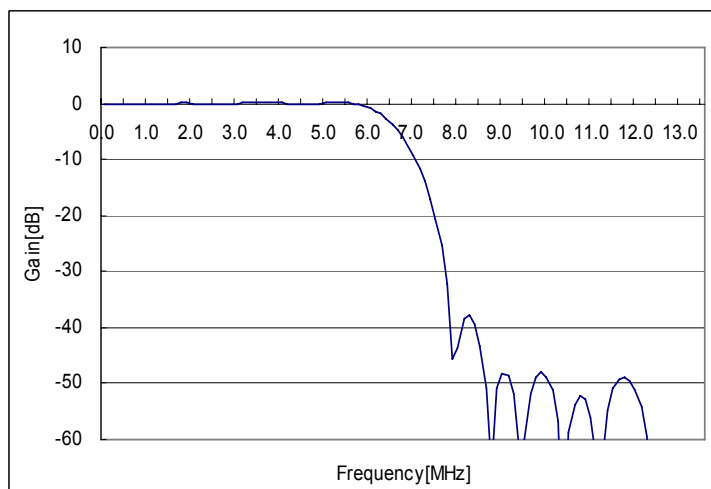


Fig. 43 x4 Over-sampling filter for 525p/625p

(3) Case of 1125i (1080i) 750P(720P) data input

Y/Cb/Cr data should be input with 16-bit width at 74.25MHz clock-rate.

x2 Over-sampling filter for Y-data and x4 Over-sampling filter for Cb/Cr data is equipped.

The block diagram is shown as follows,

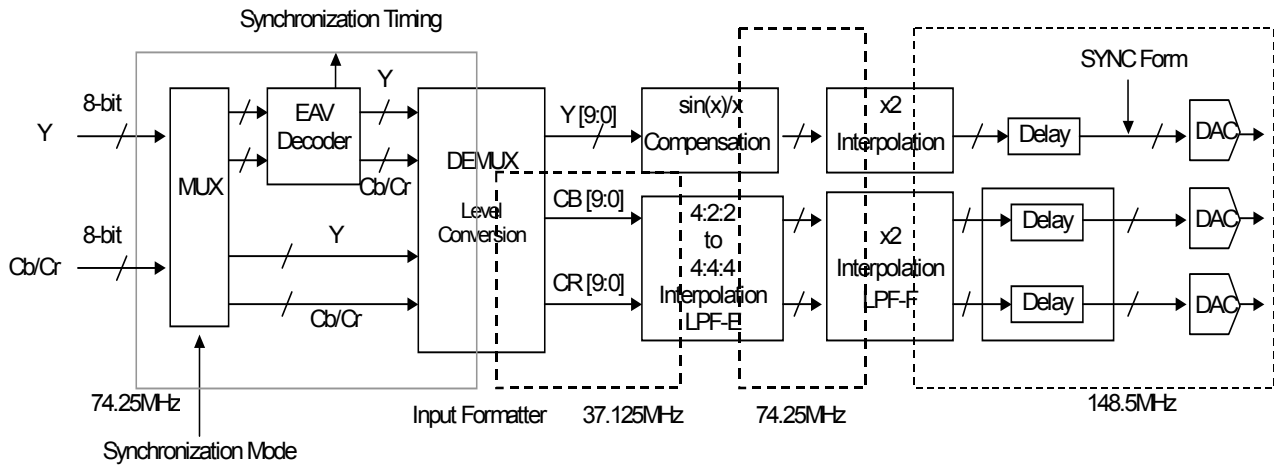


Fig. 44 1080i/720P mode Block Diagram

Over-sampling filter with aperture-effect compensation for Luminance (1080i/720P)

AK8826 equips the aperture-effect compensation filter for Luminance Signal.

This filter can be set with HDAFT [1:0]-bit of **HD Block Miscellaneous Control Register [Sub Address 0x0A]**. Compensation degree can be set with this register-bit. "Mode 0" is less compensation and "Mode 3" is more compensation.

HD Block Miscellaneous Control Register

Sub Address 0x0A

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	STD770_2C	HDCEA805B	CCWSSSUE	Reserved	HDAFLT1	HDAFLT0
Default Value							
0	0	0	0	0	0	0	0

HDAFLT[1:0]-bit	Filter Mode	Note
00	MODE0	
01	MODE1	
10	MODE2	
11	MODE3	

X2 Over-sampling Filter for Y-data

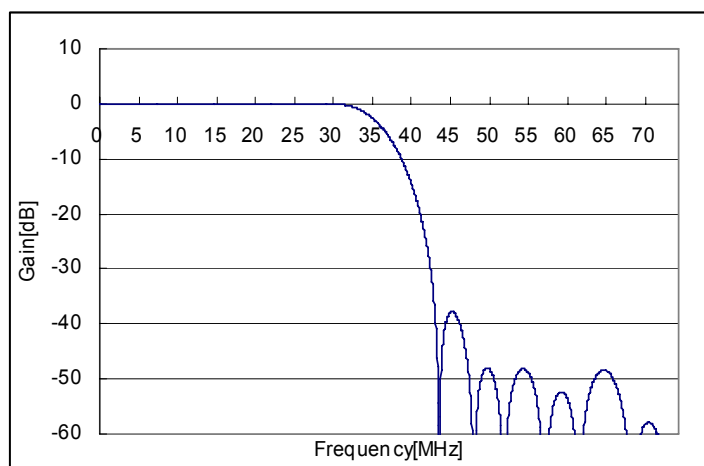


Fig. 46 x2 Over-sampling filter for 1080i/720p

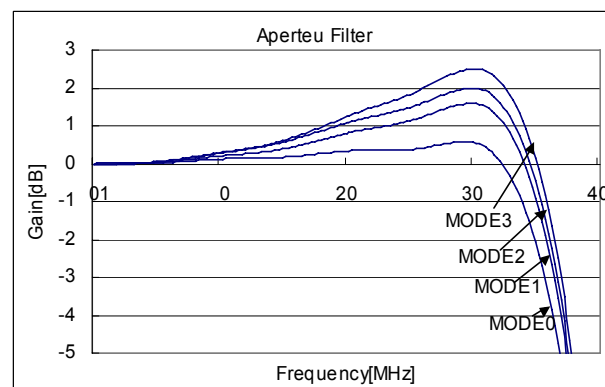


Fig. 45 Aperture Filter

x4 Over-sampling Filter for Cb/Cr

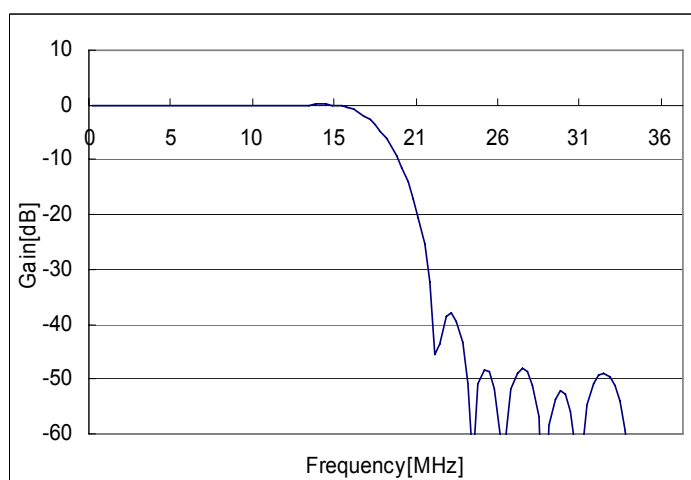


Fig. 47 x4 Over-sampling filter for 1080i/720p

■ Luminance, Chrominance Band-Width Limitation Filter

AK8826 equips Band-Width Limit Filter for Luminance and Chrominance.

For Luminance, Filter is set by HDYFLT[1:0]-bit of **HD Block Control Register (R/W) [SubAddress 0x07]**.

For Chrominance, Filter is set by HDCFLT[1:0]-bit of **HD Block Control Register (R/W) [Sub Address 0x07]**.

HD Block Control Register

Sub Address 0x07

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDWSS	HDCFLT1	HDCFLT0	HDYFLT1	HDYFLT0	Reserved	COLSNCEN	HDVRATIO

HDYFLT[1:0]	Filter	Note
00	Normal	Default (no limit)
01	Mid	YFLT1 on Next Page
10	Soft	YFLT2 on Next Page
11	Reserve	

HDCFLT[1:0]	Filter	Note
00	Normal	Default (no limit)
01	Mid	CFLT1 on Next Page
10	Soft	CFLT2 on Next Page
11	Reserve	

Frequency response of Band-Width Limitation Filter

The default frequency response (HDYFLT [1:0]= 00 / HDCFLT[1:0]=00) is shown in the previous section.

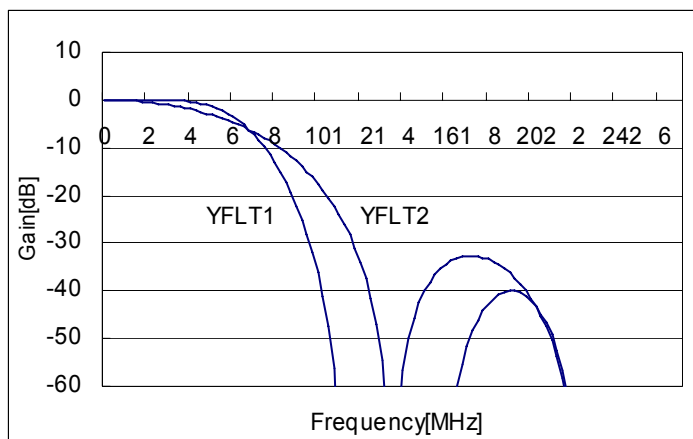


Fig. 49 525i / 625i Luminance Band-Width Limitation Filter

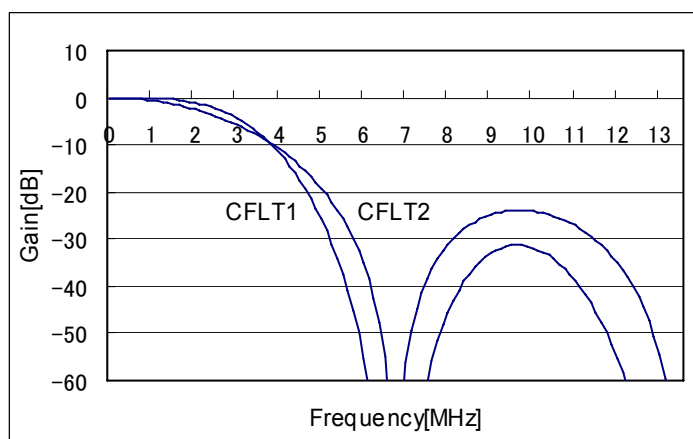


Fig. 48 525i / 625i Chrominance Band-Width Limitation Filter

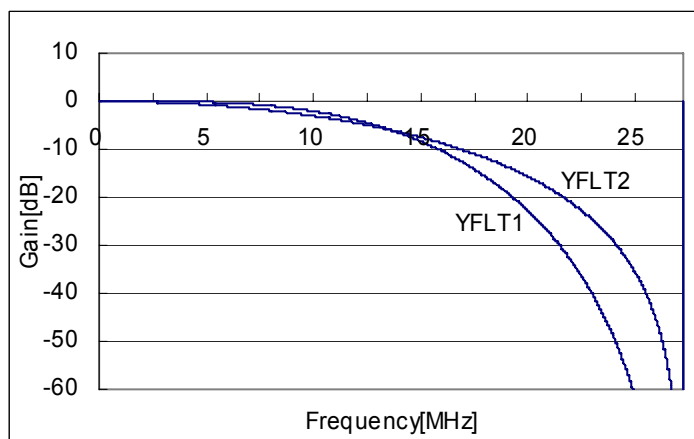


Fig. 50 525P / 625P Luminance Band-Width Limitation Filter

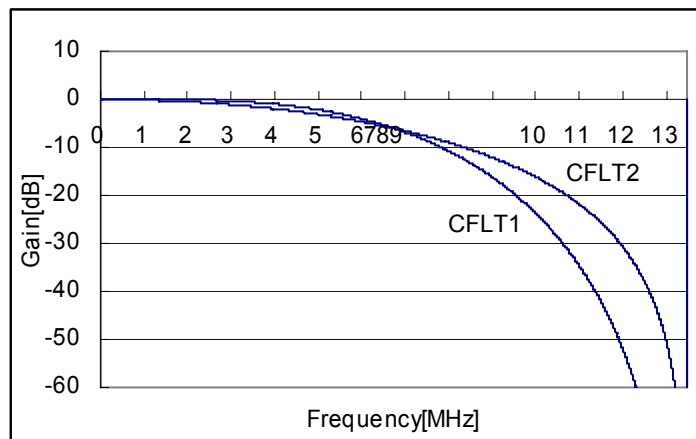


Fig. 51 525P / 625P Chrominance Band-Width Limitation Filter

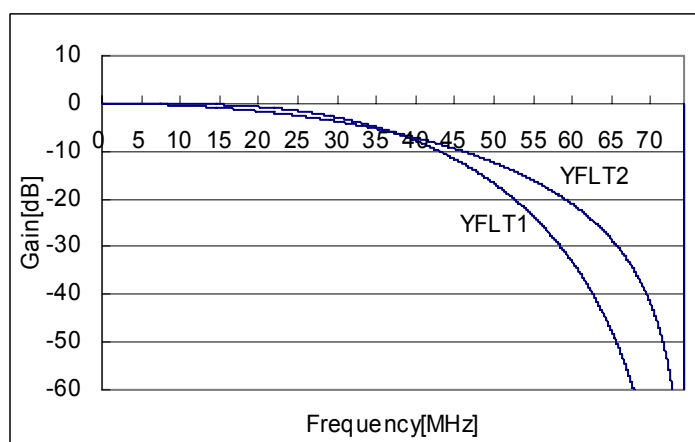


Fig. 53 1080i/720P Luminance Band-Width Limitation Filter

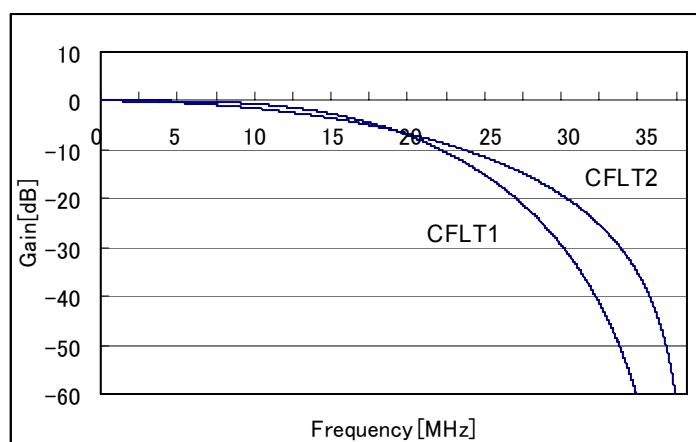


Fig. 52 1080i/720P Chrominance Band-Width Limitation Filter

■ Video Interface Timing

AK8826 has 2 types of Video Interface, EAV Decode mode and Slave SYNC mode.

Interface Mode is set by the HDEAVDEC-bit of **HD Mode Register [Sub Address 0x00]**.

HD Mode Register

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG	HDBBG	HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH

HDEAVDEC-bit	Interface mode	Note
0	HD/VD Slave mode	
1	EAV Decode mode	Set HDCEA861-bit = 0

(1) EAV Decode mode

(1-1) EAV Decode

EAV code which is encoded on input data stream is decoded, and the device makes synchronization with its timing. At the time of 16-bit width data input case, synchronization is made with EAV of the Y7-Y0 data, and it is not reference to the EAV/SAV which are contained in CbCr7-0 data.

In case of RGB data input mode, AK8826 doesn't support this interface mode.

EAV/SAV Code

Those codes succeeding 0xFF - 0x00 - 0x00 which are fed as input data become EAV/SAV codes.

EAV/SAV codes have following meanings, started with MSB.

Bit Number		MSB								LSB
WORD	VALUE	7	6	5	4	3	2	1	0	
0	0xFF	1 1		1 1		1 1 1				1
1	0x00	0 0		0 0		0 0 0				0
2	0x00	0 0		0 0		0 0 0				0
3	0xxx 1		F	V	H	P3 P	2 P	1		P0

F = 0 : Field 1

= 1 : Field 2

(F-bit is always 0 in case of Progressive data)

V = 0 : Field Blanking (V-Blanking) 以外

= 1: Field Blanking (V-Blanking)

H = 0: SAV

= 1: EAV

P3, P2, P1, P0: Protection Bit

Following is a relation between Protection bit and F/V/H-bit.

F	V	H	P3	P2	P1	P0
0 0 0 0 0					0	0
0 0 1 1 1					0	1
0 1 0 1 0					1	1
0 1 1 0 1					1	0
1 0 0 0 1					1	1
1 0 1 1 0					1	0
1 1 0 1 1					0	0
1 1 1 0 0					0	1

Reference standards

Input Data	Reference
525i	ITU-R.BT656
625i	ITU-R.BT656
525p	SMPTE 293M
625p	ITU-R. BT1358
1080i	SMPTE 274M
720p	SMPTE 296M

(1-2) Synchronization for Horizontal direction (EAV-Sync mode)

AK8826 synchronizes with input data horizontally using EAV code
EAV code and horizontal position is shown as following table.

525i (480i) case

Cb	Y	Cr	Y	Cb	Y	Cr	Y	...	Cb	Y	Cr	Y	Cb	Y	Cr	Y
359	718		359	719	360	720	360	721	428	856	428	857	0	0	0	1
EAV									SAV							

625i (576i) case

Cb	Y	Cr	Y	Cb	Y	Cr	Y	...	Cb	Y	Cr	Y	Cb	Y	Cr	Y
359	718		359	719	360	720	360	721	431	862	431	863	0	0	0	1
EAV									SAV							

525P (480P) case

Y	718	719	720	721	722		723	...	854	855	856	857	0	1	2	
TRS						EAV			SAV							

625P (576P) case

Y	718	719	720	721	722		723	...	860	861	862	863	0	1	2	
TRS						EAV			SAV							

1125i (1080i) / 60Hz case

Y	1918	1919	1920	1921	1922		1923	...	2196	2197	2198	2199	0	1		2
TRS						EAV			SAV							

1125i (1080i) / 50Hz case

Y	1918	1919	1920	1921	1922		1923	...	2636	2637	2638	2639	0	1		2
TRS						EAV			SAV							

750P (720P) / 60Hz case

Y	1278	1279	1280	1281	1282		1283	...	1646	1647	1648	1649	0	1	2	
TRS						EAV			SAV							

750P (720P) / 50Hz case

Y	1278	1279	1280	1281	1282		1283	...	1976	1977	1978	1979	0	1	2	
TRS						EAV			SAV							

(1-3) Synchronization for Vertical direction (EAV-Sync mode)

The AK8826 makes Vertical Synchronization (Line Synchronization) with either F-bit or V-bit of EAV.

Interlaced signal: using F-bit

Progressive signal: using V-bit

(1-2-1) F-bit

Relation between F-bit and Line-Number

F-bit	525i	625i	525P/625P	1080i	720P
0	Line4 - Line265	Line1 - Line312	All Lines F = 0	Line1 - Line563	All Lines F = 0
1	Line266 - Line525 Line1 - Line3	Line313 - Line625		Line564 - Line1125	

(1-2-2) V-bit

Relation between V-bit and Line-Number

- 525i (480i), 625i (576i), 1080i case

Field	V-bit	525i	625i	1080i (60/50Hz)
Field 1	Start (V=1)	Line1 - Line19	Line624 - Line22	Line1124 - Line1125 - Line20
	End (V=0)	Line20 - Line263	Line23 - Line310	Line21 - Line560
Field 2	Start (V=1)	Line264 - Line282	Line311 - Line335	Line561 - Line583
	End (V=0)	Line283 - Line525	Line336 - Line623	Line584 - Line1123

Note: AK8826 don't care V-bit in case of 525i / 625i / 1080i mode

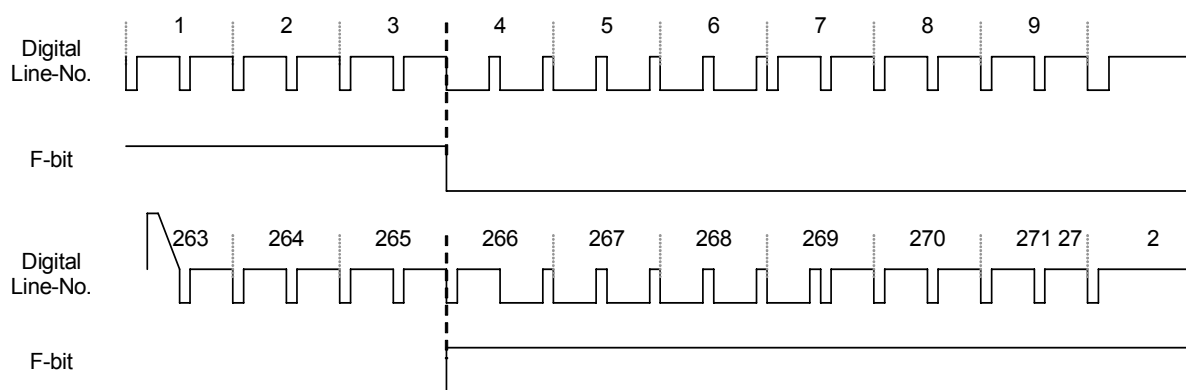
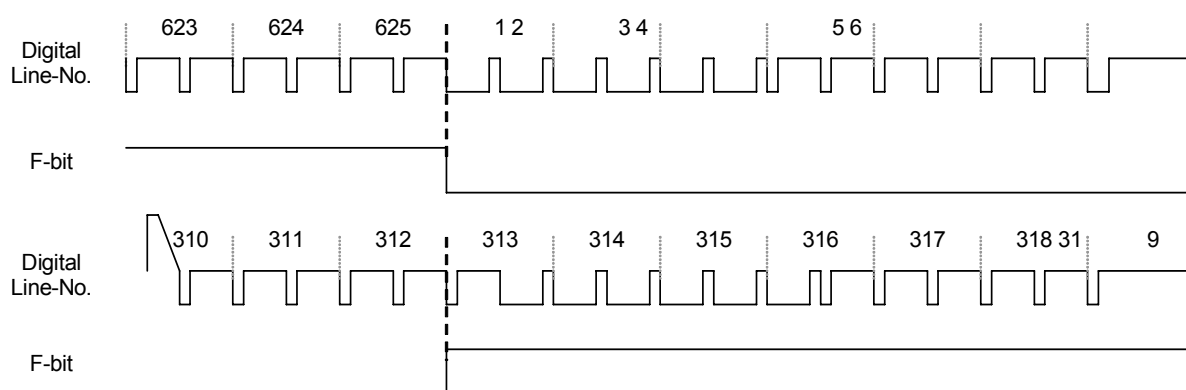
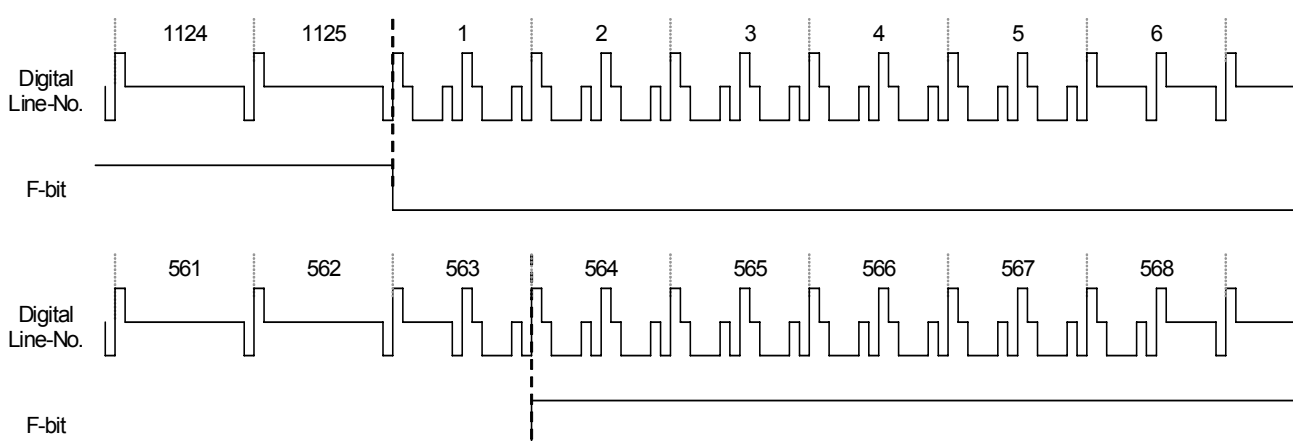
- 525P, 625P, 750P case

V-bit	525P	625P	720P
Start (V=1)	Line1 - Line42	Line621 - Line44	Line746 - Line750 - Line25
End (V=0)	Line43 - Line525	Line45 - Line625	Line26 - Line745

(1-4) Interlace data and Progressive data synchronization

(1-4-1) Interlace data (525i / 625i / 1080i)

When in the Interlaced input data cases (525i / 625i / 1080i), Line Synchronization with input data is made with F-bit of EAV.

**Fig. 54 525i mode****Fig. 55 625i mode****Fig. 56 1080i mode**

(1-3-2) Progressive Data (525p / 625p / 720p)

When in the Progressive data input cases, Line Synchronization with input data is made with V-bit of EAV.

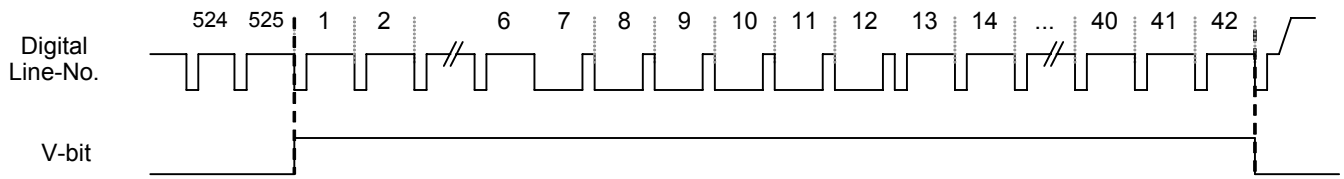


Fig. 57 525p case

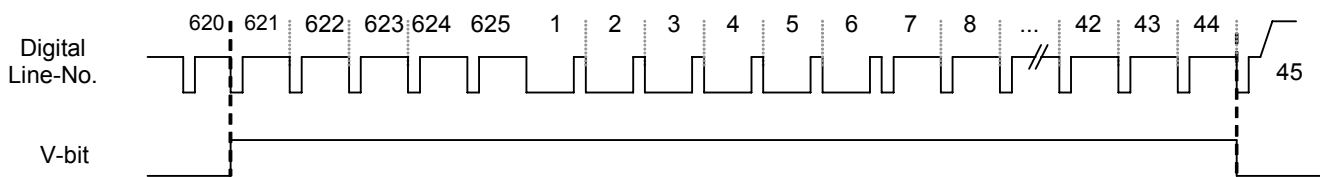


Fig. 58 625p case

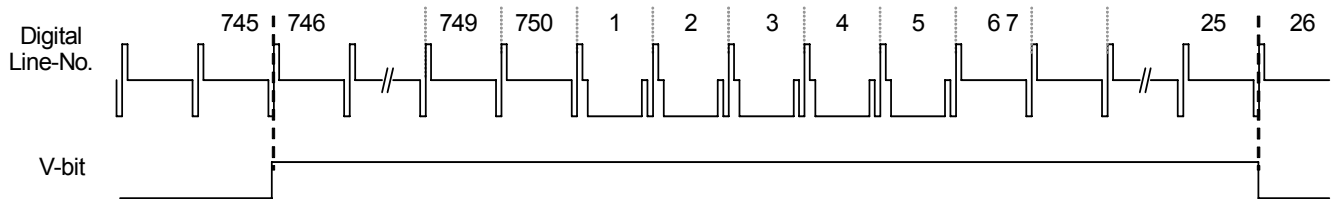


Fig. 59 720 case

(1-2) EAV/SAV and Data

(1-2-1) 525i (T: 13.5MHz)

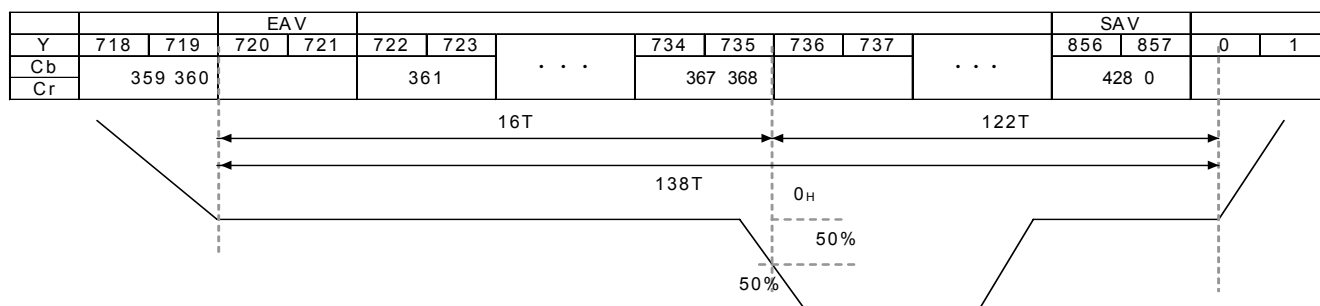


Fig. 60

Clock count between EAV to 0th data is 138T.

(1-2-2) 625i (T: 13.5MHz)

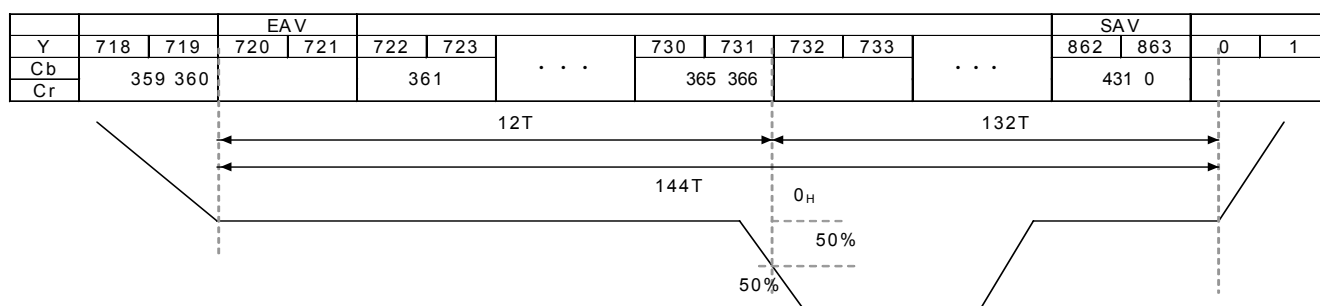


Fig. 61

Clock count between EAV to 0th data is 144T.

(1-2-3) 525P (T: 27MHz)

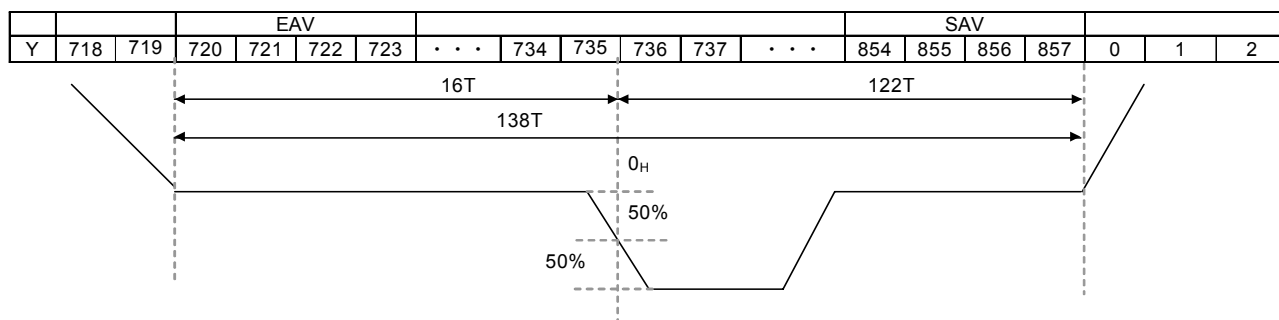


Fig. 62

Clock count between EAV to 0th data is 138T.

(1-2-4) 625P (T: 27MHz)

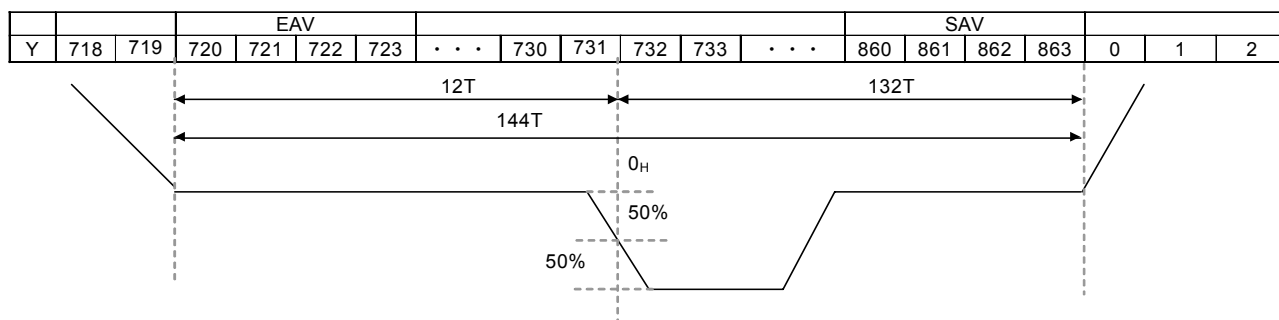


Fig. 63

Clock count between EAV to 0th data is 144T.

(1-2-5) 1080i / 60Hz (T: 74.25MHz)



Clock count between EAV to 0th data is 280T.

(1-2-6) 1080i / 50Hz (T: 74.25MHz)



Clock count between EAV to 0th data is 720T.

(1-2-7) 720P / 50Hz (T: 74.25MHz)

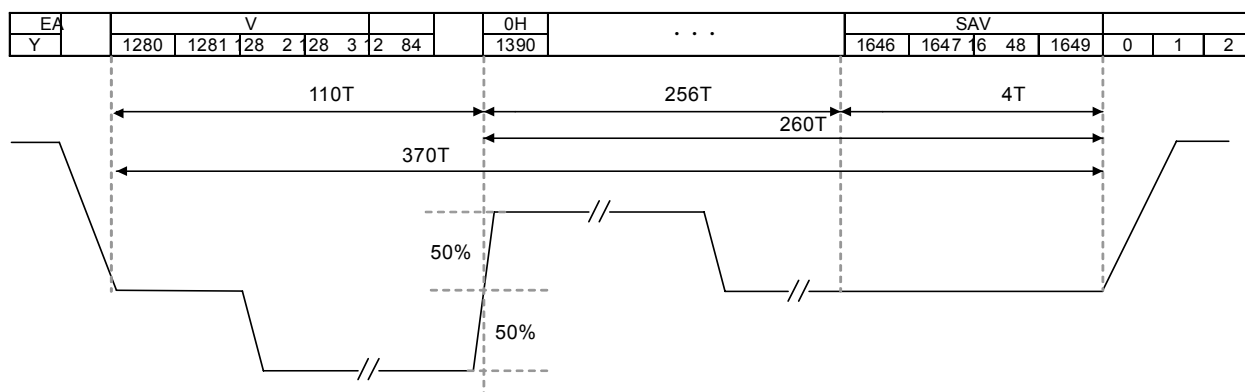


Fig. 66

Clock count between EAV to 0th data is 370T.

(1-2-8) 750P(720P) / 50Hz (T: 74.25MHz)

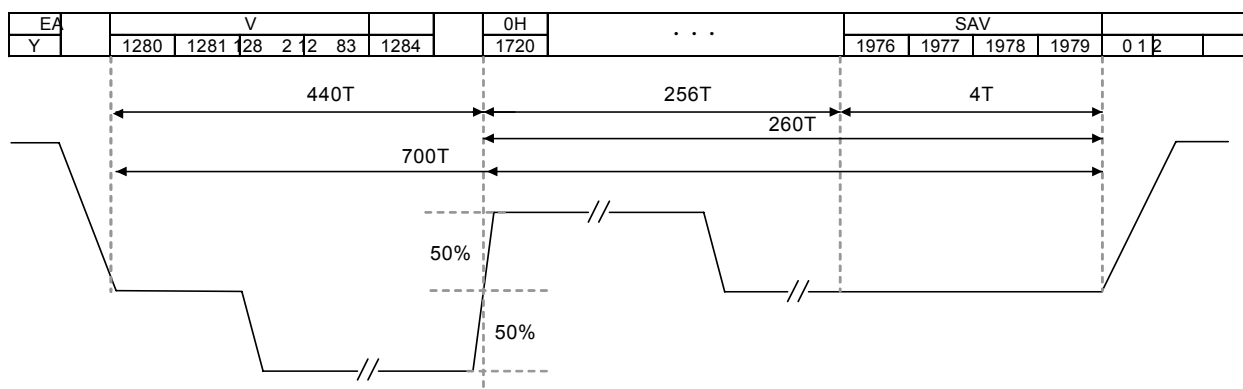


Fig. 67

Clock count between EAV to 0th data is 700T.

(1-3) Timing for Data Capture

(1-3-1) 525i / 625i 8-bit input mode

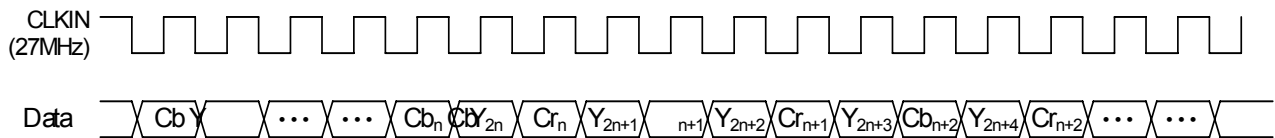


Fig. 68

Synchronization code is embedded as follows.

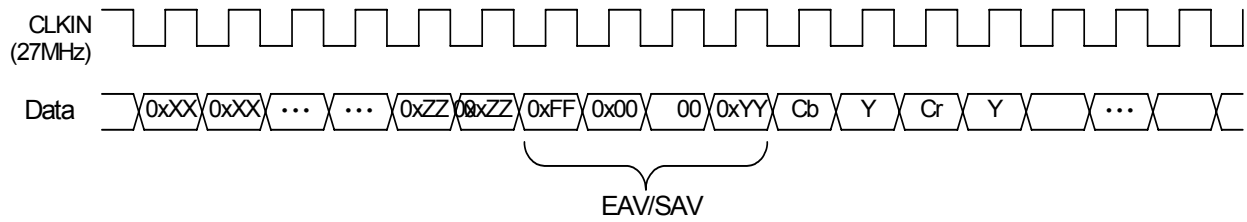


Fig. 69

(1-3-2) 525P / 625P / 1080i / 720P 16-bit data input mode

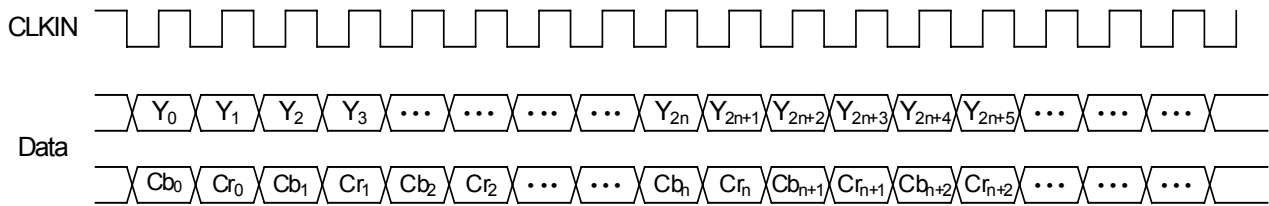


Fig. 70

Synchronization code is embedded in Ydata as follows.

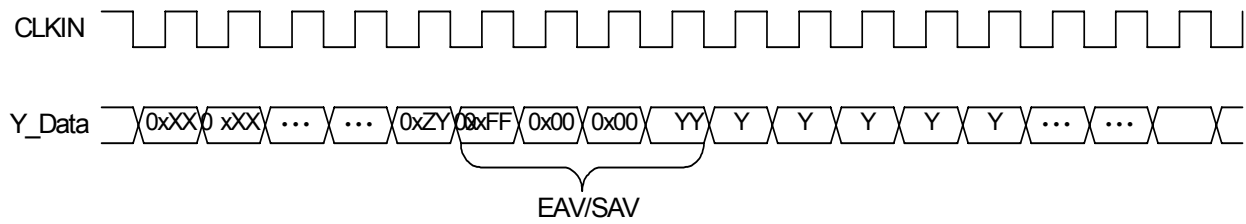


Fig. 71

(2) Slave Synchronization mode

AK8826 can make synchronization using HSYNC/VSNC timing.

The coming HSYNC is used for synchronization for horizontally, and VSYNC is used for Line-Sync.

The falling edge of the each timing signal is used for Synchronization.

Synchronization timing is AK8826 original timing and the timing defined in CEA861-D standard.

Timing is set by the register (HDCEA861-bit of **HD mode Register [Sub Address 0x00]**.

HD Mode Register

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG	HDBBG	HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH

HDCEA861-bit

HDCEA861D	Sync-timing	Note
0	AK8826 Sync timing	
1 CEA-861-D	Sync-timing	

The AK8826 recognizes 1st/2nd Field to watch the relation between HSYNC and VSYNC falling edge.

(2-1) 525i 8-bit x 1ch (Based on ITU-R .BT.601 standard)

(2-1-1) HDCEA861-bit = 0

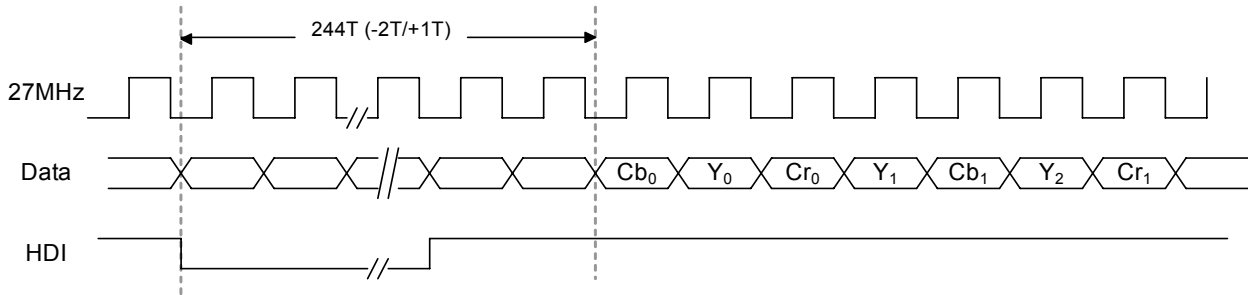


Fig. 72 525i HSYNC and data (8-bit x 1ch)

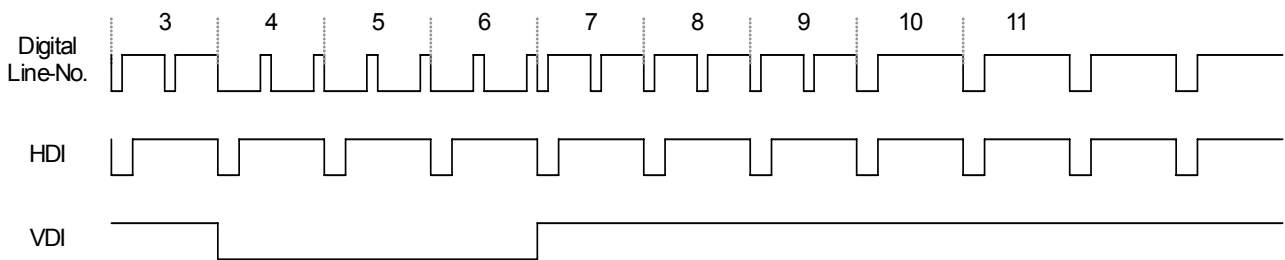


Fig. 73 525i Relation between HSYNC and VSYNC (1)

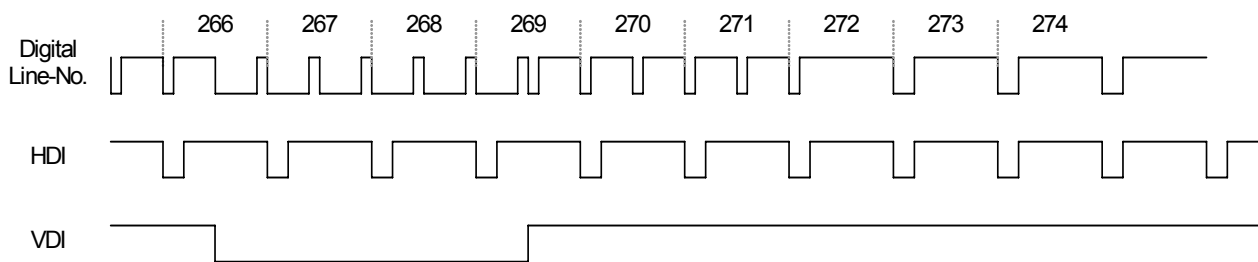


Fig. 74 525i Relation between HSYNC and VSYNC (2)

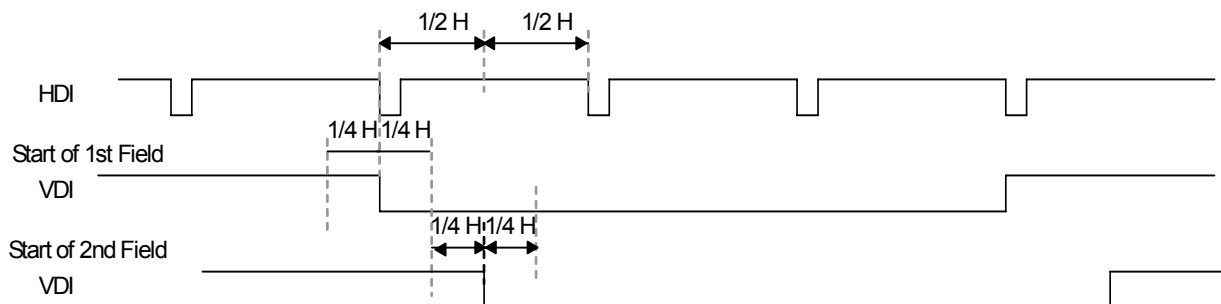


Fig. 75 Recognition of Field

**CEA 861-D : 525i(480i) / 60Hz (HDT V)
720(1440)x480i@59.94/60Hz(Formats 6 & 7)**

HDI, VDI Input Timing

Timing diagram for HDI data transfer:

- Total Horizontal Clocks per line: 1716
- Data Enable period: 1440 Clocks for Active Video
- Outside of Data Enable period: Y: 10H, CbCr: 80H
- Intervals: 124, 114 clocks, 38, 38

Fig. 76

Timing diagram for the HDI interface. The diagram shows the relationship between Data Enable, HDI, and VDI signals over time. The HDI signal is a clock signal with a period of 1716 clocks. The Data Enable signal is active during the blanking lines. The VDI signal is shown as a horizontal line. The diagram is divided into two main sections: Field 1: 22 Vertical Blanking Lines and 240 Active Vertical Lines per field. The HDI signal is labeled with clock numbers 524, 525, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 21, 22, 261, 262, 263. The Data Enable signal is labeled with 38 and 238. The VDI signal is labeled with 524, 525, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 21, 22, 261, 262, 263.

Fig. 77

The diagram illustrates the timing of the HDI interface signals. It is divided into two main sections: "Field 2: 23 Vertical Blanking Lines" and "240 Active Vertical Lines per field".

The HDI signal is a clock signal with a period of 1716 clocks. The VDI signal is a data bus. The diagram shows the relationship between the HDI clock and the VDI data bus during the active lines and vertical blanking lines.

Key timing parameters shown in the diagram include:

- Field 2: 23 Vertical Blanking Lines**: The first section of the diagram.
- 240 Active Vertical Lines per field**: The second section of the diagram.
- 1716 clocks**: The period of the HDI clock signal.
- 38**: The number of clocks from the start of the HDI signal to the start of the first active line.
- 858**: The number of clocks between the start of the first active line and the start of the second active line.
- 238**: The number of clocks between the start of the second active line and the start of the third active line.
- 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273**: Clock numbers corresponding to the start of the first active line.
- 284, 285**: Clock numbers corresponding to the start of the second active line.
- 524, 525, 1**: Clock numbers corresponding to the start of the third active line.

Fig. 78

(2-2) 625i 8-bit x 1ch (Based on ITU-R .BT.601)

(2-2-1) HDCEA861-bit = 0

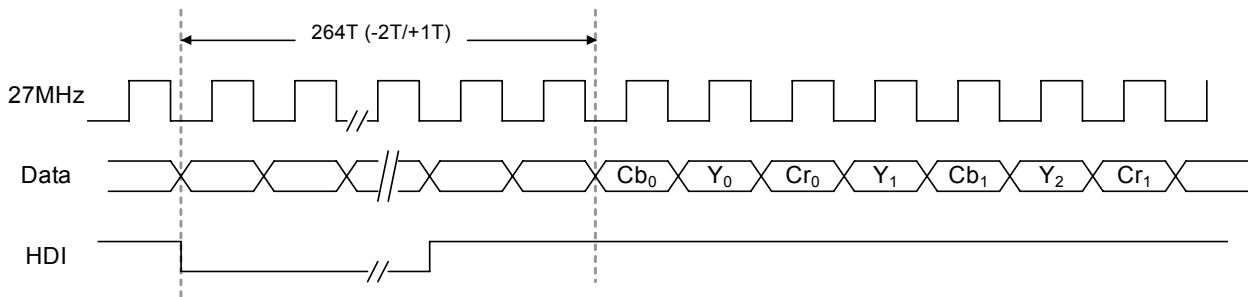


Fig. 79 625i HSYNC and data (8-bit x 1ch)

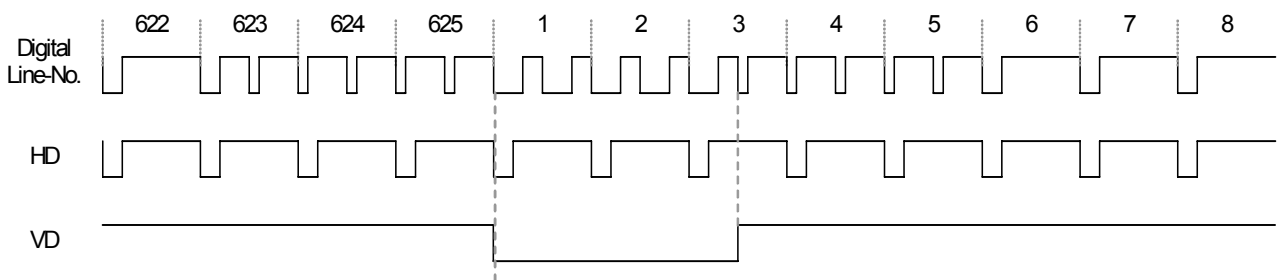


Fig. 80 625i Relation between HSYNC and VSYNC (1)

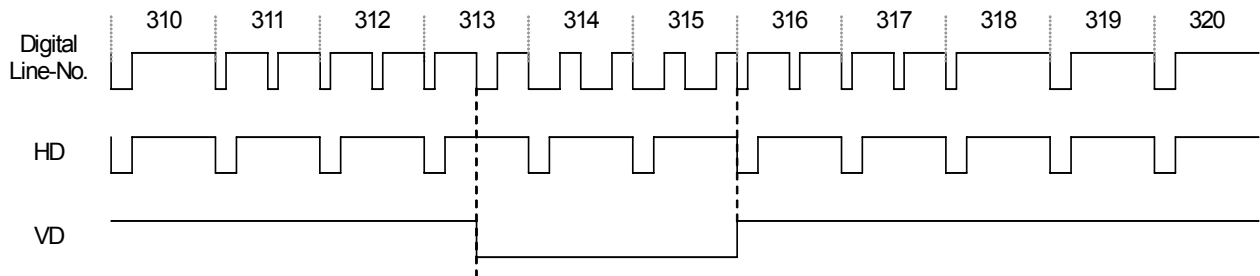


Fig. 81 625i Relation between HSYNC and VSYNC (2)

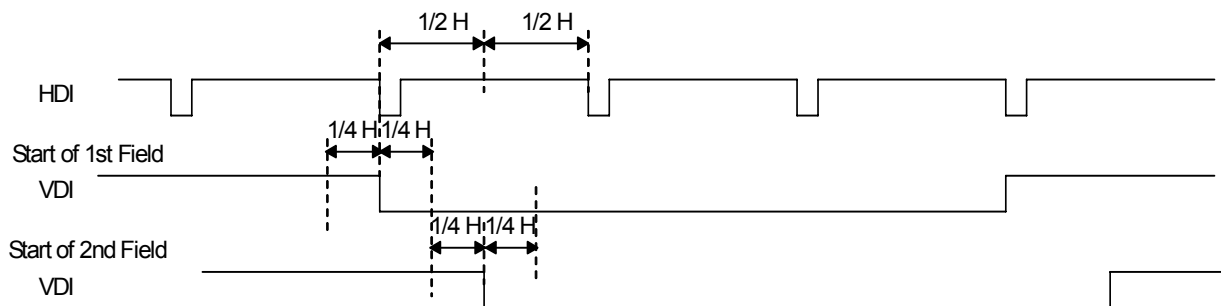


Fig. 82 Recognition of Field

(2-2-2) HDCEA861-bit = 1

CEA 861-D : 625i(576i) / 60Hz (HDT V)

720(1440)x576i@50Hz(Formats 21 & 22)

HDI and VDI timing

LINE

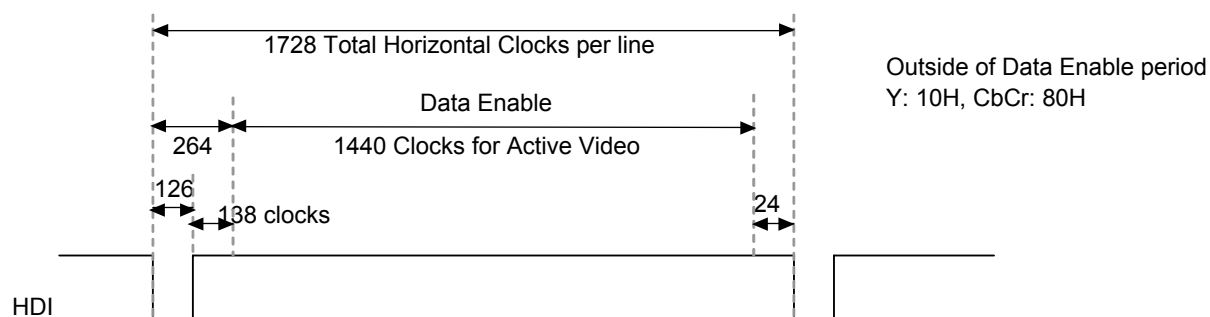


Fig. 83

Field 1

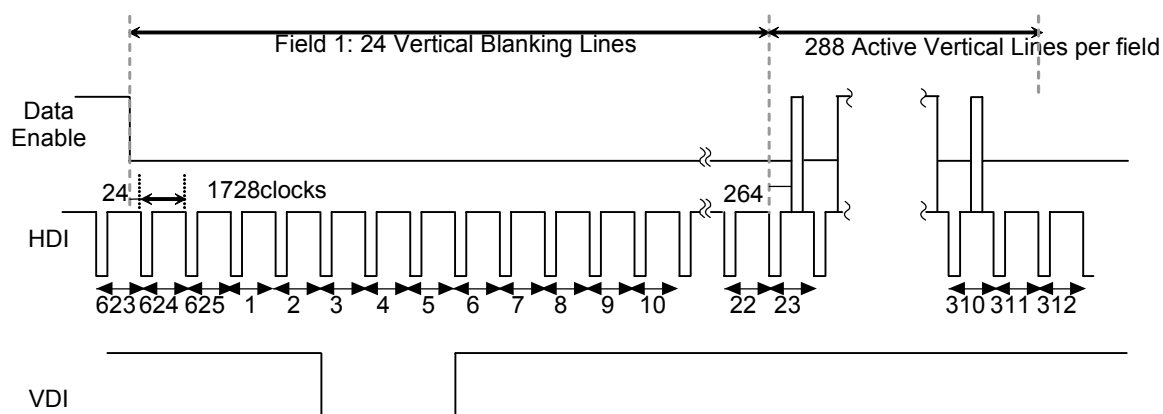


Fig. 84

Field 2

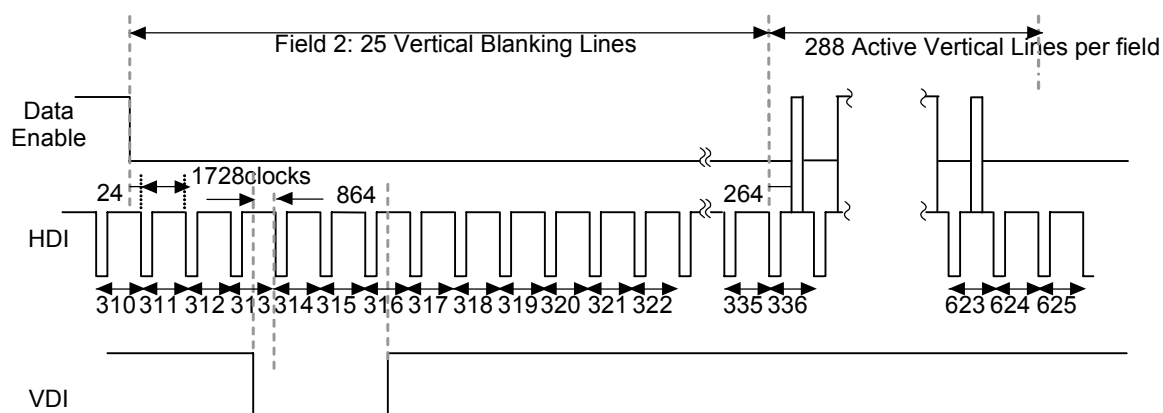


Fig. 85

(2-3) 525P 8-bit x 2ch (Based on SMPTE 293M)

(2-3-1) HDCEA861-bit = 0

HDI and VDI timing

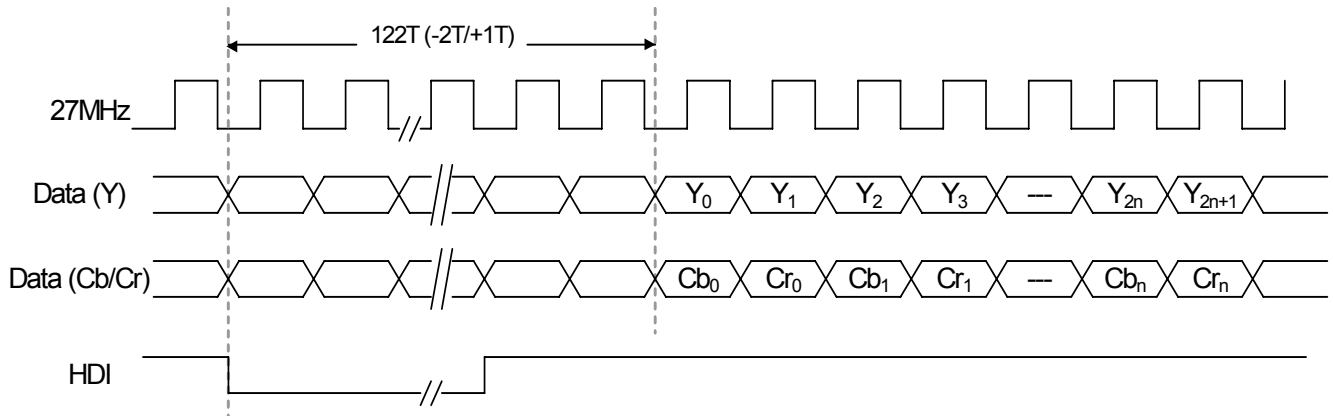


Fig. 86 525p HSYNC and data (8-bit x 2ch)

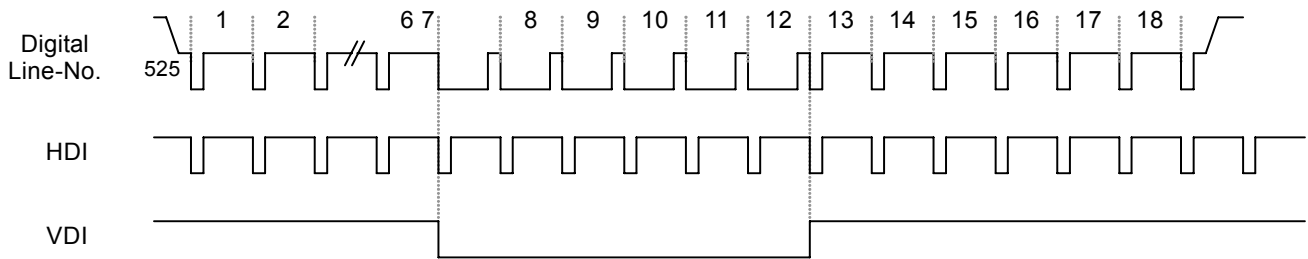


Fig. 87 525p Relation between HSYNC and VSYNC

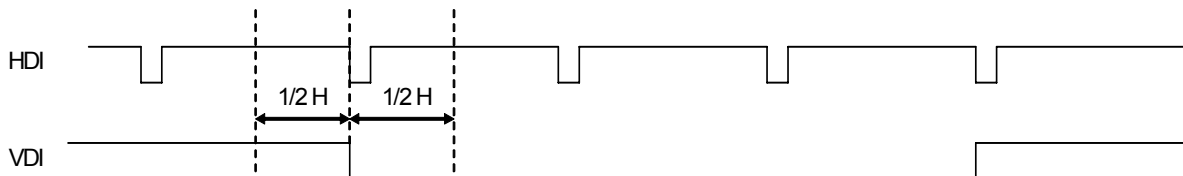


Fig. 88 Relation between HSYNC and VSYNC

(2-3-2) HDCEA861-bit = 1

CEA 861-D : 525p(480p) / 60Hz : HDTV
720x480p@59.94/60Hz(Formats 2 & 3)

HDI and VDI timing

LINE

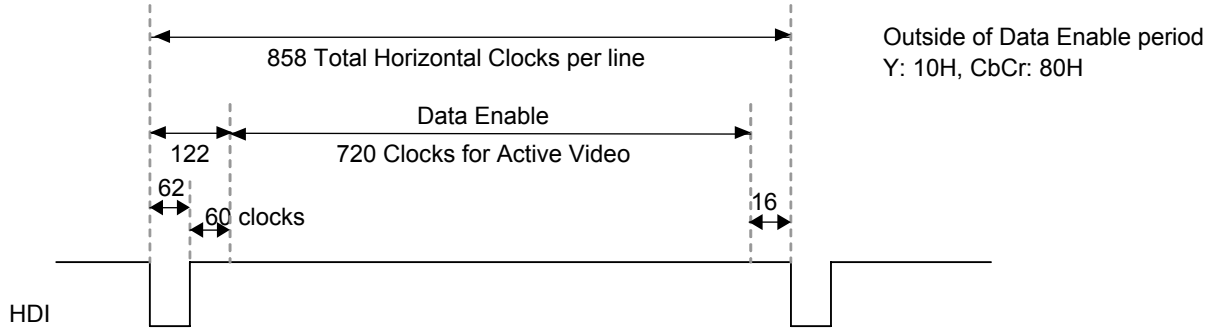


Fig. 89

Field

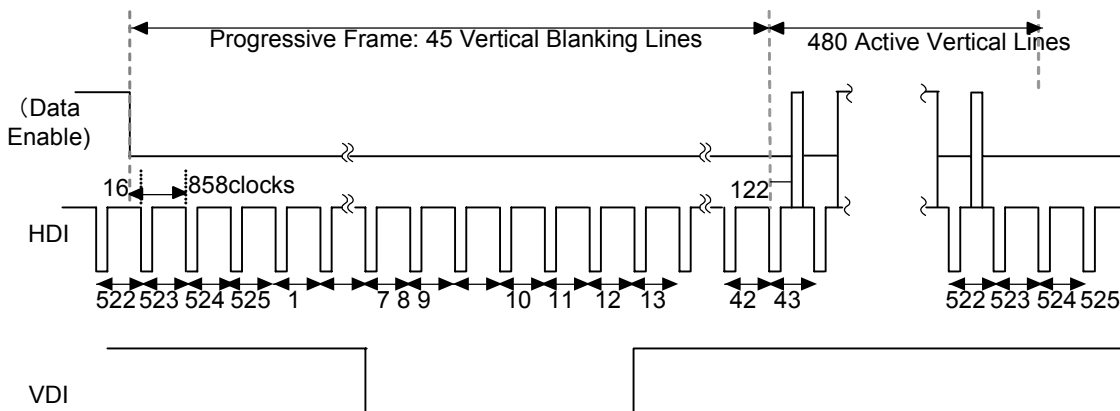


Fig. 90

(2-4) 625P 8-bit x 2ch

(2-4-1) HDCEA861-bit = 0
HDI and VDI timing

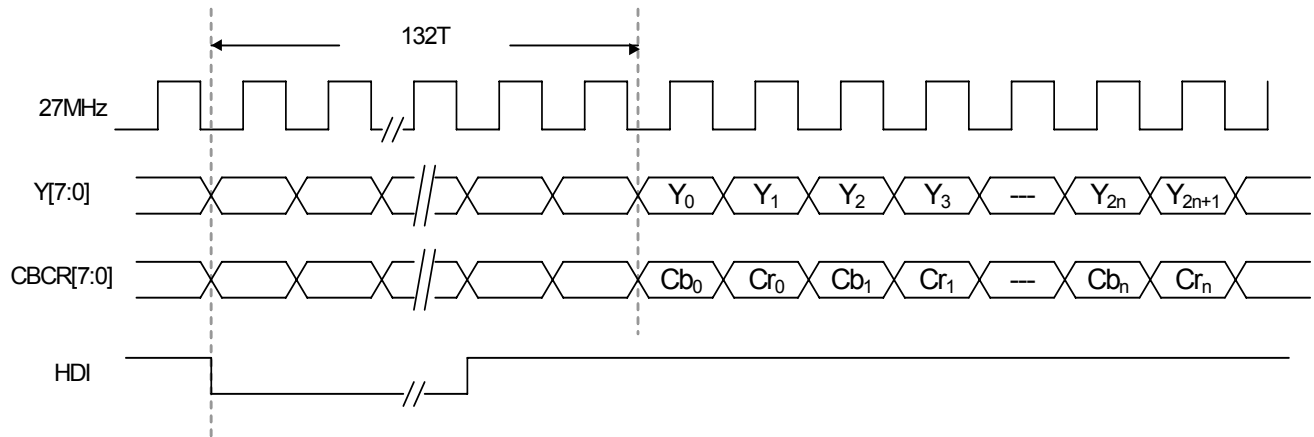


Fig. 91 625p HSYNC and data (8-bit x 2ch)

Clock count between falling edge of HDI to 0th data is 132T.

**CEA 861-D : 625p(576p) / 50Hz : HDTV
720(1440)x576p@50Hz(Formats 17 & 18)
HDI and VDI timing**

The diagram illustrates the timing of the HDI signal relative to horizontal clocks. A horizontal timeline is shown with vertical dashed lines marking key clock positions. The total horizontal clock period is 864 clocks. The data enable period is 720 clocks, starting 132 clocks after the beginning of the line and ending 12 clocks before the end of the line. The active video period is 68 clocks, starting 64 clocks after the beginning of the line and ending 12 clocks before the end of the line. The HDI signal is shown as a pulse that is active during the data enable period.

864 Total Horizontal Clocks per line

Outside of Data Enable period
Y: 10H, CbCr: 80H

Data Enable
720 Clocks for Active Video

132

64

68 clocks

12

HDI

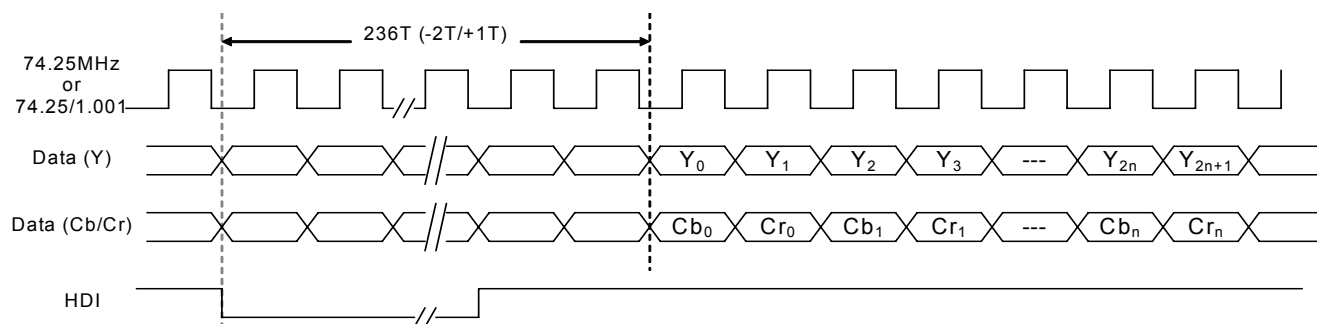
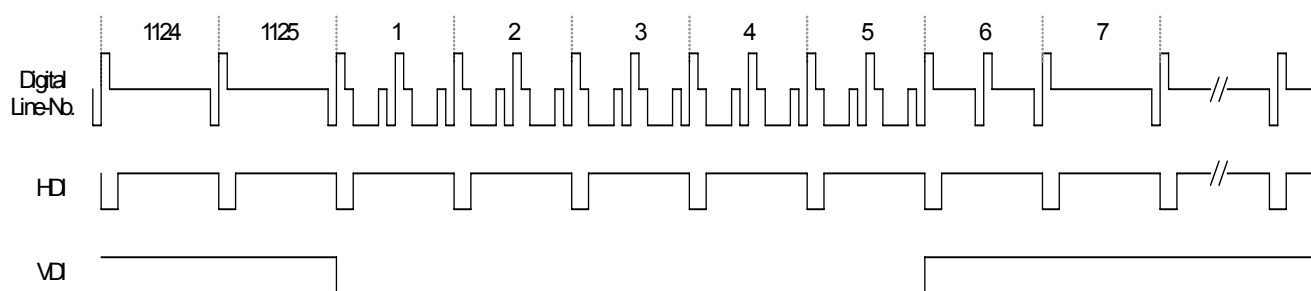
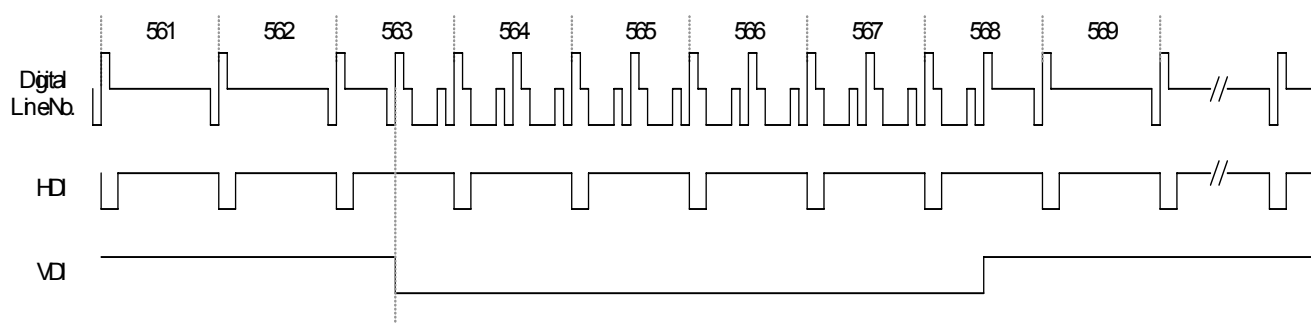
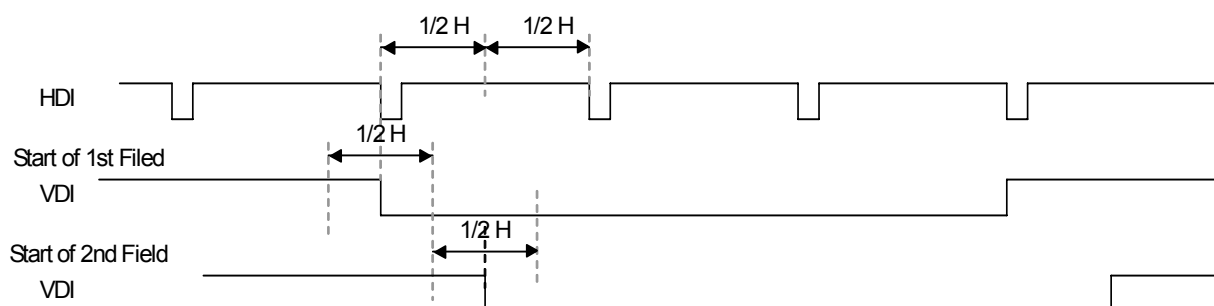
Fig. 92

Fig. 93

(2-5) 1080i / 60Hz (8-bit x 2ch)

(2-5-1) HDCEA861-bit = 0

HDI and VDi timing

**Fig. 94 1080i HSYNC and data (8-bit x 2ch)****Fig. 95 1080i Relation between HSYNC and VSYNC (1)****Fig. 96 1080i Relation between HSYNC and VSYNC (2)****Fig. 97 Recognition of Field**

(2-5-2) HDCEA861-bit = 1

CEA 861-D : 1080i / 60Hz : HDTV

1920x1080i@59.94/60Hz(Formats 5)

HDI and VDI timing

LINE

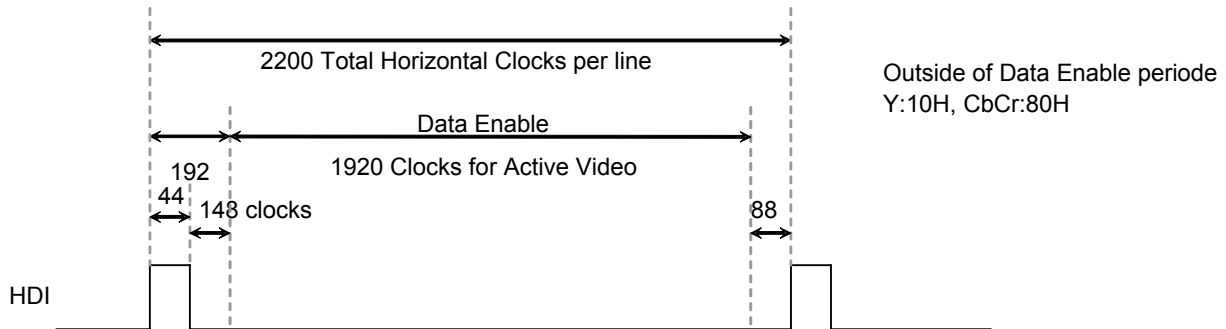


Fig. 98

Field 1

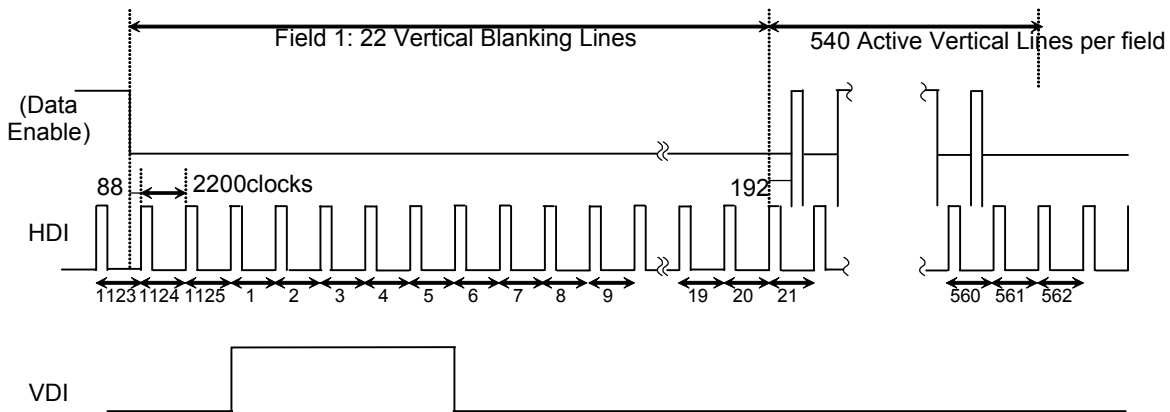


Fig. 99

Field 2

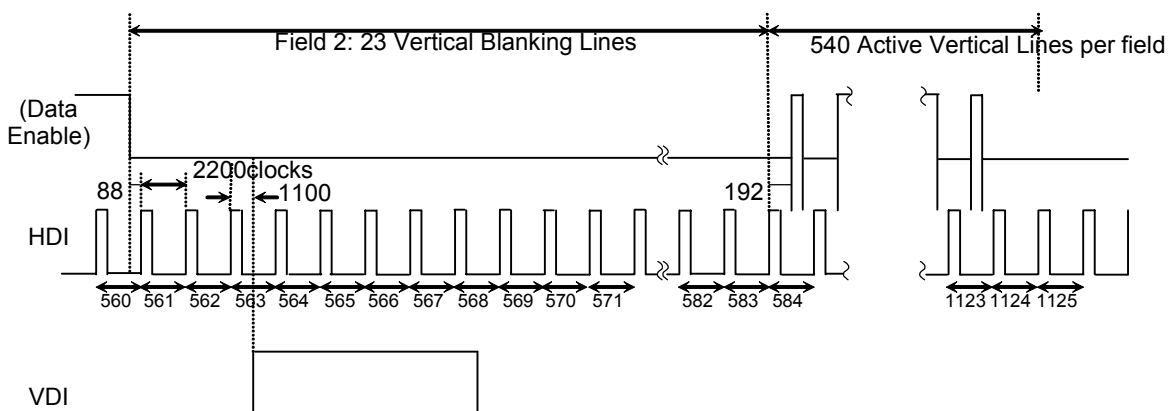
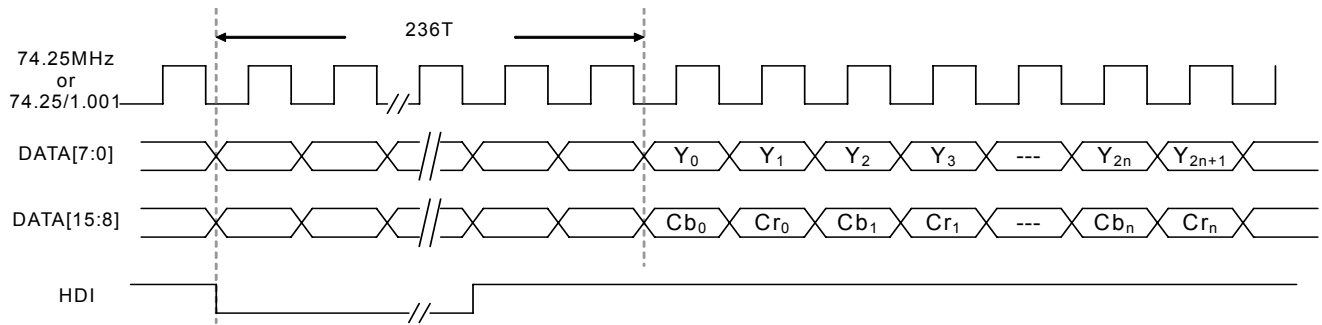
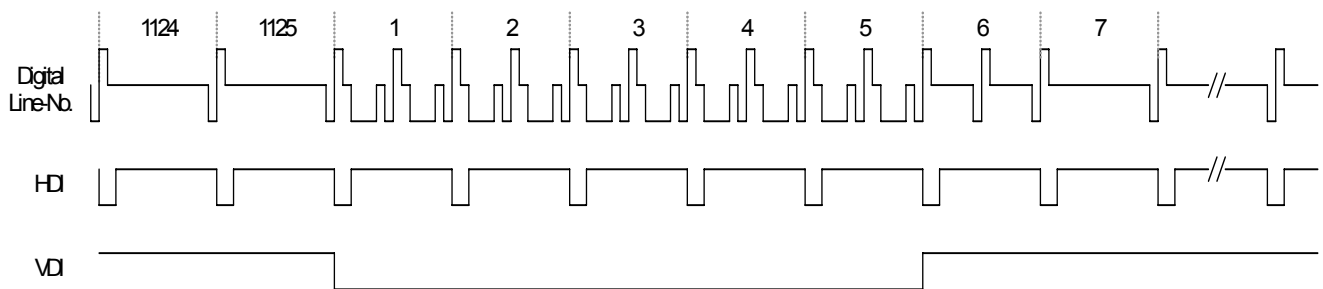
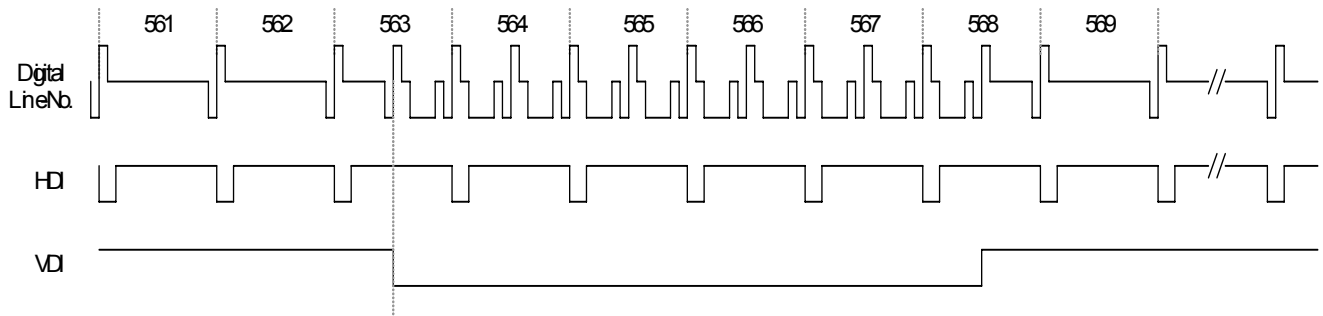
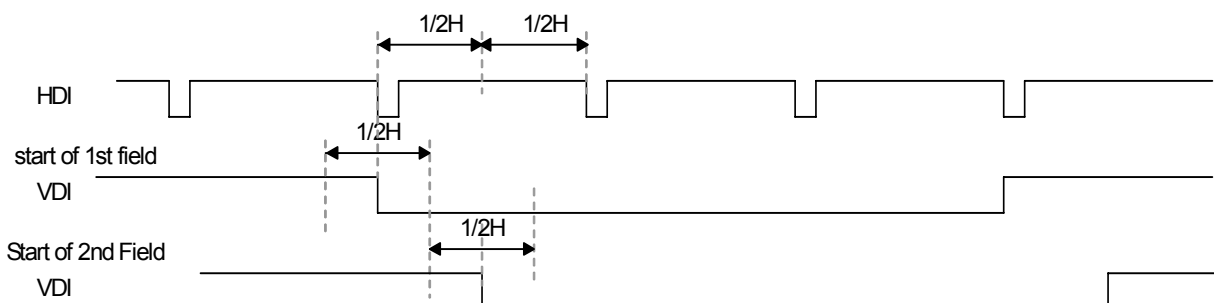


Fig. 100

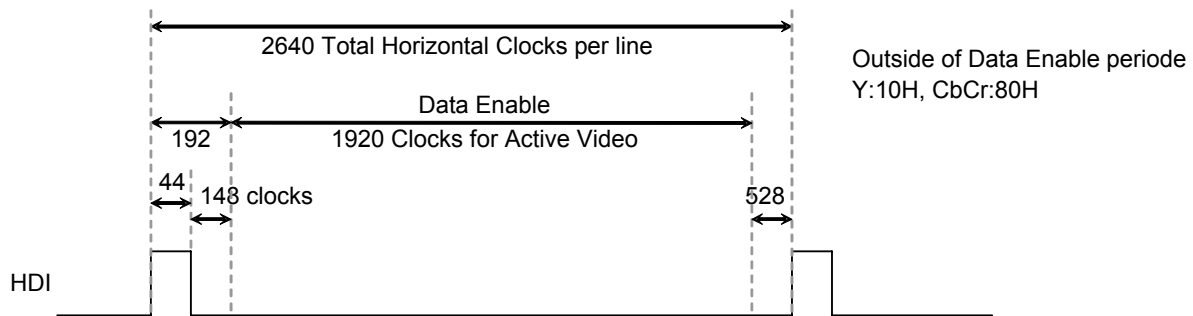
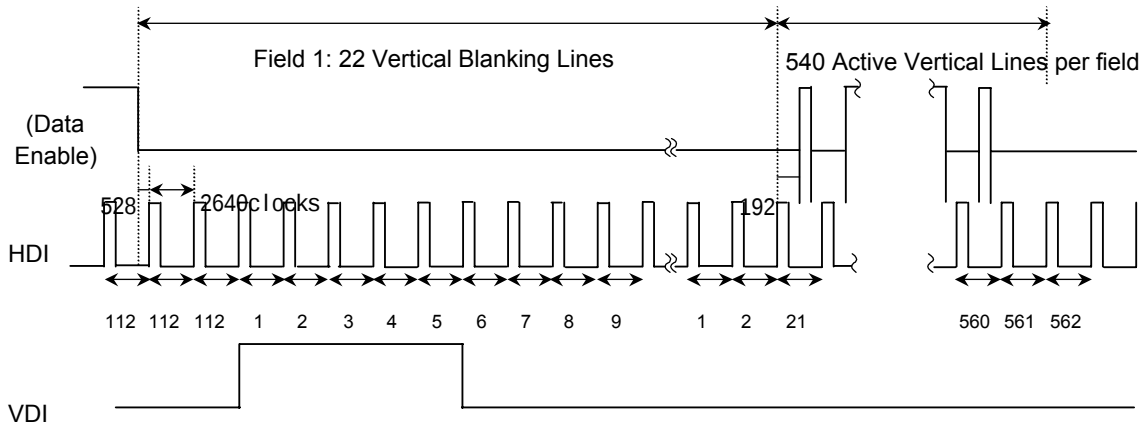
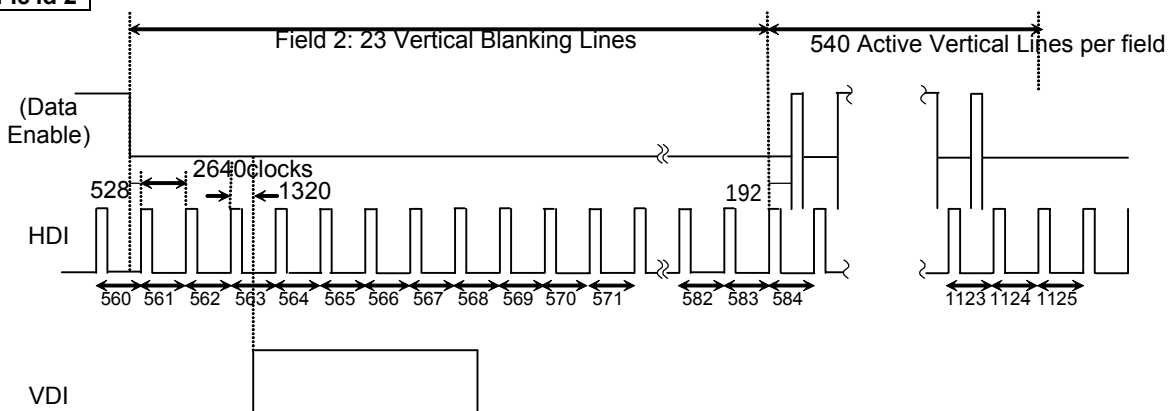
(2-6) 1080i / 50Hz (8-bit x 2ch)

(2-6-1) HDCEA861-bit = 0

HDI and VDI timing

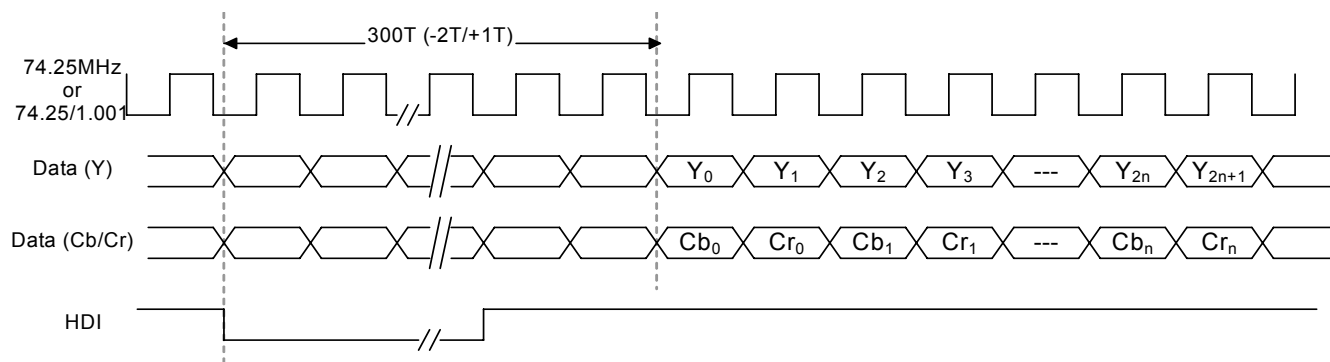
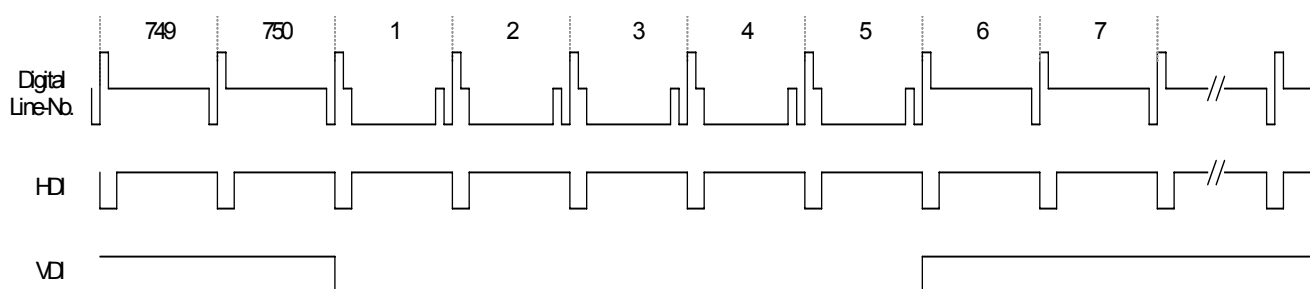
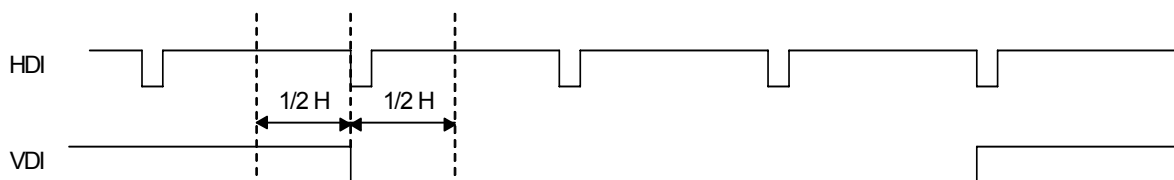
**Fig. 101 1125i(1080i) HSYNC and data (8-bit x 2ch)****Fig. 102 1125i (1080i) Relation between HSYNC and VSYNC(1)****Fig. 103 1125i (1080i) Relation between HSYNC and VSYNC(2)****Fig. 104 Field Recognition**

(2-6-2) HDCEA861-bit = 1

EIA/CEA 861-B : 1080i / 50Hz : HDTV**1920x1080i@50Hz(F or mats 20)****LINE****Fig. 105****Fie Id 1****Fig. 106****Fie Id 2****Fig. 107**

(2-7) 720P / 60Hz 8-bit x 2ch

(2-7-1) HDCEA861-bit = 0

**Fig. 108 720P HSYNC and Data (8-bit x 2ch)****Fig. 109 720P Relatio between HSYNC and VSYNC****Fig. 110 HSYNC and VSYNC**

(2-7-1) HDCEA861-bit = 1

CEA 861-B : 720p / 60Hz : HDTV
1280x720p@59.94/60Hz(Formats 4)

LINE

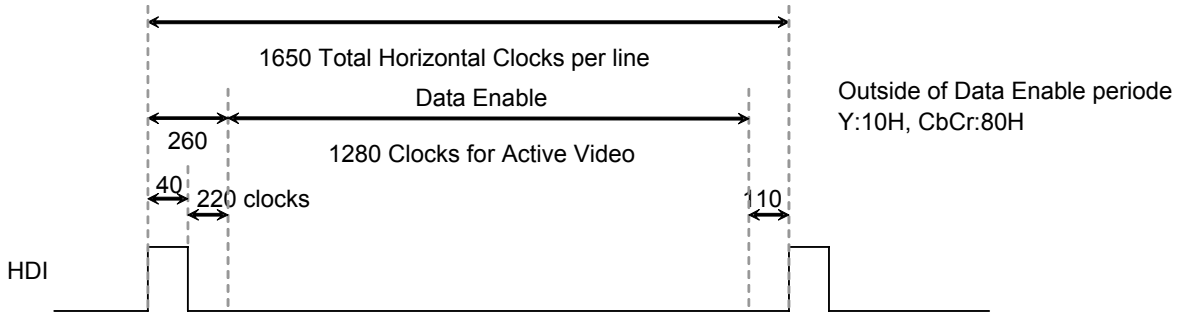


Fig. 111

File Id

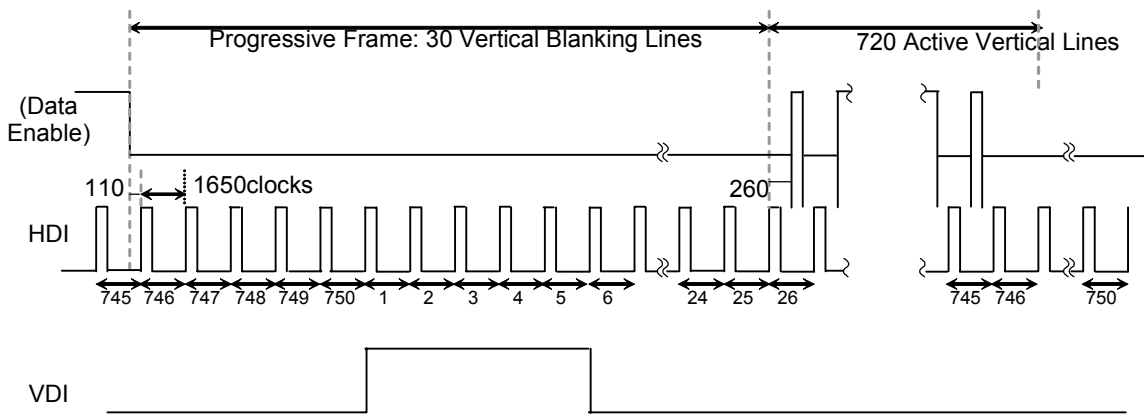


Fig. 112

(2-8) 720P / 50Hz 8-bit x 2ch

(2-8-1) HDCEA861-bit = 0

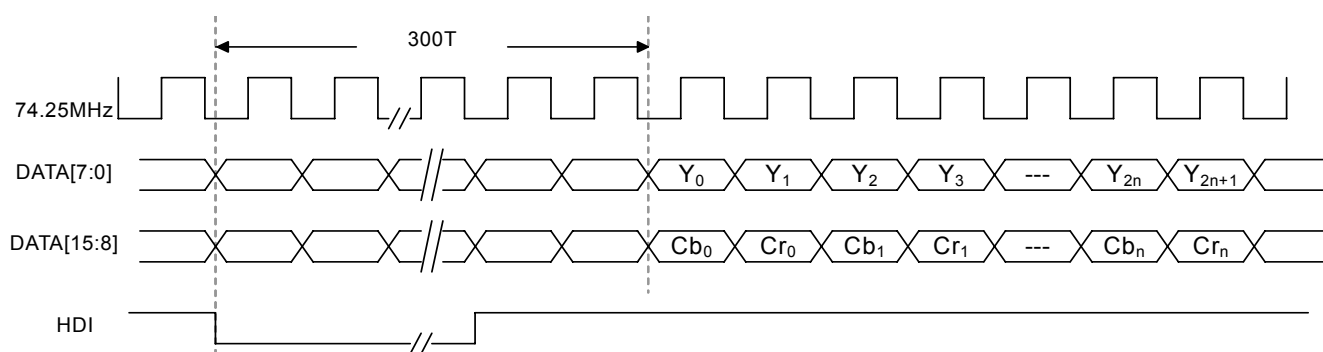


Fig. 113 720P HD and Data (8-bit x1ch)

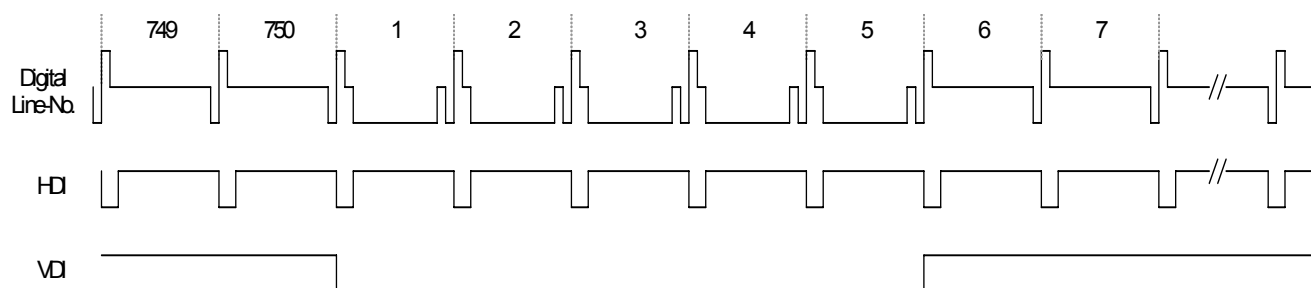


Fig. 114 720P Relation between HDI and VDI

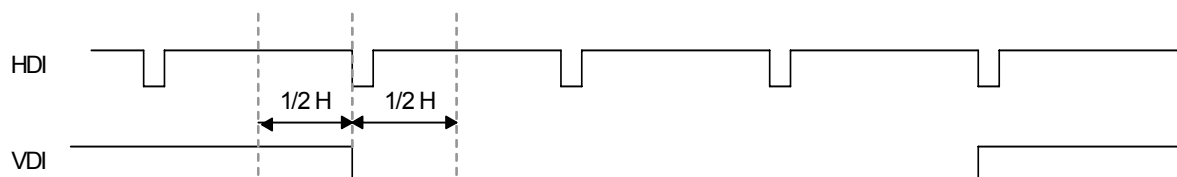
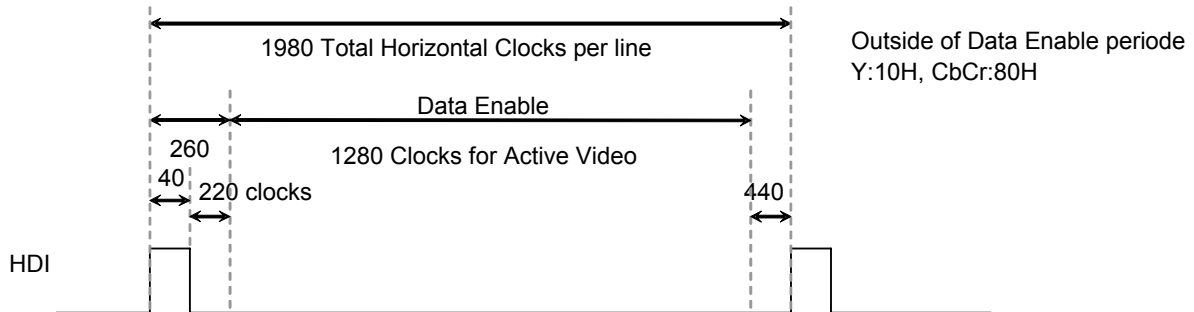
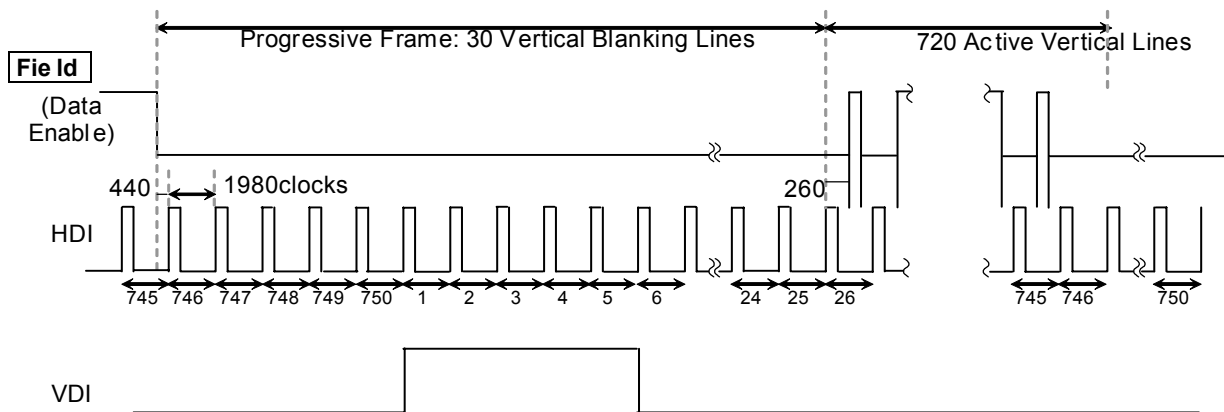


Fig. 115 HDI VDI Input Timing

(2-8-1) HDCEA861-bit = 1

CEA 861-B : 720p / 50Hz : HDTV**1280x720p@50Hz(Formats 19)****LINE****Fig. 116****Fig. 117**

■ Out put Synchronization waveform

AK8826 out put synchronization waveform on Ys signal at default, however, COLSNCEN-bit of **HD Block Control Register [SubAddress 0x27]** can add Synchronization waveform on not only Y-signal but also on Pb and Pr signal. The synchronization waveform on Pb and Pr is same as synchronization waveform on Y-signal.

HD Block Control Register

Sub Address 0x07

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDWSS	HDCFLT1	HDCFLT0	HDYFLT1	HDYFLT0	Reserved	COLSNCEN	HDVRATIO

COLSNCEN-bit	Function
0	Sync on Y-signal
1	Sync on Y, Pb, Pr signal

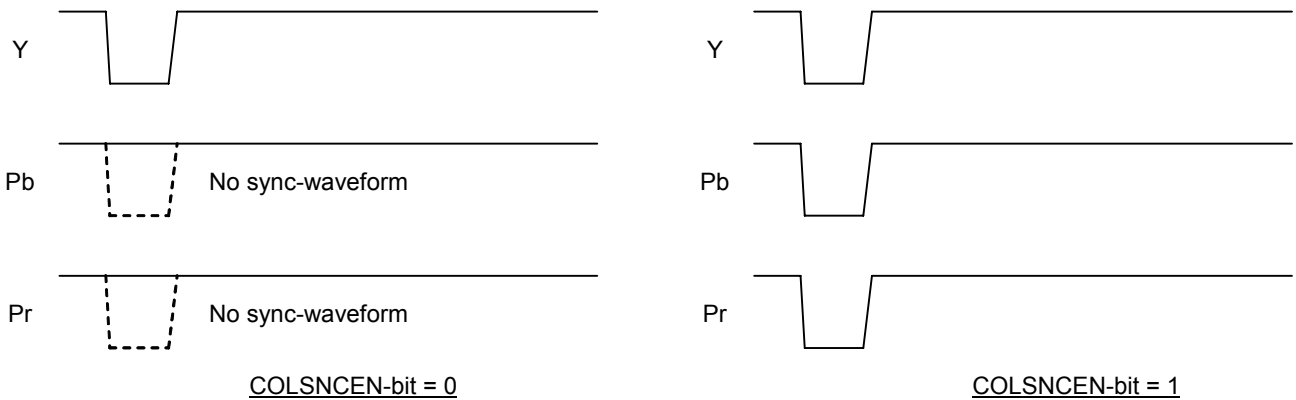


Fig. 118 525i / 625i / 525p / 625p case

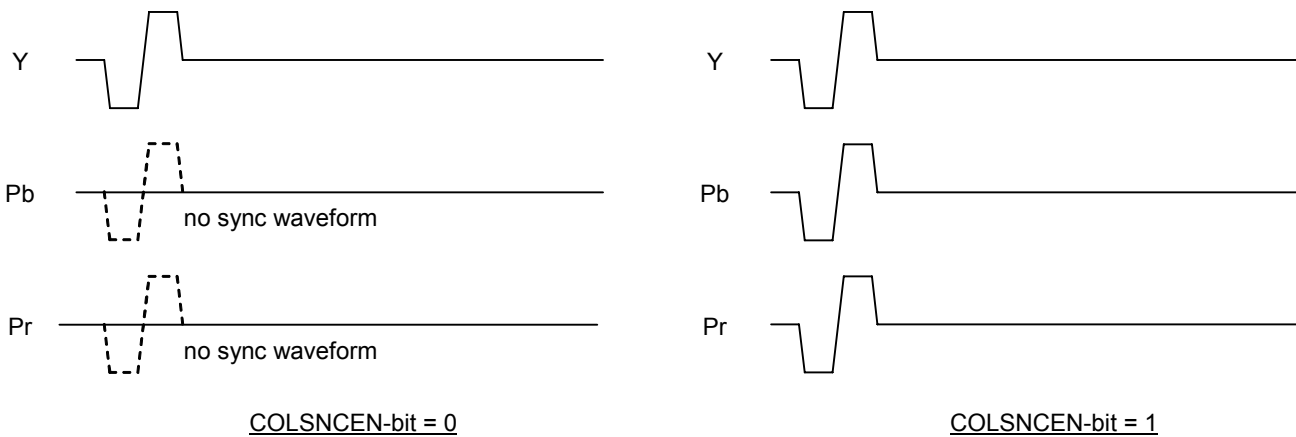


Fig. 119 1080i / 720p case

(1) 525i waveform (EIA-770.2-C)

[Sync waveform level]

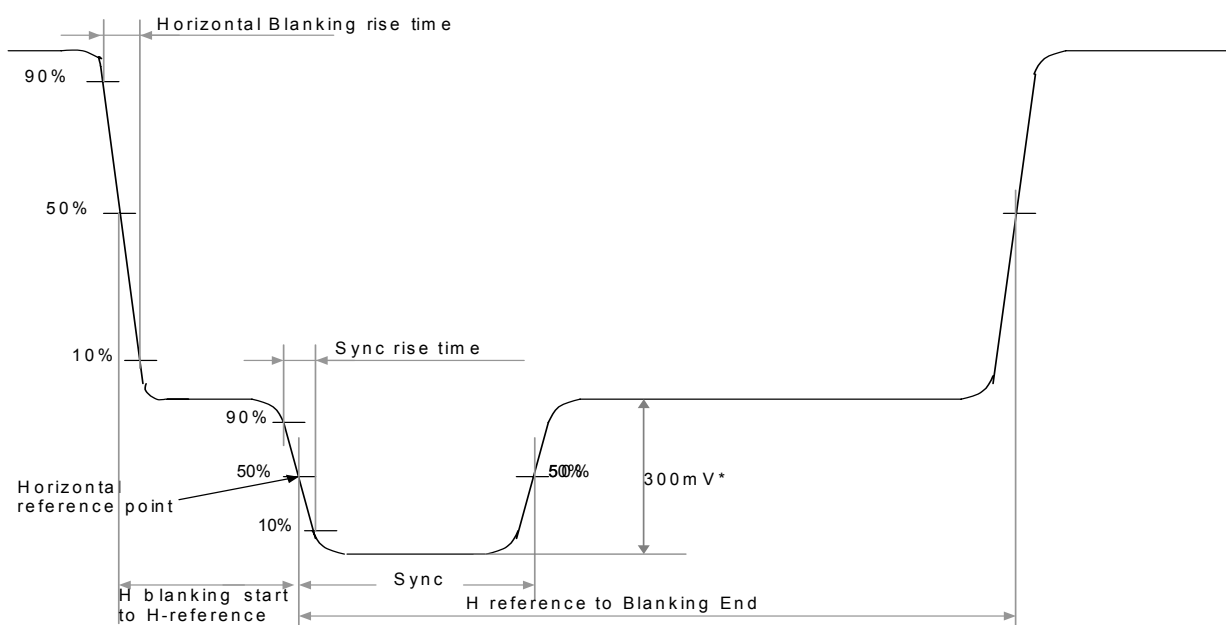
Only 525i output mode, AK8826 can output both of 286mV sync-waveform and 300mV sync-waveform with setting HDVRATIO-bit of **HD Block Control Register [SubAddress0x07]**

HD Block Control Register**Sub Address 0x07****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDWSS	HDCFLT1	HDCFLT0	HDYFLT1	HDYFLT0	Reserved	COLSNCEN	HDVRATIO

HDVRATIO-bit	Sync waveform Level
0 300mV	(EIA770.2-A)
1 286mV	(EIA770.1-A)

(1-1) 525i Sync waveform

**Fig. 120**

measurement	point	value	Recommended tolerance	units
Total line period(derived)		63.556		usec
Sync rise time	10% - 90%	140	+/- 20	nsec
Horizontal Sync	50%	4.7	+/- 0.1	usec

Design Spec (T=1/13.5MHz)

	Measurement Point	Reference Clock
H-Blanking start to H-reference	50%	16T
H reference to H-blanking end	50%	122T

* 286mV sync waveform can be output by register setting.

(1-2) 525i Frame Configuration: Vertical SYNC signal wave form timing

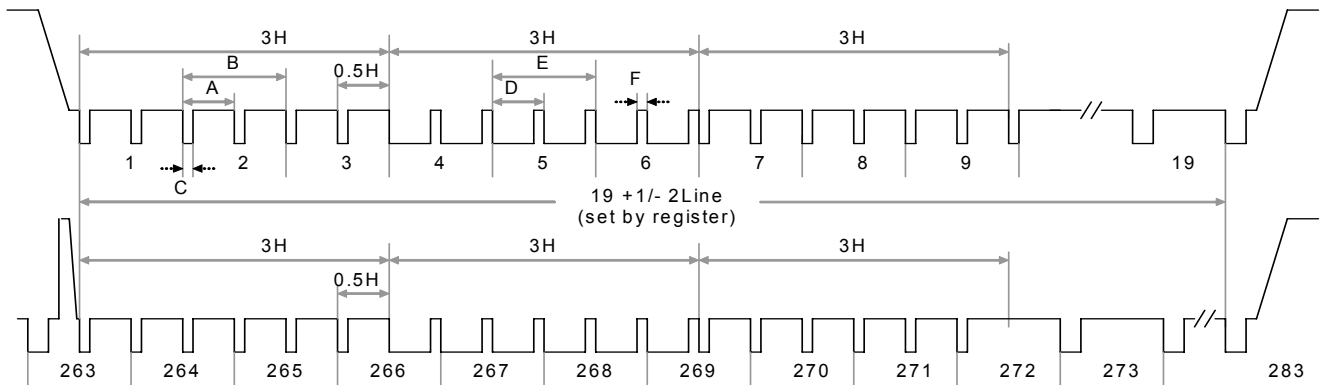


Fig. 121

Symbol	Duration	Measurement point	Reference
A 429T		50% 13.	5MHz Clock
B 858T			
C 31T			
D 429T			
E 858T			
F 63T			

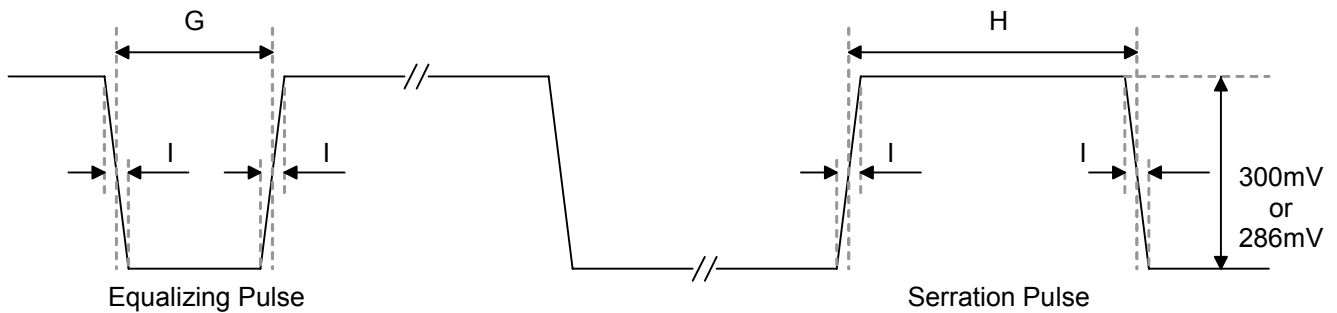


Fig. 122 Equalizing Pulse & Serration Pulse

Symbol	Measurement	point	Value	Recommended tolerance	units
	Field Period (derived)		16.6833		msec
	Frame period (derived)		33.3667		msec
	Vertical blanking start before first equalizing pulse	50% 1.	5	+/- 0.1	usec
	Vertical blanking (63.556usec x 20lines + 1.5usec)		19* lines + 1.5 usec	0 +/- 0.1	lines usec
	Pre-equalizing duration		3		lines
G	Pre-equalizing pulse width	50%	2.3	+/- 0.1	usec
	Vertical sync duration		3		lines
H	Vertical serration pulse width	50%	4.7	+/- 0.1	usec
	Post-equalizing duration		3		lines
G	Post-equalizing pulse width	50%	2.3	+/- 0.1	usec
I	Sync rise time		140	+/- 20	nsec

* There is a case of V-Blank of 20 lines. This value is pre-settable by register.

(2) 625i Sync-Signal

(2-1) 625i Horizontal SYNC waveform

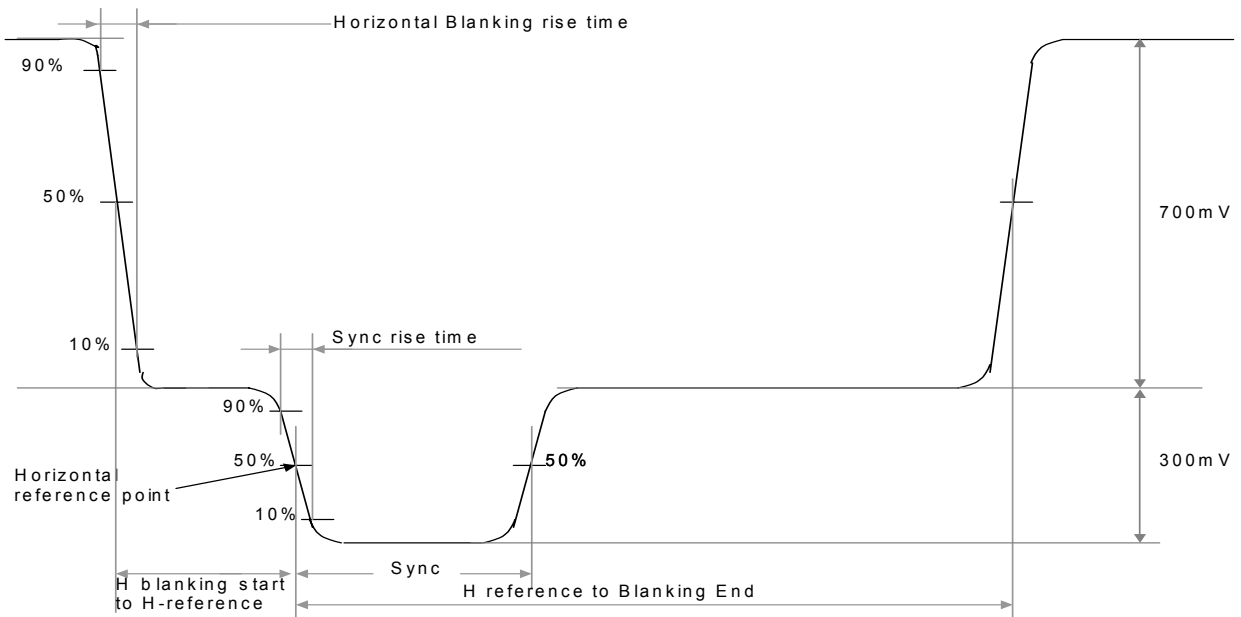


Fig. 123

measurement	point	value	Recommended tolerance	units
Total line period(derived)		64.0		usec
Sync rise time	10% - 90%	0.2	+/- 0.1	usec
Horizontal Sync	50%	4.7	+/- 0.2	usec

Design Spec. (T =1/13.5MHz)

	Measurement Point	Reference Clock
H-Blanking start to H-reference	50%	12T
H reference to H-blanking end	50%	132T

(2-2) 625i Frame Configuration and signal waveform

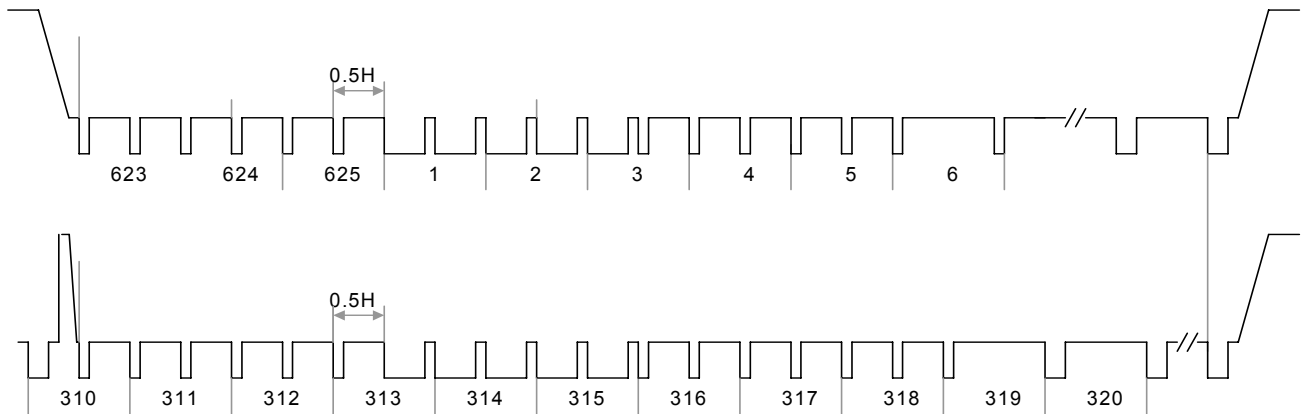


Fig. 124

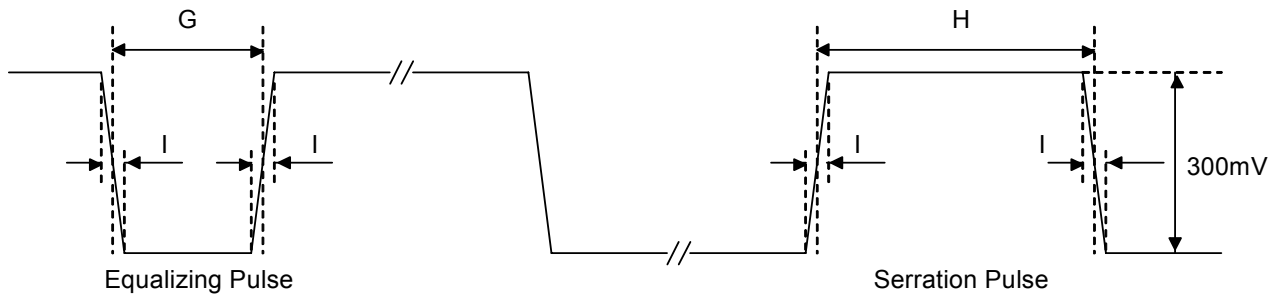


Fig. 125 Equalizing Pulse と Serration Pulse

Symbol	Measurement	point	Value	Recommended tolerance	units
G	Pre-equalizing pulse width	50%	2.35	+/- 0.1	usec
H	Vertical serration pulse width	50%	4.7	+/- 0.2	usec
G	Post-equalizing pulse width	50%	2.35	+/- 0.1	usec
I	Sync rise time		200	MAX300	nsec

* There is case where tolerance of Sync rise time is added to Pulse width tolerance.

(3) 525p waveform (EIA-770.2-C)

(3-1) 525p Horizontal Sync waveform

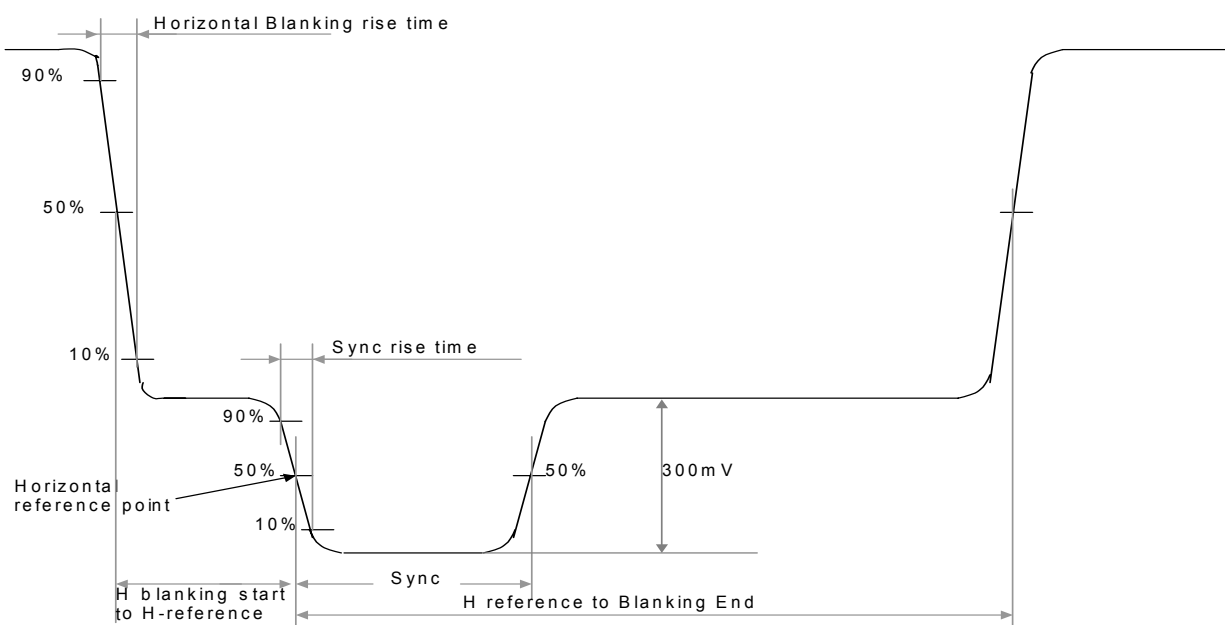


Fig. 126

measurement	point	value	Recommended tolerance	units
Total line period(derived)		31.776		usec
Sync rise time	10% - 90%	70	+/- 10	nsec
Horizontal Sync	50%	2.33	+/- 0.05	usec

(3-2) 525p Vertical Sync waveform and Timing

AK8826 supports both of CEA-770.2-A and CEA770.2-C

HD Block Miscellaneous Control Register

Sub Address 0x0A

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	STD770_2C	HDCEA805B	CCWSSSUE	Reserved	HDAFLT1	HDAFLT0

STD770_2C-bit	Standard	Remark
0 CEA	770.2-A	
1 CEA	770.2-C	

(3-2-2) CEA 770.2-A (STD770_2C-bit =0)

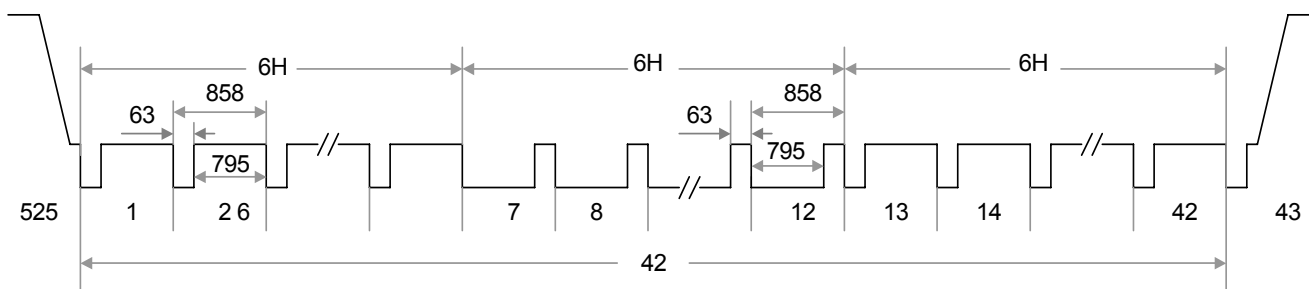


Fig. 127

Measurement	point	value	Recommended tolerance	units
Frame period (derived)		16.6833		msec
Vertical blanking (31.776usec x 42lines + 0.59usec)		42 lines + 0.59usec	0 +/- 0.05	lines usec
Vertical sync duration		6		lines
Vertical serration pulse width	50%	2.33	+/- 0.05	usec

(3-2-3) CEA 770.2-C (STD770_2C-bit =1)

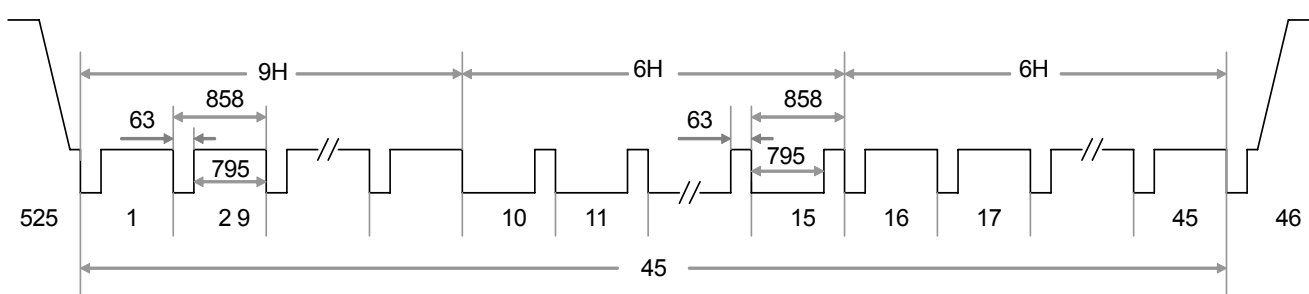


Fig. 128

Measurement	point	value	Recommended tolerance	units
Frame period (derived)		16.6833		msec
Vertical blanking (31.776usec x 45lines + 0.59usec)		45 lines + 0.59usec	0 +/- 0.05	lines usec
Vertical sync duration		6		lines
Vertical serration pulse width	50%	2.33	+/- 0.05	usec

(4) 625p Synchronization Waveform (ITU-R. BT1368)

(4-1) 625p Horizontal Sync waveform

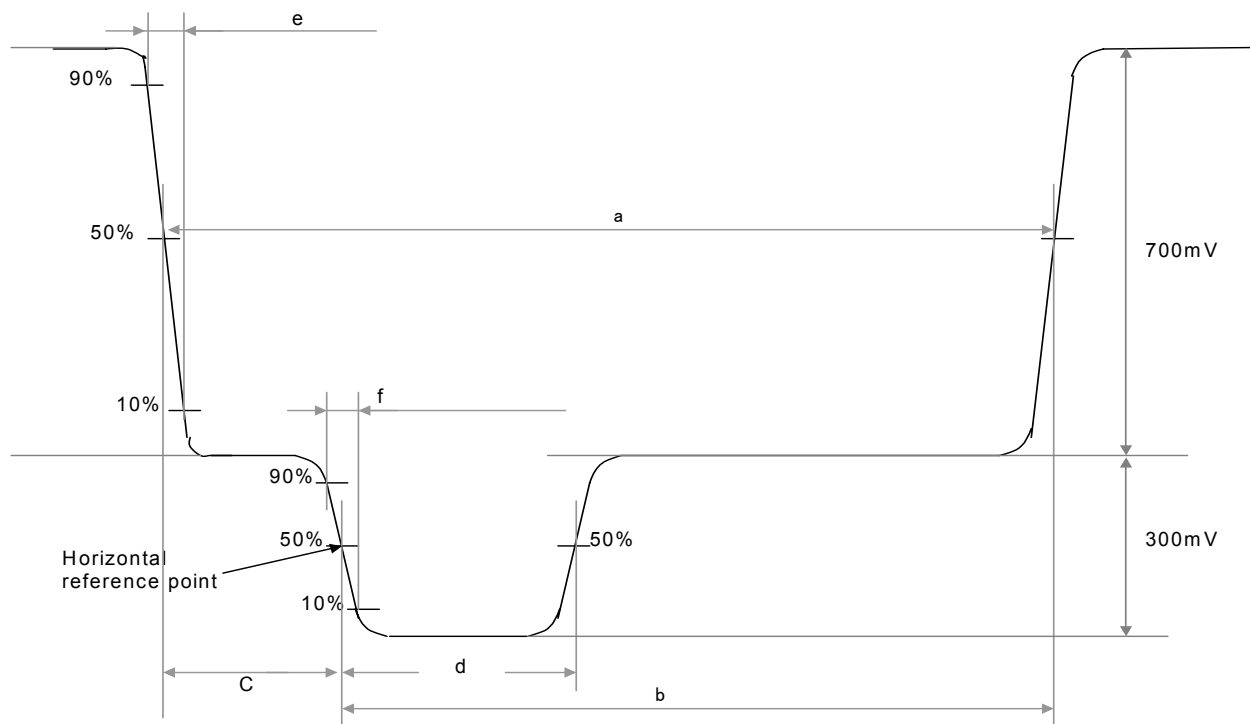


Fig. 129

Symbol	Characteristics	625/50/1:1
H	Nominal line period (us)	32
a	Horizontal blanking interval(us)	6.0±1.5
d	Synchronizing pulse (us)	2.35±0.1
f	Build-up time (10 to 90%) of the edges of the horizontal synchronizing pulses (us)	0.1±0.05

(4-2) 625p Vertical Sync waveform and timing

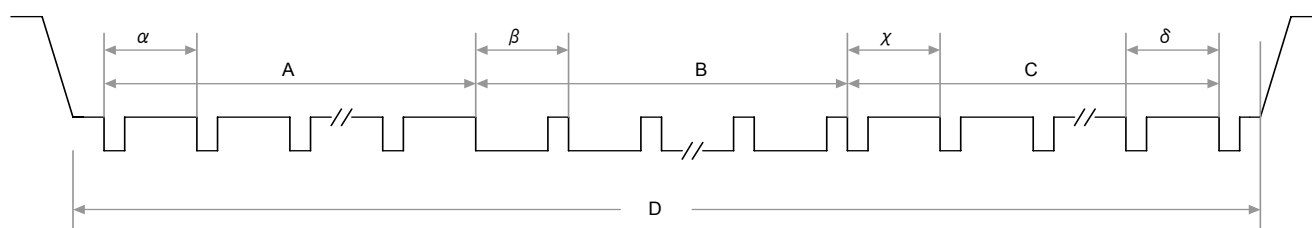


Fig. 130

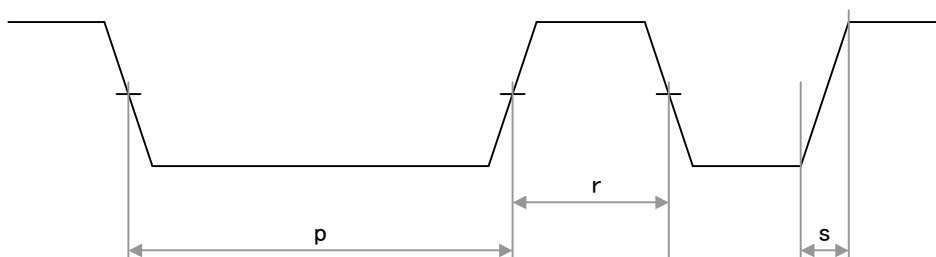


Fig. 131

Symbol	Characteristics	625/50/1:1
V	Nominal frame period (ms)	20
D	Vertical blanking interval	$49H + \alpha^*$
-	Build-up time (10 to 90%) of the edges of vertical blanking pulse (us)	0.15 ± 0.05
A	Interval between front edges of vertical blanking interval and front edges of first vertical synchronizing pulse	$5H^*$
C	Interval between back edges of last vertical synchronizing pulse and back edge of vertical blanking interval	$39H^*$
B	Duration of sequence of vertical synchronizing pulses	$5H^*$
p	Duration of vertical synchronizing pulse (us)	29.65 ± 0.1
r	Interval between vertical synchronizing pulse (us)	2.35 ± 0.1
s	Build-up time (10 to 90%) of the vertical synchronizing pulses (us)	0.1 ± 0.05

* For H and a, see Table 1 (ITU-R BT.1358)

Line number			
α	β	χ	δ
621.1		6	44

(5) 1080i Synchronization waveform (EIA-770.3-C)

(5-1-1) 1080i Horizontal Sync waveform (60Hz)

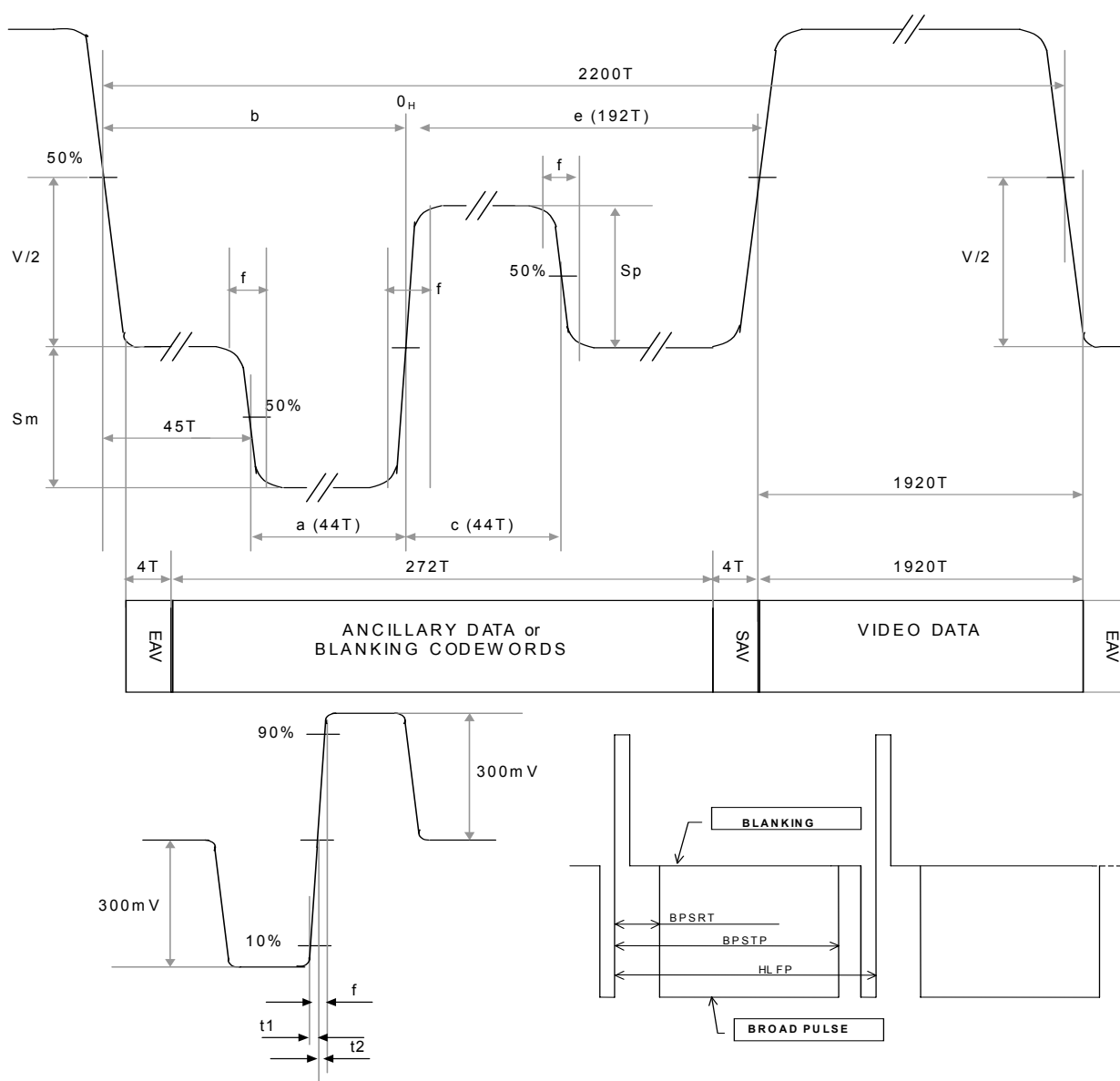


Fig. 132

1080i 60Hz

Symbol	Parameter	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
b	End of active video	1.120 [usec]	89		+0.080 [usec]
c	positive line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
e	Start of active video	2.589 [usec]	192	-0 / + 6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 - t1	Symmetry of rising edge	-	-		+/- 0.002 [usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
T	Total Lines		2200		
	Active Lines		1920	-12, +0	
BPSRT	Broad pulse start pos		132		-3 ~ +3
BPSTP	Broad pulse stop pos		1012		-3 ~ +3
HLFP	H/2 pos		1100		-3 ~ +3

(5-1-2) 1080i Vertical Sync waveform and timing (60Hz)
F frame Configuration

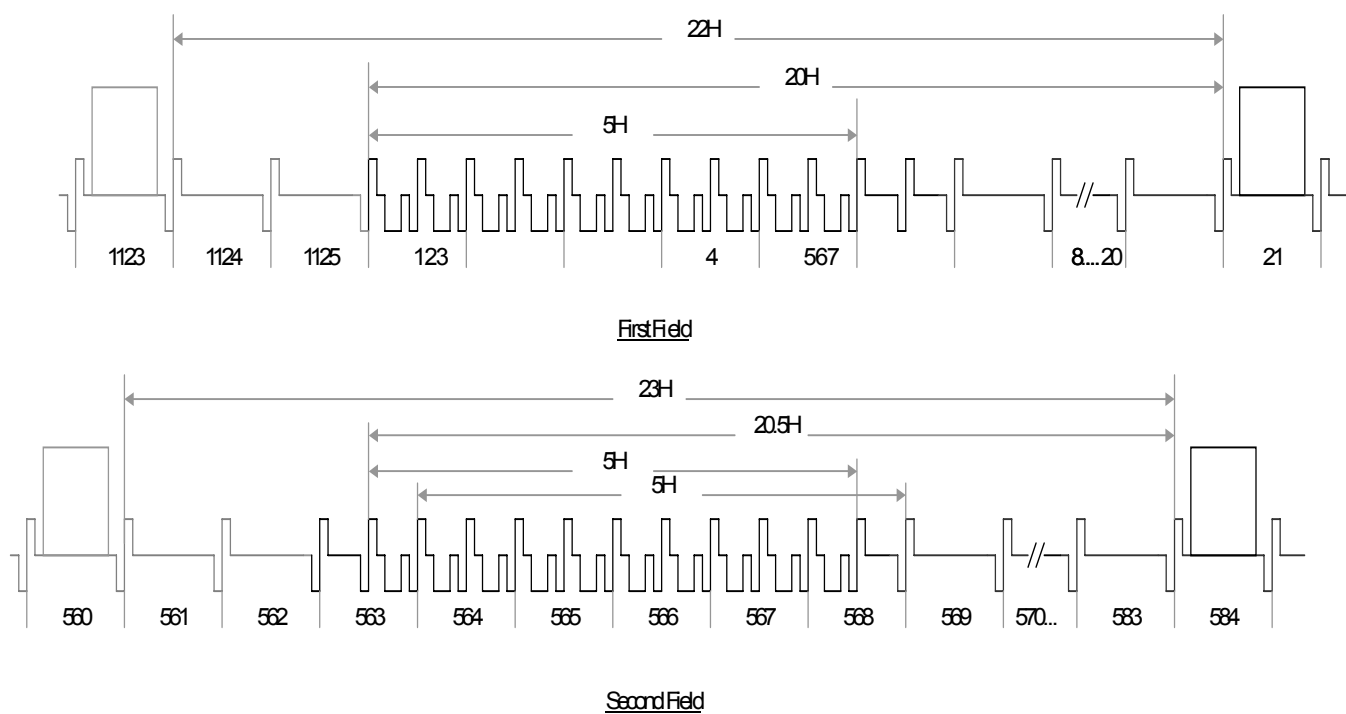
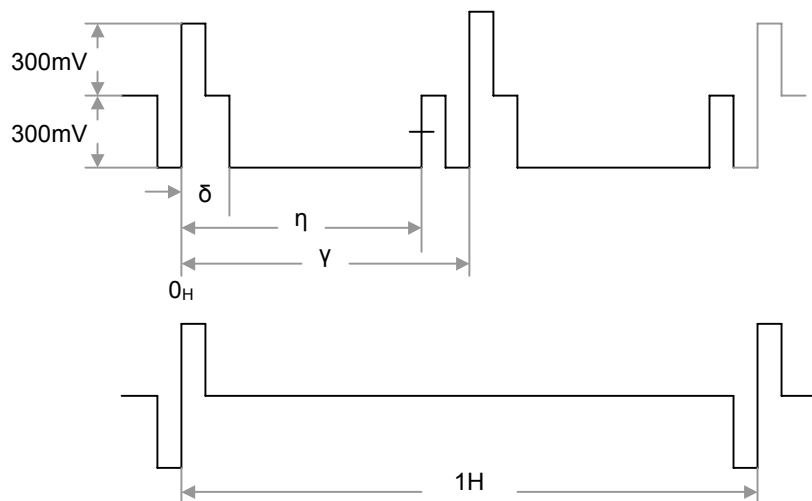


Fig. 133

Vertical Sync waveform (Refer to ITU-R.BT709)



F

ig. 134

Durat	ion	Tolerance
δ	132 T	+/- 3
γ	1100 T	+/- 3
η	1012 T	+/- 3

(5-2-1) 1080i Horizontal Sync waveform (50Hz)

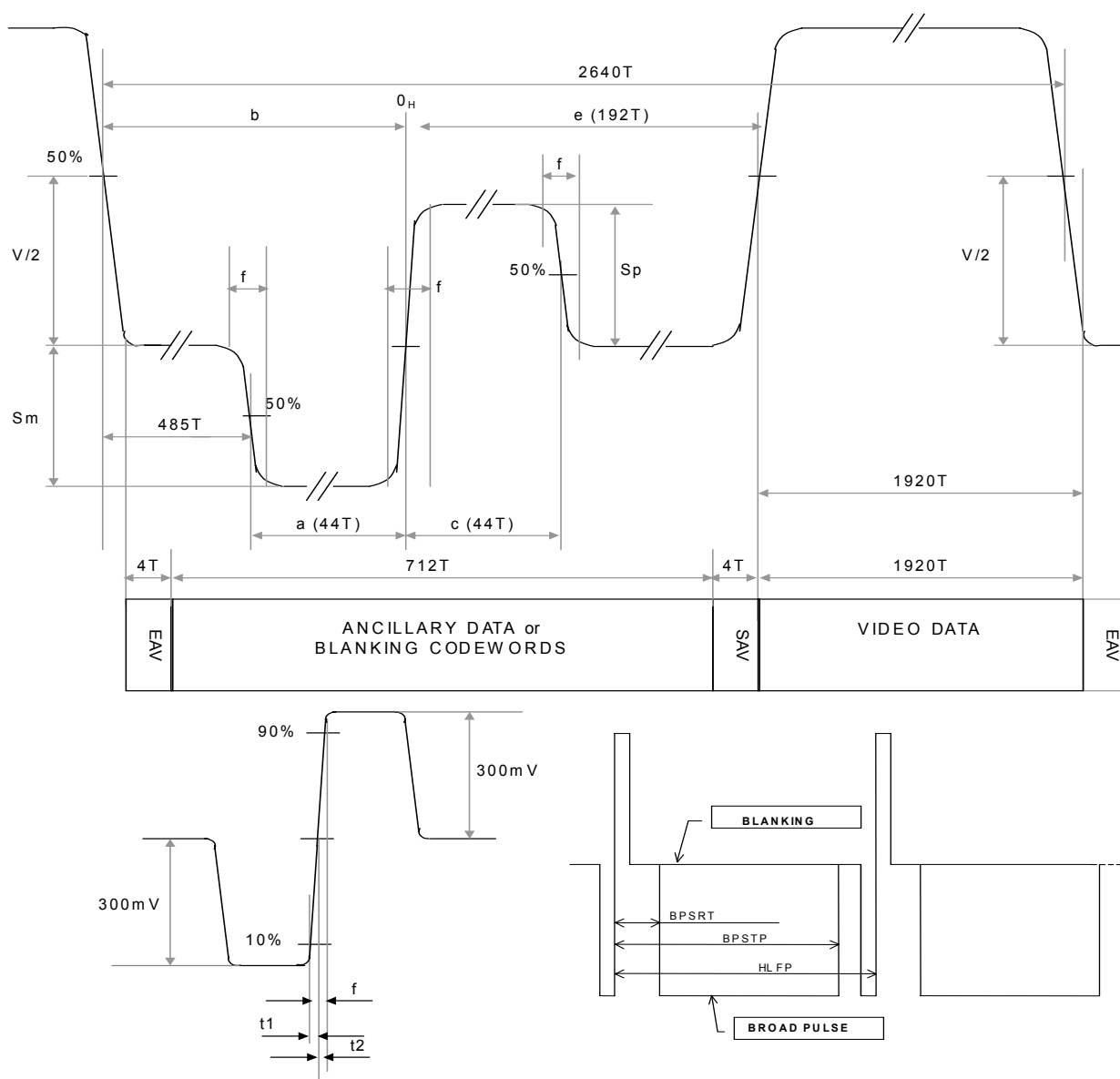


Fig. 135

1080i 60Hz

Symbol	parameter	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
b	End of active video	7.120 [usec]	529	+	0.080 [usec]
c	positive line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
e	Start of active video	2.589 [usec]	192	-0 / + 6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 - t1	Symmetry of rising edge	-	-		+/- 0.002 [usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
	Total Lines		2640		
	Active Lines		1920	-12, +0	
BPSRT	Broad pulse start pos		132		-3 ~ +3
BPSTP	Broad pulse stop pos		1012		-3 ~ +3
HLFP	H/2 pos		1100		-3 ~ +3

(5-2-2) 1080i Vertical Sync waveform(50Hz)

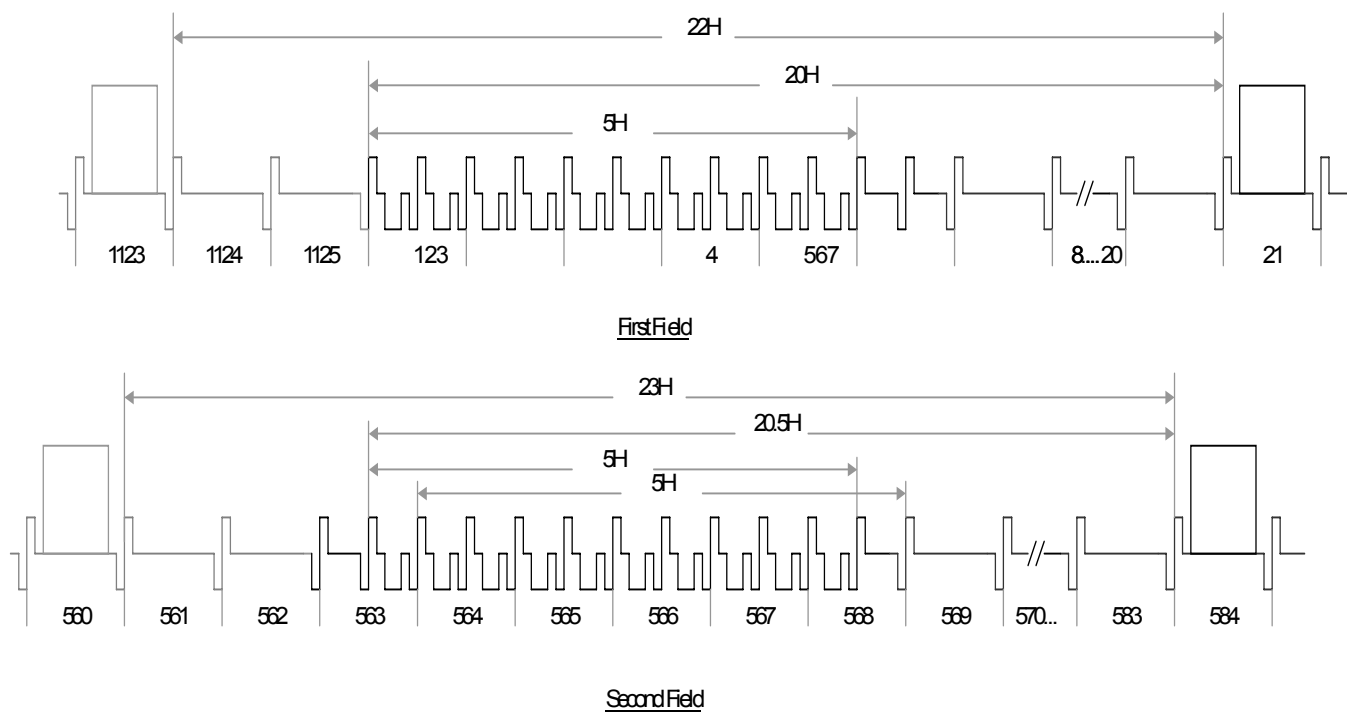


Fig. 136

Vertical Sync Waveform (Refer to ITU-R.BT709 standard)

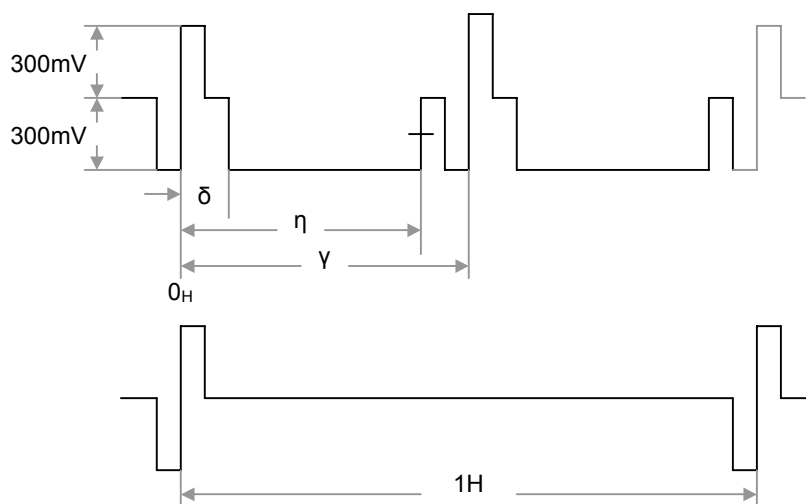


Fig. 137

Durat	ion	Tolerance
δ	132 T	+/- 3
γ	1100 T	+/- 3
η	1012 T	+/- 3

(6) 720p Synchronization waveform and timing (EIA-770.3-C)

(6-1-1) 720p Horizontal Sync waveform (60Hz)

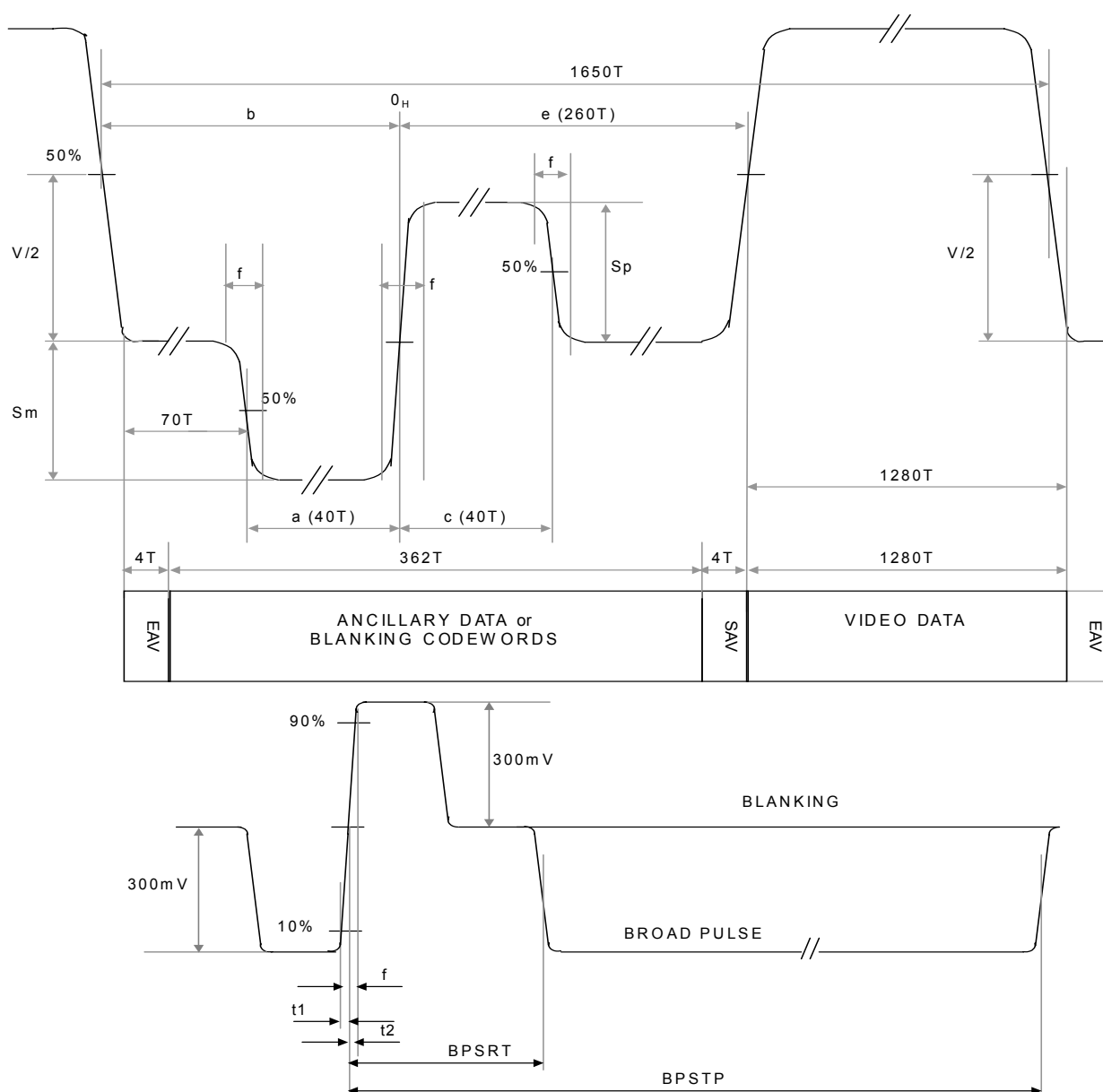


Fig. 138

Symbol	parameter	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.539 [usec]	40	+/- 3	+/- 0.040 [usec]
b	End of active video	1.495 [usec]	111	+	0.080 [usec]
c	positive line sync width	0.539 [usec]	40	+/- 3	+/- 0.040 [usec]
e	Start of active video	3.502 [usec]	260	-0 / + 6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 - t1	Symmetry of rising edge	-	-		+/- 0.002 [usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
	Total Lines		1650		
	Active Lines		1280	-12, +0	
BPSRT	Broad Pulse Start pos		260	0 ~ +6	+0.080 [usec]
BPSTP	Broad Pulse stop pos		1540	-6 ~ 0	- 0.080 [usec]

Fig. 139

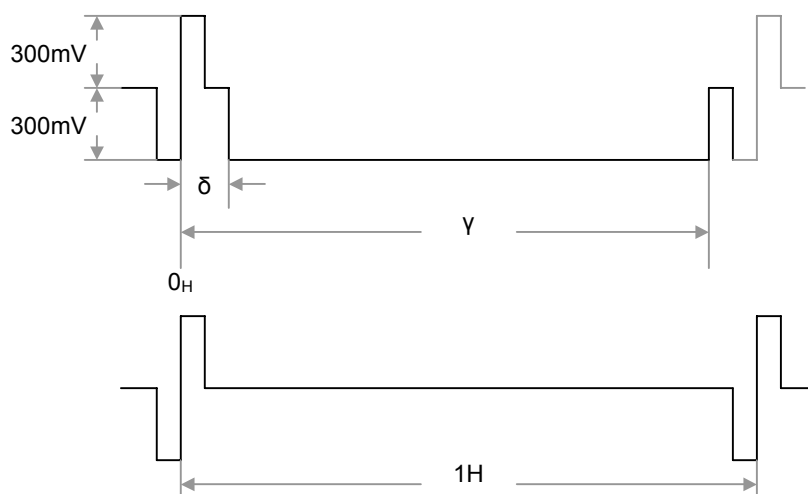


Fig. 140

Durat	ion	Tolerance
δ	260 T	-0 / +6
γ	1540T	-6 / +0

(6) 720p Synchronization waveform (EIA-770.3-C)

(6-1-1) 720p Horizontal Sync waveform (50Hz) (based on SMPTE296M)

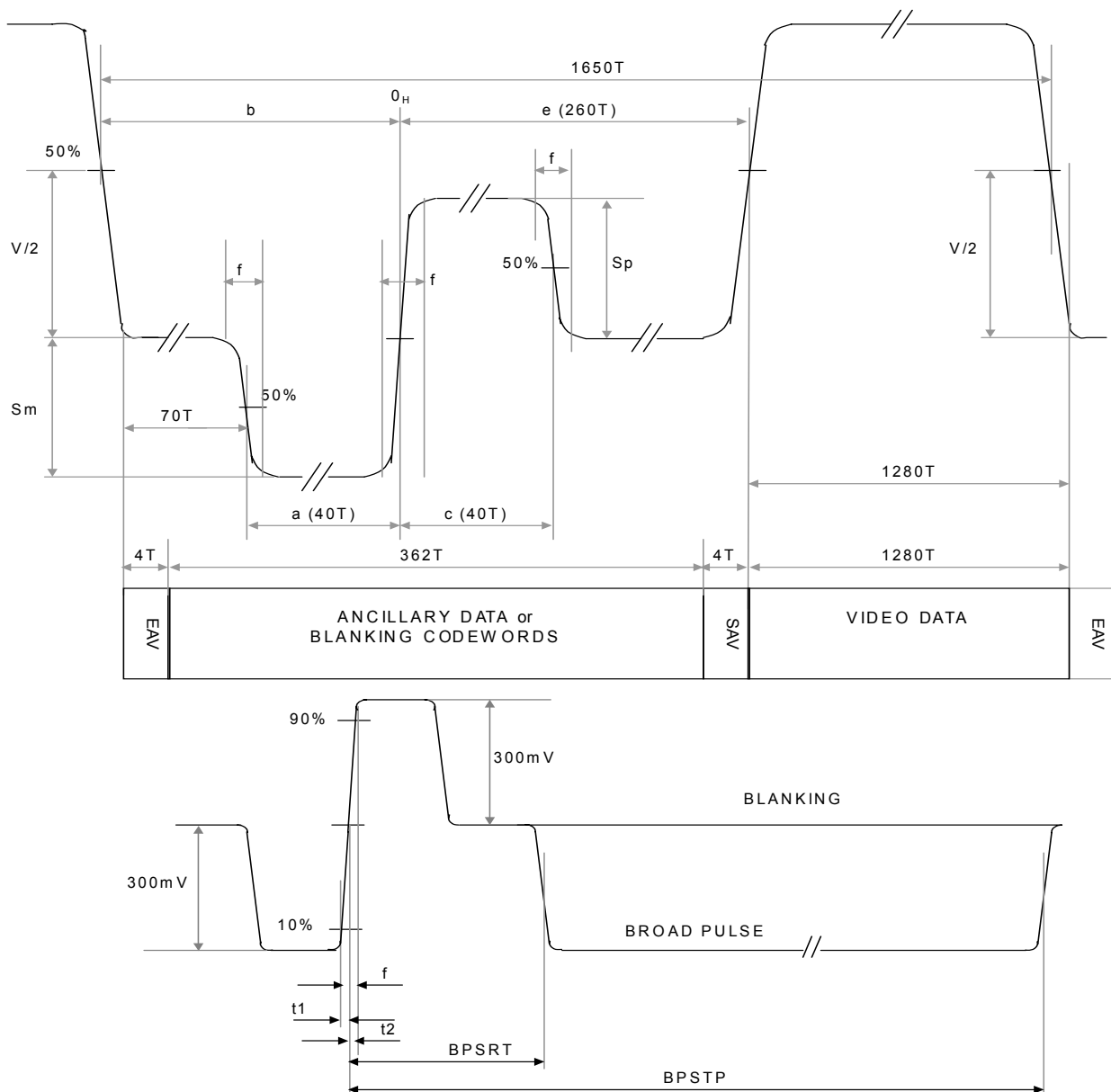


Fig. 141

Symbol	parameter	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.539 [usec]	40	+/- 3	+/- 0.040 [usec]
b	End of active video	5.926 [usec]	440		
c	positive line sync width	0.539 [usec]	40	+/- 3	+/- 0.040 [usec]
e	Start of active video	3.502 [usec]	260	-0 / +6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 - t1	Symmetry of rising edge	-	-		
Sm	Amplitude of negative pulse	300 [mV]	-		
Sp	Amplitude of positive pulse	300 [mV]	-		
V	Amplitude of video signal	700 [mV]	-		
	Total Lines		1980		
	Active Lines		1280		
BPSRT	Broad Pulse Start pos		260	0 ~ +6	+0.080 [usec]
BPSTP	Broad Pulse stop pos		1540	-6 ~ 0	- 0.080 [usec]

■ V-Blank Interval

The AK8826 has functions to set V-Blank Interval and to control Output Mode during the V-Blank Interval. V-Blank Interval is set by HDVL[1:0]bit of **HD VBI & Chip Level Control Register [SubAddress 0x01]**. The output mode during V-Blank Interval set by VUNMASK-bit.

HD VBI & Clip Level Control Register

Sub Address 0x01

default Value 0x04

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCLPLVL1	HDCLPLVL0	Reserved	Reserved	Reserved	HDVUNMSK	HDVL1	HDVL0

V-Blank Interval Setting

	HDVL[1:0]-bit			
	10	11	00	01
525i	Line1 – Line18 Line264 – Line281	Line1 – Line19 Line264 – Line282	Line1 – Line20 Line264 – Line283	Line1 – Line21 Line264 – Line284
625i	Line623 – Line20 Line311 – Line333	Line623 – Line21 Line311 – Line334	Line623 – Line22 Line311 – Line335	Line623 – Line23 Line311 – Line336
525p	Line1 – Line40	Line1 – Line41	Line1 – Line42	Line1 – Line43
625p	Line621 – Line42	Line621 – Line43	Line621 – Line44	Line621 – Line45
1080i	Line1124 – Line1125 Line1 – Line18 Line561 – Line581	Line1124 – Line1125 Line1 – Line19 Line561 – Line582	Line1124 – Line1125 Line1 – Line20 Line561 – Line583	Line1124 – Line1125 Line1 – Line21 Line561 – Line584
720p	Line746 – Line750 Line1 – Line23	Line746 – Line750 Line1 – Line24	Line746 – Line750 Line1 – Line25	Line746 – Line750 Line1 – Line26

The relation between B-Blank Interval and HDVUNMASK-bit are shown as following table

mode HDVUNMSK	525i/625i mode	525p/625p mode	1080i mode	720p mode
0	Blank Level output during V-Blank Interval	Blank Level output during V-Blank Interval	Blank Level output during V-Blank Interval	Blank Level output during V-Blank Interval
1	Input data is output even during V-Blank Interval (525i: Line1-9 & Line264-272 625i: Line623-7 & Line311-318 are excluded)	Input data is output even during V-Blank Interval (525p: Line1-12 625p: Line641-5 are excluded)	Input data is output even during V-Blank Interval (Line1124-1125-6 & Line561-568 are excluded)	Input data is output even during V-Blank Interval (Line746-750-5 are excluded)

■ Adjustable Timing Function Between SYNC signal and HDY Signal, Between HDPB Signal and HDPr signal

SYNC Timing and Y signal output relation is adjustable in the AK8826. Setting of adjustable amount is made by HDYDELAY[2:0]-bit of **HDYPBPR Delay Control Register [SubAddress 0x02]**.

Adjustable range between SYNC signal and Y signal is +/- 3clocks.

Adjustable unit in 525i / p mode is based on 27MHz clock and in 1080i/720p modes it is based on 74.25MHz clock.

By this bit manipulation, Pb/Pr are shifted similarly as in the case of Y.

Pb / Pr signals with Y signal relation are adjusted by PBPRDELAY[2:0]-bit of **HDYPBPR Delay Control Register [SubAddress 0x02]**.

Adjustable range is +/- 3clocks. Adjustable unit in 525i / p modes is based on 27MHz clock, and in 080i/720p modes, it is based on 74.25MHz.

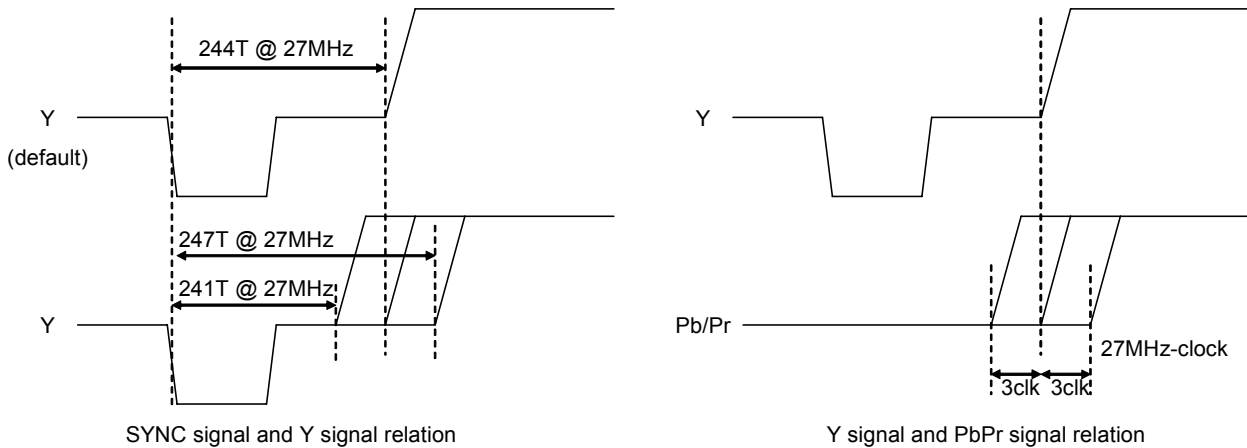


Fig. 142 525i/p, 625i/p mode

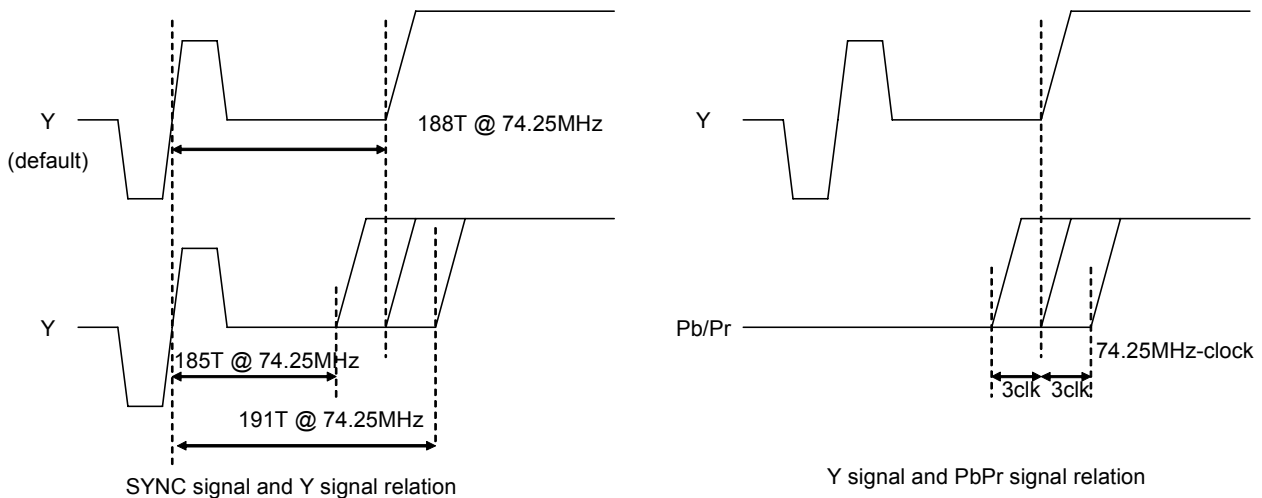
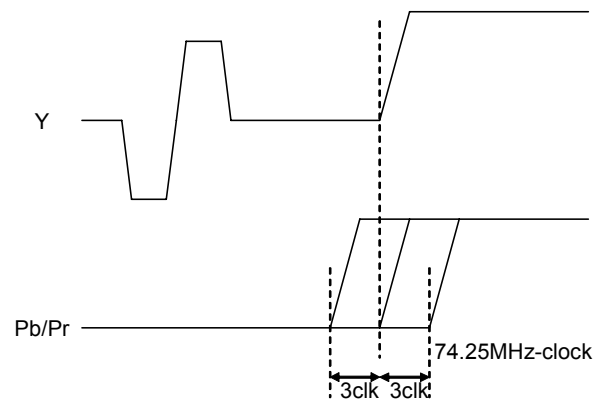
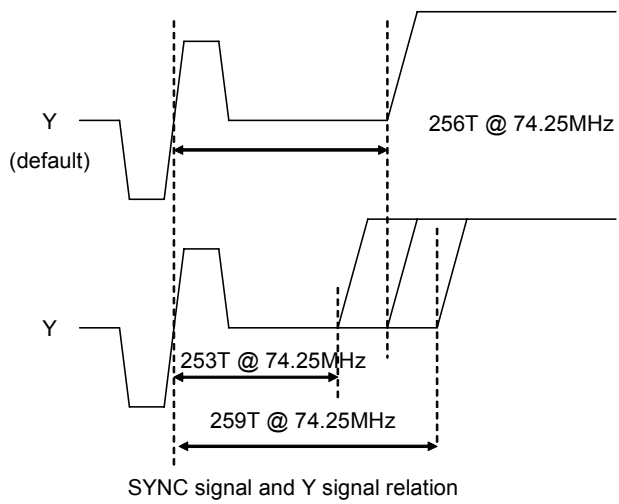


Fig. 143 1080i mode



Y signal and PbPr signal relation

Fig. 144 720p mode

■ Analog RGB Signal Output

RGB conversion (601 Color Space and always Sync-On-Green(SOG)) is possible only with 525i / 625i or SDTV input.

Conversion Factors

$$R = Y + 1.372 * (Cr + 128)$$

$$G = Y + 0.336 * (Cb + 128) + 0.698 * (Cr + 128)$$

$$B = Y + 1.732 * (Cb + 128)$$

RGB signals are output at the same timing as in YPbPr conversion and their levels are RGB Matrix results.

A similar SYNC signal is carried out on G signal.

The AK8826 outputs RGB signal by setting YC2RGB-bit of **I/O Data Format Register**.

I/O Data Format Register

Sub Address 0x0B

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDSDMASE	YC2RGB	Reserved DT	FMT	CONVMOD1	CONVMOD0	INPFMT1	INPFMT0

Input Data

Input Data	analog RGB Output YC2RGB-bit
YCbCr Data	1
RGB Data*	0

* AK8826 doesn't support EAV decode Interface mode in case of RGB Data in.

■ Video ID (CEA-805-A / CEA-805-B)

The AK8826 has a function to super impose a Copy Protect Information CGMS-A on output signal.
The AK8826 supports both of CEA-805-A and CEA-805-B standards.

(1) CEA-805-A

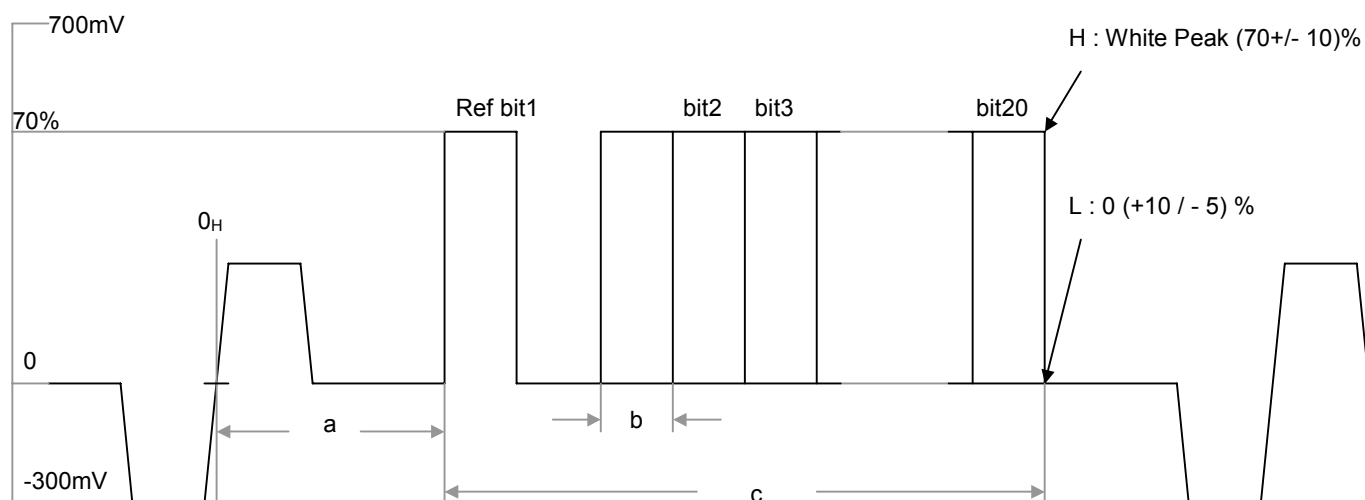


Fig. 145

a		b	c		Line
525i* (480i)	11.2 +/- 0.3usec (time from 0H)	2.235 +/- 50nsec	49.1 +/- 0.44usec		Line 20 Line 283
525P* (480P)	6T (5.8 +/- 0.15usec) (time from 0H)	T +/- 30nsec	22T (21.2 +/- 0.22usec)	$T : 1/(f_H \times 33)$ = 963nsec	Line 41
1080i	4T (4.15 +/- 0.16usec)	T +/- 30nsec	22T (22.84 +/- 0.21usec)	$T : 1/(f_H \times 2200/77)$ = 1.038usec	Line 19 Line 582
720P	4T (3.13 +/- 0.09usec)	T +/- 30nsec	22T (17.20 +/- 0.16usec)	$T : 1/(f_H \times 1650/58)$ = 0.782usec	Line 24

* SYNC signal waveform of 525i/p signals differ from the above, but timing is defined based on 0H point as starting point (time from 0H).

bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Data																				
	WORD 0 2bits		WORD 1 4bits				WORD 2 8bits								CRCC 6bits					

20 bit data is configured with WROD 0: 2bits / WROD 1: 4 bits / WORD 2: 8 bits / CRCC: 6 bits, as shown above.

When to set CGMS-A data, set HDVBIDEN-bit of **HD VBI Data 1 Register [SubAddress 0x03]** to "1", and write a setting value to **HD VBI Data 1/2 Register[SubAddress 0x03/0x04]**.

HD VBI Data 1 Register

Address 0x03

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDVBIDEN	Reserved	HDVBID1	HDVBID2	HDVBID3	HDVBID4	HDVBID5	HDVBID6

HD VBI Data 2 Register

Address 0x04

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDVBID7	HDVBID8	HDVBID9	HDVBID10	HDVBID11	HDVBID12	HDVBID13	HDVBID14

CGMS-A data should be finished being written 1-line before of the target lines.

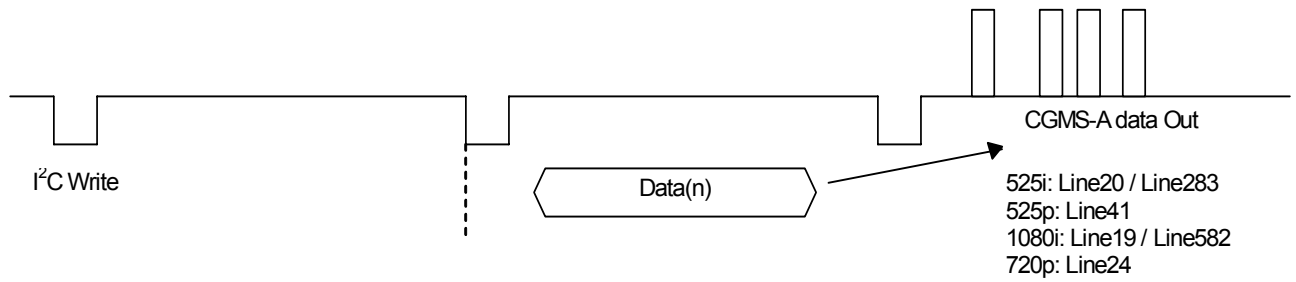


Fig. 146

CRCC is automatically calculated and added in the AK8826.

Default value of "CRCC Polynomial expressed X^6+X+1 " are all ones (see diagram below)

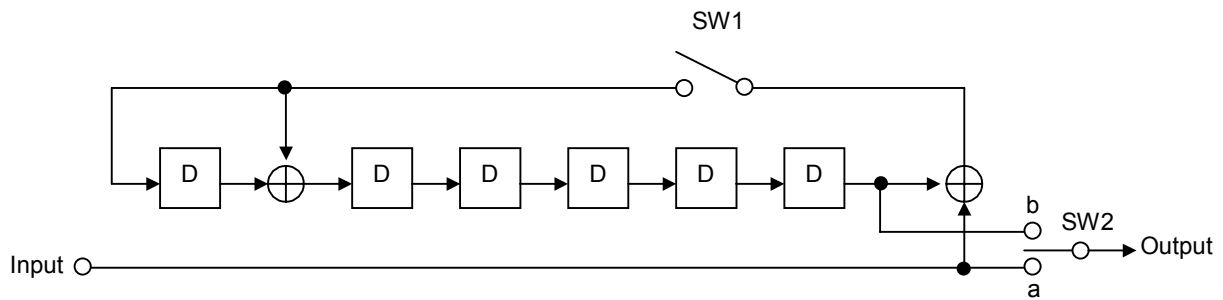


Fig. 147

CRCC generation is made as follows -

Set default values to all ones and closed SW1.

Set SW2 to "a" position and first 14bit data is input, then at the 15th bit open SW 1 and set SW 2 to "b" position, and CRCC is output.

When CGMS-A output and other signal waveforms coincide, CGMS-A precedes.

(2) CEA-805-B

This standard is adopted to 480p / 1080i / 720p output mode. CEA805-B Type-A standard is same as CEA-805-A standard.

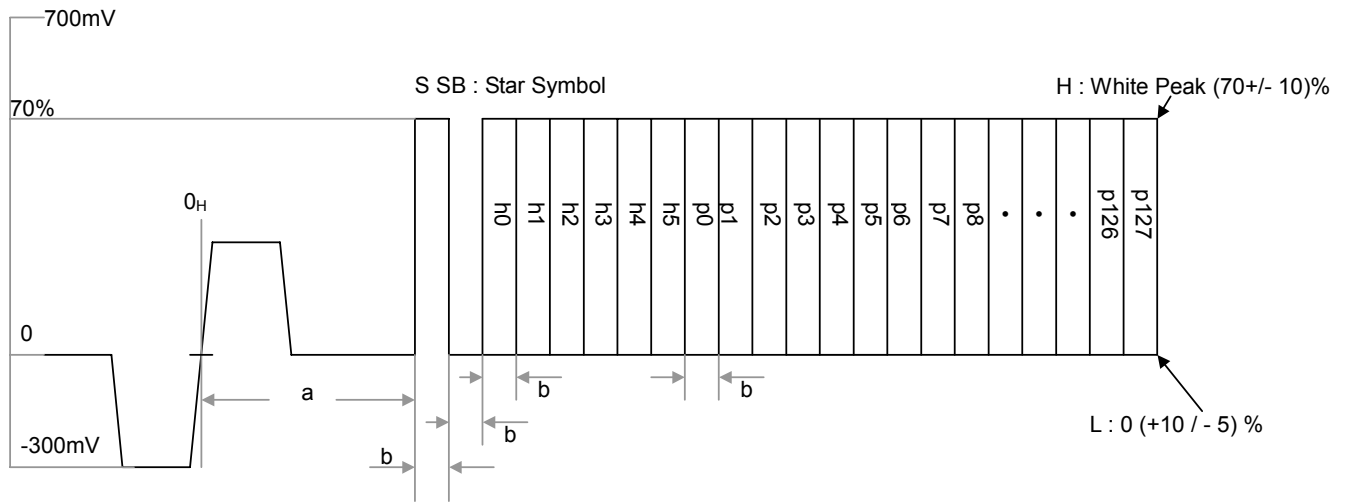


Fig. 148

	a	b	Tolerance form 0H		Line
480P* ¹	156T (Time from 0H)	4T	+/- 18.5ns	T : 1/27MHz	Line 43
1080i	308T	10T	+/- 18.5ns	T : 1/74.25MHz	Line 18 Line 581
720P 232T	* ²	8T	+/- 18.5ns	T : 1/74.25MHz	Line 23

*1 SYNC signal waveform of 480p differ from the above, but timing is defined based on 0H point as starting points.

*2 position of 232T is the position before starting active video area.

When to set CEA-805-B TypeB Data, set HDCEA805B-bit of **HD Block Miscellaneous Control Register[SubAddress 0x0A]** to "1", and write a setting value to **VBID-B Header Data Register/VBID Version Number Register/VBID Payload Packet Length Register/VBID-B Data1/2/3/4/5/6/7/8/9/10/11/12/13 Register {SubAddress 0x40 - 0x50}**

CRCC is automatically calculated and added in the AK8826.

Default values of "CRCC Polynomial expression X^6+X+1 " are all ones (see diagram bellows)

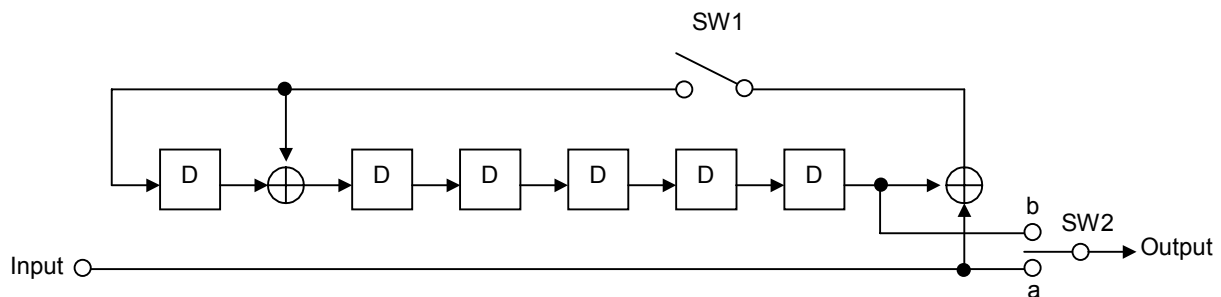


Fig. 149

■ Closed Caption

The description about “Closed Caption” is written in [6. Common Function Specification].
Closed Caption function is valid at 525i mode.

■ WSS

The description about “WSS” is written in [6. Common Function Specification].
WSS function is valid at 625i /625p mode.

■ RGB Output

The AK8826 can output Analog RGB signal with digital RGB Data in.

YC2RGB-bit of **I/O Data Format Register [SubAddress 0x0B]** is a control bit for RGB output function.

I/O Data Format Register

Sub Address 0x0B

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDSDMASE	YC2RGB	Reserved DT	FMT	CONVMOD1	CONVMOD0	INPFMT1	INPFMT0

YC2RGB-bit	Output signal	Note
0 YUV	Output	
1 RGB	Output	

■ DAC operating clock

The AK8826 has x2 PLL, DAC works with this x2 clock in Component Video Encoder mode. Following table shows DAC operation clock of each mode.

Input Data	525i/625i	525p/625p	1080i	720p
DAC Operation Clock	54MHz 54MHz		148.5MHz	148.5MHz

8. Composite Video Encoder Block

■ Block Diagram

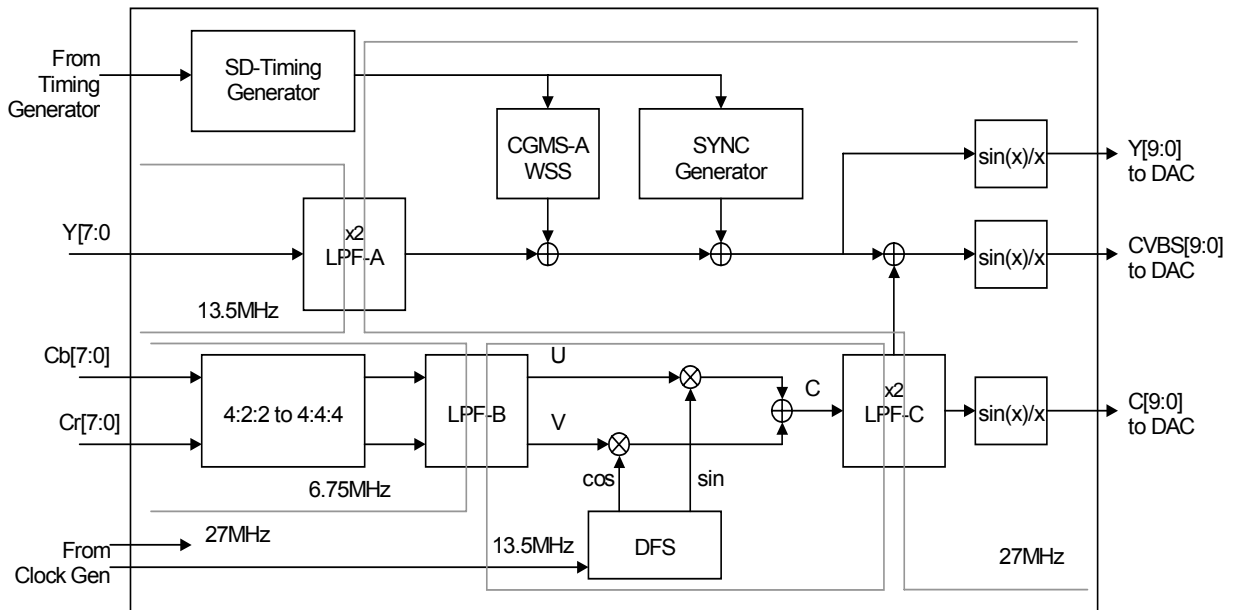


Fig. 150 Composite Video Encoder Block Diagram

■ Setting of Output Signal

SDVM[3 :0]-bit of **SD Block Control Register [SubAddress0x11]** defines the output signal from the AK8826.

SD Block Control Register

Sub Address 0x11

Default Value 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG SDCBG		SDSETUP	SCR	SDVM3	SDVM2	SDVM1	SDVM0

Table of the relation between output signal and SDVM[3:0]-bit

	SDVM0	SDVM1	SDVM2	SDVM3	SCR	Note
NTSC	0	0	0	0	1	Setup-bit should be set, if it is necessary
NTSC-4.43 1		1	0	0	0	
PAL 1		1	1	1	1	
PAL-M 1		0	1	0	1	
PAL-60 1		1	1	0	0	
PAL-Nc 0		1	1	1	1	

■ Video Signal Filter

(1) Luminance Filter

Luminance Filter of Composite Video Encoder can be selectable by register setting. Register-bit for filter setting is SD Block FLT Register(R/W) SDYLFT[1:0]-bit.

SD Block FLT Register

Sub Address 0x14

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	SDYFLT1	SDYFLT0	Reserved	Reserved	Reserved

SDYFLT [1:0] -bit	Selected Filter	Note
00 YF	LT0	Default
01	YFLT1	
10 YF	LT2	

Characteristics of each filter are shown as Fig. 152.

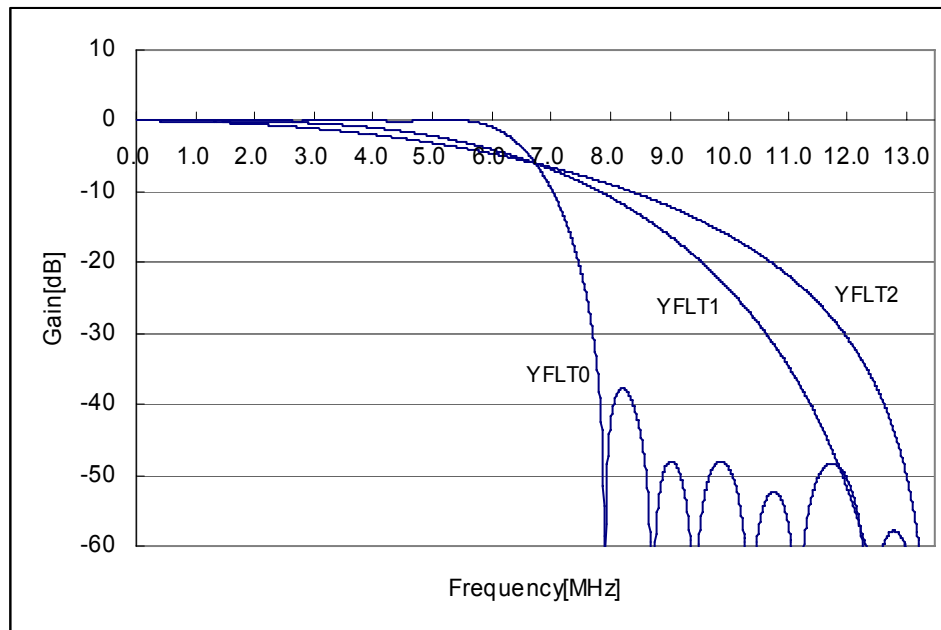


Fig. 151 L PF-A

(2) Chrominance Filter

(2-1) Over-Sampling Filter(6.75MHz → 13.5MHz) for Cb/Cr Data in Composite Video Encoder Block. (LPF-B)
Frequency Response of this Filter is shown as Fig. 153

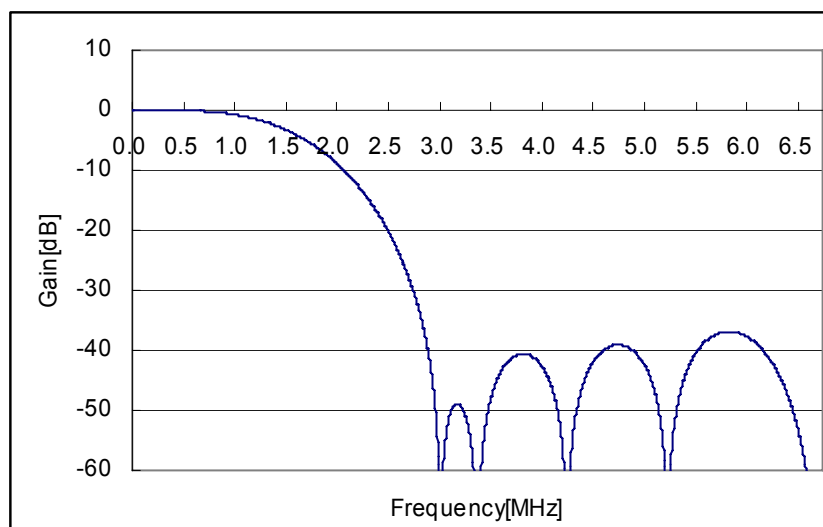


Fig. 152 LPF-B Frequency Response

(2-2) Over-Sampling Filter(6.75MHz → 13.5MHz) for C Data in Composite Video Encoder Block. (LPF-C)
Frequency Response of this Filter is shown as Fig. 154

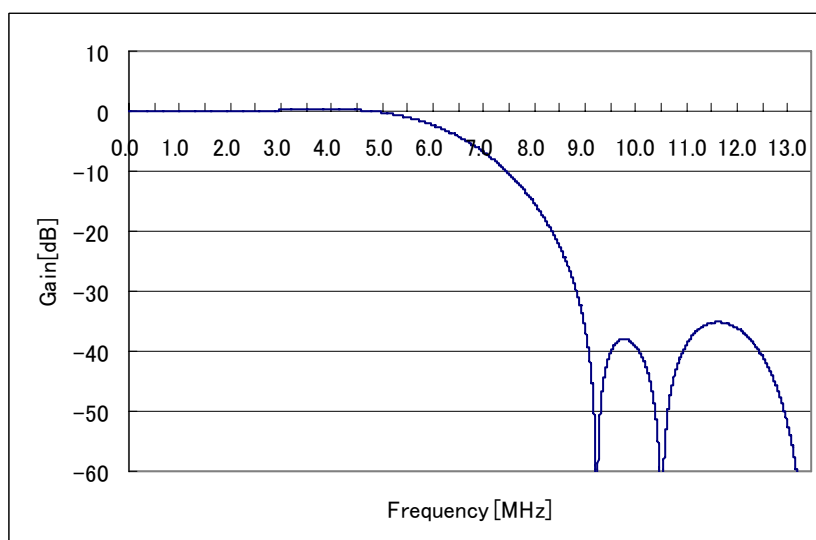


Fig. 153 LPF-C Frequency Response

■ Color Burst Signal (SDTV)

Color burst signal is generated by 32bits-length Digital Frequency Synthesizer. Subcarrier Frequency of Color-Burst is set by SDVM0-SDVM1 -bits of **SD Block Control Register (R/W) [Sub Address 0x11]**.

SD Block Control Register

Sub Address 0x11

Default Value 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG	SDCBG	SDSETUP	SCR	SDVM3	SDVM2	SDVM1	SDVM0

Standard	Subcarrier Freq (MHz)	Video Process 1 [SDVM1,SDVM0]
NTSC-M 3.	57954545	[0,0]
PAL-M 3.	57561188	[0,1]
PAL-B,D,G,H,I	4.43361875	[1,1]
PAL-N(Arg) 3.	5820558	[1,0]
PAL-N(non-Arg) 4.	43361875	[1,1]
PAL60 4.	43361875	[1,1]
NTSC-4.43 4.	43361875	[1,1]

Burst Table

Sub-carrier frequency 3.57561188MHz is allowed when PAL-M mode is selected.

Sub Carrier Frequency and Sub Carrier Phase are set by **Sub Carrier F requency Control Register (R/W) [Sub Address 0x16]** **Sub Carrier Phase Control Register (R/W) [Sub Address 0x17]**.

The burst frequency and initial phase resolution are as follows.

Frequency resolution	0.8046Hz
SCH Phase resolution	360°/256

■ Video Interface Timing (Composite Video Encoder Block)

To synchronize with input data, AK8826 supports two kinds of interface mode.

- (1) ITU-R BT.656 interface mode
- (2) Slave operation with HD/VD Interface mode

This interface mode is set by REC656-bit of **SD Blanking Set Register (R/W) [Sub Address 0x10]**.

SD Blanking Set Register

Sub Address 0x10

Default Value 0xA1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBLN4	SDBLN3	SDBLN2	SDBLN1	SDBLN0	Reserved	Reserved	REC656

REC656-bit	Interface mode	Note
0	Slave operation with HD/VD	
1	ITU-R.BT656 I/F mode	

(1) ITU-R BT.656 I/F mode

When AK8826 receives IT U-R BT. 656 signal, AK8826 decodes [EAV] code in the data for synchronization then outputs the HSYNC. AK8826 outputs HSYNC at the rising edge of SYSCLK in the timing of the 32nd/24th (NTSC/PAL) data slot, which is counted from the [EAV] starting point as below.

REC656-bit=1 of **SD Blanking Set Register (R/W) [Sub Address 0x10]** should be "0" for setting to this mode.

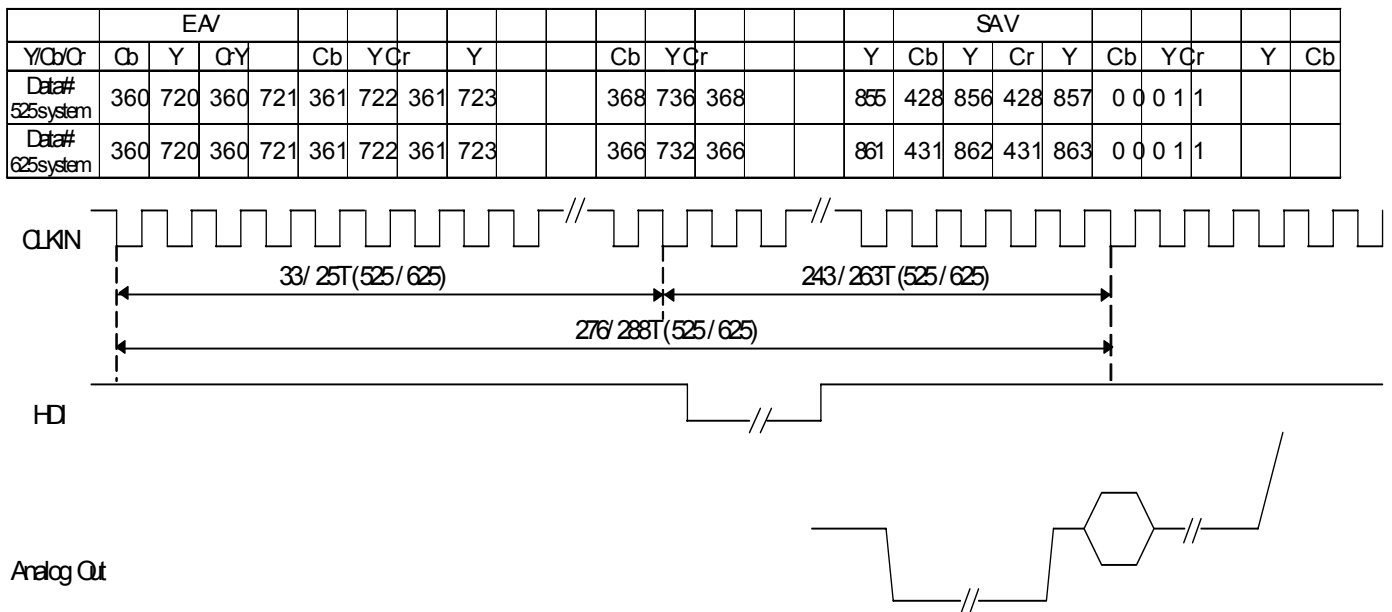


Fig. 154

(2) Slave mode

On slave mode operation, HSYNC and VSYNC are input to AK8826.

AK8826 monitors the transition of HSYNC at the timing of the rising edge of SYSCLK. After AK8826 recognizes HSYNC is Low-logic, AK8826 sets the slot number to the 32nd/24th (NTSC/PAL), internally, then AK8826 starts to sample the data as Cb on 276th/288th (NTSC/PAL) slot.

Video field is recognized the transition timing between VSYNC and HSYNC. As in the figure, there is a tolerance of $\pm 1/4H$.

This interface mode is set by REC656-bit = 0 of **SD Blanking Set Register (R/W) [Sub Address 0x10]**.

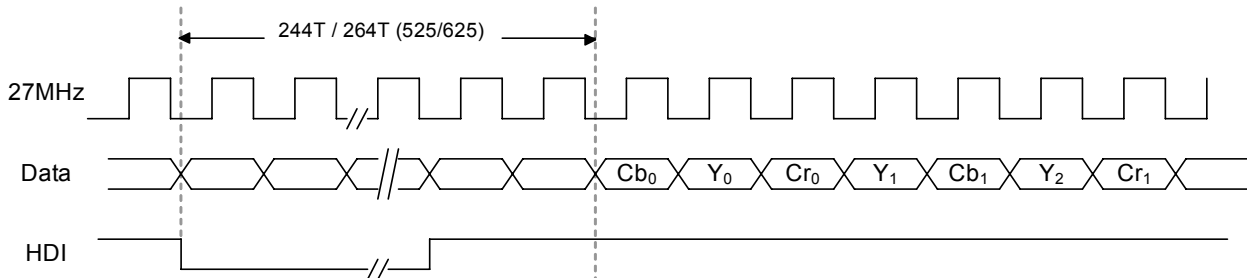


Fig. 155 Relation between HSYNC and Data

Field Detection with HSYNC and VSYNC

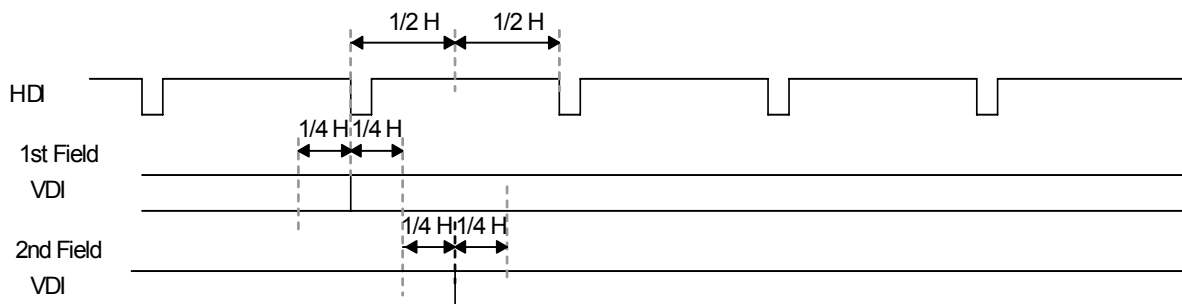


Fig. 156 HD/VD timing

Relation between Line# and VD is shown as Fig.158

525-Line System

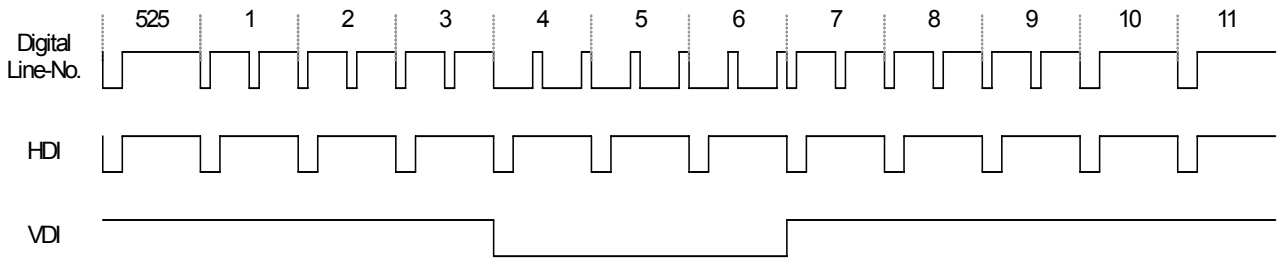


Fig. 157 1st Field

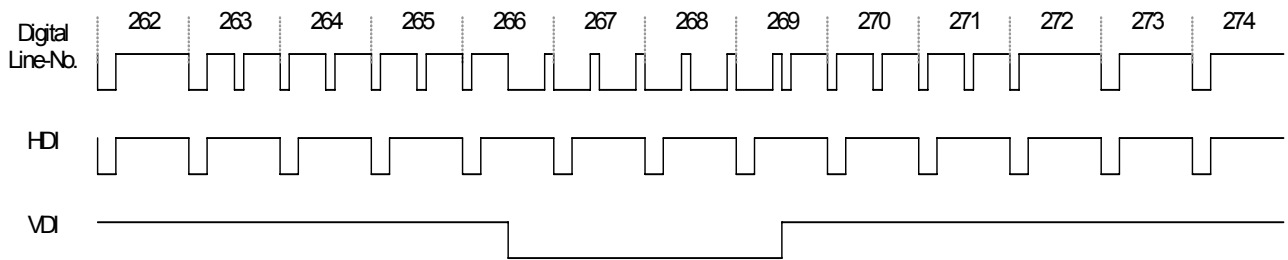


Fig. 158 2nd Field

625 Line System

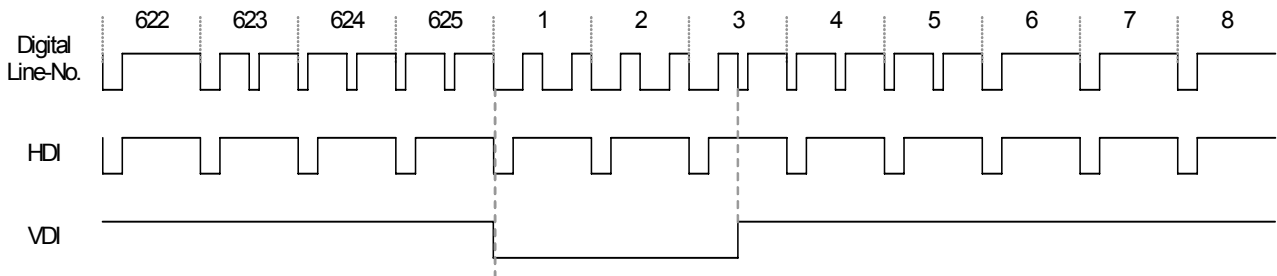


Fig. 159 1st Field

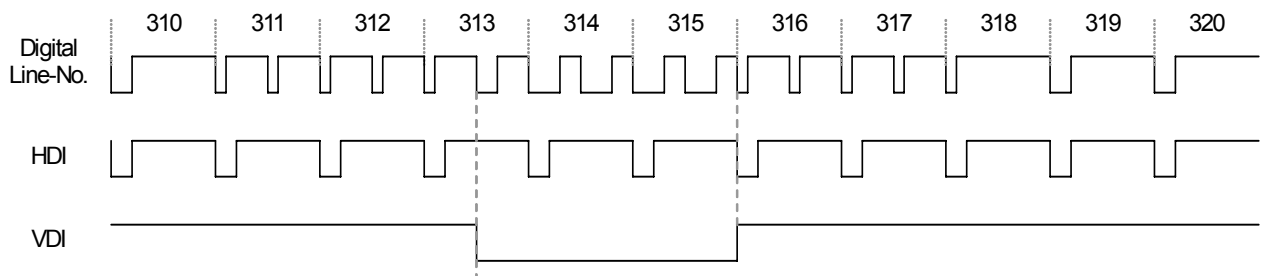


Fig. 160 2nd Field

■ SYNC Signal Waveform, Burst Waveform (SD)

(1-1) NTSC / NTSC-4.43 / PAL-M(SD Block Control Register [SDVM3:SDVM2]-bit = 00 / 01 の場合) (SMPTE-170M)

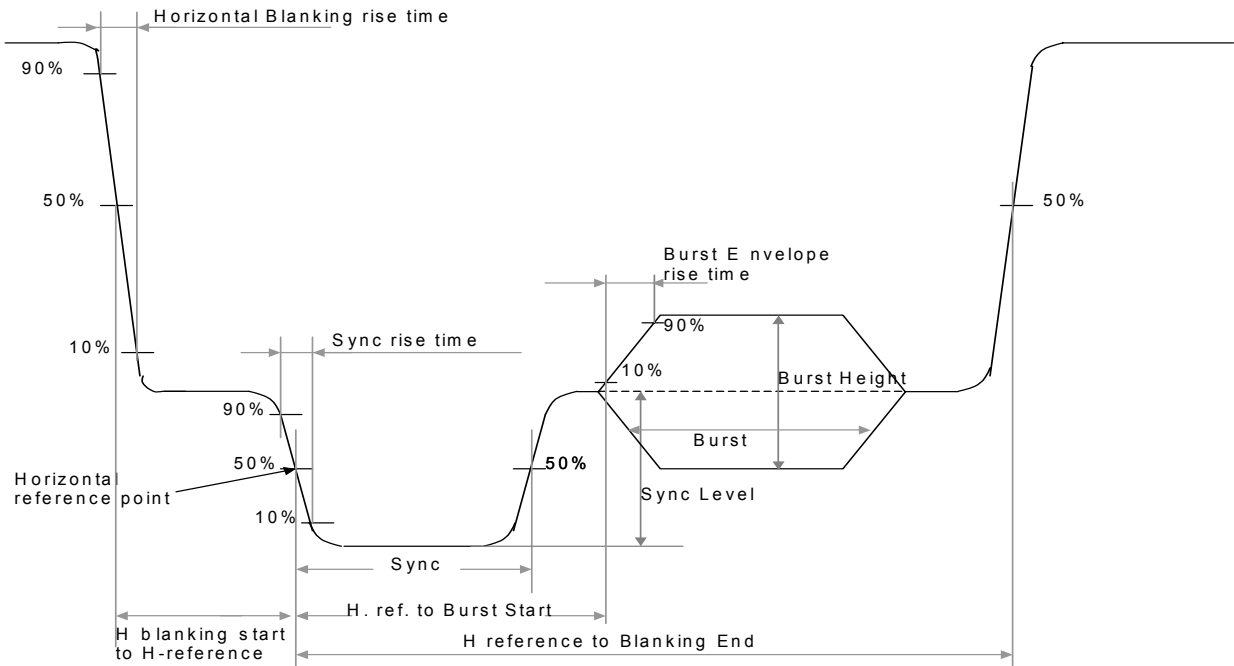


Fig. 161

measurement	point	value	Recommended tolerance	units
Total line period(derived)		63.556		usec
Sync Level		40	+/- 1	IRE
Horizontal Blanking rise time	10% - 90%	140	+/- 20	nsec
Sync rise time	10% - 90%	140	+/- 20	nsec
Burst envelope rise time	10% - 90%	300	+200 -100	nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.1	usec
Horizontal Sync	50%	4.7	+/- 0.1	usec
Horizontal reference point to burst start	50%	19	defined by SC/H	cycles
H reference to H-blanking end	50%	9.2	+ 0.2 - 0.1	usec
Burst * 50%		9	+/- 1	cycles
Burst Height **		40	+/- 1	IRE

* measurement of Burst Timing Length is made bet ween the Burst Start Point which is defined as the zero-cross point, preceding the first-half cycle of the sub-carrier where Burst Amplitude becomes higher than 50 % level and the Burst End Point, defined in the same manner.

Burst Time Length (period) is 10 cycles in NTSC-4.43 mode.

** Burst Height of PAL-M mode is 306 mV.

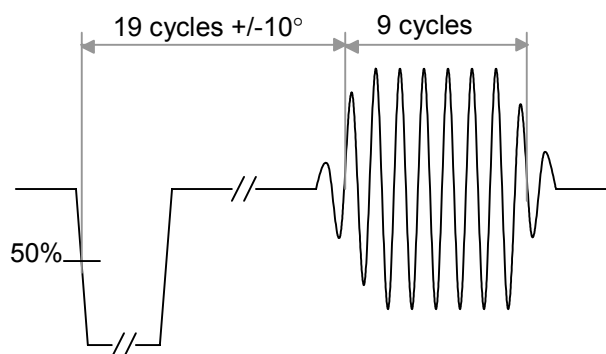


Fig. 162 NTSC Color Burst

(1-2-1) Vertical SYNC Signal Timing (NTSC/NTSC4.43)

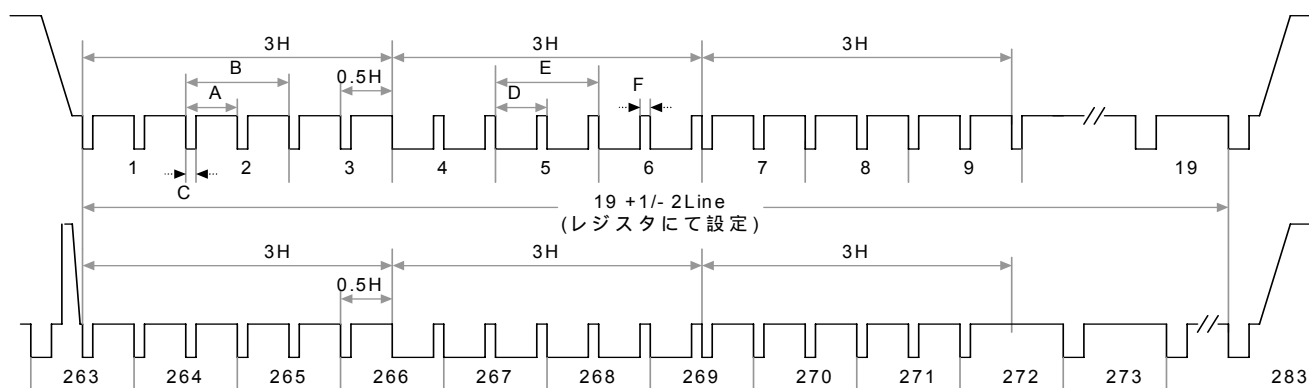


Fig. 163

Symbol	Duration	Measurement point	Reference
A	429T	50% 13.	5MHz Clock
B	858T		
C	31T		
D	429T		
E	858T		
F	63T		

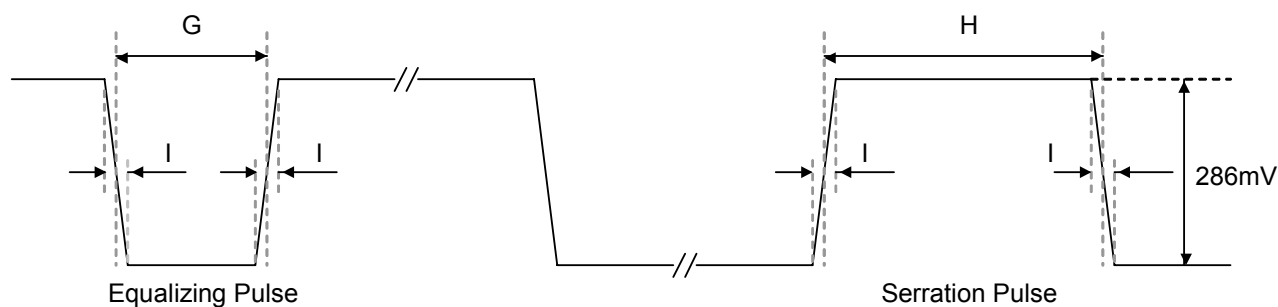
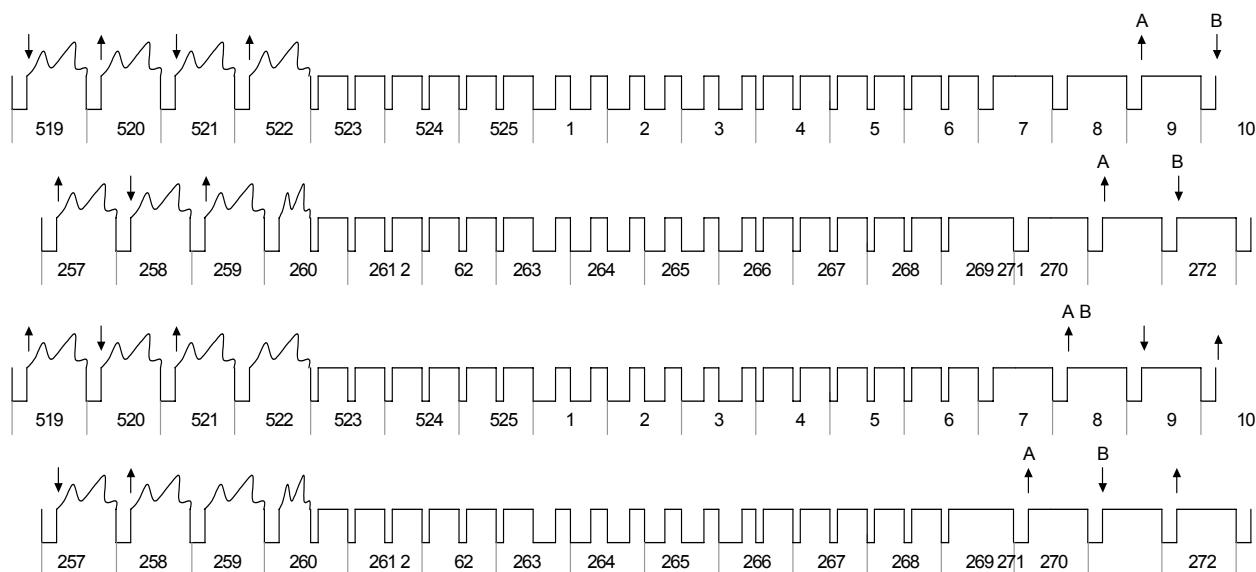


Fig. 164 Equalizing Pulse and Serration Pulse

Symbol	Measurement	point	Value	Recommended tolerance	units
	Field Period (derived)		16.6833		msec
	Frame period (derived)		33.3667		msec
	Vertical blanking start before first equalizing pulse	50% 1.	5	+/- 0.1	usec
	Vertical blanking (63.556usec x 20lines + 1.5usec)		19* lines + 1.5 usec	0 +/- 0.1	lines usec
	Pre-equalizing duration		3		lines
G	Pre-equalizing pulse width	50%	2.3	+/- 0.1	usec
	Vertical sync duration		3		lines
H	Vertical serration pulse width	50%	4.7	+/- 0.1	usec
	Post-equalizing duration		3		lines
G	Post-equalizing pulse width	50%	2.3	+/- 0.1	usec
I	Sync rise time		140	+/- 20	nsec

* There is a case with V-Blank of 20 Lines. This value is pre-settable by register.

(1-2-2) Vertical SYNC Signal Timing and Burst Phase (PAL-M)

**Fig. 165**

A: Phase of Burst: nominal Value + 135°

B: Phase of Burst : nominal Value - 135°

(2-1) PAL-B,D,G,H,I,N / PAL-60 (SD Block Control Register[SDVM3:SDVM2]-bit = 11)

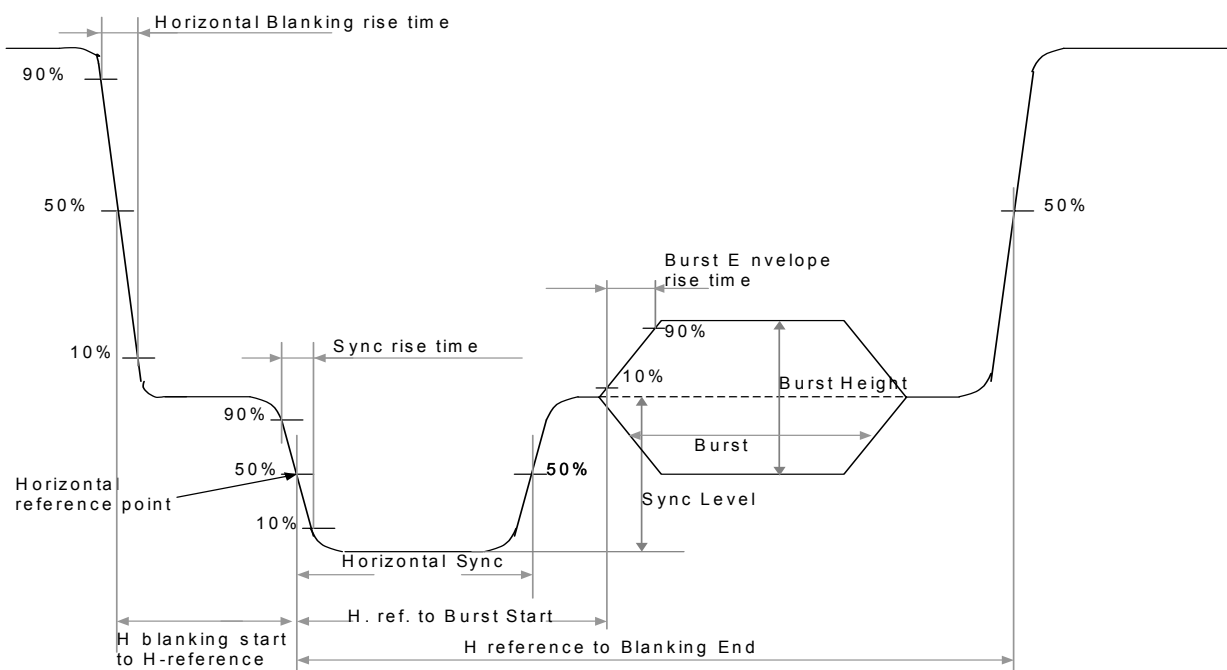


Fig. 166

measurement	point	value	Recommended tolerance	units
Total line period(derived)		64.0		usec
Sync Level		300		mV
Horizontal Blanking rise time	10% - 90%	0.3	+/- 0.1	usec
Sync rise time	10% - 90%	0.2	+/- 0.1	usec
Burst envelope rise time	10% - 90%			nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.3	usec
Horizontal Sync	50%	4.7	+/- 0.2	usec
Horizontal ref erence point t o burst start	50%	19	defined by SC/H	cycles
H reference to H-blanking end	50%	10.5		usec
Burst * 50%		10	+/- 1	cycles
Burst Height **		300		mV

(2-2) Vertical SYNC Signal Timing and Burst Phase

PAL-B,D,G,H,I,N / PAL-60 (SD Block Control Register [SDVM3:SDVM2]-bit = 11)

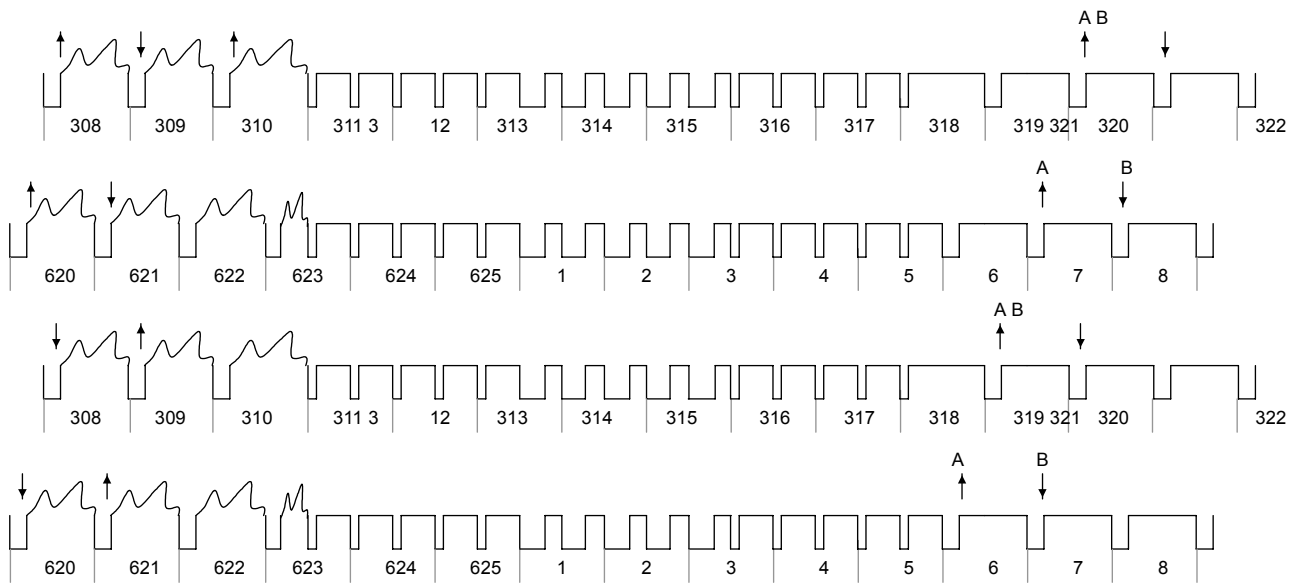


Fig. 167

A: Phase of Burst: nominal Value + 135°

B: Phase of Burst: nominal Value - 135°

■ Video ID

The AK8826 supports to encode the Video ID (EIAJ CPR-1204) which distinguishes the Aspect Ratio etc...

This is also used as CGMS (Copy Generation Management System).

Turning "ON / OFF" of this function is controlled by SDVBI-D-bit of **SD/HD V-Blanking Control Register (R/W) [Sub Address 0x12]** and setting data is set by **SD VBI-D-A Data1/Data2 Register (0x2A, 0x2B)**.

As for the Video ID setting for component Video Encoder mode is described in another section.

VBID Data Up-date Timing

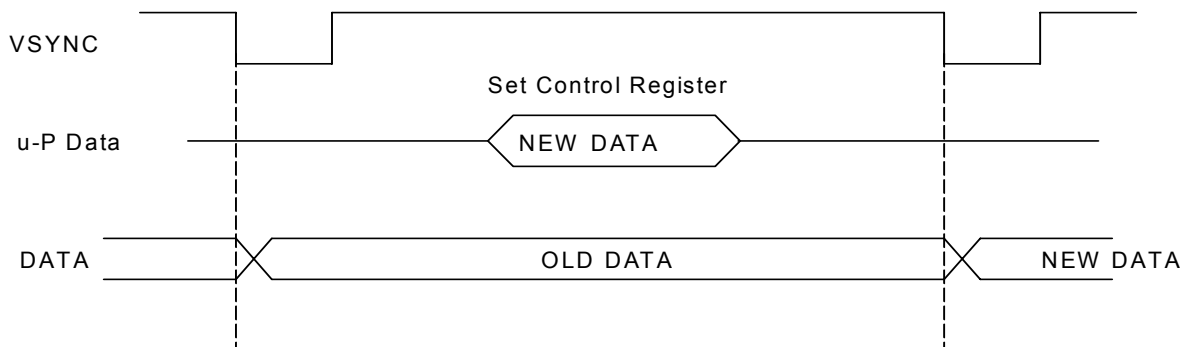


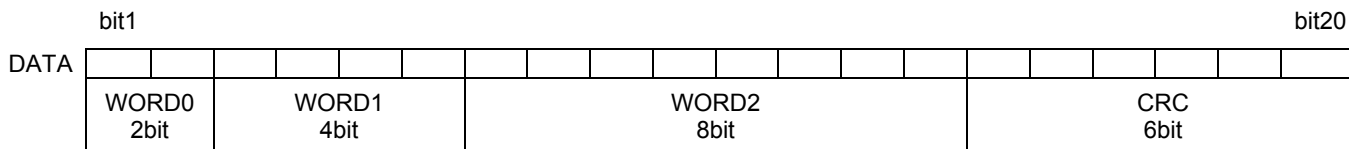
Fig. 168

VBID Data Code Assignment

20 bit data is configured with Word0 = 2 bits, Word1 = 4 bits, Word2 = 8 bits, CRC = 6 bits.

CRC is automatically calculated and added in the AK8826.

Default values of "CRC Polynomial Expression $X^6 + X + 1$ " are all ones.



VBID Waveform

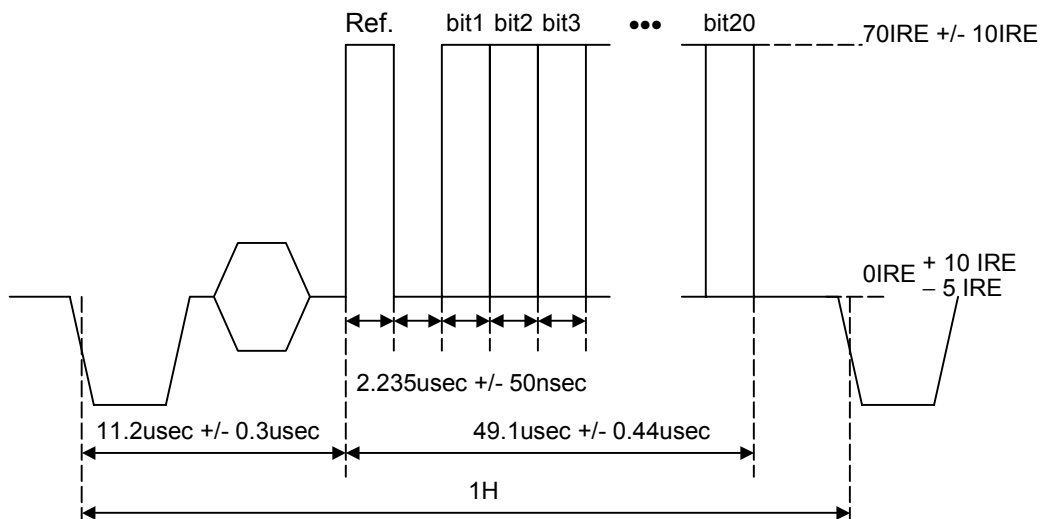


Fig. 169

525/	60 System
amplitude	70IRE
encode line	20/283

- Closed Caption

The description about “Closed Caption” is written in [6. Common Function Specification].

- WSS

The description about “WSS” is written in [6. Common Function Specification].

9. High Speed Video DAC mode

■ Block Diagram

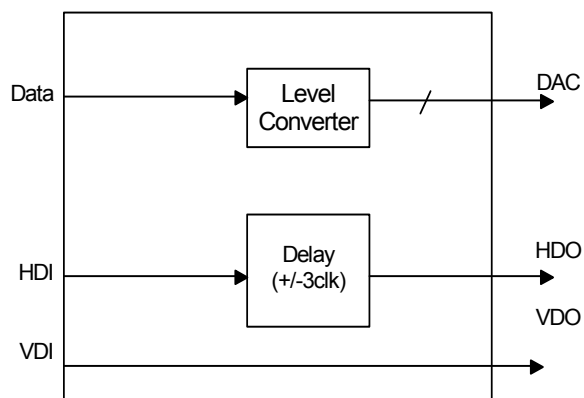


Fig. 170 High Speed Video DAC mode

■ Input Data Format

Input Data	Output	Operation
RGB565	Analog RGB	Digital RGB Data is converted to Analog RGB signal by DAC
RGB666	Analog RGB	Digital RGB Data is converted to Analog RGB signal by DAC

■ Full-Scale Code and Level Conversion

Input data is expanded to 10-bit, then it is converted to analog signal with DAC.
Full-Scale code is shown as following table.

RGB565		RGB666	
Full-Scale Code	R=0x3E0 G=0x3F0 B=0x3E0	R=0x3F0 G=0x3F0 B=0x3F0	

The DAC output Level at Full-Scale Code can be set with OLVL-bit of **DAC Control Register [SubAddress 0x0D]**.

DAC Control Register

Sub Address 0x0D

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	OLVL	DTRSTN	CVBSSEL	DAC3EN	DAC2EN	DAC1EN

OLVL-bit	Output Level [V]
0 1.	28V (typ)
1 0.	7V (typ)

■ Delay Function for Input Timing Signal

Input Timing Signal can be delayed by setting Register. Amount of adjustment is +/- 3-clock.
Delay adjustment is controlled by **Video DAC Delay Control Register [SubAddress0x51]**.

Video DAC Delay Control Register

Sub Address 0x51

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	HDLY2	HDLY1	HDLY0

Amount of Delay is set with 2's Complement.

HDLY[2:0]-bit	Delay
000	Delay 0
001 1CLK	Delay
010 2CLK	Delay
011 3CLK	Delay
111 1CLK	Advanced
110 2CLK	Advanced
101 3CLK	Advanced

10. AK8826 Register Definition

■ Register Map

Sub-Address	Register	Default	R/W	Function
0x00	HD Mode Register	0x00	R/W	Component Video Encoder Setting
0x01	HD VBI & Clip Level Control Register	0x04	R/W	Setting for VBI Intervale & Clip
0x02	HDYPBPR Delay Control Register	0x00	R/W	Delay Adjustment for Component Video Block
0x03	HD VBID Data 1 Register	0x00	R/W	VBID Data Setting Reigster
0x04	HD VBID Data 2 Register	0x00	R/W	
0x05	Reserved Register	0x00	R/W	
0x06	Powerdown Mode Register	0x00	R/W	Setting for Power Down
0x07	HD Block Control Register	0x00	R/W	
0x08	HD WSS Data 1 Register	0x00	R/W	WSS Data Register for Component Video Encoder
0x09	HD WSS Data 2 Register	0x00	R/W	
0x0A	HD Block Miscellaneous Control Register	0x00	R/W	Control Register for Component Video Encoder
0x0B	I/O Data Format Register	0x00	R/W	Setting I/O Data format
0x0C	I/O Pin Control Register	0x00	R/W	Setting I/O Pin configuration
0x0D	DAC Control Register	0x00	R/W	Control DAC
0x10	SD Blanking Set Register	0xA1	R/W	Setting VBI Interval for Composite Video Encoder
0x11	SD Block Control Register	0x10	R/W	Control Regsiter for Composite Video Encoder mode
0x12	SD/HD V-Blanking Control Register	0x00	R/W	Setting VBI Interval signal
0x13	SD Block Delay Register	0x00	R/W	Delay Control Register for Composite Video Encoder
0x14	SD Block FLT Register	0x00	R/W	Setting Luminance Filter
0x15	Reserve Register	0x00	R/W	
0x16	Sub Carrier Frequency Control Register	0x00	R/W	Adjust Subcarrier Frequency
0x17	Sub Carrier Phase Control Register	0x00	R/W	Adjust Subcarrier Phase.
0x18	SD WSS Data 1 Register	0x00	R/W	WSS Data Register for WSS
0x19	SD WSS Data 2 Register	0x00	R/W	
0x1A	Reserved	0x0F	R/W	Reserved Register
0x1B	Reserved	0xFC	R/W	
0x1C	Reserved	0x20	R/W	
0x1D	Reserved	0xD0	R/W	
0x1E	Reserved	0x6F	R/W	
0x1F	Reserved	0x0F	R/W	
0x20	Reserved	0x00	R/W	
0x21	Reserved	0x00	R/W	
0x22	Reserved	0x0C	R/W	
0x23	Reserved	0xF3	R/W	
0x24	Reserved	0x09	R/W	
0x25		0x00	R/W	
0x26	Closed Caption Data 1 Register	0x00	R/W	Closed Caption Data Set -Register f or Composite Video Encoder Block
0x27	Closed Caption Data 2 Register	0x00	R/W	
0x28	CC Extended Data 1 Register	0x00	R/W	Closed Caption Extended Data Set -Register f or Composite Video Encoder block
0x29	CC Extended Data 2 Register	0x00	R/W	
0x2A	SD VBID-A Data1 Register	0x00	R/W	VBID Data Set -Register f or Composite Video Encoder Block
0x2B	SD VBID-A Data2 Register	0x00	R/W	
0x2C				
0x2D	Reserved	0xE3	R/W	Reserved Register
0x2E	Reserved	0xBD	R/W	
0x2F	Reserved	0x66	R/W	
0x30	Reserved	0xB5	R/W	
0x31	Reserved	0x90	R/W	
0x32	Reserved	0xB2	R/W	
0x33	Reserved	0x7D	R/W	
0x34	Status Register	0x00	R	Status Register
0x35	Device ID & Revision ID Register	0x25	R	Device ID and Revision ID Register

0x38	TEST Register 1	0x00	R/W	Test Register
0x39	TEST Register 2	0x00	R/W	Test Register
0x3A	TEST Register 3	0x00	R/W	Test Register
0x3B	TEST Register 4	0x00	R/W	Test Register
0x3C	TEST Register 5	0x00	R/W	Test Register
0x3D	TEST Register 6	0x00	R/W	Test Register
0x3E	TEST Register 7	0x00	R/W	Test Register
0x3F	TEST Register 8	0x00	R/W	Test Register
0x40	VBID-B Header Data Register	0x08	R/W	Setting VBID Header
0x41	VBID-B Version Number Register	0x00	R/W	Setting VBID Version Number
0x42	VBID-B Payload Packet Length Register	0x00	R/W	Setting VBID Packet Length
0x43	VBID-B Payload Data1 Register	0x00	R/W	Setting VIBD Payload Data
0x44	VBID-B Payload Data2 Register	0x00	R/W	Setting VIBD Payload Data
0x45	VBID-B Payload Data3 Register	0x00	R/W	Setting VIBD Payload Data
0x46	VBID-B Payload Data4 Register	0x00	R/W	Setting VIBD Payload Data
0x47	VBID-B Payload Data5 Register	0x00	R/W	Setting VIBD Payload Data
0x48	VBID-B Payload Data6 Register	0x00	R/W	Setting VIBD Payload Data
0x49	VBID-B Payload Data7 Register	0x00	R/W	Setting VIBD Payload Data
0x4A	VBID-B Payload Data8 Register	0x00	R/W	Setting VIBD Payload Data
0x4B	VBID-B Payload Data9 Register	0x00	R/W	Setting VIBD Payload Data
0x4C	VBID-B Payload Data10 Register	0x00	R/W	Setting VIBD Payload Data
0x4D	VBID-B Payload Data11 Register	0x00	R/W	Setting VIBD Payload Data
0x4E	VBID-B Payload Data12 Register	0x00	R/W	Setting VIBD Payload Data
0x4F	VBID-B Payload Data13 Register	0x00	R/W	Setting VIBD Payload Data
0x50	VBID-B Payload Data14 Register	0x00	R/W	Setting VIBD Payload Data
0x51	Video DAC Delay Control Register	0x00	R/W	Delay control Register for High Speed DAC mode

* Write default values (0x00) to TEST Register(TEST Register 1 to TEST Register 8), if it is necessary to access these registers.

HD Mode Register (R/W) [Sub Address 0x00]

[Component Video Encoder]

Register to set the AK8826 mode at Component Video Encoder mode

Sub Address 0x00

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCBG	HDBBG	HDSETUP	HDEAVDEC	HDCEA861	HDMODE1	HDMODE0	HDRFRSH
Default Value							
0 0		0 0		0 0		0	0

HD Mode Register (R/W) [Sub Address 0x00]

BIT	Register Name		R/W	Definition
bit 0	HDRFRSH	Refresh Rate bit	R/W	to select refresh rate 0 : 60Hz 1 : 50Hz
bit1 ~ bit2	HDMODE0 ~ HDMODE1	Mode Set bit	R/W	to select input / output signals [HDMODE1:HDMODE0] 00 : 525i/625i 01 : 525p/625p 10 : 1080i 11 : 720p
bit3	HDCEA861	H/V timing std bit	R/W	to appoint relation when to synchronize with HSYNC / VSYNC 0: Data capture is done by the AK8826 timing. 1: it is done by the compatible timing specified in CEA 861B. When EAVDEC: 1, this bit is ignored.
bit 4	HDEAVDEC	EAV Decode bit	R/W	to select the AK8826 Sync mode 0 : to be synchronized with HSYNC / VSYNC signals 1 : to be synchronized with EAV
bit 5	HDSETUP	HD Setup-bit	R/W	to set on / off of 7.5 % set-up 0: no set-up process is done. 1: set-up process is done.
bit 6	HDBBG	HD Black Burst bit	R/W	to output Black Burst Signal (SYNC Signal Output only) 0 : normal output 1: Black Burst Signal Output is enabled.
bit 7	HDCBG	HD Color Bar bit	R/W	to output Color Bar Signal 0 : normal output 1: Color Bar Signal is output. When HDBB bit is set, HDBB is prioritized.

HD VBI & Clip Level Control Register (R/W) [Sub Address 0x01] [Component Video Encoder]

VBI, Clipping level of output is set.

Sub Address 0x01

default Value 0x04

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCLPLVL1	HDCLPLVL0	Reserved	Reserved	Reserved	HDVUNMSK	HDVL1	HDVL0
Default Value							
0	0	0	0	0	1	0	0

HD VBI & Clip Level Control Register (R/W) [Sub Address 0x01]

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	HDVL0 ~ HDVL1	HD VB Setting	R/W	Adjust VBI blanking lines. Final lines of the blanking period are adjusted. Values are relative number of the default line (line 20). [HDVL1:HDVL0]-bit 01: increased by 1 line 00: default 11: decreased by 1 line. 10: decreased by 2 lines.
bit 2	HDVUNMSK	V-Blank Unmask bit	R/W	Sets the masking action during V-Blanking periods. 0 : during V-Blanking outputs are masked. (Black is outputs) 1: normal operation. (Input data is output during V-Blanking periods.) Following lines are in the interest. 525i : 10 - 20(+/-VL[1:0]) and 273- 283(+/-VL[1:0]) Line 525P : 13 - 42(+/-VL[1:0]) Line 1080i : 7 - 20(+/-VL[1:0]) line and 569 - 583(+/-VL[1:0]) line 720P : 6 - 24(+/-VL[1:0]) line
bit 3 ~ bit 5	Reserved	Reserved bit	R/W	Reserved, write 0x00
bit 6 ~ bit 7	HDCLPLVL0 ~ HDCLPLVL1	HD Clamp Level bit	R/W	Define clipping level of the over sampling filter. [HDCLPLVL1:HDCLPLVL0] = 00: no clipping 01: clips at about -7.0 IRE below pedestal level. 10: clips at about -1.5 IRE below pedestal level. 11: Reserved

HDYPBPR Delay Control Register (R/W) [Sub Address 0x02] [Component Video Encoder]

Delay amounts of Y signal and Pb / Pr signals are set.

Sub Address 0x02

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved PBPRDLY2	PBPRDLY1	PBPRDLY0	Reserved	HDYDELAY2	HDYDEALY1	HDYDELAY0	
Default Value							
0 0		0 0		0	0	0	0

HDYPBPR Delay Control Register (R/W) [Sub Address 0x02]

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	HDYDELAY0 ~ HDYDELAY2	HDY Delay Set bits	R/W	Luminance signal delay amount is set . It is a delay from SYNC signal. Delay amount is set based on 27 MHz clock in 480i / p modes, and 74.25 MHz in 1080i / 720p modes. [HDYDELAY2 : YDELAY1] - bit 000 : delay amount 0 001: 1 CLK time is delayed. 010: 2 CLK time is delayed. 011: 3 CLK time is delayed. 111: advance 1 CLK time to output. 110: advance 2 CLK time to output. 101: advance 3 CLK time to output. 100 : reserved
bit 3	Reserved	Reserved bit	R/W	Reserved, write "0 ".
bit 4 ~ bit 6	PBPRDLY0 ~ PBPRDLY2	C Delay Set bits	R/W	Chroma signal delay amount is set . It is a delay from Luminance signal. Delay amount is set, based on 27 MHz clock in 480i/p modes, and 74.25 MHz in 1080i / 720p modes. Both Pb / Pr are delay ed by same amount by Delay Amount setting. [PBPRDLY2 : PBPRDLY0] – bit 000: delay amount 0 001: 1 CLK time is delayed. 010: 2 CLK time is delayed. 011: 3 CLK time is delayed. 111: advance 1 CLK time to output. 110: advance 2 CLK time to output. 101: advance 3 CLK time to output. 100: reserved
bit 7	Reserved	Reserved bit	R/W	Reserved, write "0 ".

HD VBID Data 1 Register (R/W) [Address 0x03]**HD VBID Data 2 Register (R/W) [Address 0x04]**

[Component Video Encoder]

Registers to set CGMS-A Data

CGMS-A Data is set. CRCC Data is automatically generated and added.

Address 0x03**Default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDVBIDEN	Reserved	HDVBID1	HDVBID2	HDVBID3	HDVBID4	HDVBID5	HDVBID6
Default Value							
0	0	0 0 0			0	0	0

Address 0x04**Default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDVBID7	HDVBID8	HDVBID9	HDVBID10	HDVBID11	HDVBID12	HDVBID13	HDVBID14
Default Value							
0	0 0		0 0 0			0	0

HD VBID Data 1 Register (R/W) [Address 0x03]

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	HDVBID6 ~ HDVBID1	VBID DATA bit	R/W	VBID (CGMS-A) Data is set. Data to be set are CGMS1 ~ CGMS6. CGMS7 ~ CGMS14 should be set at CGMS Data 2 Register.
bit 6	Reserved	Reserved bit	R/W	Reserve, write "0".
bit 7	HDVBIDEN	VBID Enable bit	R/W	This bit is set when VBI D (CGMS-A) signal is to be super-imposed. Target Line to be super-imposed with, is automatically decided by setting [HDMODE1 : HDMODE0]-bits for HDMODE Register. 0: CGMS-A function is "OFF". 1: CGMS-A signal is super-imposed.

HD VBID Data 2 Register (R/W) [Address 0x04]

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	HDVBID14 ~ HDVBID7	VBID Data bit	R/W	VBID (CGMS-A) Data is set. Data to be set are CGMS7 ~ CGMS14. CGMS1 ~ CGMS6 should be set at CGMS Data 1 Register.

- About Outputting CGMS Data

Write Operation of CGMS Data via I2C interface must be completed by the time when the preceding 2 Lines are completed, from a target output Line.

Each Line starts at EAV.

Reserved Register (R/W) [Sub Address 0x05]

Reserve Register

Sub Address 0x05
Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0 0		0 0		0	0	0	0

Reserved Register (R/W) [Sub Address 0x05]

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	Reserved	Reserved bit	R/W	Reserve, write "0x00 ".

Powerdown Mode Register (R/W) [Sub Address 0x06] [Common Register for all Function block]

to set Power-Down and Operation modes of the AK8826.

Sub Address 0x06

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	PLLPDN	SLPEN1	SLPEN0
Default Value							
0 0		0 0		0 0		0	0

BITS	Register Name		R/W	Definition
bit 0 ~ bit 1	SLPEN0 ~ SLPEN1	Sleep Enable bit	R/W	to control operation of SD / HD blocks (digital portion) [SLPEN1 : SLPEN0]-bit 00: both SD /HD blocks are enabled. 01: HD block only is enabled. 10: SD block only is enabled. 11: entire device is put into Power-Down mode.
bit 2	PLLPDN	PLL Power Down bit	R/W	to control Power-Down of PLL 0 : Power Down 1 : release from Power-Down
bit 3 ~ bit 6	Reserved	Reserved bit	R/W	Reserved, write "0 ".

HD Block Control Register (R/W) [Sub Address 0x07]

[Component Video Encoder]

to set miscellaneous function to register

Sub Address 0x07**default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDWSS	HDCFLT1	HDCFLT0	HDYFLT1	HDYFLT0	Reserved	COLSNCEN	HDVRATIO
Default Value							
0	0	0	0	0	0	0	0

HD Block Control Register

BIT	Register Name		R/W	Definition
bit 0	HDVRATIO	Video ratio bit	R/W	286 / 714 Ratio Video Signal is output at D1 / 60Hz operation. 0 : 300 / 700 Ratio Video Signal is output (770.2-A) 1 : 286 / 714 Ratio Video Signal is output (770.1-A)
bit 1	COLSNCEN	Color SYNC Enable bit	R/W	to add sync signal on Pb/Pr signal. 0: No sync on Pb/Pr signal 1: Sync on Pb/Pr signal
bit 2	Reserved	Reserved-bit	R/W	Reserved, write "0".
bit3 ~ bit4	HDYFLT0 ~ HDYFLT1	HDY Filter select	R/W	to select HDY Video Signal Band Limit Filter [HDYFLT 1: HDYFLT 0] = 00 : Normal 01 : Mild 10 : Soft 11 : Normal
bit5 ~ bit6	HDCFLT0 ~ HDCFLT1	HDPBPR Filter select	R/W	to select HDPB / HDPR Video Signal Band Limit Filter [HDCFLT 1: HDCFLT 0] = 00 : Normal 01 : Mild 10 : Soft 11 : Normal
bit 7	HDWSS	WSS set bit	R/W	to encode WSS signal It is turned on only when D1/50Hz is Output 0 : WSS off 1 : WSS on

HD WSS Data 1 Register (R/W) [Sub Address 0x08]
HD WSS Data 2 Register (R/W) [Sub Address 0x09]

[Component Video Encoder]

Register to set WSS Data

Sub Address 0x08 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDG2-7 HDG2-6	HDG2-5 HDG2-4	HDG1-3 HDG1-2	HDG1-1	HDG1-0			
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x09 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	HDG4-13	HDG4-12	HDG4-11	HDG3-10	HDG3-9	HDG3-8
Default Value							
0	0	0	0	0	0	0	0

Note) WSS Data is written in order of 0x08 and then 0x09.

When the second byte (0x09) of WSS Data is written, the AK8826 interprets that data has been up-dated and it encodes the WSS signal on the next Video Line (Line23).

Data is retained till it is up-dated with a new one.

HD Block Miscellaneous Control Register (R/W) [Sub Address 0x0A] [Component Video Encoder]

to set miscellaneous function to register

Sub Address 0x0A

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	STD770_2C	HDCEA805B	CCWSSSUE	Reserved	HDAFLT1	HDAFLT0
Default Value							
0 0		0 0		0 0		0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	HDAFLT0 ~ HDAFLT1	HD Aperture Filter Set bit	R/W	to set aperture compensation filter [AFLT1:AFLT0] 00: Mode0 : Less compensation (default) 01: Mode1 10: Mode2 11: Mode3 : much compensation
bit 2	Reserved	Reserved	R/W	Reserved, write "0 ".
bit 3	CCWSSSUE	CC, WSS, Setup Enable bit	R/W	to set the Set-up on the CC/WSS line. 0: no Set-up on CC/WSS line. 1: 7.5% Set-up is added on CC/WSS line
bit 4	HDCEA805B	CEA 805B Encode bit	R/W	to Encode CEA805B TypeB data 0: no encoding TypeB data 1: encoding TypeB data
bit 5	STD770_2C	CEA 770.2-C bit	R/W	to adapt CEA770.2-C standard 0: to adapt CEA770.2.A standard 1: to adapt CEA770.2.C standard
bit 6 ~ bit 7	Reserved	Reserved	R/W	Reserved, write "0 ".

I/O Data Format Register (R/W) [Sub Address 0x0B]

[Common Register for all Function block]

to set input / output configuration

Sub Address 0x0B**default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDSDMASE	YC2RGB	Reserved	DTFMT	CONVMOD1	CONVMOD0	INPFMT1	INPFMT0
Default Value							
0	0	0	0	0	0	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	INPFMT0 ~ INPFMT1	Input Data Format bit	R/W	to set input data bit width format [INPFMT1: INPFMT0] 00: 8bit data input 01: 16bit data input 10: 18bit data input 11: prohibited to set
bit 2 ~ bit 3	CONVMOD0 ~ CONVMOD1	Convert Module Select bit	R/W	to select encoding block CONVMOD[1:0]= 00: to select Composite Video Encoder Block Component Video Encoder Block becomes sleep mode automatically. 01: to select Component Video Encoder Block Composite Video Encoder Block becomes sleep mode automatically. 10: to select High Speed DAC Block Composite Video Encoder Block and Component Video Encoder Block becomes sleep mode automatically. 11: Prohibited to set
bit 4	DTFMT	Data Format bit	R/W	to set Input data format 0: YCbCr data 1: RGB data
bit 5	Reserved	Reserved bit	R/W	Reserved, write "0".
bit 6	YC2RGB	YCbCr to RGB bit	R/W	to set YCbCr to RGB data conversion This mode only work at CONVMOD[1:0]=01. 0: no conversion 1: YCbCr to RGB conversion is worked
bit 7	HDSDMASE	HD/SD Master mode Enable bit	R/W	to set self-sync mode* in case of HDBBG-bit / HDCBG-bit / SDBBG-bit / SDCBG-bit is set. self-sync mode: working without HD/VD and EAV timing signal 0: no self-sync mode. 1: self-sync mode

I/O Pin Control Register (R/W) [Sub Address 0x0C]

[Common Register for all Function block]

to set the attribute of I/O pins.

Sub Address 0x0C

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDOEN	HDOEN	VDI_INV	HDI_INV	Reserved	VDOPOL	HDOPOL	CLKINV
Default Value							
0 0		0 0		0 0		0	0

BIT	Register Name		R/W	Definition
bit 0	CLKINV	Clock Invert -bit	R/W	to set polarity of Clock for CLKIN pin 0: Capturing the data at the rising edge of clock 1: Capturing the data at the falling edge of clock
bit 1	HDOPOL	HDO Polarity bit	R/W	to set polarity of HDO 0: Same polarity as Input data. 1: Inverted polarity as Input data
bit 2	VDOPOL	VDO Polarity bit	R/W	to set polarity of VDO 0: Same polarity as Input data. 1: Inverted polarity as Input data
bit 3	Reserved	Reserved	R/W	Reserved, write "0".
bit 4	HDI_INV	HD polarity select	R/W	to set polarity of HDI 0 : Active Lo 1 : Active High
bit 5	VDI_INV	VD polarity select	R/W	to set polarity of VDI 0 : Active Lo 1 : Active High
bit 6	HDOEN	HDO Output Enable bit	R/W	to control HDO 0: Disable to output the timing signal from HDO 1: Enable to output the timing signal from HDO
bit 7	VDOEN	VDO Output Enable bit	R/W	to control VDO 0: Disable to output the timing signal from VDO 1: Enable to output the timing signal from VDO

DAC Control Register(R/W) [Sub Address 0x0D]

[Common Register for all Function block]

to set on / off of DACs

Sub Address 0x0D**default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	OLVL	DTRSTN	CVBSSEL	DAC3EN	DAC2EN	DAC1EN
Default Value							
0	0	0	0	0	0	0	0

BIT	Register Name		R/W	Definition
bit 0	DAC1EN	DAC1 Enable bit	R/W	to control DAC1 ON/OFF 0: OFF (Output pin is Hi-z States) 1: ON
bit 1	DAC2EN	DAC2 Enable bit	R/W	to control DAC2 ON/OFF 0: OFF (Output pin is Hi-z States) 1: ON
bit 2	DAC3EN	DAC3 Enable bit	R/W	to control DAC3 ON/OFF 0: OFF (Output pin is Hi-z States) 1: ON
bit 3	CVBSSEL	CVBS Select bit	R/W	to select the DAC for CVBS output 0: DAC3 outputs CVBS 1: DAC1 outputs CVBS
bit 4	DTRSTN	Data Clear bit	R/W	to Reset all block 0: Initialize the circuit 1: to release initialized states
bit 5	OLVL	Output Level bit	R/W	to control DAC output Level This bit is valid at High Speed DAC mode. 0: to output about 1.28V at 0xFF code. 1: to output about 0.7V at 0xFF code.
bit 6 ~ bit 7	Reserved	Reserved bit	R/W	Reserved, write "0 ".

SD Blanking Set Register (R/W) [Sub Address 0x10]

[Composite Video Encoder Block]

to set AK8826 Interface mode and V-Blanking Length at composite Video Encoder mode.

Sub Address 0x10

Default Value 0xA1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBLN4	SDBLN3	SDBLN2	SDBLN1	SDBLN0	Reserved	Reserved	REC656
Default Value							
1 0		1 0		0 0		0	1

BIT	Register Name		R/W	Definition
bit 0	REC656	REC 656 bit	R/W	set this bit when to synchronize with ITU-R. BT.656 (compatible) EAV. 0 : EVA is not decoded (in case of synchronization with HSYNC / VSYNC) 1: EVA is decoded and the timing is synchronized with it.
bit 1 ~ bit 2	Reserved	Reserved bit	R/W	Reserved, write "0 ".
bit 3 ~ bit 7	SDBLN0 ~ SDBLN4	SD Blanking Line No.	R/W	to set Line Blanking output.

SD Block Control Register (R/W) [Sub Address 0x11]

[Composite Video Encoder Block]

to set Output signals

Sub Address 0x11

Default Value 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG	SDCBG	SDSETUP	SCR	SDVM3	SDVM2	SDVM1	SDVM0
Default Value							
0	0	0	1	0	0	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	SDVM0 ~ SDVM3	Video Mode 0 Register ~ Video Mode 3 Register	R/W	[SDVM1 : SDVM0] – bit 00 : 3.57954545 MHz 01 : 3.57561188 MHz 10 : 3.5820558 MHz 11 : 4.43361875 MHz [SDVM3 : SDVM2] – bit 00 : 525 / 60 01: 525 / 60 PAL (PAL-M etc...) 10 : reserved 11 : 625 / 50 PAL (PAL-B, D, G, H, I, N)
bit 4	SCR	Sub Carrier Reset bit	R/W	to set enable / disable reset of Sub-carrier for each color sequence 0: no sub-carrier reset is done. 1: sub-carrier reset is enabled. NTSC: reset at every 2 Frames. PAL: reset at every 4 Frames.
bit 5	SDSETUP	SD Setup-bit	R/W	to set the Set-Up 0 : no set-up 1: 7.5 % set-up is added. Even when the set-up is turned on, set-up (Pedestal) is not added while Blanking Line is being output.
bit 6	SDCBG	SD Color Bar Generator Control bit	R/W	setting bit of On-Chip Color Bar 0: input data is encoded. 1: On-Chip Color Bar is output. When SDBBG bit is set, SDCBG is prioritized.
bit 7	SDBBG	SD Black Burst Generator Control bit	R/W	Black Burst Generator bit to output Black Burst signal 0: input data is encoded. 1: Black Burst signal is output. Even when SDCBG bit is set, SDBBG is prioritized.

SDVM3 – SDVM0 settings for each Standard are as follows.

SDVM3:SDVM0	
NTSC	0000
PAL-B,D,G,H,I	1111
PAL-M	0101
PAL-60	0111
NTSC-4.43	0011

SD/HD V-Blanking Control Register (R/W) [Sub Address 0x12] [Composite Video Encoder / Component Video Encoder Block]

to set V-Blanking Interval output Data

Sub Address 0x12

Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	SDWSS	SDHDCC284	SDHDCC21	SDVBID
Default Value							
0 0		0 0		0	0	0	0

BIT	Register Name		R/W	Definition
bit 0	SDVBID	SD Video ID bit	R/W	to set VBID data for Composite Video Encoder mode/ 0: VBID OFF 1: VBID ON
bit 1	SDHDCC21	Closed Caption bit	R/W	to make Closed Caption signal enable for Composite Video Encoder and Component Video Encoder mode. 0: OFF 1: ON
bit 2	SDHDCC284	Closed Caption Extended Data bit	R/W	to make Closed Caption Extended signal enable for Composite Video Encoder and Component Video Encoder mode. 0: OFF 1: ON
bit 3	SDWSS	WSS set bit	R/W	to make WSS enable for Composite Video Encoder. 0: OFF 1: ON
bit 4 ~ bit 7	Reserved	Reserved bit	R/W	Reserved, write "0".

SD Block Delay Register (R/W) [Sub Address 0x13] [Composite Video Encoder Block]

to adjust YC Delay amount of output signal

Sub Address 0x13

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDCLPLVL1	SDCLPLVL0	SYD2	SYD1	SYD0	Reserved	Reserved	Reserved
Default Value							
0 0		0 0		0 0		0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	Reserved	Reserved bit	R/W	Reserved, write "0 ".
bit 3 ~ bit 5	SYD0 ~ SYD2	S-video Y Delay bit	R/W	[[SYD2 : SYD0] – bit 101: Y component output advances 3 clock times to C component. 110: Y component output advances 2 clock times to C component. 111: Y component output advances 1 clock time to C component. 000 : no delay between Y component and C component 001 : Y component output is delayed by 1 clock time to C component. 010 : Y component output is delayed by 2 clock time to C component. 011 : Y component output is delayed by 3 clock time to C component.
bit 6 ~ bit 7	SDCLPLVL0 ~ SDCLPLVL1	SD Clip Level Set bit	R/W	to clip t he under-shoot of t he Over-Sampling Filter Outputs to a pre-set value. [SDCLPLVL1:SDCLPLVL1] 00: no clipping 01: to be clipped at approximately - 7.0IRE 10: to be clipped at approximately -1.5IRE 11: reserved

SD Block FLT Register (R/W) [Sub Address 0x14] [Composite Video Encoder Block]

to set Band Limit Filter.

Sub Address 0x14							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	SDYFLT1	SDYFLT0	Reserved	Reserved	Reserved
Default Value							
0 0		0 0		0 0		0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	Reserved	Reserved bit	R/W	Reserved, write "0 ".
bit 3 ~ bit 4	SDYFLT0 ~ SDYFLT1	SDY Filter Select bit	R/W	to set SDY Video Signal Band Limit Filter [SDYFLT1:SDYFLT0]= 00: Normal 01: Mild 10: soft 11: Inhibited
bit 5 ~ bit 7	Reserved	Reserved	R/W	Reserved, write "0 ".

Reserve Register (R/W) [Sub Address 0x15] [Composite Video Encoder]

Reserved Register

Sub Address 0x15							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0 0		0 0		0 0		0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	Reserved	Reserved bit	R/W	Reserved, write "0 ".

Sub Carrier Frequency Control Register (R/W) [Sub Address 0x16] [Composite Video Encoder]

to set subcarrier Frequency

Sub Address 0x16

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SUBF7	SUBF6	SUBF5	SUBF4	SUBF3	SUBF2	SUBF1	SUBF0
Default Value							
0	0	0	0	0	0	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SUBF0 ~ SUBF7	Sub Carrier Frequency control bit	R/W	to fine-tune the sub-carrier Frequency adjustment can be done, ranging from + 127 to _ 128 and adjustable step is in 0.8 Hz / step.

Sub Carrier Phase Control Register (R/W) [Sub Address 0x17] [Composite Video Encoder]

to set subcarrier Phase

Sub Address 0x17							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SUBP7 SUBP6	SUBP5 SUBP4	SUBP3 SUBP2	SUBP1	SUBP0			
Default Value							
0 0		0 0		0 0		0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SUBP0 ~ SUBP7	Sub Carrier Phase control bit	R/W	bit 0 ~ bit 7 Sub-Carrier Phase Control bits to set default value of sub-carrier phase Adjustable step: 360 / 255 [deg.] Sub-Carrier Phase is set at _ 180 degrees at default condition. Phase rotates counter-clockwise to the set value.

SD WSS Data 1 Register (R/W) [Sub Address 0x18]
SD WSS Data 2 Register (R/W) [Sub Address 0x19]

[Composite Video Encoder]

to set WSS Data for Composite Video Encoder mode

Sub Address 0x18
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDG2-7 SDG2-6		SDG2-5 SDG2-4		SDG1-3 SDG1-2		SDG1-1	SDG1-0
Default Value							
0 0		0 0		0 0		0	0

Sub Address 0x19
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	SDG4-13	SDG4-12	SDG4-11	SDG3-10	SDG3-9	SDG3-8
Default Value							
0	0	0	0	0	0	0	0

Note) WSS Data is written in order of 0x18 and then 0x19.

When the second byte (0x19) of WSS Data is written, the AK8826 interprets that Data has been up-dated and it encodes the Data on the next Video Line (Line 23).

Data is retained till it is up-dated with a new one.

Closed Caption Data 1 Register (R/W) [Sub Address 0x26]**Closed Caption Data 2 Register (R/W) [Sub Address 0x27]**

[Component Video Encoder/ Composite Video Encoder Block]

to set Closed Caption Data

Sub Address 0x26							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7 CC6		CC5 CC4		CC3 CC2		CC1	CC0
Default Value							
0 0		0 0		0 0		0	0

Sub Address 0x27							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15 CC14		CC13 CC12		CC11 CC10		CC9	CC8
Default Value							
0 0		0	0	0	0	0	0

Note) Closed Caption Data is written in order of 0x26 and then 0x27.

When the second byte (0x27) of Closed Caption Data is written, the AK8826 interprets that Data has been updated and it encodes the Data on the next Video Line.

Null Codes are automatically output on those, not-data-updated lines.

It is assumed that Parity bit of each Byte Data is added by the Host side.

CC Extended Data 1 Register (R/W) [Sub Address 0x28]
CC Extended Data 2 Register (R/W) [Sub Address 0x29]
 [Component Video Encoder/ Composite Video Encoder Block]

to set Closed Caption Extended Data

Sub Address 0x28							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7 EX	T6	EXT5 EX	T4	EXT3 EX	T2	EXT1	EXT0
Default Value							
0 0		0 0		0 0		0	0

Sub Address 0x29							default Value 0x00
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15 EXT	14	EXT13 EXT	12	EXT11 EX	T10	EXT9	EXT8
Default Value							
0 0		0	0	0	0	0	0

Note) Closed Caption Extended Data is written in order of 0x28 and then 0x29.
 When the second byte (0x29) of Closed Caption Extended Data is written, the AK8826 interprets that Data has been up-dated and it encodes the Data on the next Video Line.
 Null Codes are automatically output on those, not-data-updated lines.
 It is assumed that Parity bit of each Byte Data is added by the Host side.

SD VBID-A Data1 Register (R/W) [Sub Address 0x2A]
SD VBID-A Data2 Register (R/W) [Sub Address 0x2B]

[Composite Video Encoder Block]

to set VBID-A Data

Sub Address 0x2A
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	SDVBID1	SDVBID2	SDVBID3	SDVBID4	SDVBID5	SDVBID6
Default Value							
0 0		0 0		0 0		0	0

Sub Address 0x2B
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDVBID7	SDVBID8	SDVBID9	SDVBID10	SDVBID11	SDVBID12	SDVBID13	SDVBID14
Default Value							
0 0		0 0		0 0		0	0

Note) write "0" to reserved bits.

VBID1 ~ VBID14 correspond to bit 1 ~ bit 14 which are described at {VBID Data Code Assignment} diagram at item { Video ID }.

A 6 Bit CRC Code from bit 15 ~ bit 20 is automatically added by the AK8826.

Data is retained till it is up-dated with a new one.

Status Register (R) [Sub Address 0x34]

to show Status of the AK8826

Sub Address 0x34

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN284	EN21

BIT	Register Name		R/W	Definition
bit 0	EN21	Encode 21 bit	R	to indicate up-date timing of the Closed-Caption Data When EN21 bit is "1 ", the AK8826 waits for data input coming. This bit becomes "0 "after data is written at the second byte (0x27).
bit 1	EN284	Encode 284 bit	R	to indicate up-date timing of the Closed-Caption Extended Data When EN284 bit is "1 ", the AK8822 waits for data input coming. This bit becomes "0 "after data is written at the second byte (0x29).
bit 2 ~ bit 7	Reserved	Reserved bit	R	Reserved bit write "0 ".

Device ID & Revision ID Register (R) [Sub Address 0x35]

to indicate the AK8826 Device ID and Revision ID

Sub Address 0x35 **default Value 0x26**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV1 REV0		DEV5 DEV4		DEV3 DEV2		DEV1	DEV0
0 0		1 0		0 1		1	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	DEV0 ~ DEV5	Device ID bit	R	to indicate Device ID 0x26 is assigned to the AK8826
bit 6 ~ bit 7	REV0 ~ REV1	Revision ID	R	to indicate Revision ID Revision ID is up-dated when a possible software modification is made. It starts at 0x00.

VBID-B Header Data Register (R/W) [Sub Address 0x40]

[Component Video Encoder Block]

to set Video ID Type-B Header data

Sub Address 0x40**default Value 0x08**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	h5 h4		h3	h2	h1	h0
Default Value							
0 0		0 0		1 0		0	0

VBID-B Version Number Register (R/W) [Sub Address 0x41]

[Component Video Encoder Block]

to set Video ID Type-B Payload Data

Sub Address 0x41**default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p7	p6	p5	p4	p3	p2	p1	p0
Default Value							
0	0	0	0	0	0	0	0

VBID-B Payload Packet Length Register (R/W) [Sub Address 0x42]

[Component Video Encoder Block]

to set Video ID Type-B Payload data

Sub Address 0x42**default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p15	p14	p13	p12	p11	p10	p9	p8
Default Value							
0	0	0	0	0	0	0	0

VBID-B Data1 Register (R/W) [Sub Address 0x43] - VBID-B Data13 Register (R/W) [Sub Address 0x2B]
 [Component Video Encoder Block]

to set Video ID data.

CRC code is automatically appended by AK8826.

The data is hold till new data is up-dated.

VBID-B Payload Data1 Register (R/W) [Sub Address 0x43]
Sub Address 0x43
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p23 p22		p21 p20		p19	p18	p17	p16
Default Value							
0 0		0 0		0	0	0	0

VBID-B Payload Data2 Register (R/W) [Sub Address 0x44]
Sub Address 0x44
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p31 p30		p29 p28		p27 p26		p25	p24
Default Value							
0 0		0 0		0 0		0	0

VBID-B Payload Data3 Register (R/W) [Sub Address 0x45]
Sub Address 0x45
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p39	p38	p37	p36	p35	p34	p33	p32
Default Value							
0 0		0	0	0	0	0	0

VBID-B Payload Data4 Register (R/W) [Sub Address 0x46]
Sub Address 0x46
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p47 p46		p45	p44	p43	p42	p41	p40
Default Value							
0 0		0 0		0	0	0	0

VBID-B Payload Data5 Register (R/W) [Sub Address 0x47]
Sub Address 0x47
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p55 p54		p53 p52		p51	p50	p49	p48
Default Value							
0 0		0 0		0 0		0	0

VBID-B Payload Data6 Register (R/W) [Sub Address 0x48]
Sub Address 0x48
default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p63 p62		p61 p60		p59 p58		p57	p56
Default Value							
0 0		0 0		0 0		0	0

VBID-B Payload Data7 Register (R/W) [Sub Address 0x49]**Sub Address 0x49****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p71 p70		p69 p68		p67 p66		p65	p64
Default Value							
0 0		0 0		0 0		0	0

VBID-B Payload Data8 Register (R/W) [Sub Address 0x4A]**Sub Address 0x4A****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p79	p78	p77	p76	p75	p74	p73	p72
Default Value							
0	0	0	0	0	0	0	0

VBID-B Payload Data9 Register (R/W) [Sub Address 0x4B]**Sub Address 0x4B****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p87	p86	p85	p84	p83	p82	p81	p80
Default Value							
0	0	0	0	0	0	0	0

VBID-B Payload Data10 Register (R/W) [Sub Address 0x4C]**Sub Address 0x4C****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p95	p94	p93	p92	p91	p90	p89	p88
Default Value							
0	0	0	0	0	0	0	0

VBID-B Payload Data11 Register (R/W) [Sub Address 0x4D]**Sub Address 0x4D****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p103	p102	p101	p100	p99	p98	p97	p96
Default Value							
0	0	0	0	0	0	0	0

VBID-B Payload Data12 Register (R/W) [Sub Address 0x4E]**Sub Address 0x4E****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p111	p110	p109	p108	p107	p106	p105	p104
Default Value							
0 0		0	0	0	0	0	0

VBID-B Payload Data13 Register (R/W) [Sub Address 0x4F]**Sub Address 0x4F****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
p119	p118	p117	p116	p115	p114	p113	p112
Default Value							
0 0		0 0		0 0		0	0

VBID-B Payload Data14 Register (R/W) [Sub Address 0x50]**Sub Address 0x50****default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	p121	p120
Default Value							
0	0	0	0	0	0	0	0

Video DAC Delay Control Register(R/W) [Sub Address 0x51]

[High Speed Video DAC mode]

to set Video DAC delay

Sub Address 0x51

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	HDLY2	HDLY1	HDLY0
Default Value							
0	0	0	0	0	0	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	HDLY0 ~ HDLY2	HD Delay bit	R/W	to adjust HDI timing delay 000 : 3CLK delay 001 : 2CLK delay 010 : 1CLK delay 011 : no delay 111 : 1CLK advanced 110 : 2CLK advanced 101 : 3CLK advanced 100 : inhibited to set
bit 3 ~ bit 7	Reserved	Reserved	R/W	Reserved, write "0"

11. SYSTEM CONNECTION EXAMPLE

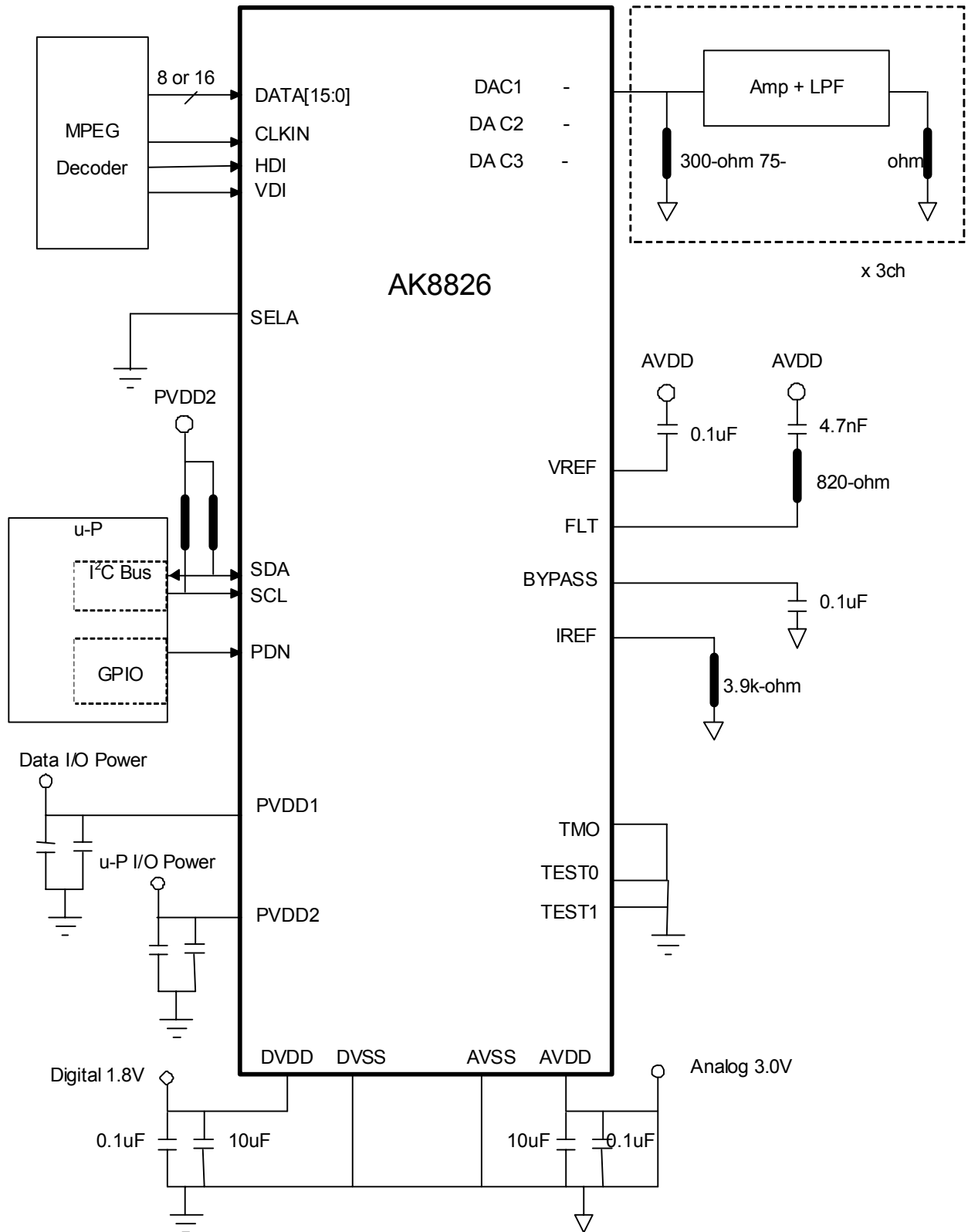


Fig. 171 System Connection example

12. Package

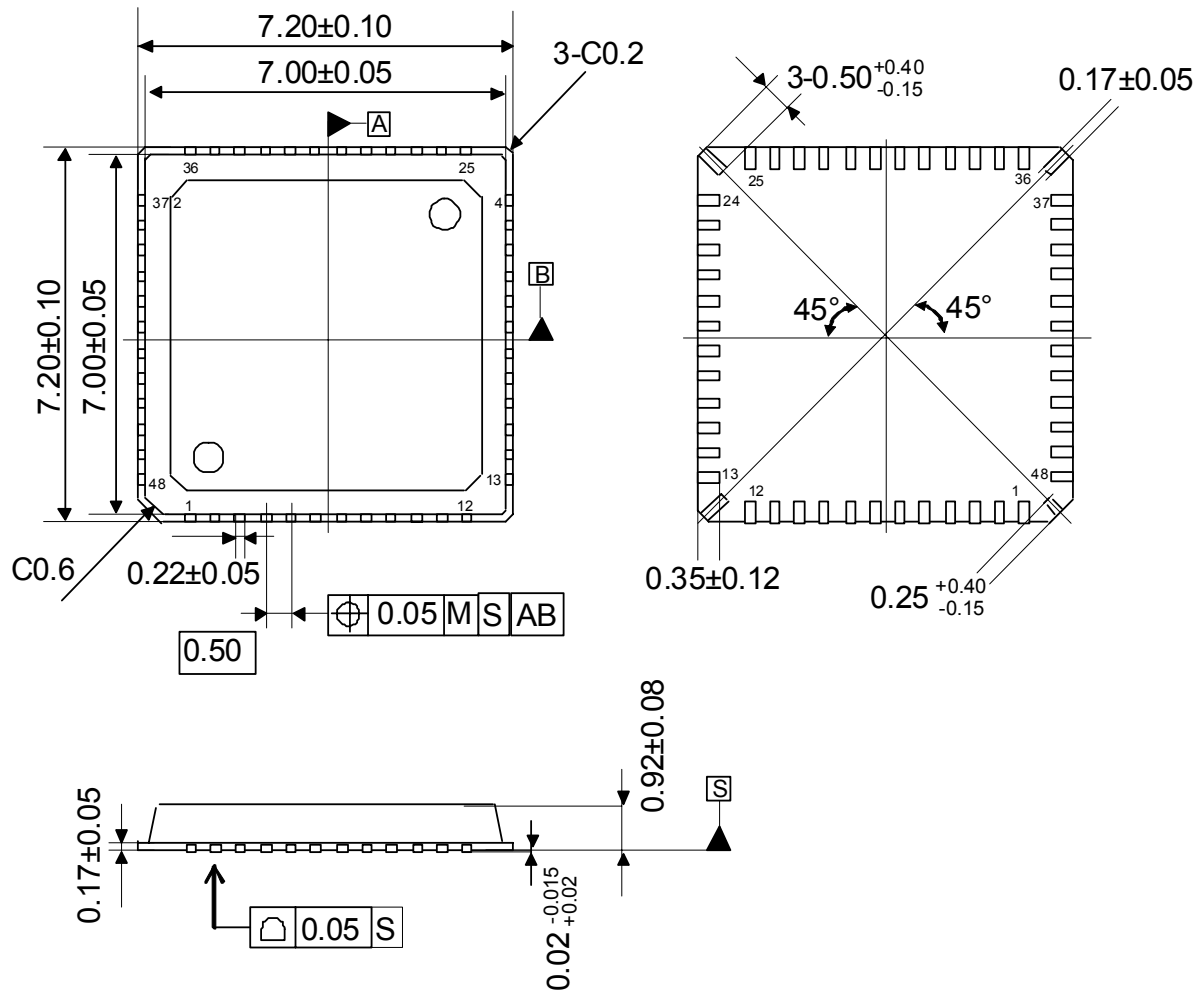
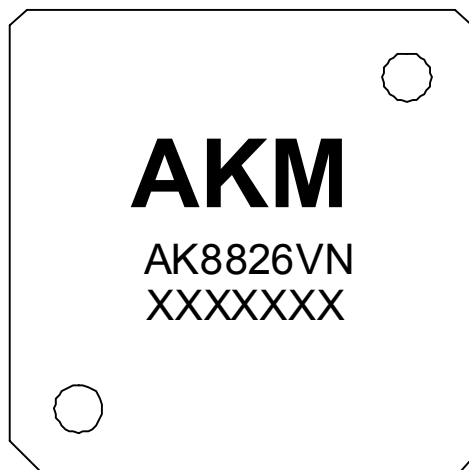


Fig. 172 Package (QFN48 7.2mm x 7.2mm)

13. Marking



1

- a. Pin Type : QFN
- b. Pin count : 48pin
- c. Product Number : 8826VN
- d. Control Code : XXXXXXXX (7 digits)



Revised History

MS0972-E-00 -> MS0972-E-01

Package drawing and Marking are changed.
The numeric values in Package drawing are not changed.

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