AK9231
Dual 12-Bit 1MSPS SAR A/D Converter

1. General Description

The AK9231 is a 12-bit, 1MSPD, SAR A/D converter. It is housed in a space saving ultra-small package (16-pin QFN).

2. Features

- ☐ Simultaneous Sampling 12-bit SAR A/D Converter
- ☐ Sampling Rate: 1MSPS
- ☐ Unipolar Input Range: 0 ~ VDD
- ☐ S/(N+D): 71.25dB(Typ.) at 100kHz Input
- ☐ INL: ±1.25 SB (Max.)
- ☐ DNL: ±1.0 LSB(Max.)
- ☐ Power Consumption: IDD=50mW (fs=1MSPS, VDD= 5V)
- ☐ Power Supply: VDD=2.35 ~ 5.25V
- ☐ Operational Temperature Range: Ta=-40 ~ 105ºC
- ☐ Package: Ultra-small 16-pin QFN (3mm x 3mm) Package

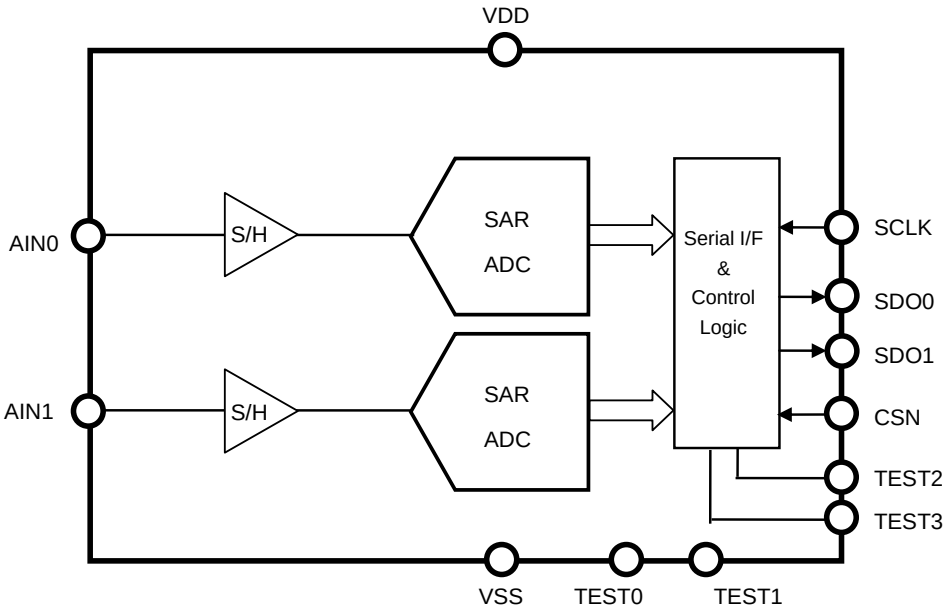
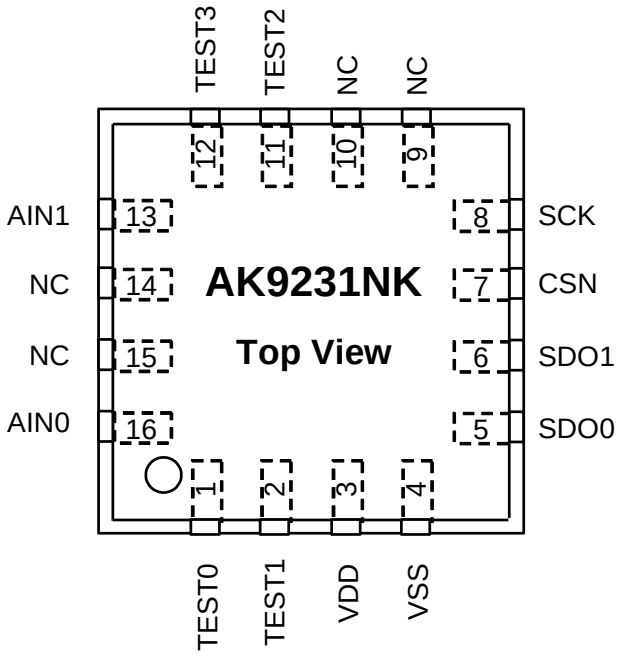


Figure 1. AK9231 Block Diagram

3. Table of Contents

4. Pin Configurations and Functions

4.1. Pin Layout



4.2. Pin Functions

Pin No.	Pin Name	I/O	Function
1	TEST0	I	TEST0 (Internal pull down: 50kΩ. Typ.) This pin must be connected to VSS.
2	TEST1	I	TEST1 (Internal pull down: 50kΩ. Typ.) This pin must be connected to VSS.
3	VDD	-	Power Supply: 2.35 ~ 5.25V
4	VSS	-	Ground
5	SDO0	O	Serial Data Output 0
6	SDO1	O	Serial Data Output 1
7	CSN	I	Chip Select
8	SCK	I	Serial Clock Input
9	NC	-	No Connection. No internal bonding. This pin must be connected to VSS
10	NC	-	No Connection. No internal bonding. This pin must be connected to VSS
11	TEST2	I	TEST2 (Internal pull down: 50kΩ. Typ.) This pin must be connected to VSS.
12	TEST3	I	TEST3 (Internal pull down: 50kΩ. Typ.) This pin must be connected to VSS.
13	AIN1	I	ADC1 Input
14	NC	-	No Connection. No internal bonding. This pin must be connected to VSS
15	NC	-	No Connection. No internal bonding. This pin must be connected to VSS
16	AIN0	I	ADC0 Input

Note:
* 1. Digital input pins (CSN, SCK, TEST0, TEST1, TEST2, TEST3) must not be allowed to float.

4.3. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AIN0, AIN1	VSS

5. Absolute Maximum Ratings

(VSS= 0V, * 2)

Parameter	Symbol	Min.	Max.	Unit
Power Supply	VDD	-0.3	6.0	V
Analog Input Current (AIN+, AIN-)	AIN	-	±10	mA
Analog Input Voltage	AVIN	-0.3	VDD+0.3	V
Digital Input Current	DIIN	-	±10	mA
Digital Input Voltage	DVIN	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	105	ºC
Storage Temperature	Tstg	-65	150	ºC

Note:
* 2. All voltages are with respect to ground (VSS).

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

6. Recommended Operating Conditions

(VSS= 0V, * 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply	VDD	2.35		5.25	V

Note:
* 2. All voltages are with respect to ground (VSS).

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

7. Analog Characteristics

(Ta = -40 ~ 105ºC; VDD= 2.35 ~ 5.25V; fs= 1MHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
Resolution		12			bit
No Missing Codes		12			bit
Integral Nonlinearity (INL) Error		-1.25	±0.65	1.25	LSB
Differential Nonlinearity (DNL) Error		-1	+0.4/-0.65	1	LSB
Offset Error	VDD= 2.35 ~ 3.6V	-2.5	±0.5	2.5	LSB
	VDD= 4.75 ~ 5.25V	-2	±0.5	2	LSB
Offset Error Drift			±7		µV/ºC
Offset Error match: ADC to ADC		-2	±0.1	2	LSB
Gain Error		-1.75	±0.5	1.75	LSB
Gain Error Drift			±0.4		ppm/ºC
Gain Error match: ADC to ADC		-1.75	±0.5	1.75	LSB
Sampling Dynamics					
Throughput Rate		25		1000	kSPS
Acquisition time		325			nsec
tA match			50	200	psec
Aperture Delay			5		nsec
Dynamic Characteristics (fin= 0.5dBFS)					
THD	fI= 100kHz		-84		dB
S/H	VDD=2.35 ~ 3.6V, fI= 100kHz	69	71.25		dB
	VDD=4.75 ~ 5.25V, fI= 100kHz	70	72.25		dB
S/(N+D)	VDD=2.35 ~ 3.6V, fI= 100kHz	69	71.25		dB
	VDD=4.75 ~ 5.25V, fI= 100kHz	70	72.25		dB
SFDR	sine wave 100kHz		85.5		dB
Channel to Channel Isolation			-88		dB
Full power bandwidth	At -3dB		12		MHz
Analog Input					
Full scale input:		0		VDD	V
Absolute input voltage range		-0.2		VDD+0.2	V
Input Capacitance			27		pF
Input leakage Current			-0.3/0.5		µA
Power Supplies					
Power Supply Current:					
Normal Operation (fs=1MSPS) VDD= 5V			10	12.3	mA
Normal Operation (fs=1M SPS) VDD=3V			7.2	9.0	mA
Static state VDD= 5V			4.4	5.8	mA
Static state VDD= 3V			4.2	5.5	mA
Power-Down State			0.1	10	µA
Invalid conversions after power up or reset				1	

8. DC Characteristics

(Ta= -40 ~ 105ºC)

Parameter		Symbol	Min.	Max.	Unit
High-Level Input Voltage	VDD= 2.35 ~ 3.6V	VIH1	1.8	-	V
	VDD= 4.75 ~ 5.25V	VIH2	2.4	-	V
Low-Level Input Voltage	VDD= 5V	VIL1	-	0.8	V
	VDD= 3V	VIL2	-	0.4	V
High-Level Output Voltage (Iout = -200µA)		VOH	VDD-0.2	-	V
Low-Level Output Voltage (Iout = 200µA)		VOL	-	0.4	V
Load Capacitance		CL		30	pF
Input Leakage Current (* 3)		Iin	-	±1	µA

Note:

* 3. Except TEST0, TEST1, TEST2 and TEST3 pins. These pins are internally pulled-down. (Typ.50kΩ)

9. Switching Characteristics

(Ta= -40 ~ 105ºC)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCK Clock Frequency		fSCK			20	MHz
SCK High Pulse Width (* 4)		tSCKH	0.4 x tSCK		-	nsec
SCK Low Pulse Width (* 4)		tSCKL	0.4 x tSCK		-	nsec
Minimum time from bus 3-state to start of next conversion		tq	40			nsec
CSN "↓" to First SCK "↓"		tCSS	10		-	nsec
CSN "↓" to DOUT "0" Delay		tCSD	-		25	nsec
SCK "↓" to DOUT Valid Delay		tDCD	-		30	nsec
SCK "↓" to DOUT Valid Hold time	VDD= 3V	tDCH1	7		-	nsec
	VDD= 5V	tDCH2	5.5		-	nsec
Minimum CS pulse		tCS	25			nsec
16th SCK"↓" to SDO Hi-Z State	VDD= 3V	tCCZ1	-		30	nsec
	VDD= 5V	tCCZ2	-		20	nsec

Note:

* 4. tSCK = 1/ fSCK

9.1. Timing Diagram

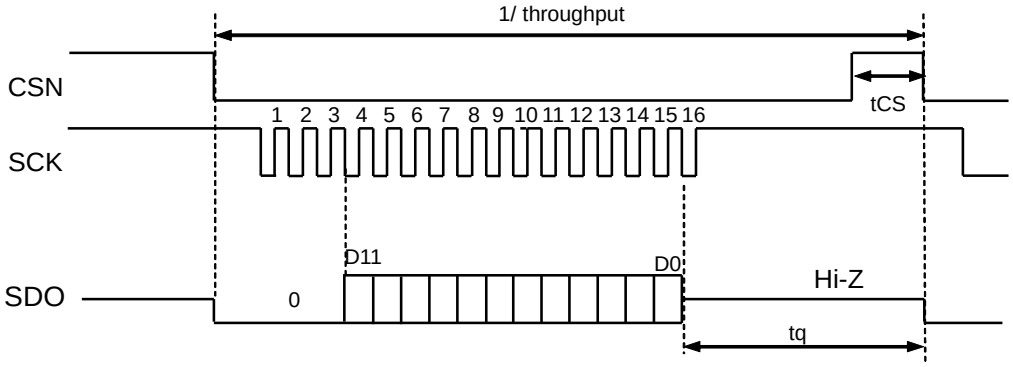


Figure 2. Data Output Timing 1

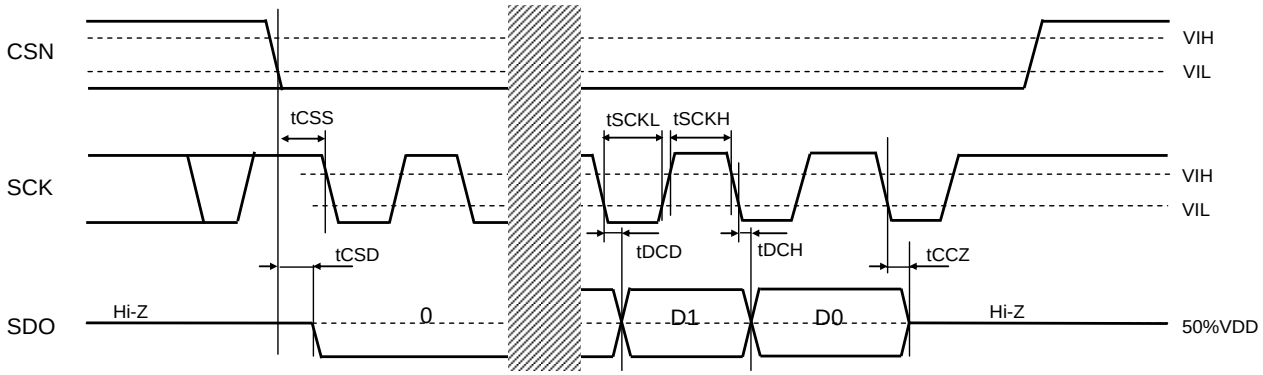


Figure 3. Data Output Timing 2

9.2. Digital I/F

The AK9231 starts sampling input signals by a falling edge of the CSN pin and the AD conversion process is initiated. Converted data is output from the SDOx pin (x= 0 or 1) during the conversion. After a falling edge of the CSN pin, “0” data (4-bit) is output and then after four falling edges of SCK, AD converted data (12-bit) is output from the SDOx pin in MSB first.

SDO data becomes Hi-Z on the 16th falling edge of SCK clock and the AD conversion ends. The AK9231 enters the acquisition phase on the first rising edge of SCK after the 13th falling edge (“b” period in Figure 4). The CSN pin can be set to “H” after the 16th falling edge of SCK clock. It is necessary not to start the next conversion by pulling CSN low until the end of the quiet time (tq). Do not put the CSN pin to “L” during the “tq” period after SDO data becomes Hi-Z. Normally, the CSN pin should not be set to “H” until “b” timing in Figure 4.

The AD conversion stops and SDO data becomes Hi-Z if the CSN pin is put to “H” during the conversion. At the same time, the AK9231 enters the acquisition phase. The CSN pin should be set to “L” after waiting the acquisition time (minimum 325nsec) when re-starting the sampling.

The high level of the digital input is not limited to device VDD. For example, a 5.25V “H” level input is accepted when the device supply voltage is 2.35V. It enables to connect other systems that have different power supply level to the digital interface of the AK9231. Also this feature relaxes restriction on power up sequencing. However, it should be noted that VOH and VOL are dependent on the device VDD.

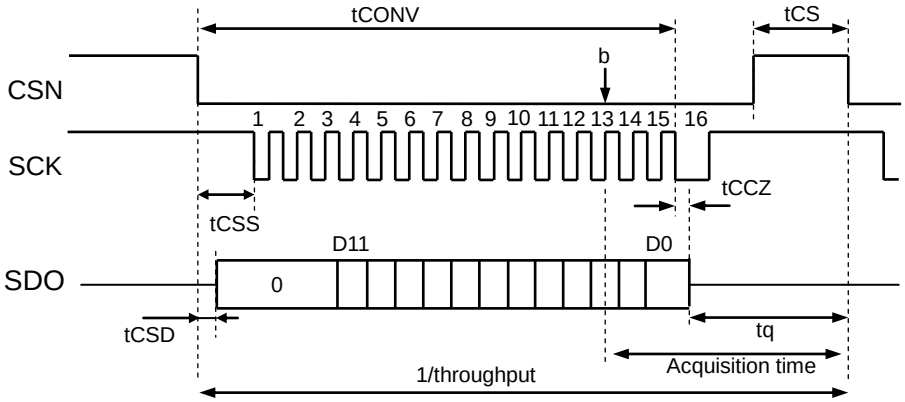
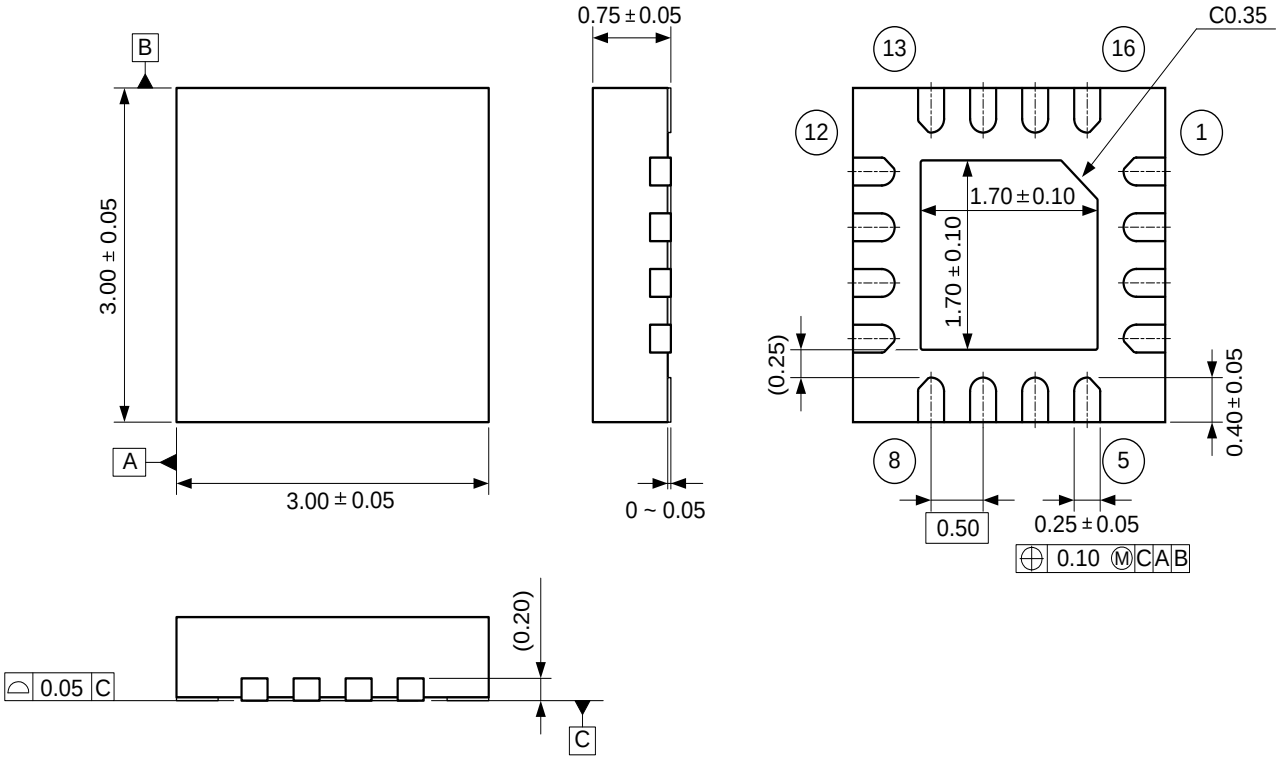


Figure 4. Digital I/F

10. Package

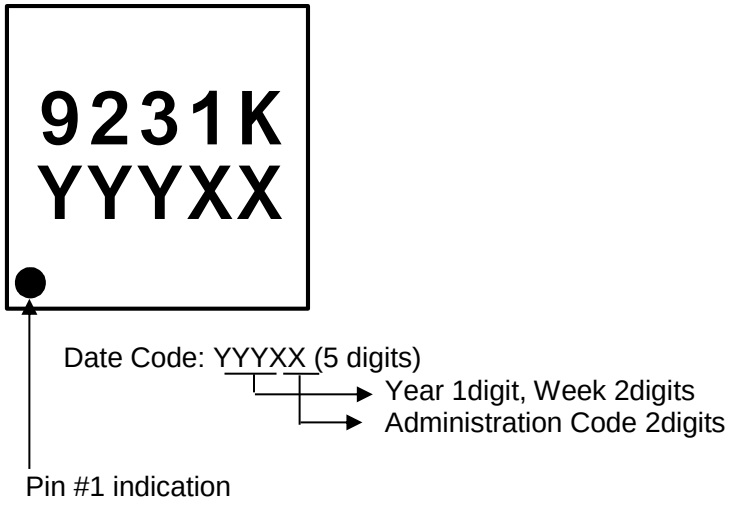
10.1. Outline Dimensions

16-pin QFN (Unit: mm)



* The exposed pad on the bottom surface of the package must be open or connected to the ground.

10.2. Marking



11. Ordering Guide

AK9231NK	-40 ~ +105ºC	16pin QFN (3.0mm x 3.0mm, 0.5mm pitch)
AKD9231	Evaluation Board for the AK9231	

12. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
14/12/09	00	First edition		

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