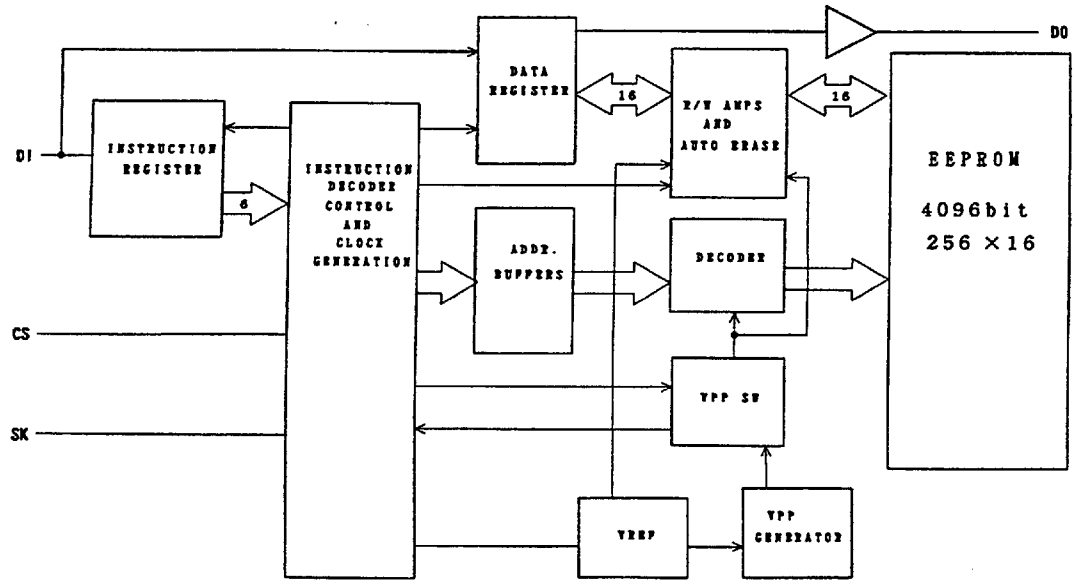
AK93C65/L

4096bit Serial EEPROM

Features

- ☐ ADVANCED CMOS E2PROM TECHNOLOGY
- ☐ READ/WRITE NON-VOLATILE MEMORY
- ☐ WIDE VCC OPERATION
  AK93C65 ••• Vcc = 2.5V ~ 5.5V
  AK93C65L••• Vcc = 1.8V ~ 5.5V
- ☐ 4096 bits, 256 × 16 organization
- ☐ SERIAL INTERFACE
  - Interfaces with popular microcontrollers and standard microprocessors
- ☐ LOW POWER CONSUMPTION
  - 1mA max. Read Operation
  - 3 μA Max. Standby, CMOS interface
- ☐ Automatic write cycle time-out with auto-ERASE
- ☐ Busy/Ready status signal
- ☐ Software and Hardware controlled write protection
- ☐ IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package
- ☐ APPLICATION VERSATILITY
  - Portable equipment, Telephones, Alarm Devices, Electronic Locks, Appliances, Terminals, Smart Cards, Satellite Receivers, Tuners, etc.



Block Diagram

General Description

The AK93C65/L is a 4096-bit serial CMOS E2PROM divided into 256 registers of 16 bits each. Each register is independently addressable for read, write and erase operations. The AK93C65/L has 4 instructions such as READ, WRITE, EWEN (erase/write enable) and EWDS (erase/write disable). Those instructions control the AK93C65/L.
The AK93C65 can operate full function under wide operating voltage range from 2.5V to 5.5V (AK93C65L : 1.8V to 5.5V). The charge up circuit is integrated for high voltage generation that is used for write operation.
A serial interface of AK93C65/L, consisting of chip select (CS), serial clock (SK), data-in (DI) and data-out (DO), can easily be controlled by popular microcontrollers or standard microprocessors.
AK93C65/L takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin (SK). And at read operation, AK93C65/L takes out the read data from a register to data output pin (DO) synchronously with rising edge of SK.
The DO pin is usually in high impedance state. The DO pin outputs "L" or "H" in case of data output or Busy/Ready signal output.

• Software and Hardware controlled write protection

The AK93C65/L has 2 write protection functions. When Vcc is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of ERASE/WRITE instructions is disabled. Before ERASE/WRITE instructions are executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or Vcc is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.
The PE is internallly pulled up to VCC. If the PE is left unconnected, the part will accept WRITE, EWEN and EWDS instructions.

• $\overline{\text{Busy/Ready}}$ status signal

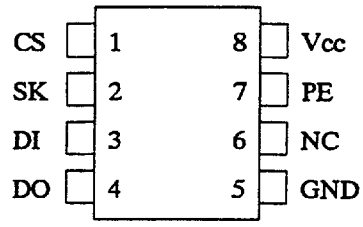
After a write instruction, the DO output serves as a $\overline{\text{Busy/Ready}}$ status indicator. After the falling edge of the CS initiates the self-timed programming cycle, the DO indicates the $\overline{\text{Busy/Ready}}$ status of the chip if the CS is brought high after a minimum of 250ns (Tcs). DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.
The Busy/Ready status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state.
The Busy/Ready signal outputs until a start bit (Logic"1") of the next instruction is given to the part.

Product Selection Guide

Model	Temp.Range	Vcc	Package
AK93C65	-30 ℃～ 70 ℃	2.5V ～ 5.5V	8pin Plastic DIP
AK93C65F	-30 ℃～ 70 ℃	2.5V ～ 5.5V	8pin Plastic SOP
AK93C65L	-30 ℃～ 70 ℃	1.8V ～ 5.5V	8pin Plastic DIP
AK93C65LF	-30 ℃～ 70 ℃	1.8V ～ 5.5V	8pin Plastic SOP

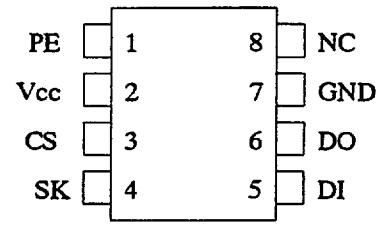
Pin Configuration

AK93C65/AK93C65L



8pinDIP

AK93C65F/AK93C65LF



8pinSOP

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
PE	Program Enable
GND	Ground
Vcc	Power Supply
NC	Not Connected

Functional Description

The AK93C65/L has 4 instructions such as READ, WRITE, EWEN (erase/write enable) and EWDS (erase/write disable). A valid instruction consists of a Start Bit (Logic"1"), the appropriate Op Code and the desired memory Address location.
The CS pin must be brought low for a minimum of 250ns (Tcs) between each instruction when the instruction is continuously executed.

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	A7–A0	D15–D0	Reads data stored in memory, at specified address.
WRITE	1	01	A7–A0	D15–D0	Writes register.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXXXX		Disables all programming instructions.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers.

The WRAL instruction are used for factory function test only.
User can't use the WRAL instruction.

Write

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the DI pin, the CS pin must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO indicates the Busy/Ready status of the chip if the CS is brought high after a minimum of 250ns (Tcs). DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.
It is not necessary for the AK93C65/L to erase instruction before write instruction since the AK93C65/L provides automatic erase function.

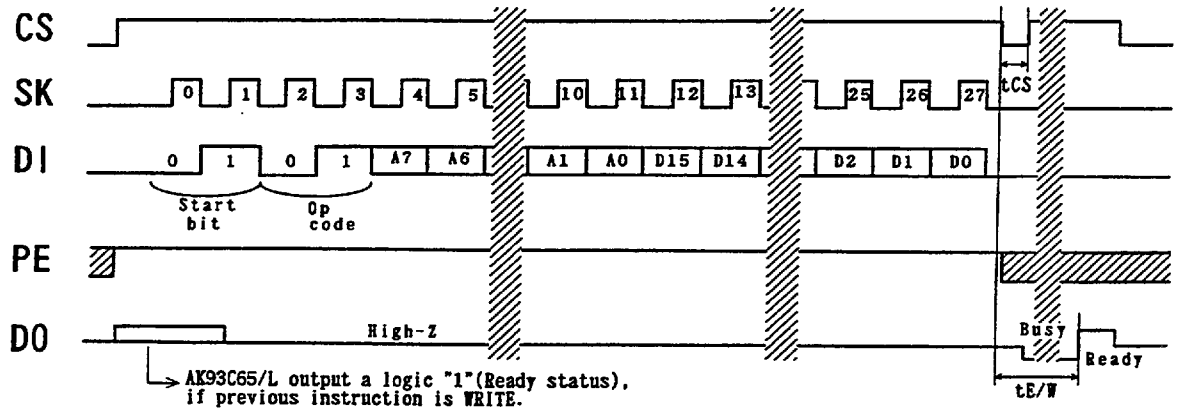


Fig1. WRITE

Read

The read instruction is the only instruction which outputs serial data on the DO pin.
Following the Start bit, first Op code and address are decoded, then the data from the selected memory location is available at the DO pin. A dummy bit (logical "0") precedes the 16-bit data from the selected memory location. The output data changes are synchronized with the rising edges of the serial clock (SK).

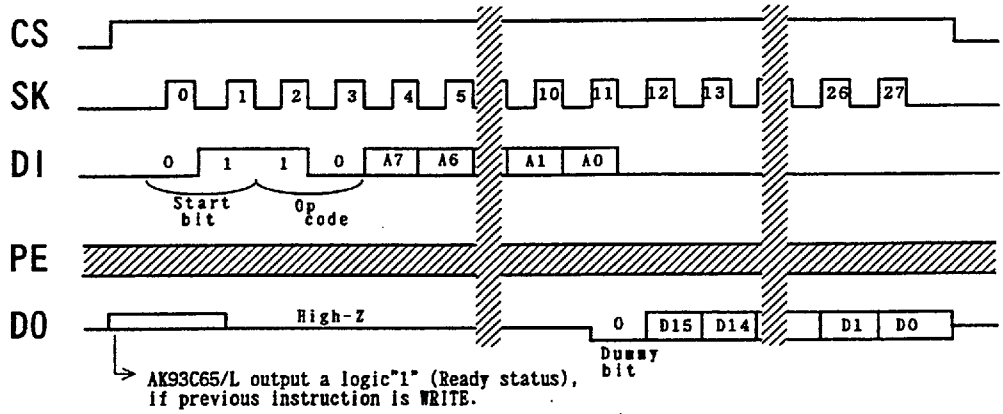


Fig2. READ

Erase/Write Enable and Disable

When Vcc is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of ERASE/WRITE instructions is disable. Before ERASE/WRITE instructions are executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or Vcc is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.

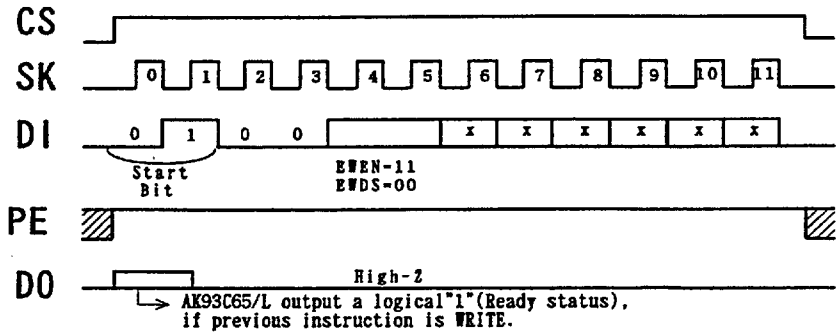


Fig3. EWEN/EWDS

Precautions for use

The treatment and assembly of AK93C65/L require careful attention to electrical over-stress, just like general CMOS devices.
When the part is assembled, human bodies, work benches and measurement equipments should be connected to ground. On the boards, decoupling capacitors (0.1uF) between VCC and GND should be located as near as possible to the part.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+6.0	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	℃

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

◇ AK93C65

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	2.5	5.5	V
Ambient Operating Temperature	Ta	-30	+70	℃

◇ AK93C65L

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	1.8	5.5	V
Ambient Operating Temperature	Ta	-30	+70	℃

ELECTRICAL CHARACTERISTICS

■ AK93C65 Electrical Characteristics

1) D.C. ELECTRICAL CHARACTERISTICS

(2.5V ≦ Vcc ≦ 5.5V, -30 ℃≦ Ta ≦ 70 ℃ , unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation	ICC	VCC=5.5V VIN=VIH//VIL tSK=1us 、DO=OPEN Read Operation		1	mA
Current Dissipation (Standby)	I_{CCSB}	VCC=5.5V 、CS=GND VIN=VCC/GND DO=OPEN		3	uA
Input High Voltage	VIH1	VCC=5V ± 10%	2.0	VCC + 0.5	V
	VIH2	2.5V ≦ VCC ≦ 5.5V	0.8 × VCC	VCC + 0.5	V
Input Low Voltage	VIL1	VCC=5V ± 10%	-0.1	0.8	V
	VIL2	2.5V ≦ VCC ≦ 5.5V	-0.1	0.15 × VCC	V
Output High Voltage	VOH1	VCC=5V ± 10% IOH1=-0.1mA	2.2		V
	VOH2	2.5V ≦ VCC ≦ 5.5V IOH2=-0.1mA	0.8 × VCC		V
Output Low Voltage	VOL1	VCC=5V ± 10% IOL1=1.0mA		0.4	V
	VOL2	2.5V ≦ VCC ≦ 5.5V IOL2=0.1mA		0.4	V
Input Leakage	ILI	VCC=5.5V 、VIN=5.5V		± 10	uA
Output Leakage	ILO	VCC=5.5V VOUT=5.5V 、CS=GND		± 10	uA

AK93C65 is TTL compatible under Vcc=5.0V ± 10%.

2) A.C. ELECTRICAL CHARACTERISTICS

(2.5V ≦ Vcc ≦ 5.5V, -30 ℃≦ Ta ≦ 70 ℃ , unless otherwise specified)

Parameter	Simbol	Condition	Min.	Max.	Unit
SK Cycle Time	tSKP1	4.5V ≦ VCC ≦ 5.5V	1		us
	tSKP2	2.5V ≦ VCC < 4.5V	2		us
SK Pulse Width	tSKW1	4.5V ≦ VCC ≦ 5.5V	500		ns
	tSKW2	2.5V ≦ VCC < 4.5V	1		us
CS Setup Time	tCSS		100		ns
CS Hold Time	tCSH		0		ns
Data Setup Time	tDIS1	4.5V ≦ VCC ≦ 5.5V	200		ns
	tDIS2	2.5V ≦ VCC < 4.5V	400		ns
Data Hold Time	tDIH1	4.5V ≦ VCC ≦ 5.5V	200		ns
	tDIH2	2.5V ≦ VCC < 4.5V	400		ns
Output delay	tPD1	4.5V ≦ VCC ≦ 5.5V		500	ns
	tPD2	2.5V ≦ VCC < 4.5V		1	us
Selftimed Programming Time	tE/W			15	ms
Min CS Low Time	tCS		250		ns
CS to Status Valid	tSV	CL=100pF		500	ns
CS to Output High-Z	tOZ			100	ns

■ AK93C65L Electrical Characteristics

1) D.C. ELECTRICAL CHARACTERISTICS

(1.8V ≦ Vcc ≦ 5.5V, -30 ℃≦ Ta ≦ 70 ℃ , unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation	ICC	VCC=5.5V VIN=VIH//VIL tSK=1us 、DO=OPEN Read Operation		1	mA
Current Dissipation (Standby)	I_{CCSB}	VCC=5.5V 、CS=GND VIN=VCC/GND DO=OPEN		3	uA
Input High Voltage	VIH1	VCC=5V ± 10%	2.0	VCC + 0.5	V
	VIH2	2.5V ≦ VCC ≦ 5.5V	0.8 × VCC	VCC + 0.5	V
	VIH3	1.8V ≦ VCC < 2.5V	0.8 × VCC	VCC + 0.5	V
Input Low Voltage	VIL1	VCC=5V ± 10%	-0.1	0.8	V
	VIL2	2.5V ≦ VCC ≦ 5.5V	-0.1	0.15 × VCC	V
	VIL3	1.8V ≦ VCC < 2.5V	-0.1	0.2 × VCC	V
Output High Voltage	VOH1	VCC=5V ± 10% IOH1=-0.1mA	2.2		V
	VOH2	2.5V ≦ VCC ≦ 5.5V IOH2=-0.1mA	0.8 × VCC		V
	VOH3	1.8V ≦ VCC < 2.5V IOH3=-0.1mA	0.8 × VCC		V
Output Low Voltage	VOL1	VCC=5V ± 10% IOL1=1.0mA		0.4	V
	VOL2	2.5V ≦ VCC ≦ 5.5V IOL2=0.1mA		0.4	V
	VOL3	1.8V ≦ VCC < 2.5V IOL3=0.1mA		0.4	V
Input Leakage	ILI	VCC=5.5V 、VIN=5.5V		± 10	uA
Output Leakage	ILO	VCC=5.5V VOUT=5.5V 、CS=GND		± 10	uA

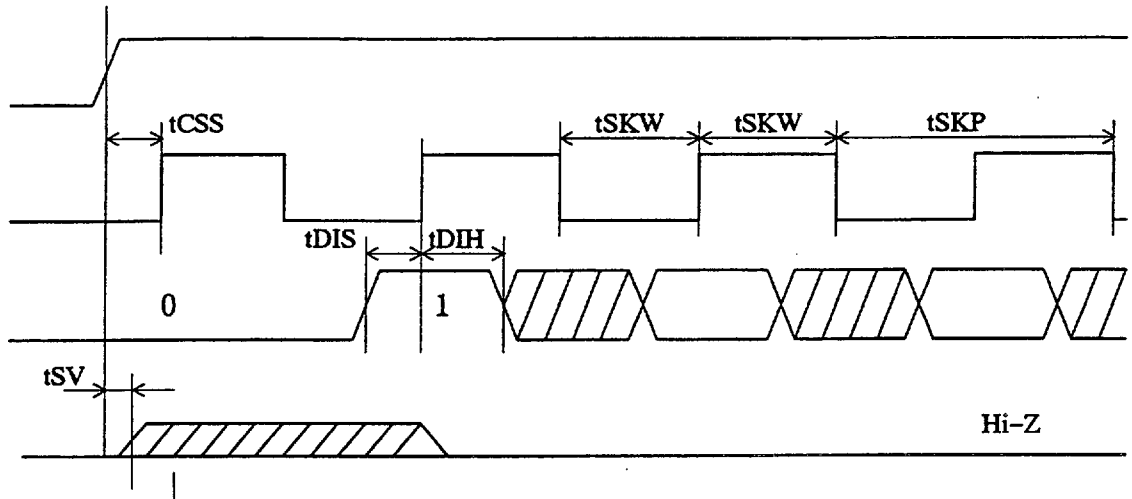
AK93C65L is TTL compatible under Vcc=5.0V ± 10%.

2) A.C. ELECTRICAL CHARACTERISTICS

(1.8V ≦ Vcc ≦ 5.5V, -30 ℃≦ Ta ≦ 70 ℃ , unless otherwise specified)

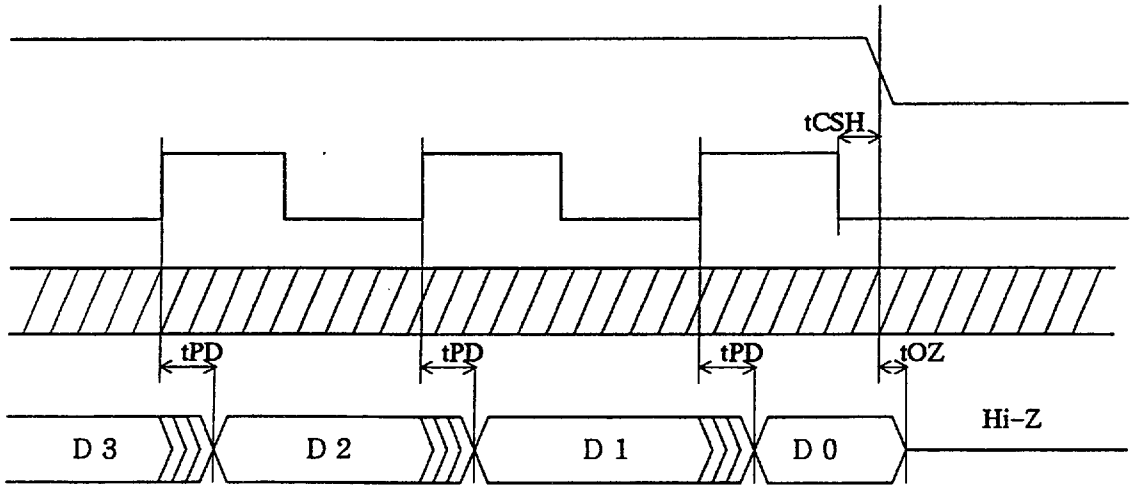
Parameter	Simbol	Condition	Min.	Max.	Unit
SK Cycle Time	tSKP1	4.5V ≦ VCC ≦ 5.5V	1		us
	tSKP2	2.0V ≦ VCC < 4.5V	2		us
	tSKP3	1.8V ≦ VCC < 2.0V	4		us
SK Pulse Width	tSKW1	4.5V ≦ VCC ≦ 5.5V	500		ns
	tSKW2	2.0V ≦ VCC < 4.5V	1		us
	tSKW3	1.8V ≦ VCC < 2.0V	2		us
CS Setup Time	tCSS		100		ns
CS Hold Time	tCSH		0		ns
Data Setup Time	tDIS1	4.5V ≦ VCC ≦ 5.5V	200		ns
	tDIS2	2.5V ≦ VCC < 4.5V	400		ns
	tDIS3	1.8V ≦ VCC < 2.5V	800		ns
Data Hold Time	tDIH1	4.5V ≦ VCC ≦ 5.5V	200		ns
	tDIH2	2.5V ≦ VCC < 4.5V	400		ns
	tDIH3	1.8V ≦ VCC < 2.5V	800		ns
Output delay	tPD1	4.5V ≦ VCC ≦ 5.5V		500	ns
	tPD2	2.5V ≦ VCC < 4.5V		1	us
	tPD3	1.8V ≦ VCC < 2.5V		2	us
Selftimed Programming Time	tE/W1	2.5V ≦ VCC ≦ 5.5V		15	ms
	tE/W2	1.8V ≦ VCC < 2.5V		25	ms
Min CS Low Time	tCS		250		ns
CS to Status Valid	tSV	CL=100pF		500	ns
CS to Output High-Z	tOZ1	2.5V ≦ VCC ≦ 5.5V		100	ns
	tOZ2	1.8V ≦ VCC < 2.5V		250	ns

Synchronous Data timing

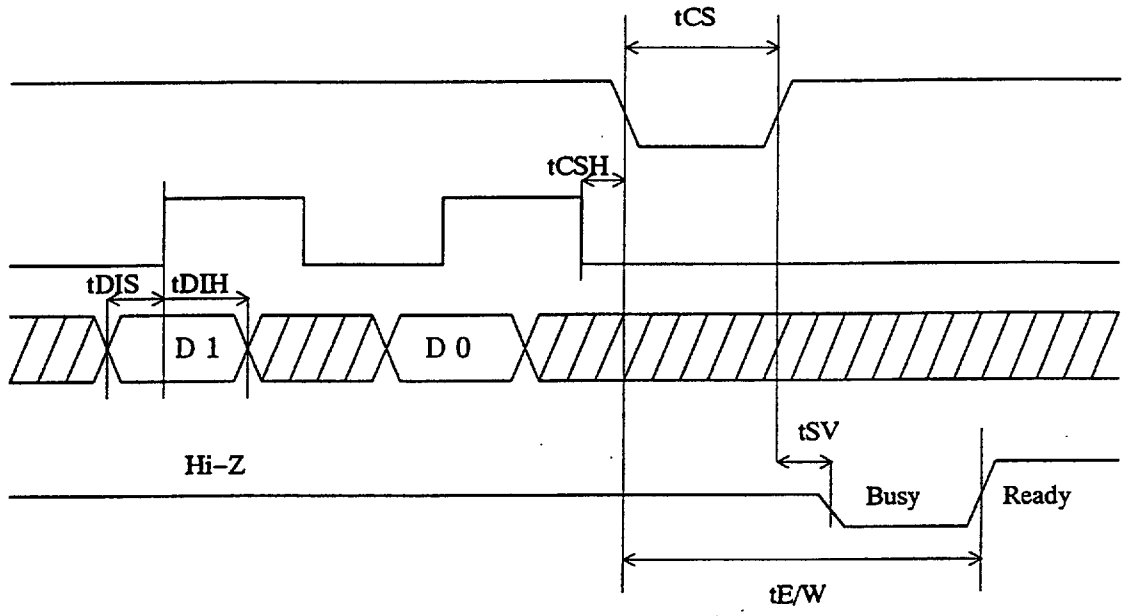


→ AK93C65/L output a logical "1" (Ready status), if previous instruction is WRITE.

The Start of Instruction



The End of Instruction

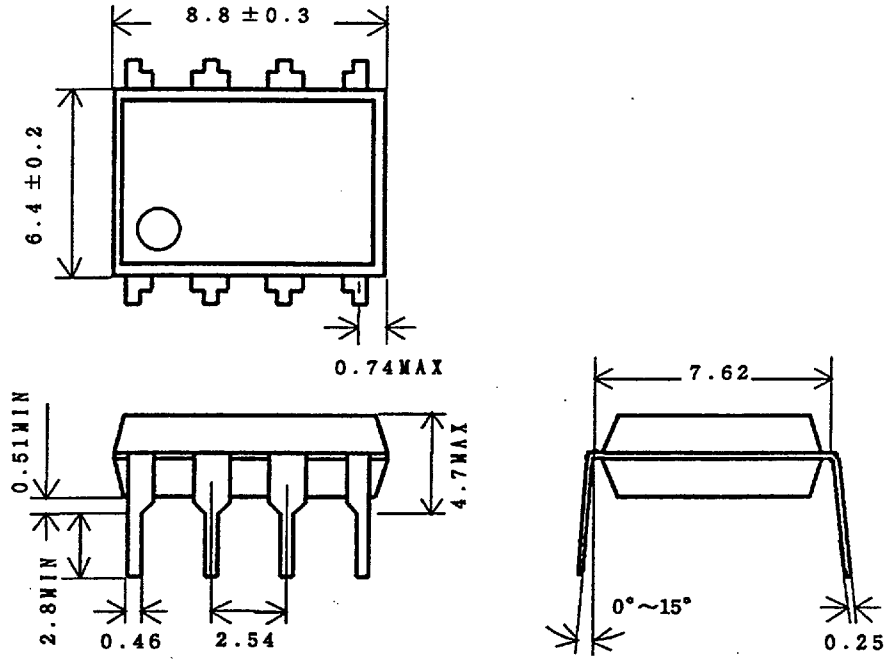


$\overline{\text{Busy}}$/Ready Signal Output

PACKAGE OUTLINE

(UNIT:mm)

■ 8pinDIP



■ 8pinSOP