



AK9753

IR Sensor IC with I²C I/F

1. General Description

The AK9753 is a low power and compact infrared-ray (IR) sensor module. It is composed of four quantum IR sensors and an integrated circuit (IC) for characteristic compensation. The four IR sensors' offset and gain variations are calibrated at shipment. An integral analog-to-digital converter provides 16-bits data outputs. The AK9753 is suitable for several feet human detector by using external lens.

2. Features

- ☐ Quantum-type IR Sensor with Four IR Elements
- ☐ 16-bits Digital Outputs to I²C bus
- ☐ Integrated temperature sensor: -10 ~ 60°C output on I²C bus
- ☐ Built in Optical filter
- ☐ Serial Interface: I²C (Standard mode and Fast mode) Compatible
- ☐ Interrupt Function

INT pin can be used as a read-trigger or an interrupt request of signal level monitoring.

- ☐ Built in Switch Mode (Standalone Mode)

By writing the threshold into the internal EEPROM at the customer's production testing, the presence detection state will be output to the INT pin. In this mode, neither the control by I²C bus nor Host MCU is necessary.

- ☐ Low Voltage Operation: VDD: 1.71 ~ 3.63V
 DVDD: 1.65V ~ VDD
- ☐ Low Current Consumption: Max. 100 µA (@Continuous Mode "0")
 Max. 1µA (@ Power down Mode)
- ☐ Small and Thin Package: 10-pin SON

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4. Block Diagram and Functions

4.1. Block Diagram

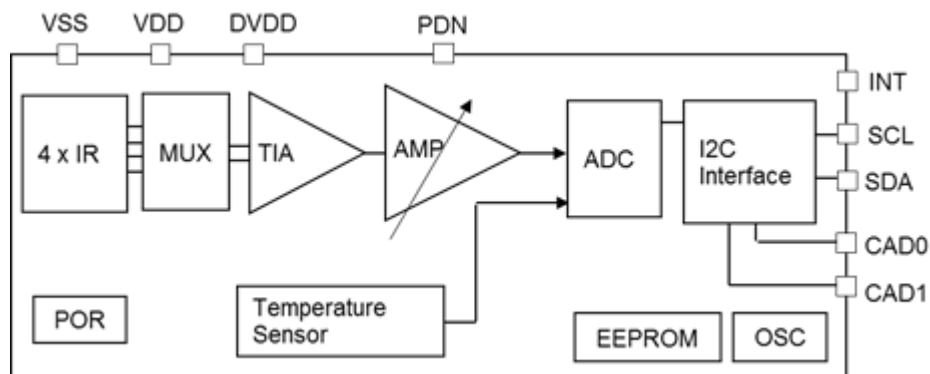


Figure 4.1 AK9753 Block Diagram

4.2. Block Functions

Table 4.1. Block Functions

Block	Function
4 x IR	Four IR Sensor
MUX	Matrix Switch
TIA	Photocurrents of IR Sensor are converted to voltage signals.
AMP	Programmable gain amplifier to adjust the outputs.
Temperature Sensor	Built-in Temperature Sensor
ADC	The amplifier output and the built-in temperature sensor output are converted to digital signals.
I ² C Interface	Interface to external host controller. SCL and SDA pins are provided for I ² C Interface. The interface operates up to 400kHz rate and down to 1.65V low voltage condition.
EEPROM	EEPROM
OSC	Internal Oscillator.
POR	Power On Reset circuit.

5. Pin Configurations and Functions

5.1. Pin Configurations

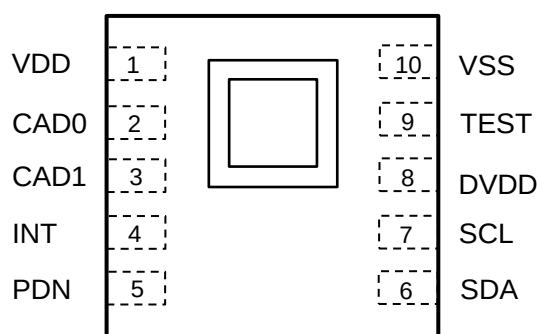


Figure 5.1 Pin Configurations

5.2. Pin Functions

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	VDD	-	Analog Power Supply Pin
2	CAD0	I	Slave address 0. CAD0 pin should be connected to VDD or VSS. Set up an address so that two or more same address of devices do not exist on the same bus.
3	CAD1	I	Slave address 1. CAD0 pin should be connected to VDD or VSS. Set up an address so that two or more same address of devices do not exist on the same bus.
4	INT	O	Functions are selected by INTEN register. INT pin goes “Active”, when the ADC output are ready to be read or the differential signal of two IR sensor(one observes the upper (or left)side and another observes lower (or right) side) exceeds threshold levels. It is composed of an open drain output (N-type transistor). INT pin is connected to DVDD voltage through a pull-up resistor, with other open drain or open collector output of the other devices to form “wired-OR”.
5	PDN	I	Power down pin. When PDN pin= “H”, AK9753 can operate. PDN pin is not connected to VDD (or VSS) through a pull-up (or pull-down) resistor. This pin must be connected to “H” or “L” voltage level.
6	SDA	I/O	I ² C Data Output Pin. SDA is a bidirectional pin which is used to transmit data into and out of the device. It is composed of a signal input and an open drain output (N-type transistor). SDA is connected to DVDD voltage through a pull-up resistor, and to open drain outputs or open collector outputs of the other devices as “wired-OR”
7	SCL	I	I ² C Clock Input pin. Signal processing is executed at the rising and falling edge of SCL clock. Observe rise time tR and fall time tF. SCL is connected to DVDD voltage through a pull-up resistor.
8	DVDD	-	Digital I/F Power Supply pin.
9	TEST	I	Test pin. TEST pin should be connected to VSS.
10	VSS	-	Ground pin.

6. IR Sensors Configuration / Observable Area

6.1. IR Sensor's Configurations

The four IR sensors which AK9753 includes are arranged as shown in Figure 6.1. IR1(2, 3, 4) is defined as the measurement data of IR sensor 1(2, 3, 4).

The upper (left, lower, right) side is defined as the side on which IR sensor 1(2, 3, 4) is arranged.

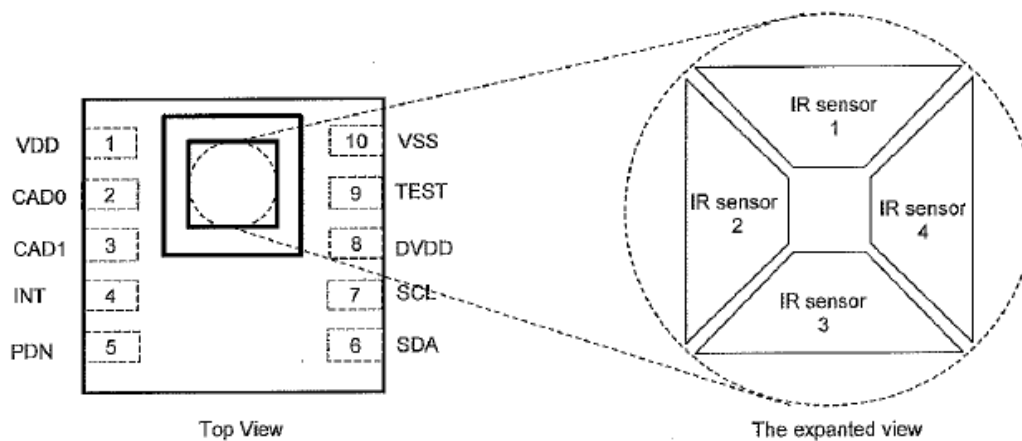


Figure 6.1. IR Sensor's Configurations

7. Absolute Maximum Ratings

(VSS= 0V)

Parameter		Symbol	Min.	Max.	Unit
Power Supply	VDD pin, DVDD pin	V+	-0.6	4.6	V
Input Current	All pins	Iin	-10	10	mA
Input Voltage (* 1)	CAD0 pin, CAD1 pin, INT pin, PDN pin, TEST pin, SCL pin, SDA pin	Vin	-0.6	4.6	V
Storage Temperature		Tst	-30	85	°C

Note:

* 1. Vin should be always lower than (V+) + (0.6V).

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

(VSS= 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supply (* 2)	During normal operation	VDD	1.71	3.3	3.63	V
	During the EEPROM write	EVDD	3.00	3.3	3.63	V
Digital Power Supply		DVDD	1.65	3.3	VDD	V
Operating Temperature		Ta	-30	25	85	°C

Notes:

* 2. VDD should always be higher than DVDD.

* 3. Keep environment no dew condensation.

9. Power Supply Conditions

(Unless otherwise specified, VDD=1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Power Supply Rise Time (* 4, * 5)	Time until VDD, DVDD, and PDN are set to the operating voltage from 0.2V.	VDD pin, DVDD pin	PSUP			50	ms
Power-on Reset Time (* 4, * 5)	Time until AK9753 becomes Power down Mode after PSUP.	VDD pin	PORT			3000	μs
Shutdown Voltage (* 5, * 6)	Shutdown Voltage for POR re-starting.	VDD pin, DVDD pin	SDV			0.2	V
Power Supply Interval Time (* 4, * 5, * 6)	Voltage retention time below SDV1 for POR re-starting.	VDD pin, DVDD pin	PSINT	3000			μs

Notes:

* 4. Reference data only, not tested.

* 5. Power-on Reset circuit detects the rising edge of VDD, resets the internal circuit, and initializes the registers. After Power-on reset, Stand-by Mode is selected.

* 6. The condition that POR surely works at the power-up the power-up again after power supply goes down. Unless this condition is satisfied, the reset may not be correctly expected.

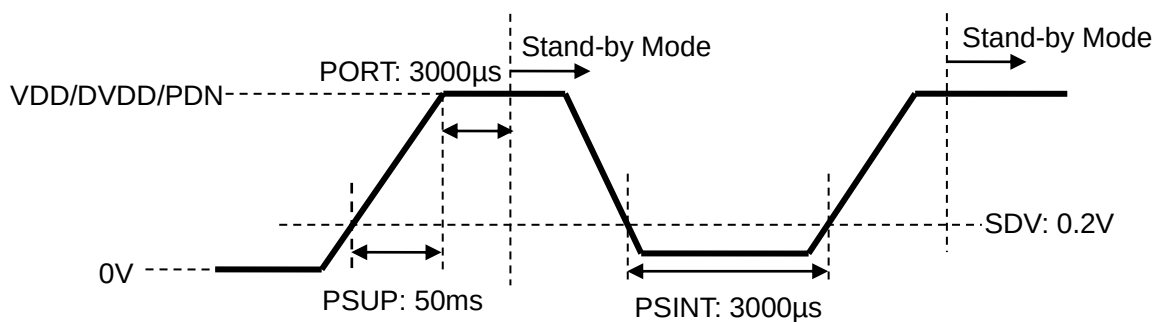


Figure 9.1. Power Supply Conditions

10. Electrical Characteristics • Optical Characteristics

10.1. Analog Characteristics

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

The following are the characteristics of sensor without lens.

Parameter		Symbol	Min.	Typ.	Max.	Unit
IR output resolution				16		bit
IR offset code	All output currents of four IR sensors are Zero. • Reference data only, not tested.		-36	0	36	Code
IR output code	• Ttgt= 35°C, Ta= 25°C ±3°C • 2's complement		4434H	4650H	486CH	Code
Relative sensitivity variations of four IR sensors	Ta= 25°C ±3°C				5	%
Temperature output resolution				10		bit
Temperature sensor range	• Linear to internal temperature (excludes noise) • 2's complement		-10		60	°C
			B980H		4380H	Code
Temperature sensor accuracy (* 7)	Ta= 35°C		-5.5		5.5	°C
Field of View	The combined range observed by Upper/Lower (Left/Right) • Reference data only, not tested. • Without lens	FOV		±80		deg(°)
Averaged current consumption	Power Down Mode PDN= "L"	SIDD			1	μA
	Stand-by Mode PDN= "H", EMODE [2:0] = "000"	IDD0			10	μA
	Continuous Mode 0 PDN= "H", EMODE [2:0] = "100"	IDD1			100	μA
	Continuous Mode 1 PDN= "H", EMODE [2:0] = "101"	IDD2			60	μA
	Continuous Mode 2 PDN= "H", EMODE [2:0] = "110"	IDD3			38	μA
	Continuous Mode 3 PDN= "H", EMODE [2:0] = "111"	IDD4			25	μA
Digital filter cut-off frequency	Eight levels can be selected by setting register. Typ. Fc=8.8/2 ⁿ (n=0 ~ 5)	Fc	0.2		9.7	Hz

Note:

* 7. Temperature sensor's output is as the following

At Ta= 35°C, (Temperature sensor's output)= (VDD-1.71) × 1.45+33.5±4.0 [°C]

10.2. Digital Characteristics**10.2.1. EEPROM**

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Retention Time	@Ta= 85°C	Ehold	10			years
Endurance			1000			times

Note:

* 8. VDD (EVDD) should be greater than 3.0V, when writing EEPROM.

10.2.2. DC Characteristics

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage 1		PDN pin	VIH1	80%DVDD			V
Low Level Input Voltage 1		PDN pin	VIL1			20%DVDD	V
High Level Input Voltage 2		SCL pin, SDA pin	VIH2	70%DVDD			V
Low Level Input Voltage 2		SCL pin, SDA pin	VIL2	-0.5		30%DVDD	V
High Level Input Voltage 3		CAD1 pin, CAD0 pin	VIH3	80%VDD			V
Low Level Input Voltage 3		CAD1 pin, CAD0 pin	VIL3			20%VDD	V
High Level Input Voltage 4	DVDD Monitor Function	DVDD pin	VIH4	80%VDD			V
Low Level Input Voltage 4		DVDD pin	VIL4			0.2	V
Hysteresis Voltage (* 9)	DVDD ≥ 2V	SCL pin, SDA pin	Vhys	5%DVDD			V
Low Level Output Voltage 1	IOL= 3mA DVDD ≥ 2V	SDA pin, INT pin	VOL1			0.4	V
Low Level Output Voltage 2	IOL= 3mA DVDD < 2V	SDA pin, INT pin	VOL2			20%DVDD	V

Note:

* 9. Reference data only, not tested.

10.2.3. AC Characteristics (1): Standard Mode (100 kHz)

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCL frequency		fSCL			100	kHz
SDA bus idle time to the next command input		fBUF	4.7			μs
Start condition Hold time		tHD:STA	4.0			μs
Clock Low period		tLOW	4.7			μs
Clock High period		tHIGH	4.0			μs
Start condition set-up time		tSU:STA	4.7			μs
Data hold time		tHD:DAT	0			μs
Data set-up time		tSU:DAT	250			ns
Rise time SDA, SCL (* 10)	SDA pin, SCL pin	tR			1.0	μs
Fall time SDA, SCL (* 10)	SDA pin, SCL pin	tF			0.3	μs
Stop condition set-up time		tSU:STO	4.0			μs
EEPROM write time		tWR	10			ms

Note:

* 10. Reference data only, not tested.

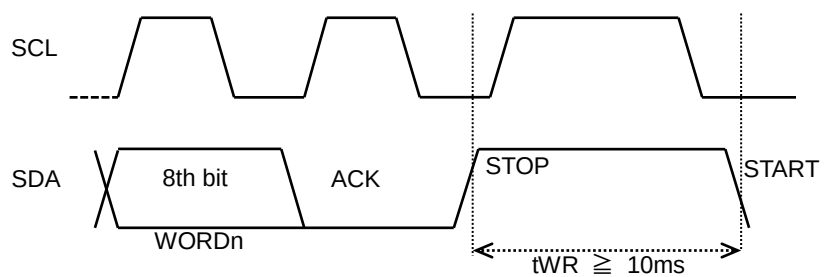
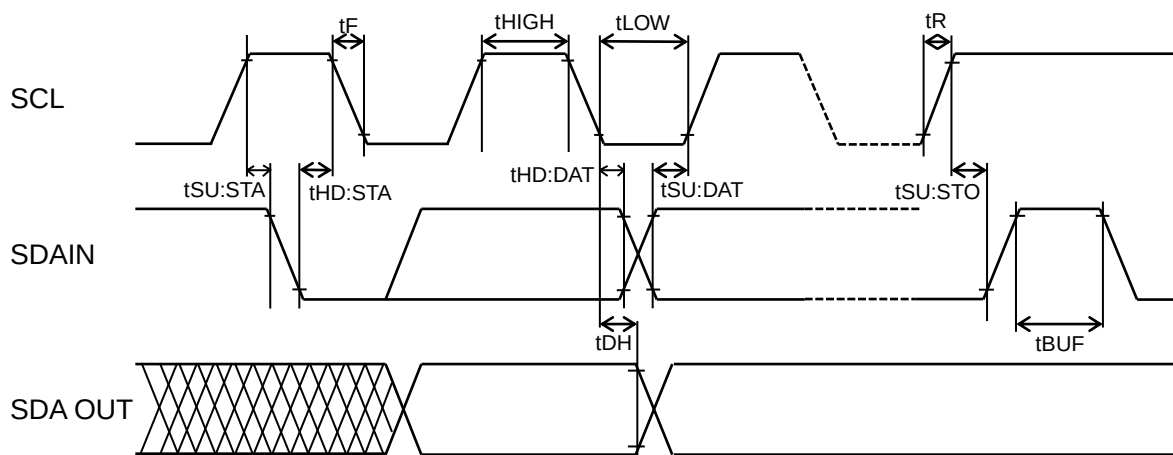
10.2.4. AC Characteristics (2): Fast Mode (400 kHz)

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCL frequency		fSCL			400	kHz
SDA bus idle time to the next command input		fBUF	1.3			μs
Start condition Hold time		tHD:STA	0.6			μs
Clock Low period		tLOW	1.3			μs
Clock High period		tHIGH	0.6			μs
Start condition set-up time		tSU:STA	0.6			μs
Data hold time		tHD:DAT	0			μs
Data set-up time		tSU:DAT	100			ns
Rise time SDA, SCL (* 11)	SDA pin, SCL pin	tR			0.3	μs
Fall time SDA, SCL (* 11)	SDA pin, SCL pin	tF			0.3	μs
Stop condition set-up time		tSU:STO	0.6			μs
EEPROM write time		tWR	10			ms

Note:

* 11. Reference data only, not tested.



11. Functional Descriptions

11.1 Power Supply States

When VDD, DVDD and PDN turn on from the state of VDD= DVDD= OFF(0V), Power-on Reset(POR) automatically operates, all registers will be initialized, and the AK9753 will be set to Stand-by Mode. Although all states of the Following table can exist, the state 2 is prohibited.

Table 11.1. Power Supply States and Functions

State	VDD pin	DVDD pin	PDN pin	I ² C	INT pin	Analog Circuit	IDD
1	OFF(0V)	OFF(0V)	"L"	Disable	Unfixed	Power Down	Unknown
2	OFF(0V)	1.65 ~ 3.63V	"H" or "L"	Disable	Unfixed	Power Down	Unknown
3	1.71 ~ 3.63V	OFF(0V)	"L"	Disable	Unfixed	Power Down	Unknown
4	1.71 ~ 3.63V	OFF(0V)	"H"	Disable	Unfixed	Power Down	Unknown
5	1.71 ~ 3.63V	1.65V ~ VDD	"L"	Disable	"H"	Power Down	< 1μA
6	1.71 ~ 3.63V	1.65V ~ VDD	"H"	Enable	"H"	POR circuit only operates	< 10μA

11.2 Reset functions

When VDD turns ON, set up DVDD lower than VDD(DVDD ≤ VDD).

Power-on Reset (POR) operates unit VDD reaches the operating voltage (1.4V Typ.). After POR, all registers are set to initial values, and Stand-by Mode is selected.

AK9753 has five reset functions.

(1) Power-on Reset(POR)

Power-on Reset circuit resets AK9753 by detecting VDD and DVDD rising.

When VDD and DVDD turns ON with PDN pin= "L", POR does not operate, because POR circuit is also in PD state.

(2) Hardware Reset

AK9753 is reset by PDN pin= "L"

(3) Software Reset

AK9753 is reset by setting SRST bit.

(4) DVDD Monitor Reset

When DVDD turns OFF (DVDD ≤ 0.2V), AK9753 is reset.

(5) Power Supply Reset

AK9753 is reset by VDD= 0V.

When AK9753 is reset, all registers are set to initial values.

11.3 Operating Mode

11.3.1. Normal Mode/Switch Mode

AK9753 has two Modes, Normal Mode and Switch Mode.

Normal Mode is the mode which controls AK9753 by using I²C interface. The digital output the four IR sensors and the internal temperature sensor can be used through the I²C interface in Normal Mode. INT output also can be used.

Switch Mode is the mode which uses only INT output without using I²C interface. When the differential output of two sensors (IR1 - IR3 / IR2 - IR4) exceeds the upper / lower thresholds which are set to EEPROM, INT output turns "active". When the differential output of two sensors (IR1 - IR3 / IR2 - IR4) is in the range which is set to EEPROM, INT output is "non-active". The hysteresis for the thresholds can be set to EEPROM for avoiding the chattering of INT output. When Switch Mode is used, the threshold and the hysteresis should be set to EEPROM beforehand. When the accuracy of HumanSensing is not cared, Switch Mode can be used.

Normal Mode / Switch Mode selection is controlled by the CAD1 pin and CAD0 pin.

When CAD1 pin and CAD0 pin are set as CAD1 pin= CAD0 pin= "H", the digital output can be used through the I²C interface.

When CAD1 pin and CAD0 pin are set as CAD1 pin= CAD0 pin= "H", Switch Mode is selected. When Switch Mode is selected, SCL pin and SDA pin should be tied to "H". (Do not access the AK9753 through the I²C interface in Switch Mode.)

Table 11.2. CAD0 / CAD1 pin Setting and Slave Address

CAD1	CAD0	I ² C output	Slave address	Mode
L	L	Enable	64H	Normal Mode
L	H	Enable	65H	Normal Mode
H	L	Enable	66H	Normal Mode
H	H	Disable	Prohibited	Switch Mode

11.3.2. Normal Mode

There are the eight Modes in Normal Mode.

<Normal Mode (CAD0 pin= "L" or CAD1 pin= "L")>

- (1) Power down Mode
- (2) Stand-by Mode
- (3) Single shot Mode
- (4) Continuous Mode 0
- (5) Continuous Mode 1
- (6) Continuous Mode 2
- (7) Continuous Mode 3
- (8) EEPROM access Mode

Power down Mode:

The all circuits are powered down for saving the current consumption.

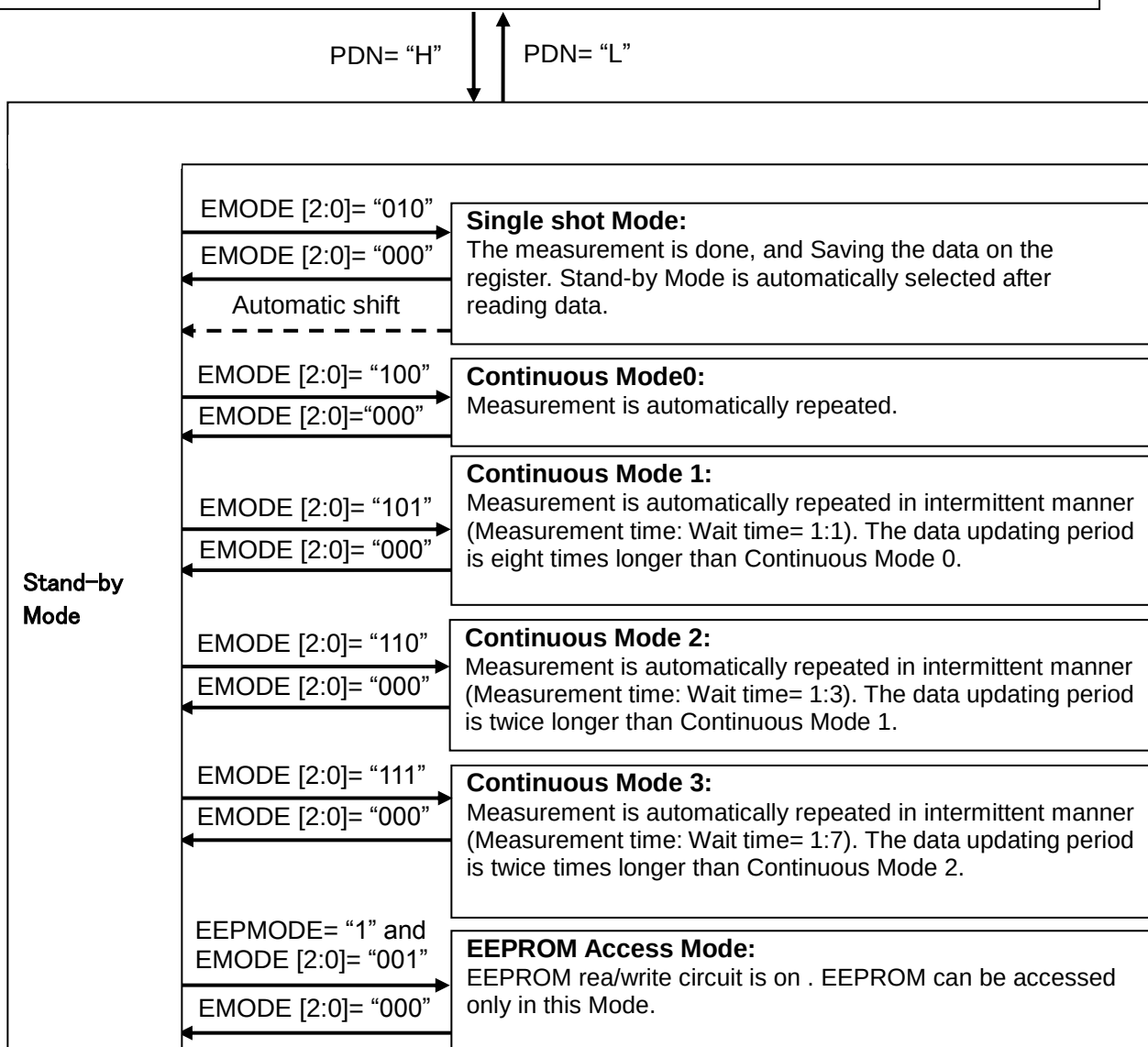


Figure 11.1. Various Modes in normal Mode.

On initial power-on with PDN pin= "H", AK9753 is in Stand-by Mode. Based on EMODE [2:0] setup, the AK9753 shifts to the selected Mode, and starts operating. Any Mode changing should be done via Stand-by Mode.

11.3.3. Switch Mode

There are two Modes in Switch Mode.

<Switch Mode (CAD0 pin= CAD1 pin= "H")>

- (1) Power down Mode
- (2) Measurement Mode

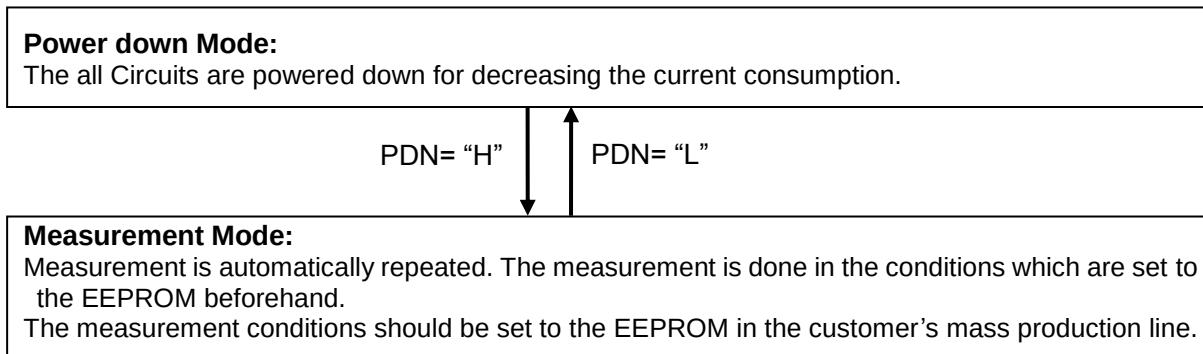


Figure 11.2. Various Modes in Switch Mode

11.4 Descriptions for each Operating Mode

11.4.1. Power down Mode (PDN pin= “L”)

All circuits are powered off and all internal resistors are reset with PDN pin= “L”. The all functions of AK9753 do not work in this Mode.

11.4.2. Stand-by Mode (EMODE [2:0] = “000”)

All circuits are powered off except for POR circuit. All registers can be accessed in this Mode.

Read / Write register data are retained, and reset by software reset.

However, EEPROM data cannot be read / written in this Mode. Reading/Writing EEPROM data must be done in EEPROM access Mode.

The data registers (ST1 to ST2) should not be accessed in Stand-by Mode. It causes the malfunction of AK9753.

11.4.3. EEPROM Access Mode (EMODE [2:0] = “001” and EEPMODE= “1”)

When EMODE [2:0] bits are changed from Stand-by Mode (EMODE [2:0] = “000”) to EMODE [2:0] = “100” and EEPROM bit is set as “1”, EEPROM Access Mode is selected. Reading / Writing EEPROM data should be done in EEPROM Access Mode. When EKEY [7:0] bit is set as “A5H” in EEPROM Access Mode, the data can be written to EEPROM.

Data measurement is not done in EEPROM Access Mode.

11.4.4. Single Shot Mode (EMODE [2:0] = “010”)

When AK9753 is set to Single shot Mode (EMODE [2:0] = “010”), measurement is done once, and the Measurement data is stored to the measurement data registers (IR1L to TMPH). Then the analog circuits except for POR circuit are automatically powered off. When the registers from ST1 to ST2 are read, the AK9753 automatically shifts to Stand-by Mode (EMODE [2:0] = “000”). Measurement time is defined in EFC [2:0] (Table16.1).

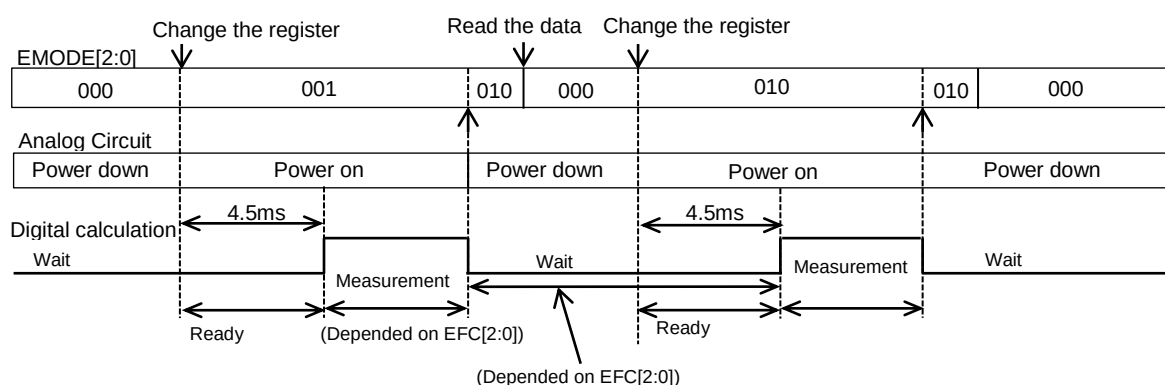


Figure 11.3. Single shot Mode

11.4.5. Continuous Mode 0 (EMODE [2:0] = "100")

When Continuous Mode 0 (EMODE [2:0] = "100") is selected the measurement is automatically repeated at the cycle which is determined by the digital filter cut-off frequency (EFC [2:0], Table 16.2).

When a measurement have been done, the measurement data is stored to the measurement register (IR1L to TMPH), and new measurement is started. * Please refer to Table16.1 for first measurement time.

This Mode is terminated by setting the AK9753 to Stand-by Mode (EMODE [2:0] = "000").

When EMODE [2:0] is re-written during a measurement, the measurement is interrupted. Then the last data is retained to the register.

When Continuous Mode 0 is selected, a register write command should be executed. If register write command should be executed during a measurement, a right measurement data cannot be gotten.

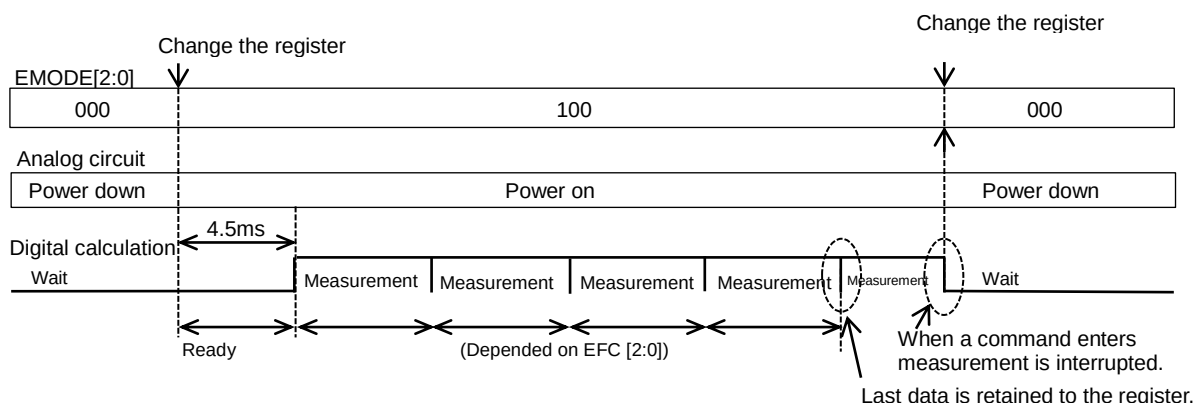


Figure 11.4. Continuous Mode 0

11.4.6. Continuous Mode 1,2,3 (EMODE [2:0] = "101", "110", "111")

When Continuous Mode 1, 2, and 3 (EMODE [2:0] = "101", "110", "111") are selected, a measurement and a wait are automatically repeated at the cycle according to the selected measurement Mode (EMODE [2:0]) and the digital filter cut-off frequency (EFC [2:0]).

A wait time length depends on the measurement Mode. When a measurement has been done, the measurement data is stored to the measurement register (IR1L to TMPH).

This Mode is terminated by setting the AK9753 to Stand-by Mode (EMODE [2:0] = "000").

When EMODE [2:0] is re-written during a measurement, the measurement is interrupted. Then the last data is retained to the register.

When Continuous Mode 1, 2, and 3 is selected, a register write command should be executed. If a register write command should be executed during a measurement, a right measurement data cannot be gotten. * Please refer to Table16.1 for first measurement time.

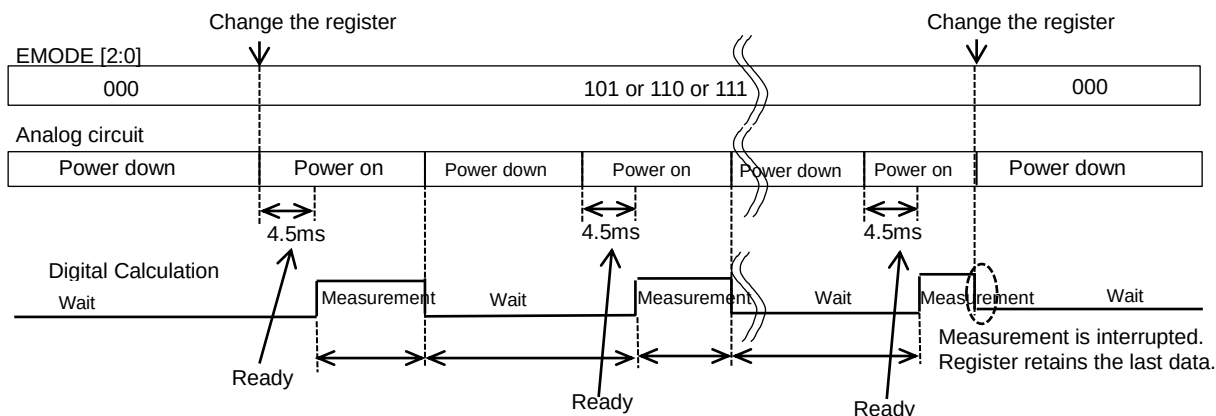


Figure 11.5. Continuous Mode 1, 2, and 3

11.5 Read Measurement Data

When a measurement data is stored to the measurement register, DRDY bit of ST1 register changes to "1". This state is called "Data Ready". It can be set up so that INT output "H", when the DRDY bit is "1", by setting up the interruption register.

The read-out procedure is detailed here. (Single shot Mode is used as an example.)

The same procedure can also be applied the Continuous Mode 0 (1, 2, and 3).

11.5.1. Normal Read-out Procedure

(1) Read-out ST1 registers

DRDY: DRDY shows whether the state is "Data Ready" or not.

DRDY = "0" means "No Data Ready".

DRDY = "1" means "Data Ready".

It is recommended that measurement data is read-out with DRDY = "1".

DOR: DOR shows whether there are any data which was not read out before initiating the current read.

DOR = "0" means that there are no data which was not read out before initiating the current read.

DOR = "1" means that there are data which was not read out before initiating the current read.

(2) Reading measurement data

Once a data read is initiated from one of the measurement data registers (IR1L to TMP) or the ST2 register, the AK9753 recognizes that a data read-out has begun. When a data read-out is initiated, DRDY and DOR change to "0".

(3) Reading ST2 Registers (Required Operation)

The AK9753 recognizes that a data read-out has finished out the ST2 registers. Because the measurement data registers are protected while reading out, data is not updated. Data protection of the measurement data registers is canceled by reading out the ST2 register. The ST2 register must be read out after accessing the measurement data register.

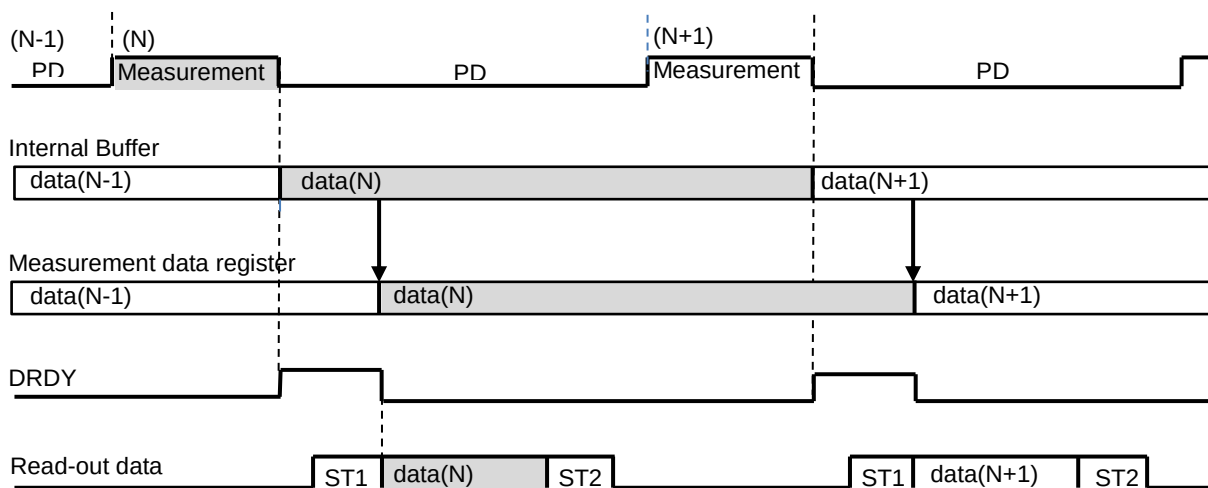


Figure 11.6. Normal Read-out Procedure

11.5.2. Read-out Data within a measurement Period

The measurement data register is retained within a measurement period, so the data can be read out within the measurement period. When data is read out within the measurement period, the previous data retained is read out.

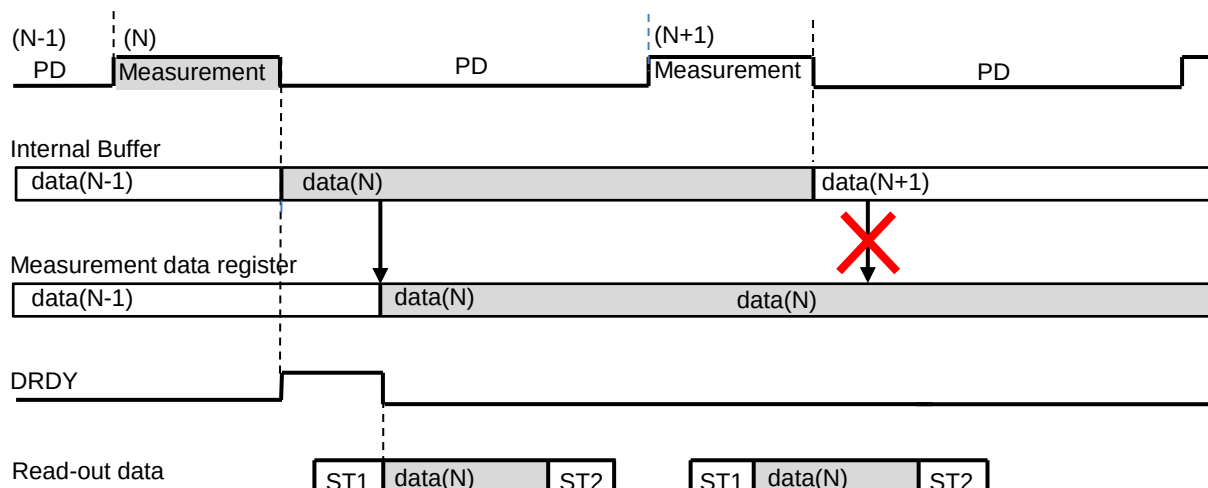


Figure 11.7. Read-out data within a measurement period

11.5.3. Skipping Data

When measurement data is not read out between the end points of (N+1)th and Nth measurement, DRDY is held until the measurement data is read out. In this case, because the Nth data was skipped, the DOR bit is "1".

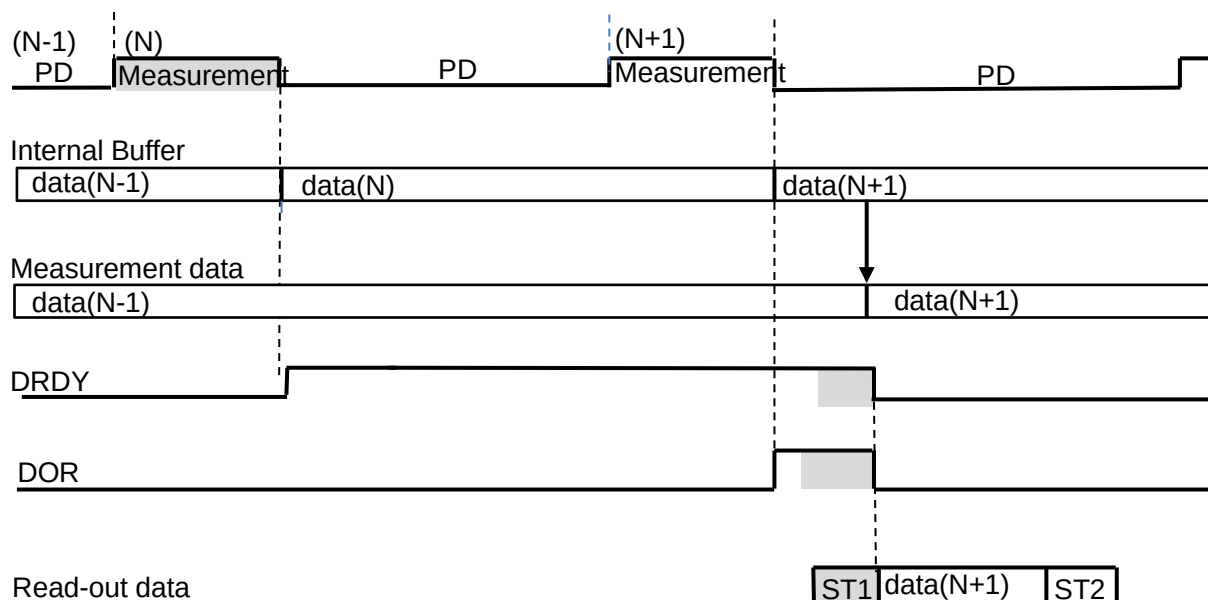


Figure 11.8. Skipping Data

When a data read begins after the end of the Nth measurement, and when data read cannot be completed until the end of the (N+1)th measurement, the measurement data registers are protected to read data normally. In this case, because the (N+1)th data has been skipped, the DOR bit transitions to “1”.

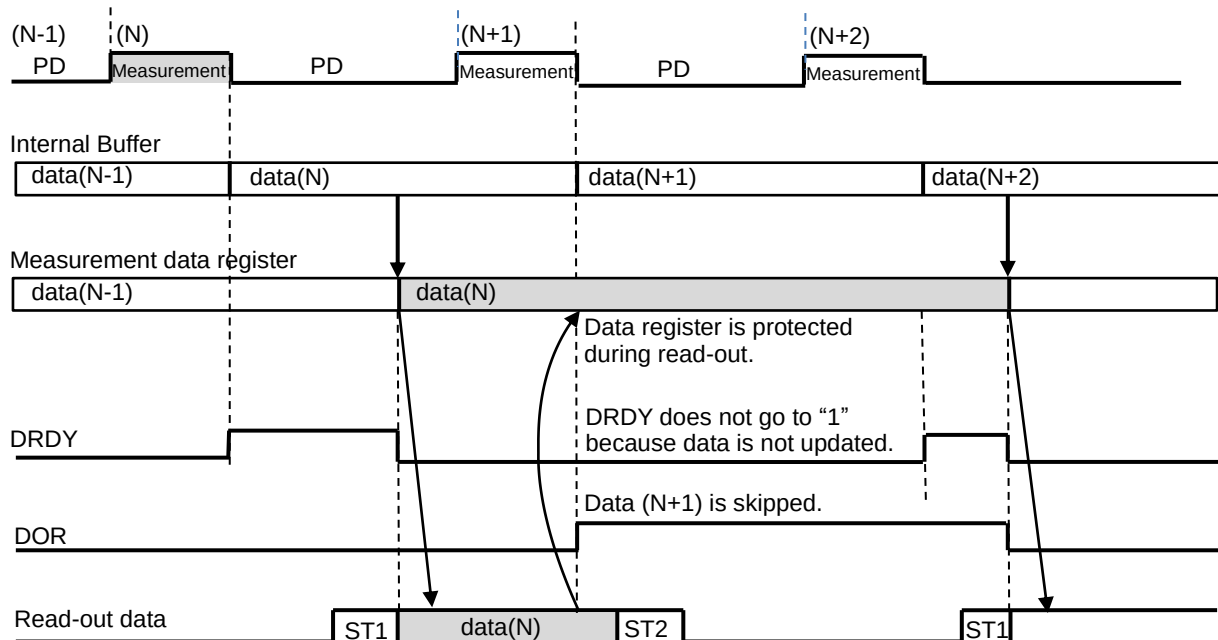


Figure 11.9. The data read cannot be completed until the beginning of the next measurement.

In both of these cases, the DOR bit changes to “0” from “1”, at the start of reading data if DRDY is “1”.

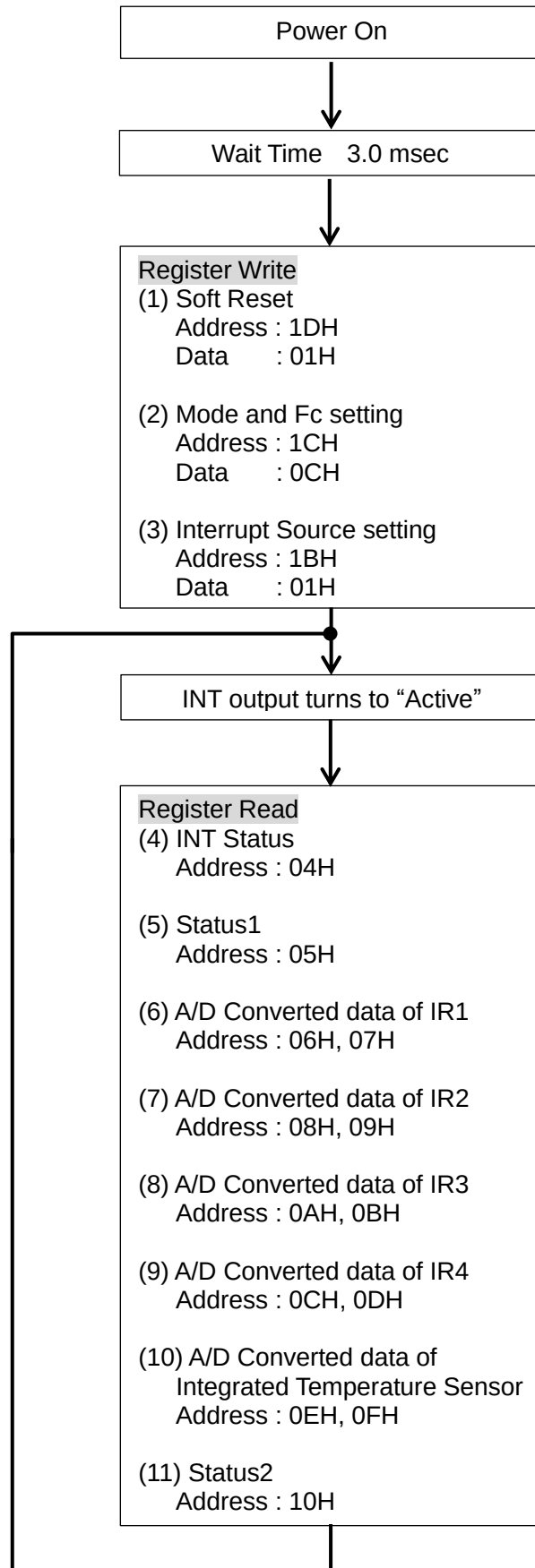
11.5.4. End Operation

Select Stand-by Mode (EMODE [2:0] = “000”) to complete the Continuous Mode 0 (1, 2, and 3).

11.5.5. Example of Read-out Procedure

Example of read-out procedure of AK9753 data is shown in the following. The below settings are assumed.

- Continuous Mode 0
 - > Measurement is automatically repeated.
- Digital Filter Cutoff Frequency $F_c=0.6\text{Hz}$
- Data ready interrupt setting is enable.
 - > INT output turns to “Active” at the timing of data ready.
 - After that, HOST MCU should read out the data.



12. Serial Interface

The I²C bus interface of the AK9753 supports Standard Mode (Max. 100kHz) and High Speed Mode (Max. 400kHz).

12.1. Data Transfer

Initially the start condition should be input to access the AK9753 through the bus. Next, send a one byte slave address, which includes the device address. The AK9753 compares the slave address, and if these addresses match, the AK9753 generates an acknowledge signal and executes a Read / Write command. The stop condition should be input after executing a command.

12.1.1. Changing state of the SDA line

The SDA line state should be changed only while the SCL line is "L". The SDA line state must be maintained while the SCL line is "H". The SDA line state can be changed while the SCL line is "H", only when a Start Condition or a Stop Condition is input.

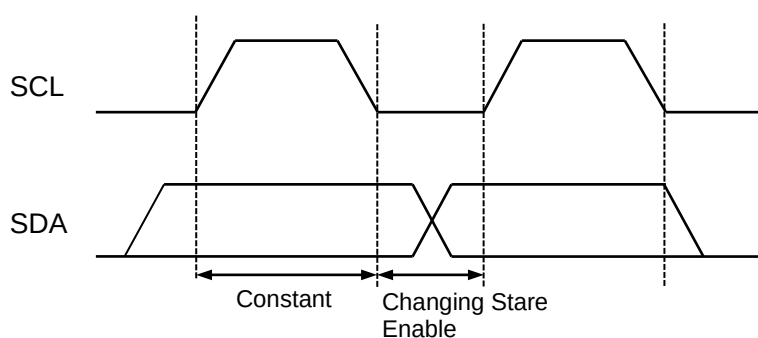


Figure 12.1. Changing state of SDA line

12.1.2. Start / Stop Conditions

A Start Condition is generated when the SDA line state is changed from "H" to "L" while the SCL line is "H". All command start from a Start condition.

A Stop condition is generated when the SDA line state is changed from "L" to "H" while the SCL line is "H". All command end after a Stop condition.

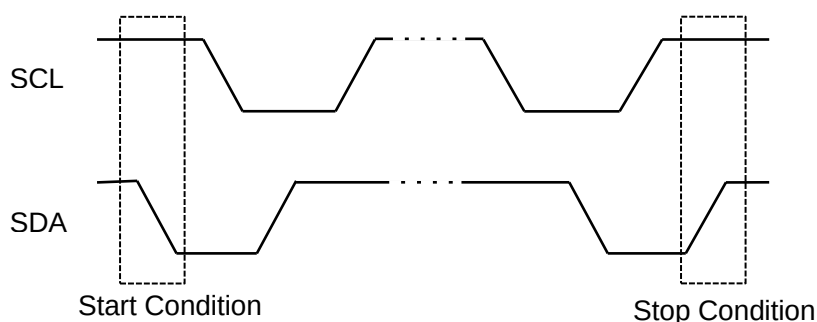


Figure 12.2. Start / Stop Conditions

12.1.3. Acknowledge

The device transmitting data will release the SDA line after transmitting one byte of data (SDA line state is “H”). The device receiving data will pull the SDA line to “L” during the next clock. This operation is called “Acknowledge”. The Acknowledge signal can be used to indicate successful data transfers.

The AK9753 will output an acknowledge signal after receiving a Start condition and Slave address.

The AK9753 will output an acknowledge signal after receiving each byte, when the WRITE instruction is transmitted.

The AK9753 will transmit the data stored in the selected address after outputting an acknowledge signal, when a READ instruction is transmitted. Then the AK9753 will monitor the SDA line after releasing the SDA line. If the master device generates an Acknowledge instead of Stop condition, the AK9753 transmits an 8-bit data stored in the next address. When the Acknowledge is not generated, transmitting data is terminated.

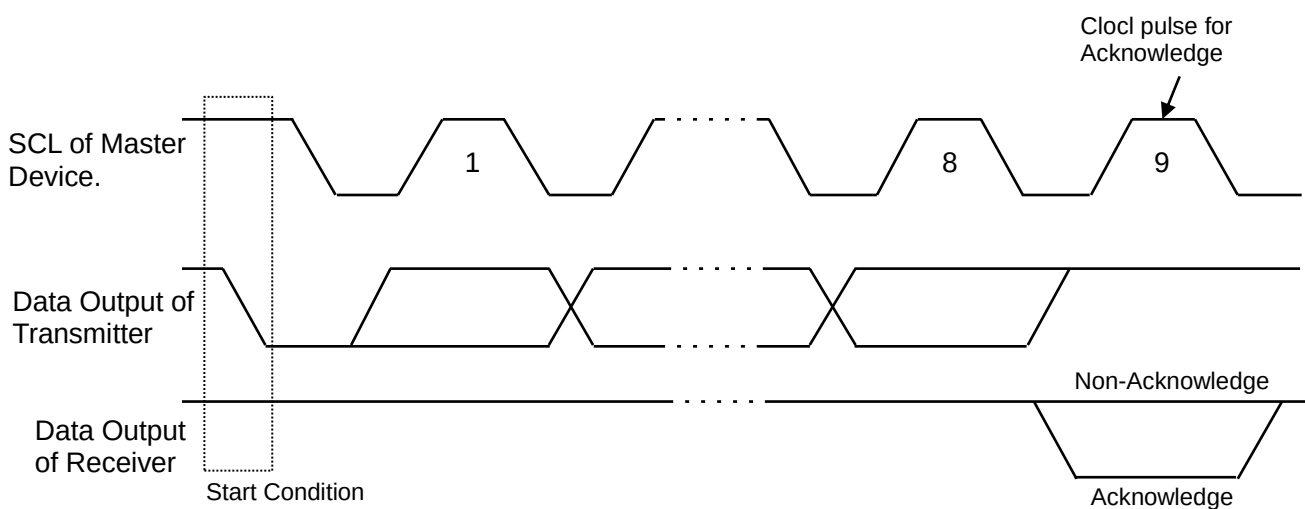


Figure 12.3. Acknowledge

12.1.4. Slave Address

The Slave address of the AK9753 can be selected from the following list by setting the CAD0/1 pins. When the CAD0/1 pins are connected to VSS, the Slave address bit is = 64H. When the CAD0/1 pins are connected to VDD, the Slave address bit is 65H. Do not set up “CAD1 pin = CAD0 pin = H” while the I²C interface is used, because the “CAD1 pin = CAD0 pin = H state is only for Switch Mode.

Table 12.1. CAD0/1 pin setting and Slave Address

CAD1 pin	CAD0 pin	Slave Address
L	L	64H
L	H	65H
H	L	66H
H	H	Switch Mode

When the first one byte data including the Slave address is transmitted after a Start condition, the device, which is specified as the communicator by the Slave address on bus, selected.

After transmitting the Slave address, the device that has the corresponding device address will execute a command after transmitting an Acknowledge signal. The 8-bit (Least Significant bit-LSB) of the first one byte is the R/W bit.

When the R/W bit is set to “1”, a READ command is executed. When the R/W bit is set to “0”, a WRITE command is executed.

MSB					LSB		
1	1	0	0	1	CAD1	CAD0	R/W

Figure 12.4. Slave Address

12.1.5. WRITE Command

When the R/w bit set to "0", the AK9753 executes a WRITE Operation. The AK9753 will out an Acknowledge signal and receive the second byte, after receiving a Start condition and first one byte (Slave address) in a WRITE Operation. The second byte has an MSB-first configuration, and specifies the address of the internal control register.

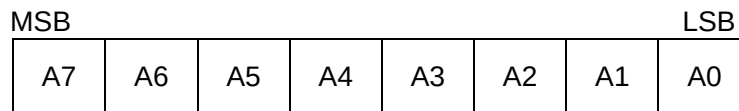


Figure 12.5. Register Address

The AK9753 will generate an Acknowledge and receive the third byte after receiving the second byte (Register Address).

The data after the third byte is the control data. The control data consists of 8-bit and has an MSB-first configuration. The AK9753 generates an Acknowledge for each byte received. The data transfer is terminated by a Stop condition, generated by the master device.

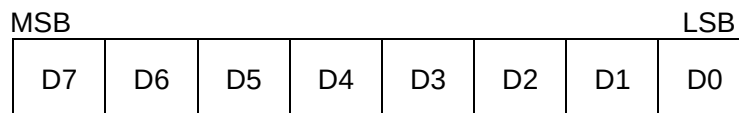


Figure 12.6. Control data

Two or more bytes can be written at once. The AK9753 generates an Acknowledge and receives the next data after receiving the third byte (Control Data). When the following data is transmitted without a Stop condition, after transmitting one byte, the internal address counter is automatically incremented, and data is written in the next address.

The automatic increment function works in the address from 11H to 1CH. When the start address is "11H", the address is repeatedly incremented as. "11H -> 12H ->.....-> 1CH -> 11H -> 12H..."

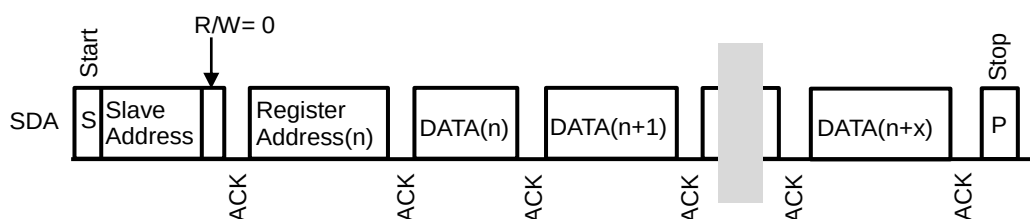


Figure 12.7. WRITE Operation

12.1.6. READ Command

When the R/W bit is set to "1", the AK9753 executes a READ Operation. When the AK9753 transmits data from the specified address, the master device generates an Acknowledge instead of a Stop condition and the next address data can be read out.

The AK9753 supports both current address read and random address read. The automatic increment function works in the address of 05H to 10H.

When the address 10H is read out, the next address returns to 05H.

(1) Current Address Read

The AK9753 has an integrated address counter. The data specified by the counter is read out in the current address read operation. The internal address counter retains the next address which is accessed at last. For example, when the address which was accessed last is "n", the data of address "n+1" is read out by the current address read instruction.

The AK9753 will generate an Acknowledge after receiving a Slave address for a Read command (R/W bit = "1") in the current address read operation. Then the AK9753 will start to transmit the data specified by the internal address counter at the next clock, and will increment the internal address counter by one. When the AK9753 generates a Stop condition instead of an Acknowledge after transmitting the one byte data, a Read out operation is terminated.

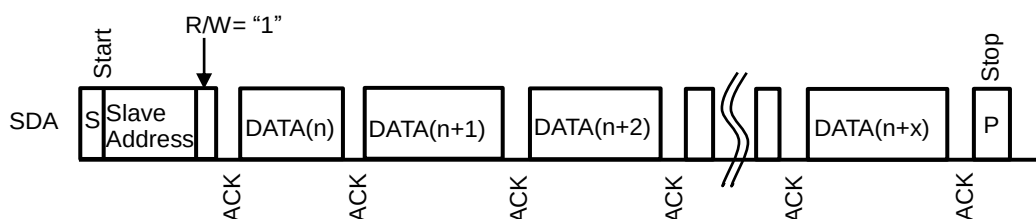


Figure 12.8. Current Address Read

(2) Random Read

Data from an arbitrary address can be read out by a random read operation. A random read requires the input of a dummy WRITE instruction before the input of a slave address of a READ instruction (R/W bit = "1"). To execute a random read, first generate a start condition, then input the slave address for a WRITE instruction (R/W bit = "0") and a read address, sequentially.

After the AK9753 generates an Acknowledge in response to this address input, generate a start condition and the slave address for a READ instruction (R/W) R/W bit = "1" again. The AK9753 generates an Acknowledge in response to the input of this slave address. Next, the AK9753 output the data at the specified address, then increments the internal address counter by one.

When a Stop condition from the master device is generated instead of an Acknowledge after the AK9753 outputs data, Read operation stops.

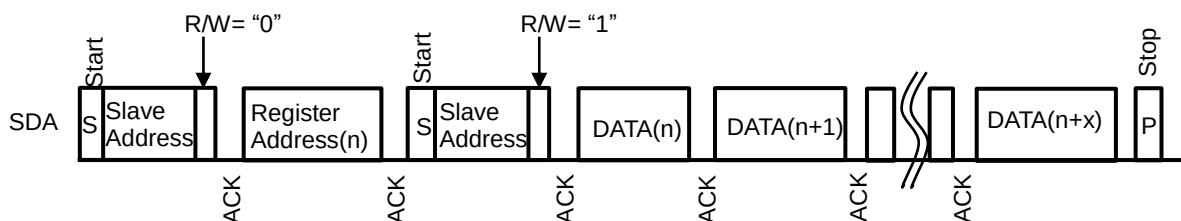


Figure 12.9. Random Read

12.1.7. EEPROM Write Timing

Writing data to EEPROM should be done at shown timing as the following.

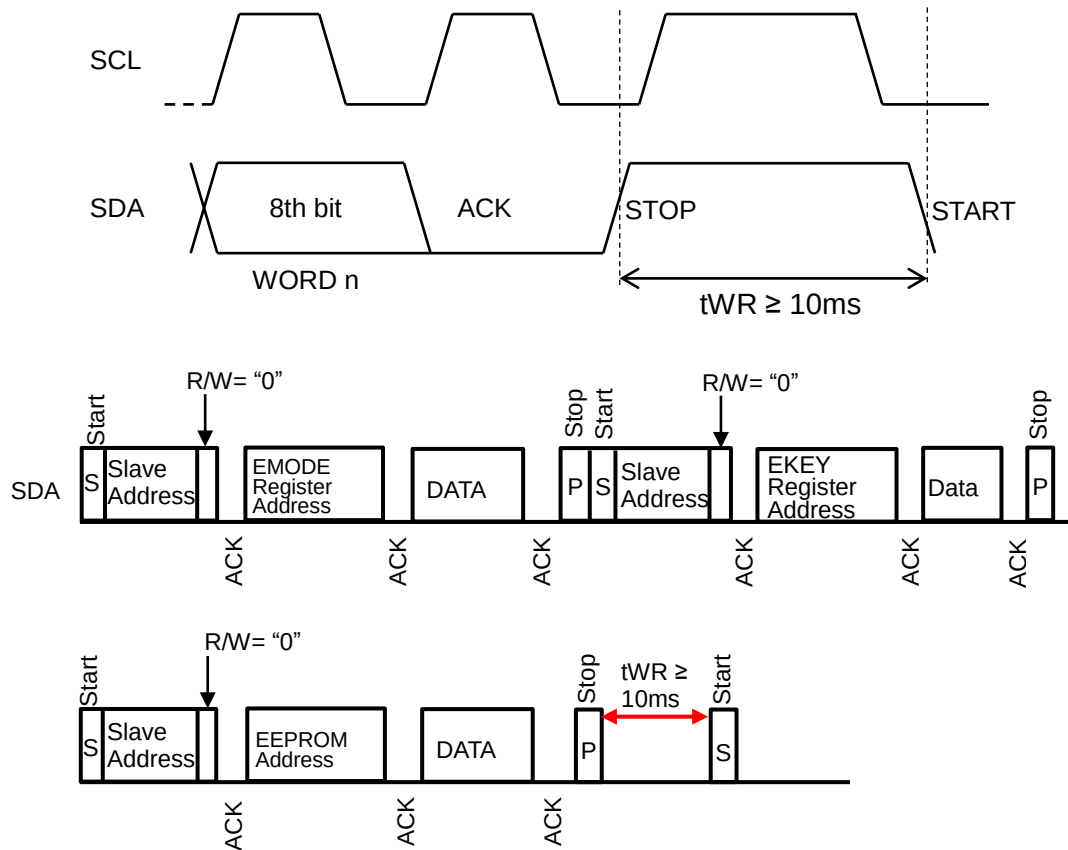


Figure 12.10. EEPROM Write Timing

Writing data to EEPROM should be done as the sequence that is shown in Figure 12.10.

Writing data to EEPROM can be done after setting EMODE [2:0] = "001", EEPROMODE = "1" and EKEY [7:0] = "A5H".

Writing data to EEPROM is started at the Stop Condition after inputting the data, and terminated at the Start Condition. EEPROM write time (t_{WR}) should be longer than 10ms.

Two or more bytes cannot be written at once in writing data to EEPROM should be done after setting EKEY [7:0] = "A5H" again.

On the other hand, reading data from EEPROM is able to be continuously done.

13. Memory Map

Table 13.1. Register Map

Name	Address	Soft Reset	R/W	Data	
				Content	bit
WIA1	00H	Disable	R	Company Code	8
WIA2	01H	Disable	R	Device ID	8
INFO1	02H	Disable	R	Information	8
INFO2	03H	Disable	R	Information	8
INTST	04h	Enable	R	Interrupt Status	3
ST1	05H	Enable	R	Status 1	2
IR1L	06H	Enable	R	IR1 A/D Converted data (Low)	8
IR1H	07H	Enable	R	IR1 A/D Converted data (High)	8
IR2L	08H	Enable	R	IR2 A/D Converted data (Low)	8
IR2H	09H	Enable	R	IR2 A/D Converted data (High)	8
IR3L	0AH	Enable	R	IR3 A/D Converted data (Low)	8
IR3H	0BH	Enable	R	IR3 A/D Converted data (High)	8
IR4L	0CH	Enable	R	IR4 A/D Converted data (Low)	8
IR4H	0DH	Enable	R	IR4 A/D Converted data (High)	8
TMPL	0EH	Enable	R	Integrated Temperature Sensor Output (Low)	8
TMPH	0FH	Enable	R	Integrated Temperature Sensor Output (High)	8
ST2	10H	Disable	R	Status 2 (dummy)	-
ETH13H	11H	Enable	R/W	IR1 – IR3 Upper Threshold level (Low)	6
ETH13H	12H	Enable	R/W	IR1 – IR3 Upper Threshold level (High)	6
ETH13L	13H	Enable	R/W	IR1 – IR3 Lower Threshold level (low)	6
ETH13L	14H	Enable	R/W	IR1 – IR3 Lower Threshold level (High)	6
ETH24H	15H	Enable	R/W	IR2 – IR4 Upper Threshold level (Low)	6
ETH24H	16H	Enable	R/W	IR2 – IR4 Upper Threshold level (High)	6
ETH24L	17H	Enable	R/W	IR2 – IR4 Lower Threshold level (Low)	6
ETH24L	18H	Enable	R/W	IR2 – IR4 Lower Threshold Level (High)	6
EHYS13	19H	Enable	R/W	IR1 – IR3 Hysteresis of Threshold	5
EHYS24	1AH	Enable	R/W	IR2 – IR4 Hysteresis of Threshold	5
EINTEN	1BH	Enable	R/W	Interrupt Source Setting	5
ECNTL1	1CH	Enable	R/W	Mode Setting Fc Setting	7
CNTL2	1DH	Enable	R/W	Soft Reset	3

Note:

* 12. When Switch Mode (CAD1 = “H” and CAD0 = “H”) is selected, “ETH13H to ECNTL1” of registers data (Address 11H to 1CH) copies “ETH13H to ECNTL1” of EEPROM data (Address 51H to 5CH).

Table 13.2. EEPROM Map

Name	Address	R/W	Data	
			Content	bit
EKEY	50H	R/W	EEPROM Access key (* 13)	8
ETH13H	51H	R/W	IR1 – IR3 Upper Threshold level (Low)	6
ETH13H	52H	R/W	IR1 – IR3 Upper Threshold level (High)	6
ETH13L	53H	R/W	IR1 – IR3 Lower Threshold level (Low)	6
ETH13L	54H	R/W	IR1 – IR3 Lower Threshold level (High)	6
ETH24H	55H	R/W	IR2 – IR4 Upper Threshold level (Low)	6
ETH24H	56H	R/W	IR2 – IR4 Upper Threshold level (High)	6
ETH24L	57H	R/W	IR2 – IR4 Lower Threshold level (Low)	6
ETH24L	58H	R/W	IR2 – IR4 Lower Threshold level (High)	6
EHYS13	59H	R/W	IR1 – IR3 Hysteresis of Threshold	5
EHYS24	5AH	R/W	IR2 – IR4 Hysteresis of Threshold	5
EINTEN	5BH	R/W	Interrupt Factor Setting	5
ECNTL1	5CH	R/W	Mode Setting Fc Setting	7

Note:

* 13. EKEY is registers. When EEPROM Access Mode (EMODE [2:0] bits = “001” and EEPMODE bit = “1”) is selected, EEPROM can be written by setting EKEY [7:0] bits = “A5H”.

14. Registers Functional Descriptions
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Table 14.1. Register Detail Map

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	WIA1	0	1	0	0	1	0	0	0
01H	WIA2	0	0	0	1	0	0	1	1
02H	INFO1	0	0	0	0	0	0	0	1
03H	INFO2	0	0	0	0	0	0	0	0
04H	INTST	1	1	1	IR13H	IR13L	IR24H	IR24L	DR
05H	ST1	1	1	1	1	1	1	DOR	DRDY
06H	IR1L	IR1_7	IR1_6	IR1_5	IR1_4	IR1_3	IR1_2	IR1_1	IR1_0
07H	IR1H	IR1_15	IR1_14	IR1_13	IR1_12	IR1_11	IR1_10	IR1_9	IR1_8
08H	IR2L	IR2_7	IR2_6	IR2_5	IR2_4	IR2_3	IR2_2	IR2_1	IR2_0
09H	IR2H	IR2_15	IR2_14	IR2_13	IR2_12	IR2_11	IR2_10	IR2_9	IR2_8
0AH	IR3L	IR3_7	IR3_6	IR3_5	IR3_4	IR3_3	IR3_2	IR3_1	IR3_0
0BH	IR3H	IR3_15	IR3_14	IR3_13	IR3_12	IR3_11	IR3_10	IR3_9	IR3_8
0CH	IR4L	IR4_7	IR4_6	IR4_5	IR3_4	IR4_3	IR4_2	IR4_1	IR4_0
0DH	IR4H	IR4_15	IR4_14	IR4_13	IR4_12	IR4_11	IR4_10	IR4_9	IR4_8
0EH	TMPL	TMP_7	TMP_6	TMP_5	TMP_4	TMP_3	TMP_2	TMP_1	TMP_0
0FH	TMPH	TMP_15	TMP_14	TMP_13	TMP_12	TMP_11	TMP_10	TMP_9	TMP_8
10H	ST2	1	1	1	1	1	1	1	1
11H	ETH13H	ETH13H_4	ETH13H_3	ETH13H_2	ETH13H_1	ETH13H_0	0	0	0
12H	ETH13H	0	ETH13H_11	ETH13H_10	ETH13H_9	ETH13H_8	ETH13H_7	ETH13H_6	ETH13H_5
13H	ETH13L	ETH13L_4	ETH13L_3	ETH13L_2	ETH13L_1	ETH13L_0	0	0	0
14H	ETH13L	0	ETH13L_11	ETH13L_10	ETH13L_9	ETH13L_8	ETH13L_7	ETH13L_6	ETH13L_5
15H	ETH24H	ETH24H_4	ETH24H_3	ETH24H_2	ETH24H_1	ETH24H_0	0	0	0
16H	ETH24H	0	ETH24H_11	ETH24H_10	ETH24H_9	ETH24H_8	ETH24H_7	ETH24H_6	ETH24H_5
17H	ETH24L	ETH24L_4	ETH24L_3	ETH24L_2	ETH24L_1	ETH24L_0	0	0	0
18H	ETH24L	0	ETH24L_11	ETH24L_10	ETH24L_9	ETH24L_8	ETH24L_7	ETH24L_6	ETH24L_5
19H	EHYS13	1	1	1	EHYS13_4	EHYS13_3	EHYS13_2	EHYS13_1	EHYS13_0
1AH	EHYS24	1	1	1	EHYS24_4	EHYS24_3	EHYS24_2	EHYS24_1	EHYS24_0
1BH	EINTEN	1	1	0	IR13HI	IR13LI	IR24HI	IR24LI	DRI
1CH	ECNTL1	1	ECPMODE	EFC_2	EFC_1	EFC_0	EMODE_2	EMODE_1	EMODE_0
1DH	CNTL2	1	1	1	1	1	1	1	SRST

[Functional Descriptions]

1). WIA1: Company Code (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	WIA1	0	1	0	0	1	0	0	0

1 Byte fixed code as Company code of AKM.

2). WIA2: Device ID (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	WIA2	0	0	0	1	0	0	1	1

1 Byte fixed code as AKM device ID.

3). INFO1: Information (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	INFO1	0	0	0	0	0	0	0	1

INFO1 [7:0]: Information for AKM use only.

4). INFO2: Information (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	INFO2	0	0	0	0	0	0	0	0

INFO2 [7:0]: Reserve

5). INTST: Interrupt Status (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	INTST				IR13H	IR13L	IR24H	IR24L	DR
Reset		1	1	1	0	0	0	0	0

When the correspondent bit in the Interrupt Source Register (EINTEN) is enabled, the interrupt to the host MCU is available. When the interruption happens, the interrupt source is confirmed by reading the interrupt status register. When INST register is read out, INT pin turns to “non-active”.
This register is reset, when the differential signal of two IR sensors (IR1 - IR3 / IR2 - IR4) are below “the upper threshold levels - hysteresis” or the differential signal of two IR sensors (IR1 - IR3 / IR2 - IR4) are above “the lower threshold levels + hysteresis” or the software reset is done or Write accessing to ECNTL1 register is done.

DR: Data Ready

“0”: Normal state

“1”: Data Ready

DR bit goes “1”, when the data is ready with DRI bit = “1”

IR13H / IR24H: The differential signals of two IR sensors (IR1 - IR3 / IR2 - IR4) are equal to or above the upper threshold levels.

“0”: The differential signals (IR1 - IR3 / IR2 - IR4) are below the upper threshold levels.

“1”: The differential signals (IR1 - IR3 / IR2 - IR4) are below the upper threshold levels.

When IR13H / IR24H bit is set to “1” in the interrupt source registers(EINTEN), IR13H / IR24H bit turns to “1”, when the differential signals (IR1 - IR3 / IR2 - IR4) are equal to or above the upper threshold levels which are set in ETH13 / ETH24H registers. Otherwise it stays at “0”.

IR13L / IR24L: The differential signals of two IR sensors (IR1 - IR3 / IR2 - IR4) are equal to or below the lower threshold levels.

“0”: The differential signals (IR1 - IR3 / IR2 - IR4) are above the lower threshold levels.

“1”: The differential signals (IR1 - IR3 / IR2 - IR4) are equal to or below the lower threshold levels.

When IR13LI / IR24LI bit set to “1” in the interrupt source registers (EINTEN), IR13L / IR24L bit turns to “1”, when the differential signals (IR1 - IR3 / IR2 - IR4) are equal to or below the lower threshold levels which are set in ETH13L / ETH24L registers. Otherwise it stays at “0”.

6). ST1: Status 1 (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	ST1							DOR	DRDY
Reset		1	1	1	1	1	1	0	0

DRDY: Data Ready

“0”: Normal State

“1”: Data Ready

The DRDY bit turns to “1”, when the data is ready to be read. This bit turns back to “0”, when either the ST2 register or one of the measured data (IRS1L to TMPH) is read.

DOR: Data Overrun

“0”: Normal State

“1”: Data Overrun

The DOR bit turns to “1”, when the data reading is skipped. This bit turns back to “0”, when either the ST2 register or one of the measured data (IRS1L to TMPH) is read.

7). IRxL, IRxH: Measurement Data of IR sensor (x= 1, 2, 3, 4) (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
06,08,0A,0C H	IRxL	IRxL_7	IRxL_6	IRxL_5	IRxL_4	IRxL_3	IRxL_2	IRxL_1	IRxL_0
07,09,0B,0D H	IRxH	IRxH_15	IRxH_14	IRxH_13	IRxH_12	IRxH_11	IRxH_10	IRxH_9	IRxH_8
Reset		0	0	0	0	0	0	0	0

Measurement Data of IR sensor

IRxL [7:0]: Least significant 8-bits in output data

IRxH [15:8]: Most significant 8-bits in output data

16-bit data is stored in two's complement format.

Table 14.2. Measurement Data of IR sensor

Measurement Data IR Sensor [15:0]			Output Current of IR Sensor	Unit
Two's Complement	Hex	Decimal		
0111 1111 1111 1111	7FFF	32767	14286.4	pA
⋮	⋮	⋮	⋮	
0101 1001 1001 1000	5998	22936	10000.1	
⋮	⋮	⋮	⋮	
0100 0000 1000 0010	4082	16514	7000.1	
⋮	⋮	⋮	⋮	
0000 1000 1111 0110	08F6	2294	1000.2	
⋮	⋮	⋮	⋮	
0000 0000 0010 0000	0020	32	14.0	
⋮	⋮	⋮	⋮	
0000 0000 0000 0000	0000	0	0	
⋮	⋮	⋮	⋮	
1111 1111 1110 0000	FFE0	-31	13.5	
⋮	⋮	⋮	⋮	
1111 0111 0000 1001	F709	-2294	-1000.2	
⋮	⋮	⋮	⋮	
1011 1111 0111 1101	BF7D	-16514	-7200.1	
⋮	⋮	⋮	⋮	
1010 0110 0110 0111	9667	-22936	-10000.1	
⋮	⋮	⋮	⋮	
1000 0000 0000 0000	8000	-32768	-14286.8	

Note:

* 14. When the digital filter cutoff frequency is set to $F_c = 1.1\text{Hz}$, the output current under 15.8pA cannot be measured by the noise.

8). TMPL, TMPH: Measurement Data of the Integrated temperature Sensor (Read / Write Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	TMPL	TMPL_7	TMPL_6	TMPL_5	TMPL_4	TMPL_3	TMPL_2	TMPL_1	TMPL_0
0FH	TMPH	TMPH_15	TMPH_14	TMPH_13	TMPH_12	TMPH_11	TMPH_10	TMPH_9	TMPH_8
Reset		0	0	0	0	0	0	0	0

Note:

* 15. TMPL_0 bit to TMPL_5 bit are fixed to "0".

Measurement Data of the Integrated Temperature Sensor

TMPL [7:0]: Least significant 8-bits in output data

TMPH [15:8]: Most significant 8-bits in output data

16-bit data is stored in two's complement format.

Table 14.3. Measurement Data of the Integrated Temperature Sensor

Measurement Data of the Integrated Temperature Sensor [15:0]			Temperature	Unit
Two's Complement	Hex	Decimal		
0100 0011 1000 0000	4380	17792	60	°C
⋮	⋮	⋮	⋮	
0000 0001 0000 0000	0100	256	26.75+0.5	
⋮	⋮	⋮	⋮	
0000 0000 0100 0000	0040	64	26.75+0.125	
0000 0000 0000 0000	0000	0	26.75	
1111 1111 1100 0000	FFC0	-64	26.75-0.125	
⋮	⋮	⋮	⋮	
1111 1111 0000 0000	FF00	-256	26.75-0.5	
⋮	⋮	⋮	⋮	
1011 1001 1000 0000	B980	-18048	-10	

The Resolution of the Integrated Temperature Sensor

Table 14.4. The Resolution of the Integrated Temperature Sensor

EFC[2:0] Setting	EFC= All Setting
Resolution	10-bit (0.125°C)

9). ST2: Status 2 (Read Only Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	ST2								
Reset		1	1	1	1	1	1	1	1

Note:

* 16. ST2 register is the dummy data register for the measured data reading routine. ST2 register MUST be read after reading out the measured data.

10). ETH13H, ETH24H, ETH12L, ETH24L: Threshold level setting for the differential outputs
(IR1 - IR3 / IR2 - IR4) (Read / Write Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	ETH13H	TEH13H_4	TEH13H_3	ETH13H_2	ETH13H_1	ETH13H_0	0	0	0
12H	ETH13H	0	ETH13H_11	ETH13H_10	ETH13H_9	ETH13H_8	ETH13H_7	ETH13H_6	ETH13H_5
13H	ETH13L	ETH13L_4	ETH13L_3	ETH13L_2	ETH13L_1	ETH13L_0	0	0	0
14H	ETH13L	0	ETH13L_11	ETH13L_10	ETH13L_9	ETH13L_8	ETH13L_7	ETH13L_6	ETH13L_5
15H	ETH24H	ETH24H_4	ETH24H_3	ETH24H_2	ETH24H_1	ETH24H_0	0	0	0
16H	ETH24H	0	ETH24H_11	ETH24H_10	ETH24H_9	ETH24H_8	ETH24H_7	ETH24H_6	ETH24H_5
17H	ETH24L	ETH24L_4	ETH24L_3	ETH24L_2	ETH24L_1	ETH24L_0	0	0	0
18H	ETH24L	0	ETH24L_11	ETH24L_10	ETH24L_9	ETH24L_8	ETH24L_7	ETH24L_6	ETH13L_5
Reset		0	0	0	0	0	0	0	0

Threshold Level setting for the differential output (IR1 - IR3 / IR2 - IR4)

TH13H [11:0], TH24H [11:0]: Upper Threshold Level setting for the differential output (IR1 - IR3 / IR2 - IR4)

TH13L [11:0], TH24L [11:0]: Lower Threshold Level setting for the differential output (IR1 - IR3 / IR2 - IR4)

The setting range is shown in Table 14.5.

Table 14.5. Threshold Level setting for the differential output (IR1 - IR3 / IR2 - IR4)

Threshold level [11:0]			Differential Current Output	Unit
Two's Complement	Hex	Decimal		
0111 1111 1111	7FF	2047	7139.32	pA
⋮	⋮	⋮	⋮	
0000 0000 0001	001	1	3.4877	
0000 0000 0000	000	0	0	
1111 1111 1111	FFF		-3.4877	
⋮	⋮	⋮	⋮	
1000 0000 0000	800	-2048	-7142.81	

Differential current output is calculated by the following formula,

$$\text{Differential current output} = 3.4877 \times \text{Threshold level [11:0]}(\text{Decimal}) \quad \text{pA}$$

Note:

* 17. The threshold levels should be set as "ETH13H > ETH13L, ETH24H > ETH24L". Otherwise, AK9753 cannot operate normally.

11). EHYS13, EHYS24: Hysteresis setting of Threshold Level / Polarity setting of INT output.
(Read / Write Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	EHYS13				EHYS13_4	EHYS13_3	EHYS13_2	EHYS13_1	EHYS13_0
1AH	EHYS24				EHYS24_4	EHYS24_3	EHYS24_2	EHYS24_1	EHYS24_0
Reset		1	1	1	0	0	0	0	0

Hysteresis setting for Threshold levels

ETHYS13, EHYS24: Hysteresis setting for threshold levels 5-bit

This register is used only in Switch Mode (ECOPY).

Table 14.6. Hysteresis setting of Threshold Level

Hysteresis [4:0]			Differential Current Output	Unit
Binary	Hex	Decimal		
11111	1F	31	108.12	pA
11110	1E	30	104.63	
⋮	⋮	⋮	⋮	
00001	01	1	3.4877	
00000	00	0	0	

The relationship between the hysteresis and the threshold level is shown in Figure 14.1.

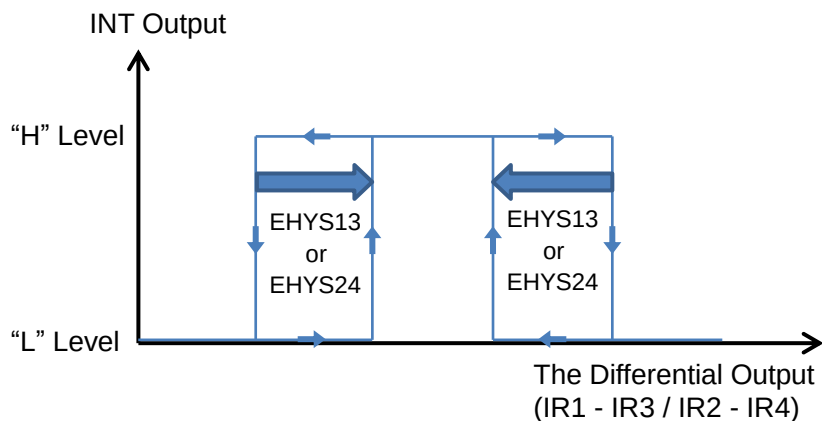


Figure 14.1. Hysteresis setting for threshold levels.

Detection is defined as the situation in which the differential output ($IR1 - IR3 / IR2 - IR4$) exceeds the threshold level.

12). EINTEN: Interrupt Source setting (Read / Write Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	EINTEN				IR13HI	IR13LI	IR24HI	IR24LI	DRI
Reset		1	1	0	0	0	0	0	0

The interrupt to the HOST MCU via the INT output can be obtained by the following methods: INT output turns to “Active”, when at least one of the enabled interrupt source conditions is satisfied. HOST MCU can identify the interrupt source by reading the Interrupt Source Status (INST).

When DRI and threshold Level interrupt (IR13HI, IR13LI, IR24HI and IR24LI) are simultaneously set to “Enable”, the priority is given to threshold level interrupt.

DRI: Data ready interrupt setting

“0”: Interrupt Disable

“1”: Interrupt Enable

Setting DRI bit to “1” enables the interrupt function at the timing of data ready.

IR13HI / IR24HI: Upper threshold level interrupt setting

“0”: Interrupt Disable

“1”: Interrupt Enable

Setting IR13H / IR24HI bit to “1” enables the interrupt function at the timing in which the differential output (IR1 - IR3 / IR2 - IR4) changes from the level which is below the upper threshold level to the level which is above the upper threshold level, or at the timing in which the differential output (IR1 - IR3 / IR2 - IR4) changes from the level which is above “the upper threshold level - hysteresis” to the level which is below “the upper threshold level - hysteresis”.

IR13LI / IR24LI: Lower threshold level interrupt setting.

“0”: Interrupt Disable

“1”: Interrupt Enable

Setting IR13LI/IR24LI bit to “1” enables the interrupt function at the timing in which the differential output (IR1 - IR3 / IR2 - IE4) changes from the level which is above the lower threshold level to the level which is below the lower threshold level, or at the timing in which the differential output (IR1 - IR3 / IR2 - IR4) changes from the level which is below “the lower threshold level +hysteresis” to the level which is above “the lower threshold level +hysteresis”.

13). ECNTL1: Mode setting/ Digital Filter Cutoff Frequency (Fc) setting (Read / Write registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	ECNTL1		EEPMODE	EFC_2	EFC_1	EFC_0	EMODE_2	EMODE_1	EMODE_0
Reset		1	0	0	0	0	0	0	0

EMODE [2:0]: Mode setting

“000”: Stand-by Mode

“001”: EEPROM Access Mode (EEPMODE bit should be set to “1” simultaneously)

“010”: Shingle Shot Mode

“011”: Be prohibited

“100”: Continuous Mode 0 (Normal operation)

“101”: Continuous Mode 1 (Intermittent operation => Measurement time: Wait time = 1:1)

“110”: Continuous Mode 2 (Intermittent operation => Measurement time: Wait time = 1:3)

“111”: Continuous Mode 3 (Intermittent operation => Measurement time: Wait time = 1:7)

EFC [2:0]: Digital Filter Cutoff Frequency (Fc) setting

“000”: Fc = 0.3Hz

“001”: Fc = 0.6Hz

“010”: Fc = 1.1Hz

“011”: Fc = 2.2Hz

“100”: Fc = 4.4Hz

“101”: Fc = 8.8Hz

“11x”: Be prohibited

The digital filter is “**sinc** function” type. The Fc is defined as the frequency at which Gain is -3dB.

EEPMODE Setting

“0”: Normal Mode

“1”: EEPROM Access Mode (EMODE [2:0] bits should be set to “001” simultaneously)

14). CNTL2: Soft Reset (Read / Write Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	CNTL2								SRST
Reset		1	1	1	1	1	1	1	0

SRST: Soft Reset

“0”: Normal State

“1”: Reset

All registers are reset by setting SRST bit to “1”. SRST bit automatically returns to “0” after reset is activated.

15. EEPROM Functional Descriptions

Table 15.1. EEPROM Detail Map

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
50H	EKEY	EKEY_7	EKEY_6	EKEY_5	EKEY_4	EKEY_3	EKEY_2	EKEY_1	EKEY_0
51H	ETH13H	1	1	ETH13H_5	ETH13H_4	ETH13H_3	ETH13H_2	ETH13H_1	ETH13H_0
52H	ETH13H	1	1	ETH13H_11	ETH13H_10	ETH13H_9	ETH13H_8	ETH13H_7	ETH13H_6
53H	ETH13L	1	1	ETH13L_5	ETH13L_4	ETH13L_3	ETH13L_2	ETH13L_1	ETH13L_0
54H	ETH13L	1	1	ETH13L_11	ETH13L_10	ETH13L_9	ETH13L_8	ETH13L_7	ETH13L_6
55H	ETH24H	1	1	ETH24H_5	ETH24H_4	ETH24H_3	ETH24H_2	ETH24H_1	ETH24H_0
56H	ETH24H	1	1	ETH24H_11	ETH24H_10	ETH24H_9	ETH24H_8	ETH24H_7	ETH24H_6
57H	ETH24L	1	1	ETH24L_5	ETH24L_4	ETH24L_3	ETH24L_2	ETH24L_1	ETH24L_0
58H	ETH24L	1	1	ETH24L_11	ETH24L_10	ETH24L_9	ETH24L_8	ETH24L_7	ETH24L_6
59H	EHYS13	1	1	1	EHYS13_4	EHYS13_3	EHYS13_2	EHYS13_1	EHYS13_0
5AH	EHYS24	1	1	1	EHYS24_4	EHYS24_3	EHYS24_2	EHYS24_1	EHYS24_0
5BH	EINTEN	1	1	0	IR13HI	IR13LI	IR24HI	IR24LI	DRI
5CH	ECNTL1	1	1	EFC_2	EFC_1	EFC_0	EMODE_2	EMODE_1	EMODE_0
5DH		1	1	1	1	1	1	1	1
5EH		1	1	1	1	1	1	1	1
5FH		1	1	1	1	1	1	1	1
60H	AKEY	AKEY_7	AKEY_6	AKEY_5	AKEY_4	AKEY_3	AKEY_2	AKEY_1	AKEY_0

[Functional Descriptions]

1). EKEY: EEPROM WRITE ENABLE setting (Read / Write Registers)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
50H	EKEY	EKEY_7	EKEY_7	EKEY_7	EKEY_7	EKEY_7	EKEY_7	EKEY_7	EKEY_7

Writing data to EEPROM is enabled by setting EKEY [7:0] to "A5H".

Since 51H of 5CH of EEPROM correspond to 11H to 1CH of registers, please refer to the details of a register function.

*The bit position in 51H, 53H, 55H and 57H of EEPROM do not correspond to the bit positions in 11H, 13H, 15H and 17H of registers.

16. First data Determination Time

The First data determination time is defined as the time between “setting the registers” and “determining the measurement data”. It depends on Measurement Mode setting and Digital Filter setting. Since the first data determination time also depends on the OCS frequency, Min./Max. is Typ. $\pm 10\%$.

<First data Determination Time (Typ.) in each Measurement Mode>

Table 16.1. First data Determination Time

EMODE [2:0]	EFC [2:0]						Unit
	EFC= “0H”	EFC= “1H”	EFC= “2H”	EFC= “3H”	EFC= “4H”	EFC= “5H”	
Single Shot Mode	2.309	1.157	0.581	0.293	0.149	0.077	sec
Continuous Mode0	2.309	1.157	0.581	0.293	0.149	0.077	
Continuous Mode1	2.309	1.157	0.581	0.293	0.149	0.077	
Continuous Mode2	2.309	1.157	0.581	0.293	0.149	0.077	
Continuous Mode3	2.309	1.157	0.581	0.293	0.149	0.077	

Note:

* 18. In Switch Mode, the first data determination time is defined as the time between “Power on Reset and determining INT output measurement data”. The first data determination time is 0.02 second longer than time shown in Table 16.1, in Switch Mode.

17. Data Sampling Period

The data sampling period is defined as the time in which AK9753 updates an IR measurement data periodically after determining the first data. The data sampling period depends on Measurement Mode setting and Digital Filter setting. Since the data sampling period also depends on the OCS frequency, Min / Max. is Typ. $\pm 10\%$.

<Data Sampling Period of IR Sensor in each Measurement Mode>

Table 17.1. Data Sampling Period (Typ.) of IR Sensor

EMODE [2:0]	EFC [2:0]						Unit
	EFC= “0H”	EFC= “1H”	EFC= “2H”	EFC= “3H”	EFC= “4H”	EFC= “5H”	
Continuous Mode 0	0.576	0.288	0.144	0.072	0.036	0.018	sec
Continuous Mode 1	4.608	2.304	1.152	0.576	0.288	0.144	
Continuous Mode 2	9.216	4.608	2.304	1.152	0.576	0.288	
Continuous Mode 3	18.432	9.216	4.608	2.304	1.152	0.576	

<Data Sampling Period of Temperature Sensor data in each Measurement Mode>

The data sampling period of the temperature sensor is changed by changing EMODE [2:0] as shown in Table 17.2. The data sampling period of the temperature sensor does not depend on the digital filter setting (EFC [2:0]).

Table 17.2. Data Sampling Period (Typ.) of Temperature Sensor

EMODE [2:0]	Period	Unit
Continuous Mode 0	0.576	sec
Continuous Mode 1	4.608	
Continuous Mode 2	9.216	
Continuous Mode 3	18.432	

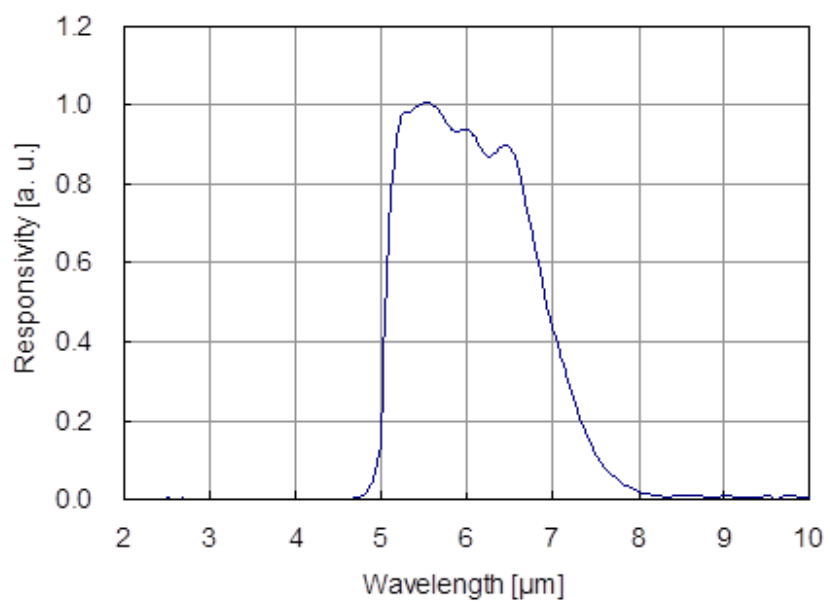
18. Spectrum Sensitivity (Reference)

Figure 18.1. Spectrum Sensitivity

<Measurement Conditions>

Sensor Temperature Ts= 25°C (298K)

19. Field of View (Reference)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Field of View (* 19)	FOV		± 80		deg($^{\circ}$)

Note:

* 19. The combined range observed by Upper/Lower (Left/Right) sensors. Reference data only, not tested.

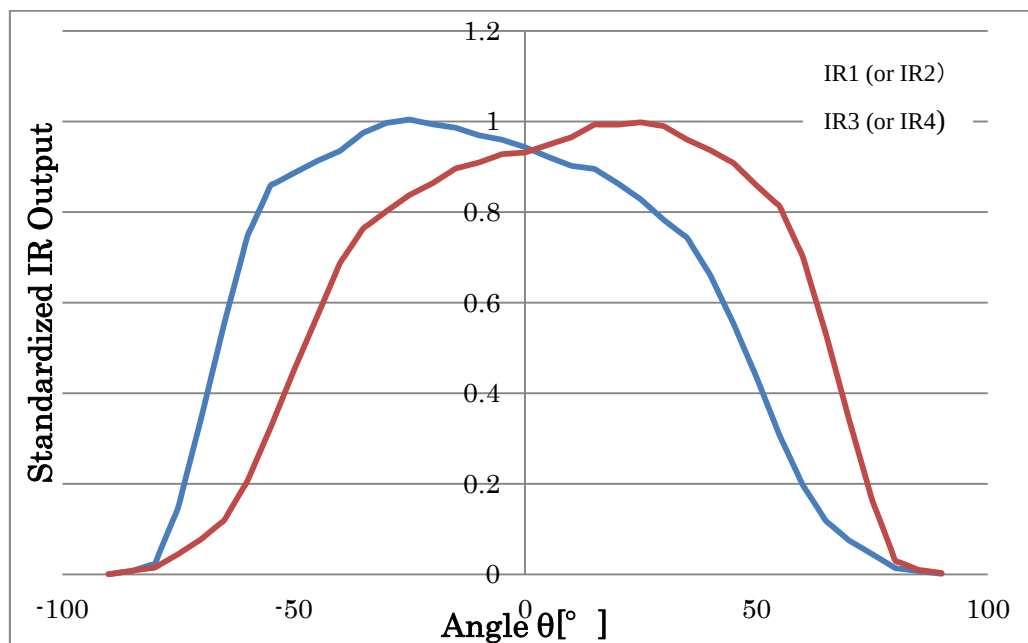


Figure 19.1. Field of View (Typ.)

<Measurement Conditions>

Ambient Temperature: $T_a = 25^{\circ}\text{C}$

Block Body: $\Phi 12.7\text{mm}$ $T_b = 500\text{K}$

Distance between Black Body and AK9753: 140mm

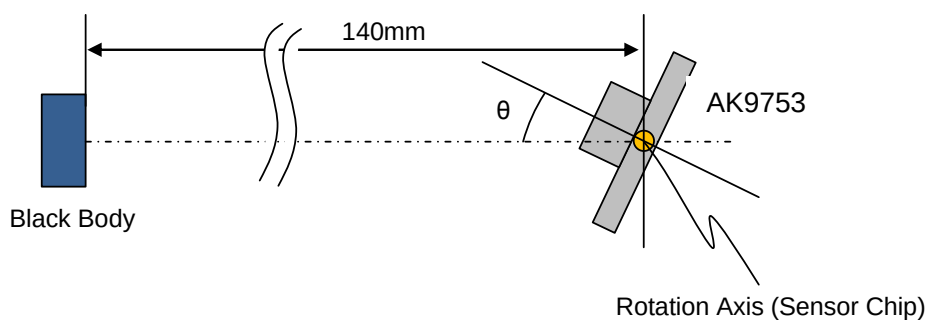


Figure 19.2. Measurement Conditions

20. Recommended External Circuits

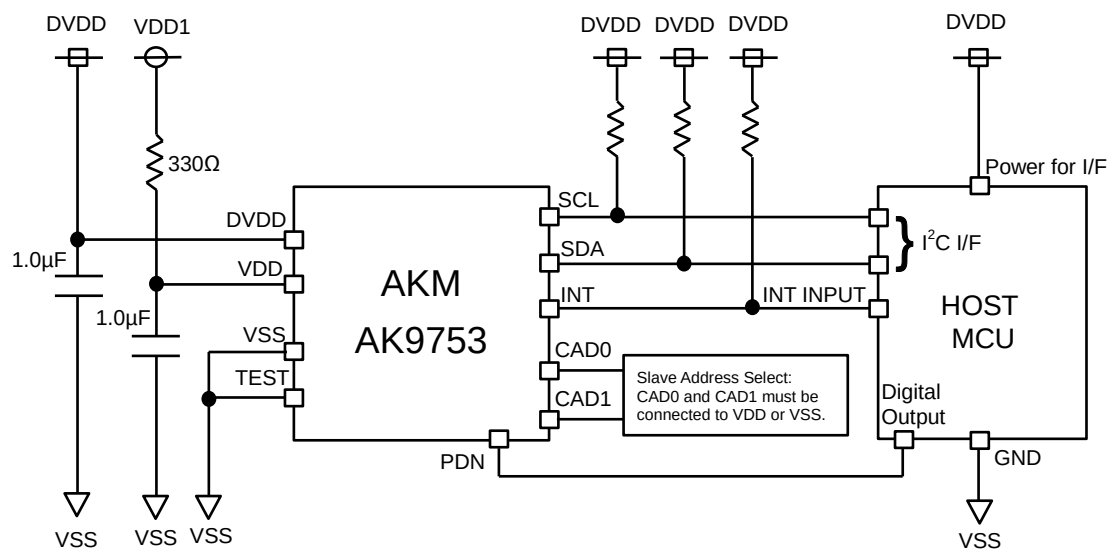
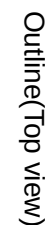


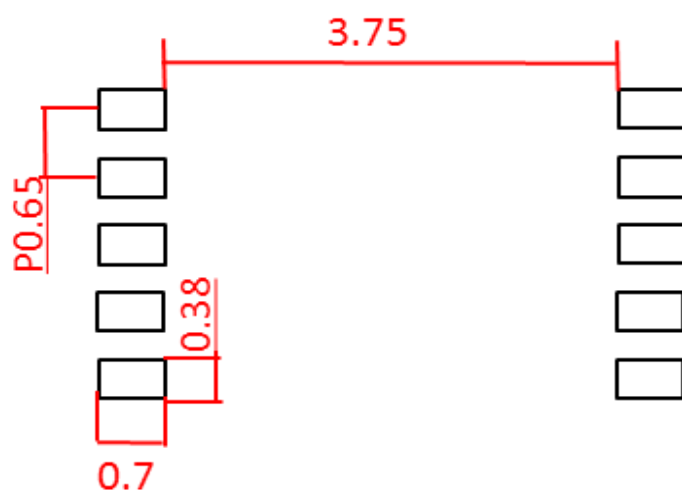
Figure 20.1. Recommended External Circuits

21.1.Outline Dimensions

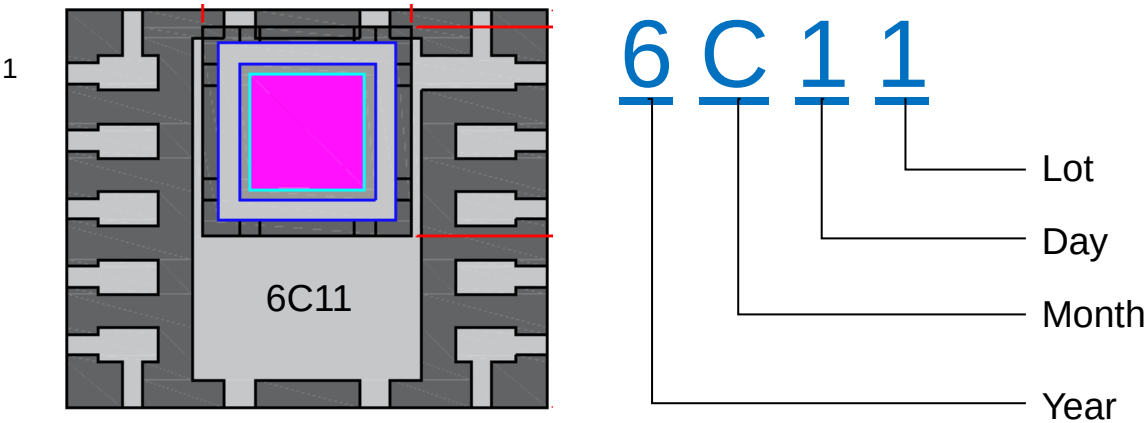
10-pin SON (Unit mm)

Unless otherwise specified: $\pm 0.1\text{mm}$



21.2. Pad Dimensions
(Unit: mm)

21.3. Marking



Year		Month		Day		Lot	
Mark	Year	Mark	Month	Mark	Day	Mark	Lot
0	2020	C	January	1	1st	1	1 Lot
1	2021	D	February	2	2nd	2	2 Lot
2	2022	E	March	3	3rd	3	3 Lot
3	2023	F	April	4	4th	4	4 Lot
4	2024	G	May	5	5th	5	5 Lot
5	2015	H	June	6	6th	6	6 Lot
6	2016	J	July	7	7th	7	7 Lot
7	2017	K	August	8	8th	8	8 Lot
8	2018	L	September	9	9th	9	9 Lot
9	2019	M	October	0	10th	0	10 Lot
		N	November	A	11th	A	11 Lot
		P	December	B	12th	B	12 Lot
				C	13th	C	13 Lot
				D	14th	D	14 Lot
				E	15th	E	15 Lot
				F	16th	F	16 Lot
				G	17th	G	17 Lot
				H	18th	H	18 Lot
				J	19th	J	19 Lot
				K	20th	K	20 Lot
				L	21th	L	21 Lot
				N	22th	M	22 Lot
				P	23th	N	23 Lot
				R	24th	P	24 Lot
				S	25th	R	25 Lot
				T	26th	S	26 Lot
				U	27th	T	27 Lot
				V	28th	U	28 Lot
				W	29th	V	29 Lot
				X	30th	W	30 Lot
				Y	31th	X	31 Lot
						Y	32 Lot
						Z	33 Lot

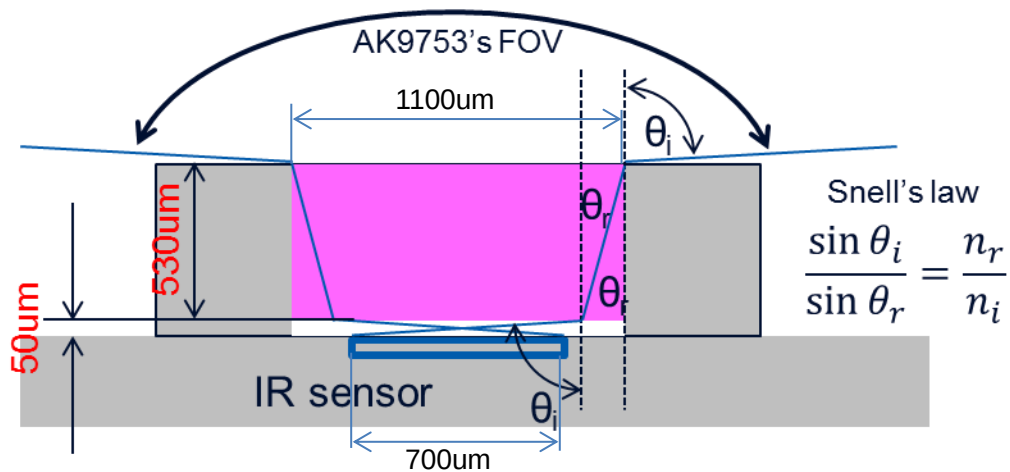
22. Structure of Filter Block and IR Sensors (Reference)

Structure of Filter Block and IR Sensors is as shown Figure 22.1.

Structure of Filter Block is as shown Figure 22.2.

Structure of IR Sensors is as shown Figure 22.3.

To consider structure and the FOV properties of AK9753 is needed for designing the external lens.



- θ_i, θ_r incidence & refraction angle respectively.
- n_i, n_r refractive index. ($n_i=1.00, n_r=3.42$)

Figure 22.1. Structure of Filter Block and IR Sensors (Cross section)

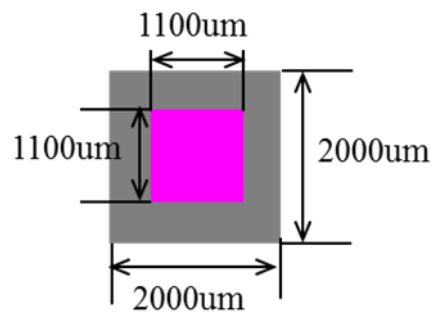


Figure 22.2. Structure of Filter Block (Overhead view)

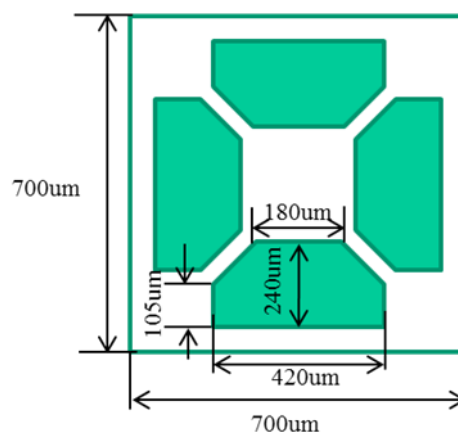


Figure 22.3. Structure of IR Sensors (Overhead view) (All sensors are same size.)

23. Ordering Guide

AK9753AE -30 ~ 85°C 10-pin SON

24. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
17/04/17	00	First edition	-	-

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