AL360A
Video Format Converter

SOC

Datasheets
Version 1.3

Doc Number: 1-D-PMK236-0001

Amendments

Date	Version	Comments	Author
27.01.2015	1.0	Formal Release Version 1.0	Ken Liu
10.03.2015	1.1	Update Pin name	Ken Liu
11.05.2015	1.2	Remove BT1120 20-bit	Ken Liu
22.06.2017	1.3	Update power & OSD information, Remove BT656 output	Ken Liu

Disclaimer

Contents:

1 Description and Features

1.1 General Description

AverLogic's AL360 is a multi-functional video conversion SOC. It includes embedded DDR memory, embedded MCU, video processing engine, RGB DAC and TV encoder.
The video processor supports video input with multiple video formats, video output with de-interlacing and scaling effects. The AverLogic's proprietary scaling algorithm supports video scaled up and scaled down function, the resolution is up to 1920x1080 independently in horizontal & vertical directions. It also provides de-interlacing, mirror, flip and processes the interlaced video to be displayed on progressive panels or analog RGB DAC output. The 256-color OSD engine is used for displaying a colorful menu tree on screen.
The AL360 supports power saving mode, and can operate under low power voltages (3.3V,1.8V and 1.2V) in 249-pin Lead Free (PBF) LFBGA packages.

1.2 Features

◆ **Video Input- Digital**
- 8-bit CMOS Sensor and ISP chip YCbCr
- 24-bit RGB888
- 16-bit YCbCr
- 8-bit BT.656 YCbCr
- Supports up to 148.5MHz pixel rate

◆ **Video Output- Digital**
- 24-bit RGB888
- 16-bit/20-bit YCbCr
- Supports digital LCD panels: 160x120, 320x240, 640x480, 800x480, 800x600 and more
- Embedded Analog RGB DAC
- Embedded TV Encoder CVBS/S-video

◆ **Video Output- Analog**
- Embedded Analog RGB DAC
- Embedded TV Encoder CVBS/S-video

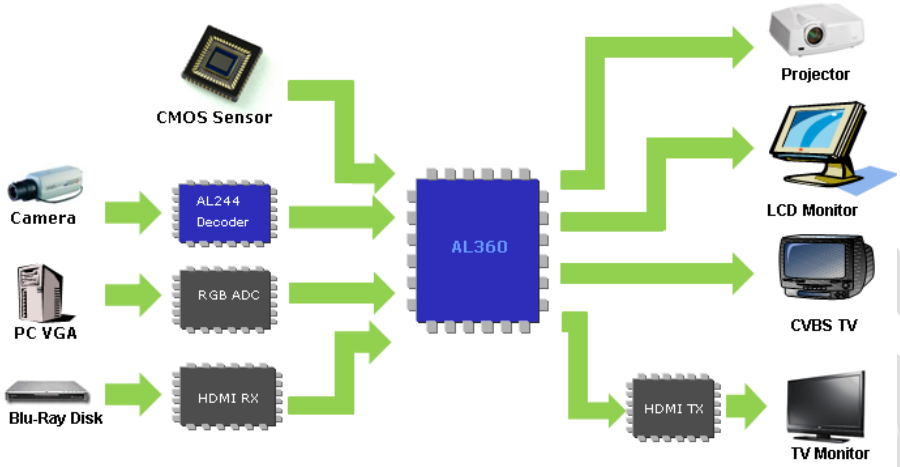
◆ **Video Processing and Scaler**

Video scaling engine (scale up/down) up to 1080 60p
- De-interlacing video engine (NTSC/PAL)
- Supports video freeze, zoom, flip, mirror, rotation, motion detection and more
- Video contrast-brightness-hue-sharpness adjustment

◆ **OSD**
- 2 OSD frames with 4 OSD windows
- 256-color bitmap palette mode

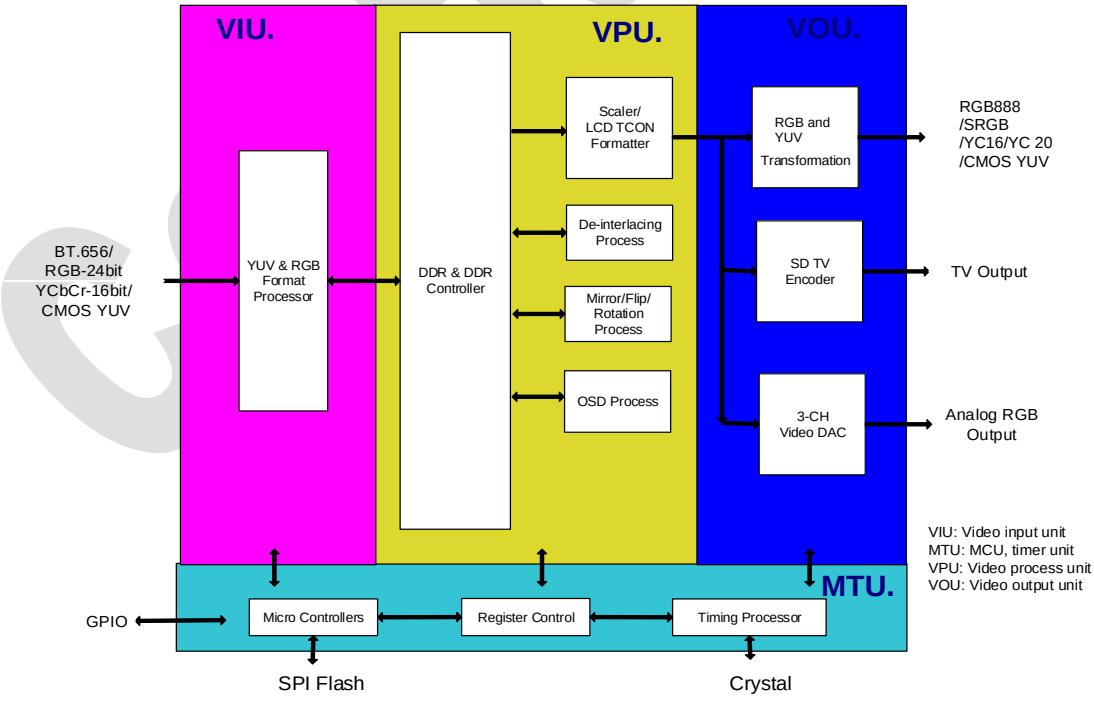
◆ **Miscellaneous**
- Built-in MCU80251 without OS controller
- Supports SPI-Flash and ISP (In-System Programming) function
- LFBGA 249 pin

1.3 Applications



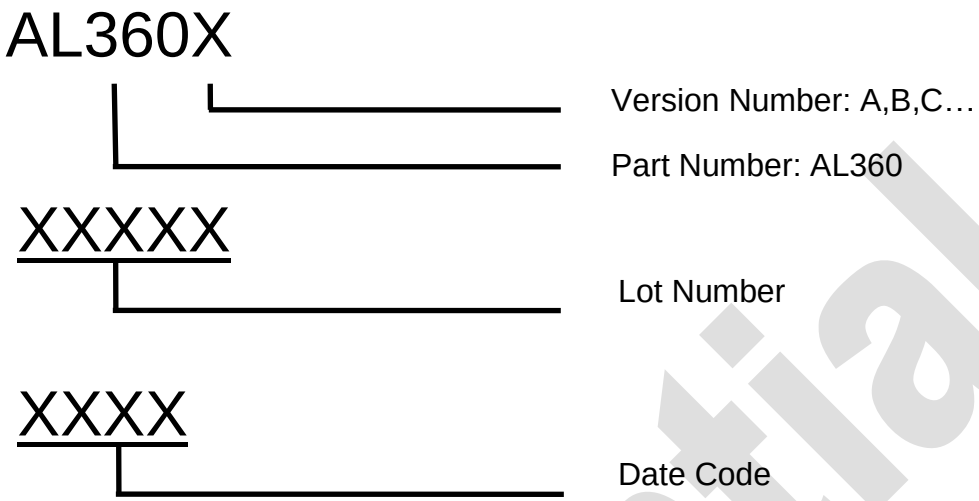
- HD and SD Video Format Converter Box
- TV to PC / PC to TV Monitor Format Converter Box
- Small-to-medium size of Multimedia TFT-LCD, AMOLED Display Monitor
- Portable TV/DTV Display System
- Vision-assisted Equipment, Electronic Magnifier for medical application
- In-Car TV/GPS/Navigation & Entertainment Display Systems

1.4 Function Block Diagram



2 Chip Information

2.1 Marking Information



2.2 Ordering Information

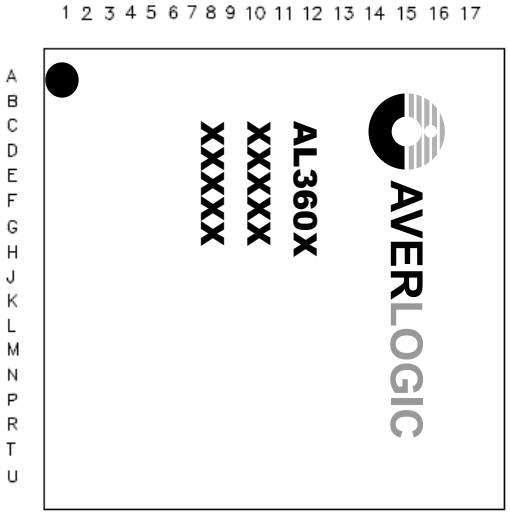
Part number	Package	PB Free	Power Supply.
AL360A	249 LFBGA	Yes	+1.2/1.8V/3.3V

Note: AverLogic Technologies PB-free products employ special PB-free material sets; molding compounds/die materials and 100% matte tin plate termination finish do not use materials containing PBB, PBDE or red phosphorus for green-product chips. AverLogic's PB-free products are MSL classified at PB-free peak reflow temperatures that meet or exceed the PB-free requirements of IPC/JEDEC J Std-020C."

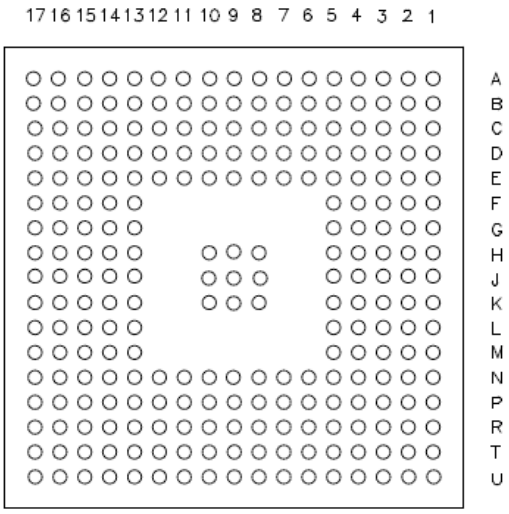
3 Pin Diagram and Description

3.1 Pin Diagram

TOP VIEW



BOTTOM VIEW



3.2 Pin Definition and Description

Top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VOUT_G_Y	VOUT_B_C	VOUT_VREF	AGND	AGND	AV12_PLL	XTALI	GND	NC	NC	VIN_HRE	VIN_CLK	VIN_DAT[22]	VIN_DAT[20]	VIN_DAT[18]	VIN_DAT[16]	VIN_DAT[15]
B	VOUT_R_CVBS	AGND	VOUT_REXT	AV33_DAC	AV33_DAC	AGND_PLL	XTALO	DV33	NC	NC	VIN_VSYN	VIN_DAT[23]	VIN_DAT[21]	VIN_DAT[19]	VIN_DAT[17]	VIN_DAT[14]	VIN_DAT[13]
C	AGND	AV33_DAC	AGND	AV33_DAC	NC	AV12_PLL	AGND_PLL	GND	NC	NC	SPI_SO	SPI_SCK	DV33	GND	GND	VIN_DAT[12]	VIN_DAT[11]
D	NC	NC	NC	NC	NC	NC	GND	GND	DV33	DV33	SPI_CE_N	SPI_SI	AV12	AV12	AV12	VIN_DAT[10]	VIN_DAT[9]
E	NC	NC	AGND	NC	NC	TEST_EN	TMODE[0]	TMODE[1]	TMODE[2]	RSTN	GND	AV12	VOUT_PWM_1	DGND	GND	VIN_DAT[8]	VIN_DAT[7]
F	LVDT	AGND	NC	NC	NC								VOUT_PWM_2	DV18	DV33	VIN_DAT[6]	VIN_DAT[5]
G	NC	NC	NC	NC	GND								VOUT_PWM_3	DV18	AV12	VIN_DAT[4]	VIN_DAT[3]
H	NC	NC	NC	NC	NC			NC	NC	NC			GND	DGND	AV12	VIN_DAT[2]	VIN_DAT[1]
J	NC	NC	NC	DV33	GND			NC	NC	NC			AV12	DV18	GND	VIN_DAT[0]	VOUT_VCOM
K	NC	NC	NC	GND	GND			GND	GND	NC			UR_RX2D	DGND	GND	VOUT_B_D[6]	VOUT_B_D[7]
L	GND	AV12	GND	DV33	AV12								UR_TX2D	GND	GND	VOUT_B_D[4]	VOUT_B_D[5]
M	GPIO[0]	GPIO[1]	GPIO[2]	GPIO[3]	GPIO[4]								UR_RX1D	GND	AV12	VOUT_B_D[2]	VOUT_B_D[3]
N	GPIO[9]	GPIO[8]	GPIO[7]	GPIO[6]	GPIO[5]	DGND	DV18	DV18	DGND	DGND	DV18	GND	UR_TX1D	AV12	AV12	VOUT_B_D[0]	VOUT_B_D[1]
P	GPIO[10]	GPIO[11]	GPIO[12]	GND	DV18	DV18	DGND	AV12	GND	DV18	DGND	GND	GND	AV12	DV33	VOUT_G_D[6]	VOUT_G_D[7]
R	DV18	DGND	DGND	DV18	DGND	GND	GND	AV12	GND	DV33	DV33	AV12	AV12	GND	GND	VOUT_G_D[4]	VOUT_G_D[5]
T	DV18	DGND	DGND	DV18	DV18	GND	GND	AV12	GND	VOUT_VSYNC	VOUT_DE	VOUT_SR_D[1]	VOUT_SR_D[3]	VOUT_SR_D[5]	VOUT_SR_D[7]	VOUT_G_D[1]	VOUT_G_D[3]
U	DGND	DV18	DV18	DGND	DGND	GND	GND	GND	GND	VOUT_DCLK	VOUT_HSYNC	VOUT_SR_D[0]	VOUT_SR_D[2]	VOUT_SR_D[4]	VOUT_SR_D[6]	VOUT_G_D[0]	VOUT_G_D[2]

The pin-out definitions and functions are described as follows:

Group	Pin Name	Pin NO	Type	Description
XTAL	XTALI	A7	I	Crystal Input 27MHz
XTAL	XTALO	B7	O	Crystal Output 27MHz
Video Output	VOUT_B_D[0]	N16	O	Video Output Bus Blue D0
Video Output	VOUT_B_D[1]	N17	O	Video Output Bus Blue D1
Video Output	VOUT_B_D[2]	M16	O	Video Output Bus Blue D2
Video Output	VOUT_B_D[3]	M17	O	Video Output Bus Blue D3
Video Output	VOUT_B_D[4]	L16	O	Video Output Bus Blue D4
Video Output	VOUT_B_D[5]	L17	O	Video Output Bus Blue D5
Video Output	VOUT_B_D[6]	K16	O	Video Output Bus Blue D6
Video Output	VOUT_B_D[7]	K17	O	Video Output Bus Blue D7
Video Output	VOUT_B_C	A2	O	Analog RGB Blue output, Analog YC C Output
Video Output	VOUT_G_Y	A1	O	Analog RGB Green output, Analog YC Y Output
Video Output	VOUT_R_CVBS	B1	O	Analog RGB Red output, Analog Composite output
Video Output	VOUT_REXT	B3	I	DAC Full-Scale Adjust Resister Input
Video Output	VOUT_VREF	A3	I	DAC Voltage Reference Input, Decoupling or bypass internal reference voltage (Pull 1uF capacitor to Low)
Video Output	VOUT_DCLK	U10	O	Video Pixel Clock Output
Video Output	VOUT_DE	T11	O	Video DE Output
Video Output	VOUT_G_D[0]	U16	O	Video Output BusGreen D0
Video Output	VOUT_G_D[1]	T16	O	Video Output Bus Green D1
Video Output	VOUT_G_D[2]	U17	O	Video Output Bus Green D2
Video Output	VOUT_G_D[3]	T17	O	Video Output Bus Green D3
Video Output	VOUT_G_D[4]	R16	O	Video Output Bus Green D4
Video Output	VOUT_G_D[5]	R17	O	Video Output Bus Green D5
Video Output	VOUT_G_D[6]	P16	O	Video Output Bus Green D6
Video Output	VOUT_G_D[7]	P17	O	Video Output Bus Green D7
Video Output	VOUT_HSYNC	U11	O	H-SYNC Output
Video Output	VOUT_PWM_1	E13	O	Video PWM 1 Output
Video Output	VOUT_PWM_2	F13	O	Video PWM 2 Output
Video Output	VOUT_PWM_3	G13	O	Video PWM 3 Output
Video Output	VOUT_SR_D[0]	U12	O	Video Output Bus Red D0 Output, Serial RGB D0 Output
Video Output	VOUT_SR_D[1]	T12	O	Video Output Bus Red D1 Output, Serial RGB D1 output
Video Output	VOUT_SR_D[2]	U13	O	Video Output Bus Red D2 Output, Serial RGB D2 output
Video Output	VOUT_SR_D[3]	T13	O	Video Output Bus Red D3 Output, Serial RGB D3 output
Video Output	VOUT_SR_D[4]	U14	O	Video Output Bus Red D4 Output, Serial RGB D4 output
Video Output	VOUT_SR_D[5]	T14	O	Video Output Bus Red D5 Output, Serial RGB D5 output
Video Output	VOUT_SR_D[6]	U15	O	Video Output Bus Red D6 Output, Serial RGB D6 output
Video Output	VOUT_SR_D[7]	T15	O	Video Output Bus Red D7 Output, Serial RGB D7 output
Video Output	VOUT_VCOM	J17	O	Video VCOM Output
Video Output	VOUT_VSYNC	T10	O	V-SYNC Output
Video Input	VIN_CLK	A12	I	Video Pixel Clock Input
Video Input	VIN_DAT[0]	J16	I	Video Input Bus D0
Video Input	VIN_DAT[1]	H17	I	Video Input Bus D1
Video Input	VIN_DAT[10]	D16	I	Video Input Bus D10
Video Input	VIN_DAT[11]	C17	I	Video Input Bus D11
Video Input	VIN_DAT[12]	C16	I	Video Input Bus D12
Video Input	VIN_DAT[13]	B17	I	Video Input Bus D13
Video Input	VIN_DAT[14]	B16	I	Video Input Bus D14
Video Input	VIN_DAT[15]	A17	I	Video Input Bus D15
Video Input	VIN_DAT[16]	A16	I	Video Input Bus D16
Video Input	VIN_DAT[17]	B15	I	Video Input Bus D17
Video Input	VIN_DAT[18]	A15	I	Video Input Bus D18
Video Input	VIN_DAT[19]	B14	I	Video Input Bus D19
Video Input	VIN_DAT[2]	H16	I	Video Input Bus D2
Video Input	VIN_DAT[20]	A14	I	Video Input Bus D20
Video Input	VIN_DAT[21]	B13	I	Video Input Bus D21
Video Input	VIN_DAT[22]	A13	I	Video Input Bus D22
Video Input	VIN_DAT[23]	B12	I	Video Input Bus D23
Video Input	VIN_DAT[3]	G17	I	Video Input Bus D3
Video Input	VIN_DAT[4]	G16	I	Video Input Bus D4
Video Input	VIN_DAT[5]	F17	I	Video Input Bus D5
Video Input	VIN_DAT[6]	F16	I	Video Input Bus D6
Video Input	VIN_DAT[7]	E17	I	Video Input Bus D7

Video Input	VIN_DAT[8]	E16	I	Video Input Bus D8
Video Input	VIN_DAT[9]	D17	I	Video Input Bus D9
Video Input	VIN_HRE	A11	I	Video HER Input
Video Input	VIN_VSYN	B11	I	Video V-SYNC Input
TEST	TEST_EN	E6	I	Test Pin (Pull 4K7 OHM to High)
TEST	TMODE[0]	E7	I/O	Low = Normal mode, High = Release SPI flash bus.
TEST	TMODE[1]	E8	I/O	Low= Normal mode, High = ISP mode.
TEST	TMODE[2]	E9	I/O	Test Pin (Pull 4K7 OHM to Low)
RSTN	RSTN	E10	I/O	Global Reset Pin, Low Active
P	AGND	C1	Ground	Ground Analog
P	AGND	C3	Ground	Ground Analog
P	AGND	A4	Ground	Ground Analog
P	AGND	A5	Ground	Ground Analog
P	AGND	E3	Ground	Ground Analog
P	AGND	F2	Ground	Ground Analog
P	AGND	B2	Ground	Ground Analog
P	AGND_PLL	B6	Ground	Ground Analog
P	AGND_PLL	C7	Ground	Ground Analog
P	AV12	P8	Power	1.2V Core Power
P	AV12	R8	Power	1.2V Core Power
P	AV12	P14	Power	1.2V Core Power
P	AV12	R12	Power	1.2V Core Power
P	AV12	M15	Power	1.2V Core Power
P	AV12	D15	Power	1.2V Core Power
P	AV12	D13	Power	1.2V Core Power
P	AV12	E12	Power	1.2V Core Power
P	AV12	G15	Power	1.2V Core Power
P	AV12	J13	Power	1.2V Core Power
P	AV12	L2	Power	1.2V Core Power
P	AV12	L5	Power	1.2V Core Power
P	AV12	D14	Power	1.2V Core Power
P	AV12	H15	Power	1.2V Core Power
P	AV12	N14	Power	1.2V Core Power
P	AV12	N15	Power	1.2V Core Power
P	AV12	R13	Power	1.2V Core Power
P	AV12	T8	Power	1.2V Core Power
P	AV12_PLL	A6	Power	1.2V PLL Power
P	AV12_PLL	C6	Power	1.2V PLL Power
P	AV33	C2	Power	3.3V Analog Power
P	AV33	C4	Power	3.3V Analog Power
P	AV33	B4	Power	3.3V Analog Power
P	AV33	B5	Power	3.3V Analog Power
P	GND	P9	Ground	Ground Digital
P	GND	R7	Ground	Ground Digital
P	GND	P13	Ground	Ground Digital
P	GND	R14	Ground	Ground Digital
P	GND	L15	Ground	Ground Digital
P	GND	C15	Ground	Ground Digital
P	GND	K9	Ground	Ground Digital
P	GND	D7	Ground	Ground Digital
P	GND	E11	Ground	Ground Digital
P	GND	E15	Ground	Ground Digital
P	GND	J15	Ground	Ground Digital
P	GND	H13	Ground	Ground Digital
P	GND	A8	Ground	Ground Digital
P	GND	G5	Ground	Ground Digital
P	GND	L1	Ground	Ground Digital
P	GND	L3	Ground	Ground Digital
P	GND	K5	Ground	Ground Digital
P	GND	C8	Ground	Ground Digital
P	GND	D8	Ground	Ground Digital
P	GND	J5	Ground	Ground Digital
P	GND	K4	Ground	Ground Digital
P	GND	K8	Ground	Ground Digital
P	GND	K15	Ground	Ground Digital
P	GND	L14	Ground	Ground Digital

P	GND	M14	Ground	Ground Digital
P	GND	N12	Ground	Ground Digital
P	GND	P4	Ground	Ground Digital
P	GND	P12	Ground	Ground Digital
P	GND	R6	Ground	Ground Digital
P	GND	R9	Ground	Ground Digital
P	GND	R15	Ground	Ground Digital
P	GND	T6	Ground	Ground Digital
P	GND	T7	Ground	Ground Digital
P	GND	T9	Ground	Ground Digital
P	GND	U6	Ground	Ground Digital
P	GND	U7	Ground	Ground Digital
P	GND	U8	Ground	Ground Digital
P	GND	U9	Ground	Ground Digital
P	GND	C14	Ground	Ground Digital
P	DGND	U1	Ground	Ground DDR
P	DGND	U4	Ground	Ground DDR
P	DGND	U5	Ground	Ground DDR
P	DGND	T3	Ground	Ground DDR
P	DGND	T2	Ground	Ground DDR
P	DGND	R2	Ground	Ground DDR
P	DGND	R3	Ground	Ground DDR
P	DGND	R5	Ground	Ground DDR
P	DGND	P7	Ground	Ground DDR
P	DGND	N6	Ground	Ground DDR
P	DGND	N9	Ground	Ground DDR
P	DGND	N10	Ground	Ground DDR
P	DGND	P11	Ground	Ground DDR
P	DGND	E14	Ground	Ground DDR
P	DGND	H14	Ground	Ground DDR
P	DGND	K14	Ground	Ground DDR
P	DV18	U2	Power	1.8V DDR Power
P	DV18	U3	Power	1.8V DDR Power
P	DV18	T5	Power	1.8V DDR Power
P	DV18	T4	Power	1.8V DDR Power
P	DV18	T1	Power	1.8V DDR Power
P	DV18	R1	Power	1.8V DDR Power
P	DV18	R4	Power	1.8V DDR Power
P	DV18	P5	Power	1.8V DDR Power
P	DV18	P6	Power	1.8V DDR Power
P	DV18	N7	Power	1.8V DDR Power
P	DV18	N8	Power	1.8V DDR Power
P	DV18	N11	Power	1.8V DDR Power
P	DV18	P10	Power	1.8V DDR Power
P	DV18	F14	Power	1.8V DDR Power
P	DV18	G14	Power	1.8V DDR Power
P	DV18	J14	Power	1.8V DDR Power
P	DV33	R10	Power	3.3V I/O Power
P	DV33	P15	Power	3.3V I/O Power
P	DV33	F15	Power	3.3V I/O Power
P	DV33	C13	Power	3.3V I/O Power
P	DV33	D10	Power	3.3V I/O Power
P	DV33	D9	Power	3.3V I/O Power
P	DV33	B8	Power	3.3V I/O Power
P	DV33	J4	Power	3.3V I/O Power
P	DV33	L4	Power	3.3V I/O Power
P	DV33	R11	Power	3.3V I/O Power
M-IO	GPIO[0]	M1	I/O	MCU GPIO
M-IO	GPIO[1]	M2	I/O	MCU GPIO
M-IO	GPIO[10]	P1	I/O	MCU GPIO
M-IO	GPIO[11]	P2	I/O	MCU GPIO
M-IO	GPIO[12]	P3	I/O	MCU GPIO
M-IO	GPIO[2]	M3	I/O	MCU GPIO
M-IO	GPIO[3]	M4	I/O	MCU GPIO
M-IO	GPIO[4]	M5	I/O	MCU GPIO
M-IO	GPIO[5]	N5	I/O	MCU GPIO

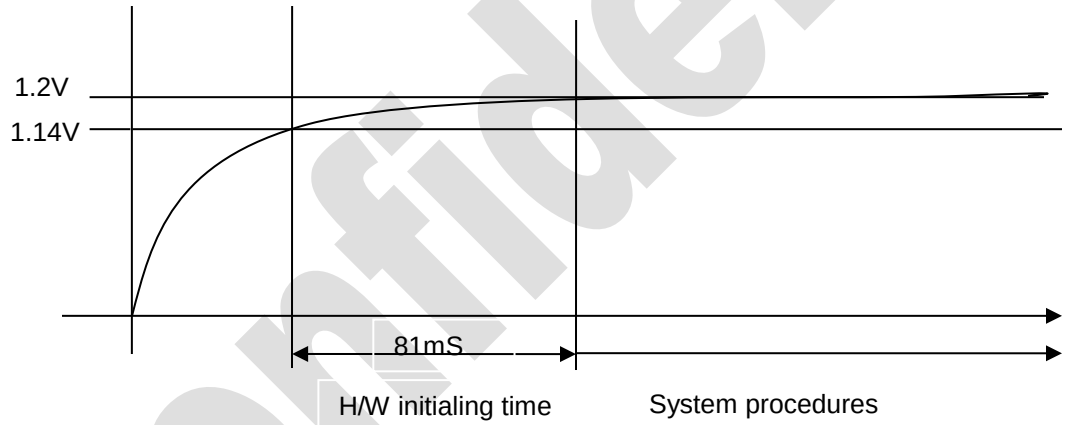
M-IO	GPIO[6]	N4	I/O	MCU GPIO
M-IO	GPIO[7]	N3	I/O	MCU GPIO
M-IO	GPIO[8]	N2	I/O	MCU GPIO
M-IO	GPIO[9]	N1	I/O	MCU GPIO
M-IO	UR_RX1D	M13	I	MCU UART RX 1D
M-IO	UR_RX2D	K13	I	MCU UART RX 2D
M-IO	UR_TX1D	N13	O	MCU UART TX 1D
M-IO	UR_TX2D	L13	O	MCU UART TX 2D
LVDT	LVDT	F1	I	Low Voltage detection
IO-SPI	SPI_CE_N	D11	O	SPI Flash Chip Select Output
IO-SPI	SPI_SCK	C12	O	SPI Flash Serial Clock Output
IO-SPI	SPI_SI	D12	O	SPI Flash Master Out, Slave In (SPI_MOSI)
IO-SPI	SPI_SO	C11	I	SPI Flash Master In, Slave Out (SPI_MISO)

Note: NC Pins -
A9,A10,B9,B10,C9,C10,D1,D2,D3,D4,D5,D6,E1,E2,E4,E5,F1,F3,F4,F5,G1,G2,G3,G4,H1,H2,H3,H4,H5,H8, H9,H10,J1,J2,J3,J8,J9,J10,K1,K2,K3,K10

4 Function Description

4.1 Power-On and Chip Reset

After power-on, the internal reset machine will be processed automatically. That means the internal engines can be reset automatically and it doesn't need any external hardware circuit to trigger the reset PIN. The reset function can be enabled by the reset pin.



After power-on and after the SOC chip has reached stable voltage, the SOC chip will do the initialization procedures automatically. The MCU needs to handle the system procedures after 81 ms.
The system procedures include video interface initialization, memory initialization, video processer initialization. After initialization the system always handles the user's interfaces. The system level initialization usually requires 300 ms ~ 500 ms.

4.2 Digital Video Input interface

Format / Pin Name	RGB 8:8:8 24 bits (Note 1)			YCbCr 4:2:2 16 bits		BT.656 8 bits	YCbCr 4:2:2 8 bits
VIN_DAT[0]	R0	G0	B0	Y0	C0	D0	D0
VIN_DAT[1]	R1	G1	B1	Y1	C1	D1	D1
VIN_DAT[2]	R2	G2	B2	Y2	C2	D1	D2
VIN_DAT[3]	R3	G3	B3	Y3	C3	D3	D3
VIN_DAT[4]	R4	G4	B4	Y4	C4	D4	D4
VIN_DAT[5]	R5	G5	B5	Y5	C5	D5	D5
VIN_DAT[6]	R6	G6	B6	Y6	C6	D6	D6
VIN_DAT[7]	R7	G7	B7	Y7	C7	D7	D7
VIN_DAT[8]	G0	B0	R0	C0	Y0	X	X
VIN _DAT[9]	G1	B1	R1	C1	Y1	X	X
VIN_DAT[10]	G2	B2	R2	C2	Y2	X	X
VIN_DAT[11]	G3	B3	R3	C3	Y3	X	X
VIN_DAT[12]	G4	B4	R4	C4	Y4	X	X
VIN_DAT[13]	G5	B5	R5	C5	Y5	X	X
VIN_DAT[14]	G6	B6	R6	C6	Y6	X	X
VIN_DAT[15]	G7	B7	R7	C7	Y7	X	X
VIN_DAT[16]	B0	R0	G0	X		X	X
VIN_DAT[17]	B1	R1	G1	X		X	X
VIN_DAT[18]	B2	R2	G2	X		X	X
VIN_DAT[19]	B3	R3	G3	X		X	X
VIN_DAT[20]	B4	R4	G4	X		X	X
VIN_DAT[21]	B5	R5	G5	X		X	X
VIN_DAT[22]	B6	R6	G6	X		X	X
VIN_DAT[23]	B7	R7	G7	X		X	X
VIN_CLK	CLOCK			CLOCK		CLOCK	CLOCK
VIN_VSYN	V-SYNC			X		X	V-SYNC
VIN_HRE	H-SYNC			X		X	H-SYNC

AL360 has 24 pins for dedicated digital video devices. It allows a variety of input formats, such as RGB 24 bits, YCbCr 8/16bits and BT.656 8bits. The digital video input mapping of AL360 is shown in below table.

NOTE 1: The low bit to high bit data bus can be flip in RGB mode

4.3 Digital Video Output Interface

AL360 has 24 pins for dedicated digital video devices. It allows a variety of output formats such as RGB 24 bits, YCbCr 20bits and serial RGB 8bits. The digital video output mapping of AL360 is shown in below table.

Format / Pin Name	RGB 8:8:8 24 bits	YCbCr 4:2:2 20 bits	YCbCr 4:2:2 16 bits	Serial-RGB 8 bits
VOUT_B_D[0]	B0	X	X	X
VOUT_B_D[1]	B1	X	X	X
VOUT_B_D[2]	B2	C0	X	X
VOUT_B_D[3]	B3	C1	X	X
VOUT_B_D[4]	B4	C2	C0	X
VOUT_B_D[5]	B5	C3	C1	X
VOUT_B_D[6]	B6	C4	C2	X

VOUT_B_D[7]	B7	C5	C3	X
VOUT_G_D[0]	G0	C6	C4	X
VOUT_G_D[1]	G1	C7	C5	X
VOUT_G_D[2]	G2	C8	C6	X
VOUT_G_D[3]	G3	C9	C7	X
VOUT_G_D[4]	G4	X	X	X
VOUT_G_D[5]	G5	X	X	X
VOUT_G_D[6]	G6	Y0	X	X
VOUT_G_D[7]	G7	Y1	X	X
VOUT_R_D[0]	R0	Y2	Y0	D0
VOUT_R_D[1]	R1	Y3	Y1	D1
VOUT_R_D[2]	R2	Y4	Y2	D2
VOUT_R_D[3]	R3	Y5	Y3	D3
VOUT_R_D[4]	R4	Y6	Y4	D4
VOUT_R_D[5]	R5	Y7	Y5	D5
VOUT_R_D[6]	R6	Y8	Y6	D6
VOUT_R_D[7]	R7	Y9	Y7	D7
VOUT_VSYNC	V-SYNC	/	V-SYNC	/
VOUT_HSYNC	H-SYNC	/	H-SYNC	/
VOUT_DCLK	Clock	Clock	Clock	Clock
VOUT_DE	/	/	DE	/

4.4 Analog Video Output Interface

There is a 3-channel digital-to-analog converter (DAC) at 10-bit of resolution embedded in AL360. It supports 200MSPS with a power-down mode to reduce the standby power dissipation.
The Full-scale current of the DAC is adjustable. The converter has a unit bias current generate circuit, and the current source array mirrors this unit bias current. When all the currents in current source array are opened, each DAC channel will be loaded with Full-scale current.
The relationship between the external resistor connected to pin FSADJ and Full-scale current is expressed in below equation
:

$$Full\_scale\_current = Vref/R_{fsadj} * 32;$$

(FSADJ pin = VOUT_DAC_REXT)

For Analog RGB output:
The Vref PIN needs to be pulled as high with an 1K OHM resistance, and the VOUT_DAC_REXT pin needs to be pulled as low with a 1.15K OHM resistance.

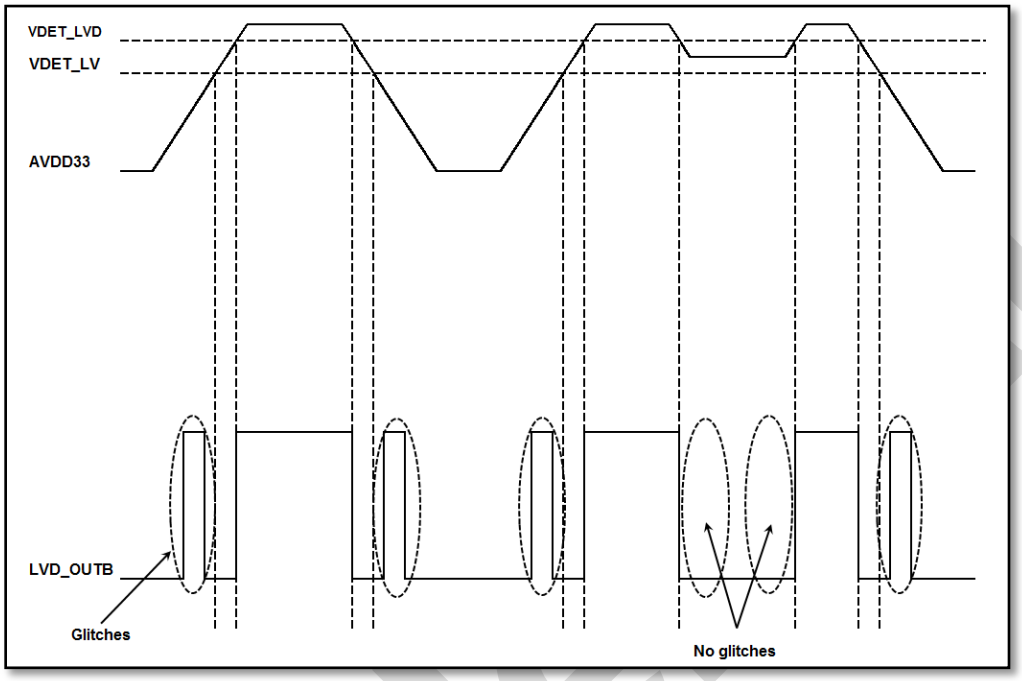
33.4mA=1.2/1.15K*32

4.5 Programmable flash interface

Serial flash memory provides a storage solution for systems limited by space, pins and power. It is ideal for code shadowing to SRAM/DDR memory for application needs. The highest performance serial flash memory interfaces are compatible with the AL360.

4.6 Voltage Detection Interface

The embedded low-voltage detector is used to detect 3.3V of electrical power from an external battery. (Refer to Application Note for related setting)



Timing Diagram

Electrical Specifications

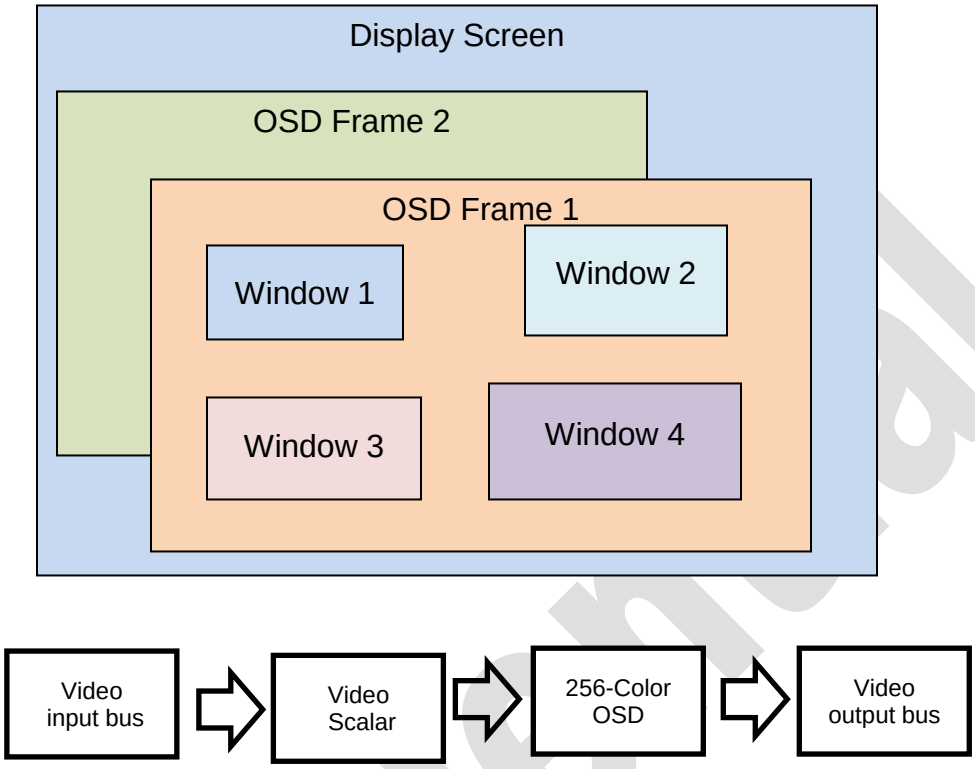
Characteristics	Symbol	MIN	TYP	MAX	UNIT	Condition
Power	AVDD33	2.0	3.30	3.6	V	
LVD Detect Levels (VDET_LVD)	VDET_LVD1	2.34	2.60	2.86	V	LVD_SEL=0, AVDD33 rises
	VDET_LVD2	2.295	2.55	2.805	V	LVD_SEL=0, AVDD33 falls
	VDET_LVD3	2.52	2.80	3.08	V	LVD_SEL=1, AVDD33 rises
	VDET_LVD4	2.475	2.75	3.025	V	LVD_SEL=1, AVDD33 falls
Low Levels (VDET_LV)	VDET_LV1	2.16	2.40	2.64	V	AVDD33 rises
	VDET_LV2	2.115	2.35	2.585	V	AVDD33 falls

4.7 OSD

The On Screen Display (OSD) function is to superimpose an image on a screen picture. The OSD engine can define characters or pictures overlaid with video streaming.
There are two OSD engines can be used in the AL360. One is basic 8-color OSD engine and the other one is 256-color OSD. They are responsible for their respective mandates.

Note- These two OSD engines can't be output with SD TV Encoder path, and the 256-color OSD engine only operates with 148.5MHz internal clock frequency.

256-color OSD Frame display:

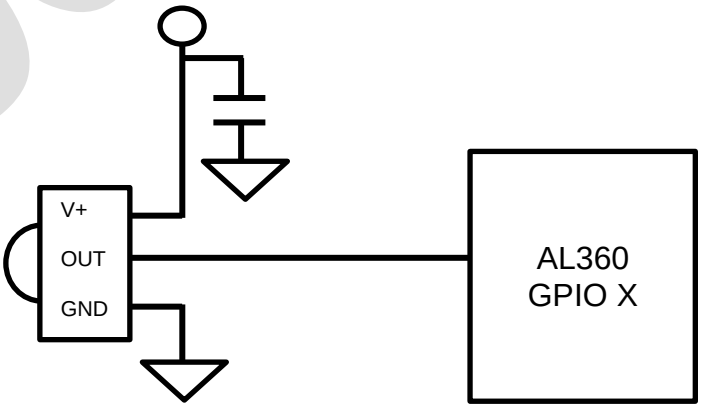


4.8 Video Scaling

AL360 supports scale-up and scale-down functions up to 1920x1080 of resolution. The scaling engine also can be enabled at input side or output side.

4.9 IR Decoder

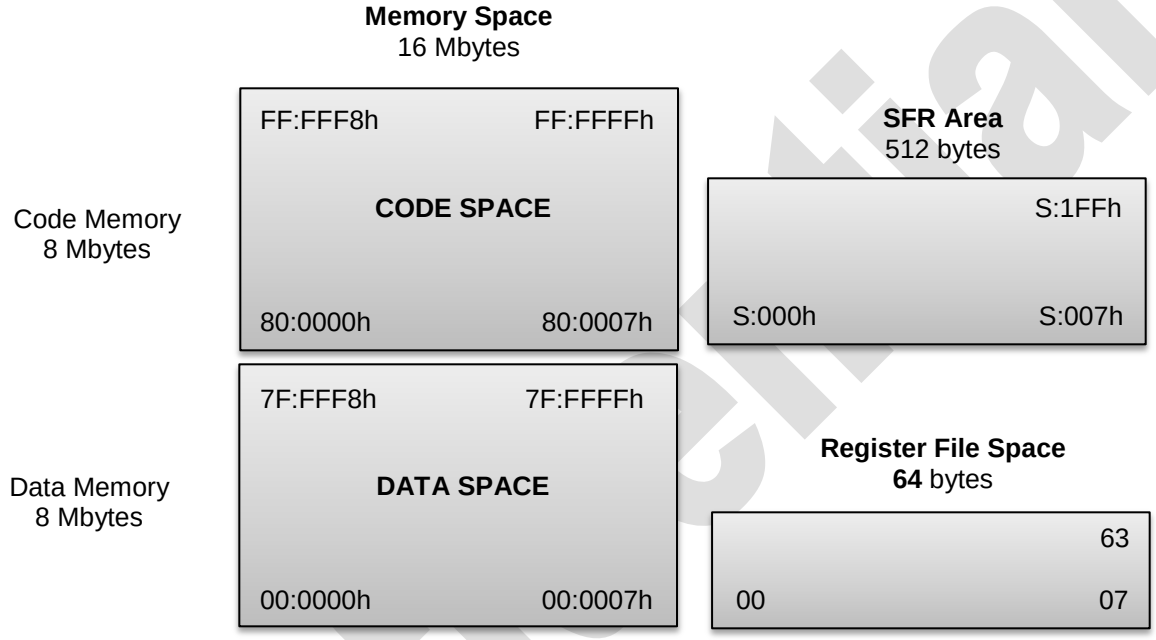
There is a hardware IR decoder embedded in the AL360. It supports decoding IR code from IR receiver. This function can be defined arbitrarily to AL360's GPIO. Also the decoded code can be loaded by registers. (Refer to Application Note for related setting)



4.10 MCU & MCU GPIO

This MCU is upward compatible with 8051 microcontrollers, including the enriched C51 instruction set, and the16-bit and 32-bit arithmetic and logic instructions. A 4-stage instruction pipeline enables execution of most of the instructions in a single cycle. 16 Mbytes of linear address space are used to allow for complicated application requirements. The MCU performance is 0.296 DMIPS/MHz based on the Dhrystone V2.1 / 200 loop test.

Regarding the MCU memory space, it is convenient to view the un-segmented, 16-Mbyte memory space as consisting of 256 regions of 64 Kbytes, numbered from 00: to FF:



The special function registers (SFRs) reside in their associated peripherals or in the core. The following tables show the SFR address space with the SFR mnemonics and reset values. SFR addresses are preceded by “S:” to differentiate them from addresses in the memory space. Unoccupied locations in the SFR space (the blank locations in SFR memory map table) are unimplemented, i.e. no register exists. If an instruction attempts to write to an unimplemented SFR location, the instruction executes, but nothing is actually written. If an unimplemented SFR location is read, it returns an unspecified value.

Core SFRs
Timers 0/1 SFRs
UART SFRs
PCA SFRs
Additional IRQ SFRs
I/O ports SFRs
Timer2 SFRs
I2CM SFRs
PWM SFRs
BIRD/POC SFRs
Port direction SFRs
WDT SFRs
SPI SFRs
CPMU SFRs
I2CS SFRs

F8	AIPL	CH	CCAP0H	CCAP1H	CCAP2H	CCAP3H	CCAP4H		FF
F0	B	STCON	SRXBUF	STXBUF		SSTAT0	SSTAT1	AIPH	F7
E8	AIE	CL	CCAP0L	CCAP1L	CCAP2L	CCAP3L	CCAP4L		EF
E0	ACC	MCON	MRXBUF	MTXBUF	MPRESC	MSTAT0	MSTAT1	MIEN0	E7
D8	CCON	CMOD	CCAPM0	CCAPM1	CCAPM2	CCAPM3	CCAPM4	CCAPO	DF
D0	PSW	PSW1	MIEN1		MCADDR	SIEN0	SIEN1	SSADDR	D7
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CF
C0	AIF								C7
B8	IPL0	SADEN					SPH		BF
B0	P3	SPCR	SPDR	SPSR				IPH0	B7
A8	IE0	SADDR			P0_DIR	P1_DIR	P2_DIR	P3_DIR	AF
A0	P2	MPAGE	PWMC	PWMDC LSB	PWMDC MSB	WDTCON	WDTRST		A7
98	SCON	SBUF							9F
90	P1						CPUINFO	MMCON	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CCMCON	CCMVAL	8F
80	P0	SP	DPL	DPH	DPXL	XTALCON	CLKCON	PCON	87

Core SFRs

Mnemonic	Address	Description	Reset value
ACC	S:0E0h	Accumulator	00h
B	S:0F0h	B Register	00h
DPH	S:083h	Data Pointer high byte	00h
DPL	S:082h	Data Pointer low byte	00h
DPXL	S:084h	Data Pointer Extended low byte	01h
MPAGE	S:0A1h	Memory page register	00h
PCON	S:087h	Power Control	00h
PSW	S:0D0h	Program Status Word	00h
PSW1	S:0D1h	Program Status Word 1	00h
SP	S:081h	Stack Pointer low - LSB of SPX	07h
SPH	S:0BEh	Stack Pointer high - MSB of SPX	00h

Interrupt SFRs

Mnemonic	Address	Description	Reset value
AIE	S:0E8h	Additional interrupt enable register	00h
AIF	S:0C0h	Additional interrupt flag register	00h
AIPH	S:0F7h	Additional interrupt priority high register	00h
AIPL	S:0F8h	Additional interrupt priority low register	00h
IE0	S:0A8h	Interrupt Enable Control 0	00h
IPH0	S:0B7h	Interrupt Priority Control high byte 0	00h
IPL0	S:0B8h	Interrupt Priority Control low byte 0	00h

I/O ports SFRs

Mnemonic	Address	Description	Reset value
P0	S:080h	Port0	FFh
P0_DIR	S:0ACh	Port0 direction	FFh
P1	S:090h	Port1	FFh
P1_DIR	S:0ADh	Port1 direction	FFh
P2	S:0A0h	Port2	FFh
P2_DIR	S:0AEh	Port2 direction	FFh
P3	S:0B0h	Port3	FFh
P3_DIR	S:0AFh	Port3 direction	FFh

Serial Port SFRs

Mnemonic	Address	Description	Reset value
SADDR	S:0A9h	Slave Address	00h
SADEN	S:0B9h	Slave Address mask	00h
SBUF	S:099h	Serial Buffer	00h
SCON	S:098h	Serial Control	00h

Timers SFRs

Mnemonic	Address	Description	Reset value
T2CON	S:0C8h	Timer/Counter 2 control	00h
T2MOD	S:0C9h	Timer/Counter 2 mode control	00h
TCON	S:088h	Timer/Counter 0 and 1 control	00h
TH0	S:08Ch	Timer/Counter 0 high byte	00h
TH1	S:08Dh	Timer/Counter 1 high byte	00h
TH2	S:0CDh	Timer/Counter 2 high byte	00h
TL0	S:08Ah	Timer/Counter 0 low byte	00h
TL1	S:08Bh	Timer/Counter 1 low byte	00h
TL2	S:0CCh	Timer/Counter 2 low byte	00h
TMOD	S:089h	Timer/Counter 0 and 1 mode control	00h
RCAP2H	S:0CBh	Timer 2 Reload/Capture high byte	00h
RCAP2L	S:0CAh	Timer 2 Reload/Capture low byte	00h
WDTCON	S:0A5h	Watchdog Timer control	07h
WDTRST	S:0A6h	Watchdog Timer enable	00h

Programmable Counter Array SFRs

Mnemonic	Address	Description	Reset value
CCAP0H	S:0FAh	PCA Compare/Capture Module 0 high byte	00h
CCAP0L	S:0EAh	PCA Compare/Capture Module 0 low byte	00h
CCAP1H	S:0FBh	PCA Compare/Capture Module 1 high byte	00h
CCAP1L	S:0EBh	PCA Compare/Capture Module 1 low byte	00h
CCAP2H	S:0FCh	PCA Compare/Capture Module 2 high byte	00h
CCAP2L	S:0ECh	PCA Compare/Capture Module 2 low byte	00h
CCAP3H	S:0FDh	PCA Compare/Capture Module 3 high byte	00h
CCAP3L	S:0EDh	PCA Compare/Capture Module 3 low byte	00h
CCAP4H	S:0FEh	PCA Compare/Capture Module 4 high byte	00h
CCAP4L	S:0EEh	PCA Compare/Capture Module 4 low byte	00h
CCAPM0	S:0DAh	PCA Compare/Capture Mode for Module 0	00h
CCAPM1	S:0DBh	PCA Compare/Capture Mode for Module 1	00h
CCAPM2	S:0DCh	PCA Compare/Capture Mode for Module 2	00h
CCAPM3	S:0DDh	PCA Compare/Capture Mode for Module 3	00h
CCAPM4	S:0DEh	PCA Compare/Capture Mode for Module 4	00h
CCAPO	S:0DFh	PCA Output for PWM and high speed mode	00h
CCON	S:0D8h	PCA Timer/Counter Control	00h
CH	S:0F9h	PCA Timer/Counter high byte	00h
CL	S:0E9h	PCA Timer/Counter low byte	00h
CMOD	S:0D9h	PCA Timer/Counter Mode	00h

Debugs SFRs

Mnemonic	Address	Description	Reset value
CCMCON	S:08Eh	Communication Control Register	00h
CCMVAL	S:08Fh	Communication Value Register	00h
CPUINFO	S:096h	CPU information (read only register)	00h
MMCON	S:097h	Monitor mode Control register	07h

PWM SFRs

Mnemonic	Address	Description	Reset value
PWMC	S:0A2h	PWM Control Register	00h
PWMDCLSB	S:0A3h	PWM Duty Cycle LSB Register	00h

PWMDCMSB	S:0A4h	PWM Duty Cycle MSB Register	00h

The I/O ports consist of four SFR registers, one for each port, plus four other SFR registers for each port direction, and the I/O port interface. The SFR register for each port is an 8-bit register, which can be addressed at the SFR location for that port.

I/O Ports Register

I/O Ports	Assembly reference	SFR address
Port0	P0	S:080h
Port1	P1	S:090h
Port2	P2	S:0A0h
Port3	P3	S:0B0h

GPIO[12:0] are shared by port0[7:0] and port1[4:0] of both MCUs. The MCU access permissions are controlled by register configuration.

Port3 and Port4 of the MCU are used for internal special data handles.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Under Free-Air Temperature

(These devices are designed to operate within the max/min ratings as specified. Operation beyond these limits may result in permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.)

Parameter		Min.	Typical	Max.	Unit of Measure
AV33	DAC supply voltage (AV33 to AGND)	-0.3	+3.3	+3.6	V
DV33	I/O supply voltage (VD33 to DGND)	-0.3	+3.3	+4.5	V
DV18_DDR	DDR supply voltage (DV18_DDR to DGND_DDR)	-0.3	1.8	+1.95	V
AV12	Core supply voltage	-0.3	+1.2	+1.44	V
AV12_PLL	PLL supply voltage	-0.3	+1.2	+1.44	V
V_P	Input pin voltage (Vp to DGND)	-0.3	+3.3	+(DV33+0.3)	V
I_O	I/O Output current	-	8	-	mA
Operating Current of Standby mode	AV33 current		0		mA
	DV33 current		5		mA

	DV18_DDR current		0		mA
	AV12 current		1		mA
	AV12_PLL current		0		mA
Operating Current of Normal run mode (720p input ,VGA DAC 1080p output, S/W Scaler and DRAM OSD Enable)	AV33 current		70		mA
	DV33 current		100		mA
	DV18_DDR current		80		mA
	AV12 current		180		mA
	AV12_PLL current		70		mA
T_{AMB}	Ambient operating temperatures	0 ~ +70		°C	
T_{stg}	Storage temperatures	-40 ~ +125		°C	

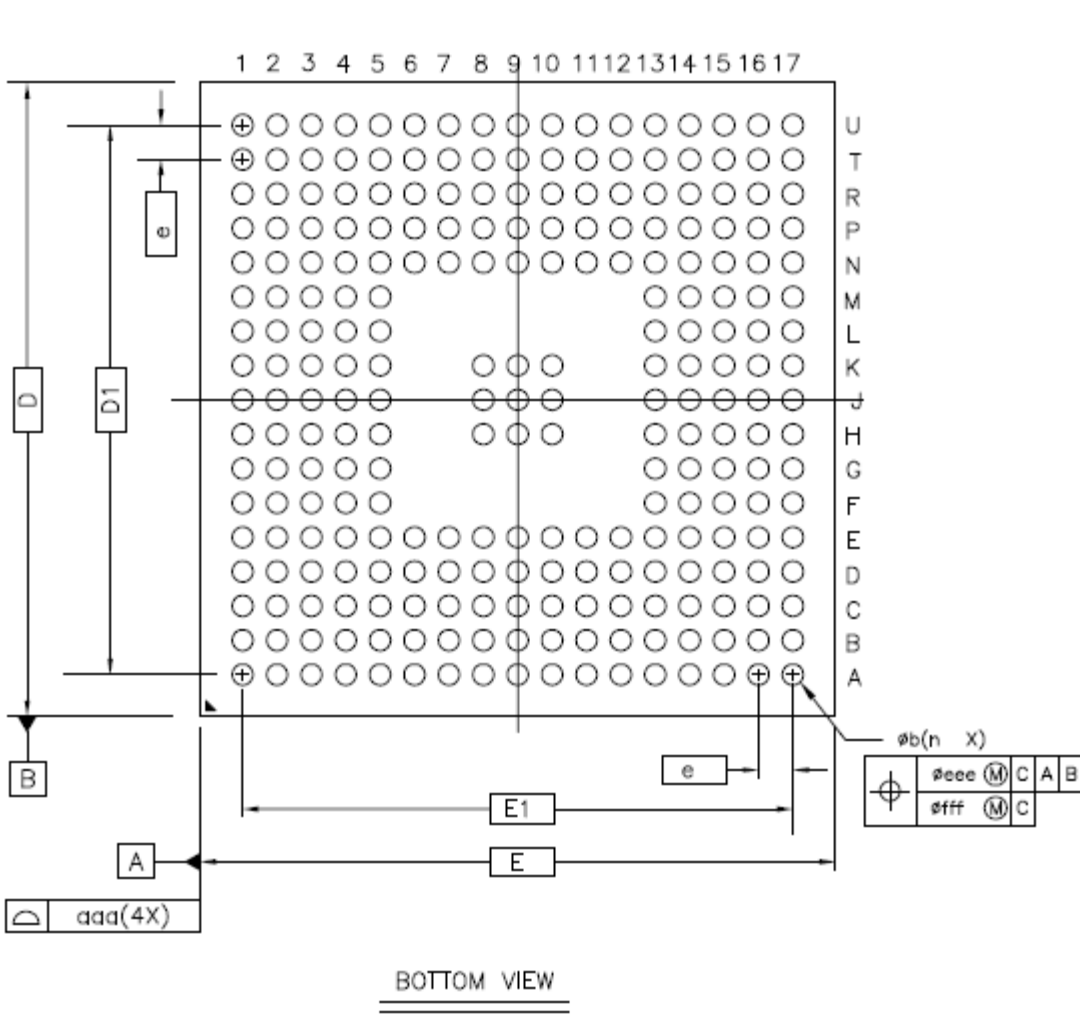
5.2 Recommended Operating Conditions

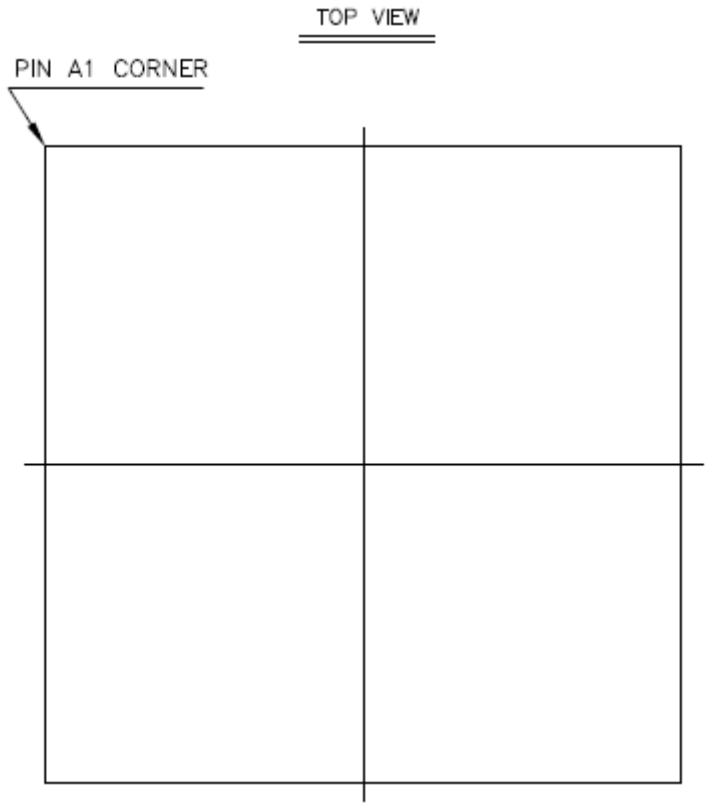
Parameter		1.2V/1.8V/3.3V Rating			Unit
		Min.	Typical	Max.	
AV33	DAC supply voltage	+3.13	+3.3	+3.47	V
DV33	I/O supply voltage	+3.0	+3.3	+3.6	V
DV18_DDR	DDR supply voltage	+1.7	+1.8	+1.95	V
AV12	Core supply voltage (for 148.5MHz internal clock)	+1.38	+1.4	+1.44	V
	Core supply voltage (for 121MHz internal clock)	+1.14	+1.2	+1.44	V
AV12_PLL	PLL supply voltage (for 148.5MHz internal clock)	+1.38	+1.4	+1.44	V
	Core supply voltage (for 121MHz internal clock)	+1.14	+1.2	+1.44	
V_{IH}	High level input voltage	0.7 VD33		VD33	V
V_{IL}	Low level input voltage	0		0.3 VD33	V

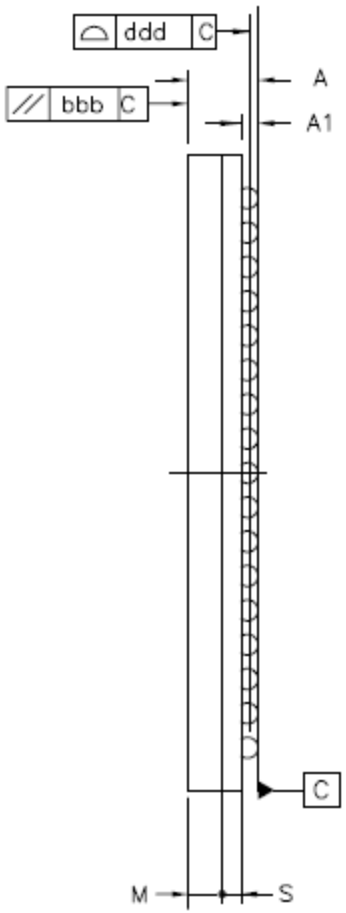
5.3 Crystal Specifications

Parameter	Rating	Unit
Frequency	27	MHz
Frequency Tolerance	±50	ppm

6 Mechanical Drawing







		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			STK LFBGA		
Body Size:	X	E	12.000		
	Y	D	12.000		
Ball Pitch :		e	0.650		
Total Thickness :		A			1.400
Mold Thickness :		M	0.650 Ref.		
Substrate Thickness :		S	0.360 Ref.		
Ball Diameter :			0.400		
Stand Off :		A1	0.270	–	0.370
Ball Width :		b	0.370	–	0.470
Package Edge Tolerance :		aaa	0.150		
Mold Parallelism :		bbb	0.200		
Coplanarity:		ddd	0.120		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	249		
Edge Ball Center to Center :	X	E1	10.400		
	Y	D1	10.400		

ASE ADVANCED SEMICONDUCTOR ENGINEERING, INC.		SCALE	PROJ.
TITLE: PACKAGE OUTLINE		DWG. NO.	REV.
		AAB0XXXX	0
249L STK LFBGA 12 x 12 x1.400		SHEET	SIZE
		1 OF 2	A4
UNIT	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	
MM			

CONTACT INFORMATION

Averlogic Technologies, Corp.
URL: http://www.averlogic.com