AL462
Ultra HD FIFO Memory
Datasheet

Version 1.0

Amendments

Revise Date	Contents	Page
08.22.2015	Preliminary version 0.01	Spec.
12.10.2015	Preliminary version 0.3	preliminary
01.20.2016	Preliminary version 0.4 Adding flash memory interface for rev. A chip on pin-out information Modify pin-description Adding Electrical Characteristic Information Adding Reference Schematic	P.8 & 13 P.15,16 & 17 P.36 & 37
02.18.2016	Preliminary version 0.5 - Adding ROCKO, REO function	P.9, P.12 & P.36
04.04.2016	Preliminary version 0.6 Pin Description (NC pins) Two Frame Mode	P.13 P.33
07.21.2016	Preliminary version 0.61 -Revised feature description	P.4
10.29.2016	Preliminary version 0.7 Change Memory size to 512Mbit in AL462B (MP version) and related configurations Chip marking Information	
11.21.2016	Preliminary version 0.8 -Modify RCKO & REO pinout	
01.25.2017	Preliminary version 0.95 -Adding power consumption data	
10.06.2017	Preliminary version 0.96 Modify Miscellaneous Signals pin description	
10.13.2017	Preliminary version 0.97 Modify RCLK information in Timing chart	
12.20.2017	Preliminary version 0.98 Modify pin description data- TEST,TMOD0~2,DLL_CFG[2:0],DRAM_CFG[5:0],XIN,VDD33A~H,FVDD33 and VD33M	P.11~12
04.09.2019	Release Version 1.0 -Modify pin description data- P6 RCKOEN to NC -Correct AC Characteristics- TDS to 1.5nS -Remove reference schematic to EVB DOCs	P.8,P.10,P.12 P.16
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Table of Contents

1 GENERAL DESCRIPTION

The AL462 is a First-In-First-Out (FIFO) memory that consists of 512-Mbits of memory density and can be configured as a 16M x 32-bit FIFO at maximum R/W operating speed of 150 MHz for HD video applications up to 4K2K Ultra HD resolution. The AL462 Ultra HD (UHD) FIFO can be used in a wide range of applications such as multimedia, video capture systems and many other varieties of video data buffering applications. The size and high-speed data access allow HD video frame capture up to 4Kx2K resolutions.

The AverLogic AL462 UHD FIFO memory provides completely independent input and output ports. The built-in address and pointer control circuits provide a straightforward bus interface to sequentially read/write memory that can reduce inter-chip design efforts.

The AL462 uses high performance process technologies support extended controller functions, like control signals polarity selectable, output clock phase adjustment, two frame mode (double buffer), that allow easy operations on FIFO read/write for uses in broadcasting systems, security systems, cameras and many other applications.

The AL462 is designed and manufactured using state-of-the-art technologies with low power consumption AC characteristics (1.8/3.3V power supply) facilitating high performance and high quality applications.

The chip is available in LFBGA 249-ball package; the small footprint allows product designers to keep board real estate to a minimum.

2 FEATURES

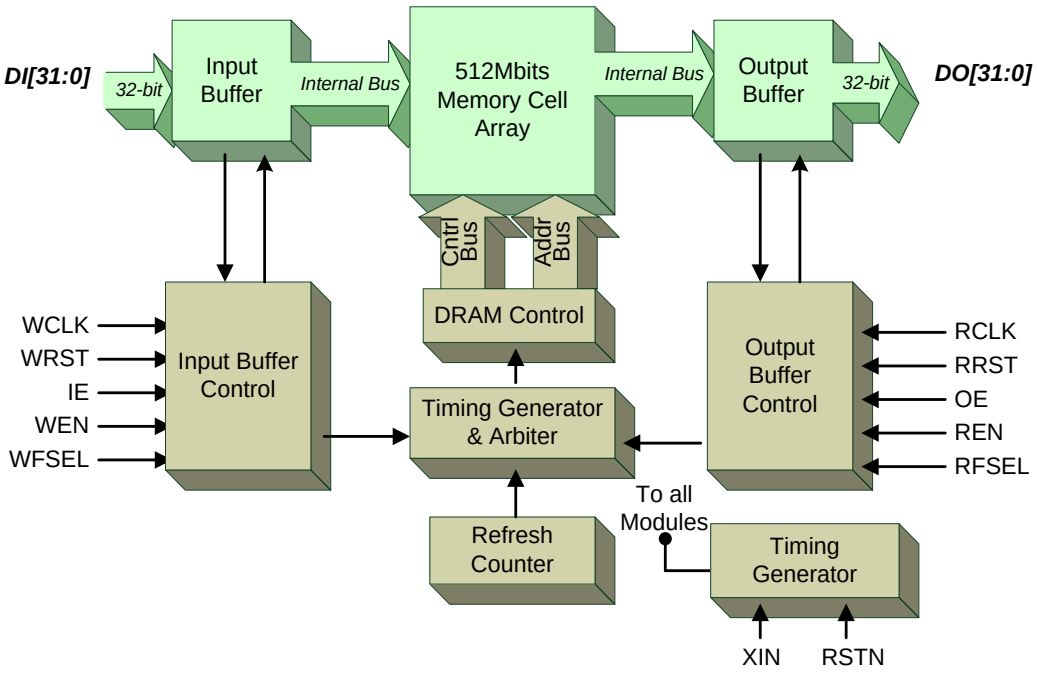
- 512-Mbit density in 16Mx32-bit configuration
- Supports video NTSC, PAL and HDTV up to 4Kx2k resolution
- Independent 32-bit read/write operations (different I/O data rates acceptable) at a maximum speed of 150 MHz (-7 version)
- High speed synchronous sequential access
- Input/ Output enable control
- Supports Output Timing Sync Clock
- Supports Two frame mode (for double buffering)
- Polarity Selectable
- 1.8/3.3V power supply
- 249-pin LFBGA package

3 APPLICATIONS

- HD video capture and editing systems
- Switcher or format converter boxes
- Video capture or editing systems
- Video data buffering for security systems
- Scan rate converters
- TBC (Time Base Correction) systems
- Frame synchronizers
- Digital video cameras
- Hard disk cache memory
- Buffer for communication systems
- 1080@60p, 4Kx2K@30p video data stream buffering

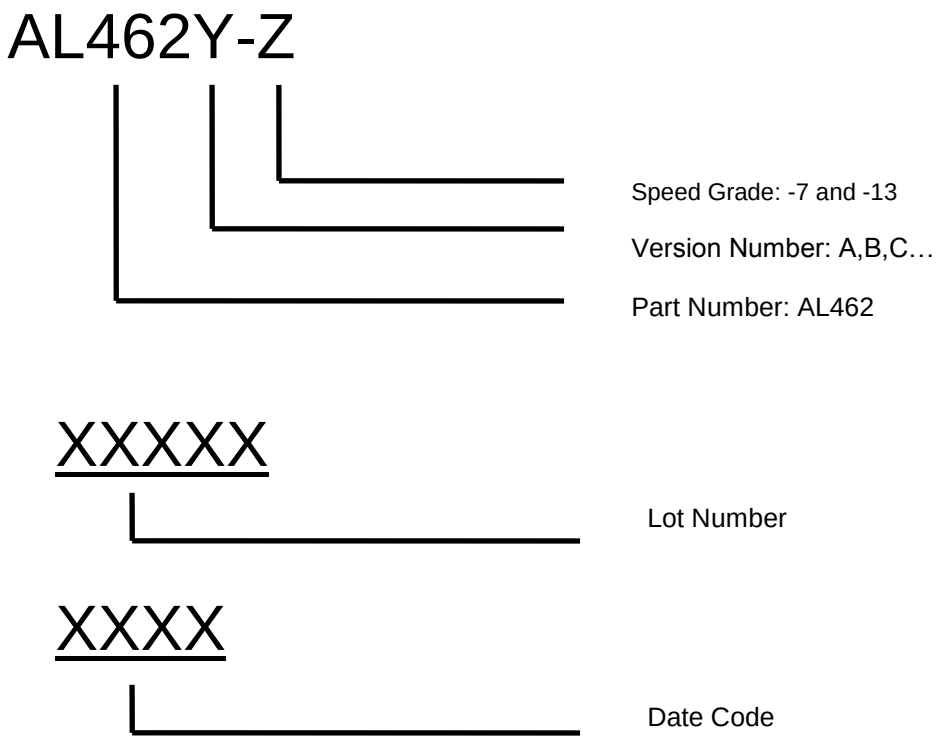
4 FUNCTION BLOCK DIAGRAM

The internal structure of each AL462 consists of Input/ Output buffers, Write Data Registers, Read Data Registers and main 16Mx32-bit memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.



5 CHIP INFORMATION

5.1 Marking Information



5.2 Ordering Information

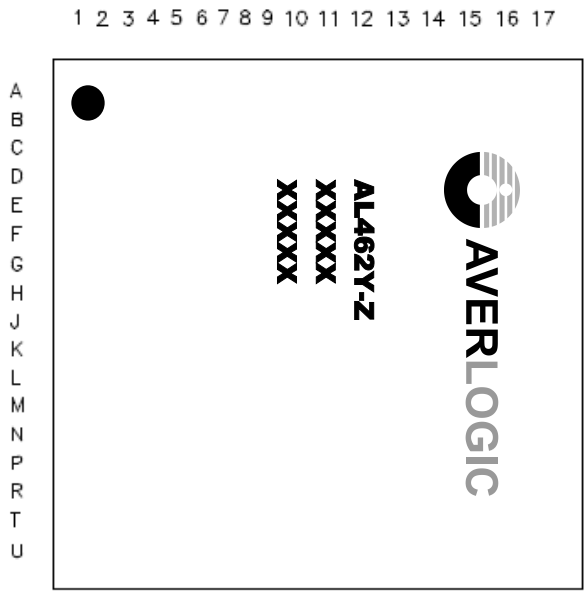
Part number	Speed Grade	Package	Power Supply	Status
AL462B-7	150 MHz	LFBGA-249	+1.8/3.3 V	
AL462B-13	75 MHz	LFBGA-249	+1.8/3.3 V	

Note: AverLogic Technologies PB-free products employ special PB-free material sets; molding compounds/die that attach materials and 100% matte tin plate termination finish do not use materials containing PBB, PBDE or red phosphorus for green-product chips. AverLogic's PB-free products are MSL classified at PB-free peak reflow temperatures that meet or exceed the PB-free requirements of IPC/JEDEC J Std-020C."

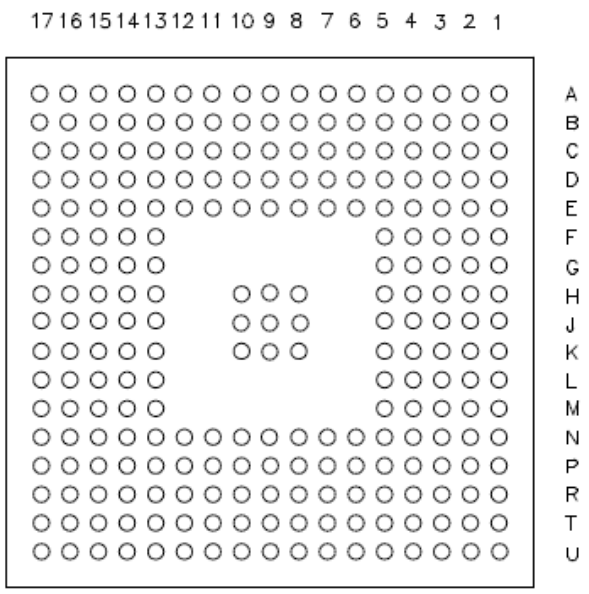
6 PIN DIAGRAM AND DESCRIPTION

6.1 Pin Diagram

TOP VIEW



BOTTOM VIEW



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	DI2	DI4	DI6	DI8	DI10	DI12	DI14	VSS33	WCLK0	VSS	NC	VSS	DI18	DI20	DI22	DI24	DI25	A
B	DI1	DI3	DI5	DI7	DI9	DI11	DI13	DI15	VDD33A	VSS33	VDD33C	DI16	DI17	DI19	DI21	DI23	DI26	B
C	DI0	NC	WEN0	WRST0	IE0	DRAM_CFG1	DRAM_CFG3	DRAM_CFG5	DLL_CFG1	NC	NC	NC	NC	TFEN	PLRTY	DI27	DI28	C
D	VSS	VSS33	NC	NC	NC	DRAM_CFG0	DRAM_CFG2	DRAM_CFG4	DLL_CFG0	DLL_CFG2	NC	NC	16EN	NC	WFSEL0	DI29	DI30	D
E	XOUT	VSS	TMOD0	TMOD1	NC	VD33M	VDD	VDD	VDD	VDD	VDD	VSS	DVC18	WFSEL1	WEN1	DI31	VSS33	E
F	XIN	DVC18	NC	TMOD2	NC								DVQ18	NC	WRST1	VDD33B	WCLK1	F
G	VSS	DVC18	DVC18	TEST	NC								VSS	NC	IE1	VSS	VSS33	G
H	NC	NC	NC	NC	NC			AVDD18_PLL1	AVSS_PLL1	DVQ18			VSS	VSS	NC	VDD33D	NC	H
J	FVDD33	FVSS33	VSS	NC	NC			AVDD18_PLL2	AVSS_PLL2	VSS			VSS	VSS	VSS	VSS	VSS	J
K	RSTN	NC	REN0	NC	NC			AVDD18_PLL3	AVSS_PLL3	DVC18			DVQ18	DVQ18	DVQ18	DVQ18	DVQ18	K
L	DO0	RENO0	RRST0	NC	NC								VSS	DVQ18	DVQ18	VSS	VREF2	L
M	DO2	DO1	NC	VSS	NC								VSS33	DVC18	DVQ18	VSS	VSSR1	M
N	DO4	DO3	NC	OE0	VDD33E	VDD	VSS	VSS33	VDD	VDD33G	VSS33	VDD	VSS	VDD	VSS	VSS33	VREF1	N
P	DO6	DO5	NC	NC	RFSEL1	NC	NC	RCKOINV0	NC	NC	RCKOINV1	NC	REN1	RRST1	OE1	VDD33H	VSS33	P
R	DO8	DO7	NC	RFSEL0	NC	NC	NC	NC	NC	NC	NC	NC	RENO1	NC	NC	VDD33F	RCKO1	R
T	DO9	DO11	DO13	DO15	VDD33E	VSS33	VSS	DO16	DO17	DO19	DO21	DO23	DO25	DO27	DO29	DO31	VDD33H	T
U	DO10	DO12	DO14	VSS33	RCLK0	VDD33G	RCKO0	VSS33	DO18	DO20	DO22	DO24	DO26	DO28	DO30	VDD33F	RCLK1	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

	Miscellaneous Signals
	Read Bus Signals
	Write Bus Signals
	NC
	PW/GND

249-BALL LFBGA Block Diagram

6.2 Pin Description

Write Bus Signals

Pin Name	Ball No	Type	Description
DI[31:0]	E16, D17, D16, C17, C16, B17, A17, A16, B16, A15, B15, A14, B14, A13, B13, B12, B8, A7, B7, A6, B6, A5,B5, A4, B4, A3, B3, A2, B2, A1, B1, C1	I	32/16-bit data inputs; synchronized with the WCLK clock. Data is acquired at the rising edge of WCLK clock. The mapping between 32-bit and 16-bit x2 bus configuration are; DI[7:0]=DIA[7:0] DI[15:8]=DIA[15:8] DI[23:16]=DIB[7:0] DI[31:24]=DIB[15:8]
WEN0 & WEN1	C3, E15	I	WEN is the write enable signal that controls the 32/16-bit input data write and write pointer operation. WEN0 is write enable signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); WEN0 and WEN1 are write enable signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
IE0 & IE1	C5, G15	I	IE is the data input enable signal that controls the enabling/ disabling of the 32/16-bit data input pins. The internal write address pointer is always incremented at the rising edge of WCLK by enabling WEN regardless of the IE level. IE0 is data input enable signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); IE0 and IE1 are data input enable signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
WCLK0 & WCLK1	A9, F17	I	WCLK is the write clock input pin. The write data input is synchronized with this clock. WCLK0 is write clock input to control all 32-bit bus operation in 32-bit mode (16EN="L"); WCLK0 and WCLK1 are write clock inputs to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
WRST0 & WRST1	C4, F15	I	The WRST is the write rest signal that resets the write address pointer to 0. WRST0 is write rest signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); WRST0 and WRST1 are write rest signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
WFSEL0 & WFSEL1	D15, E14	I	Write Frame select pin in Two Frame Mode (TFEN = H): "L": Frame 0 "H": Frame 1 WFSEL0 is write frame select signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); WFSEL0 and WFSEL1 are write frame select signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.

*Note1: For the polarity definition of all write control signals (WEN, IE and WRST), please refer to the PLRTY pin definition and “Memory Operation” section for details.

Read Bus Signals

Pin Name	Ball No	Type	Description
DO[31:0]	T16, U15, T15, U14, T14, U13, T13, U12, T12, U11, T11, U10, T10, U9, T9, T8, T4, U3, T3, U2, T2, U1, T1, R1, R2, P1, P2, N1, N2, M1, M2, L1	O	31/16-bit data outputs; synchronized with the RCLK clock. Data is output at the rising edge of the RCLK clock. The mapping between 32-bit and 16-bit x2 bus configuration are; DO[7:0]=DOA[7:0] DO[15:8]=DOA[15:8] DO[23:16]=DOB[7:0] DO[31:24]=DOB[15:8]
REN0 & REN1	K3, P13	I	REN is the read enable signal that controls the 16-bit output data read and read pointer operation. REN0 is read enable signal to control all 32-bit bus operation in 32-bit mode (16EN=“L”); REN0 and REN1 are read enable signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN=“H”) respectively.
OE0 & OE1	N4, P15	I	OE is the data input enable signal that controls the enabling/ disabling of the 16- bit data output pins. The internal read address pointer is always incremented at the rising edge of RCLK by enabling REN regardless of the OE level. OE0 is data output enable signal to control all 32-bit bus operation in 32-bit mode (16EN=“L”); OE0 and OE1 are data output enable signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN=“H”) respectively.
RCLK0 & RCLK1	U5, U17	I	RCLK is the read clock input pin. The read data output is synchronized with this clock. RCLK0 is read clock output to control all 32-bit bus operation in 32-bit mode (16EN=“L”); OCLK0 and WCLK1 are read clock outputs to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN=“H”) respectively.
RCKO0 & RCKO1	U7, R17	O	RCLK loop-out clocks
RENO0 & RENO1	L2, R13	O	RENO0 and RENO1 are “read enable” output signals that are synchronous with RCKO0 and RCKO1 output clocks respectively
RCKOINV0 &RCKOINV1	P8, P11	I	RCKO0 & RCKO1 loop-out clock inversion controls; “L”: RCKO0 & RCKO1 no inversion. “H”: RCKO0 & RCKO1 output inverted
RRST0 & RRST1	L3, P14	I	The RRST is the read reset signal that resets the read address pointer to 0. RRST0 is read rest signal to control all 32-bit bus operation in 32-bit mode (16EN=“L”); RRST0 and RRST1 are read rest signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode

			(16EN="H") respectively
RFSEL0 & RFSEL1	R4, P5	I	Read Frame select pin in Two Frame Mode (TFEN ="H"): "L": Frame 0 "H": Frame 1 RFSEL0 is read frame select signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); RFSEL0 and RFSEL1 are read frame select signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN="H") respectively.

**Note2: For the polarity definition of all read control signals (REN, OE, RRST,), please refer to PLRTY pin definition and "Memory Operation" section for details.

*Note3: Signals RCKO, REO and RCKOINV are not available in reversion "A". The active states for the loop-out read clock control signals, REO and RCKOINV are also determined by PLRTY pin definitions: active "High" when PLRTY is "GND", active "Low" when PLRTY is "VDD".

Power/Ground Signals

Pin Name	Ball No	Type	Description
DVC18, DVQ18	F2, G3, G2, M14, M15, L14, L15, K13, K14, K10, K15,K16, H10, K17, F13, E13	PW	1.8V ±5% power supply for internal memory
VDD	E7,N6,N14,N9,N12, E11,E9,E10,E8	PW	1.8V ± 5% power supply for internal control logic
AVDD18_PLL1,AVDD18_PLL2,AVDD18_PLL3	H8, J8, K8	PW	1.8V ±5% power supply for PLL
VDD33A, VDD33B, VDD33C, VDD33D	B9, F16, B11, H16	PW	3.3V ± 5% power supply for input I/O
VDD33E,VDD33F, VDD33G,VDD33H	N5, T5, U16, R16, U6, N10, T17, P16	PW	3.3V ± 5% power supply for output I/O
FVDD33	J1	PW	3.3V ± 5% power supply for internal logic
VD33M	E6	PW	3.3V ± 5% power supply for internal logic
VSS	D1,E2,G1,J3N7, N15,T7,N13,M4,M16,L13,L16,H13,J14,J15,J13,J16,J10,H14,G13,E12,J17,A12,G16,A10	GND	Internal memory chip GND
VSS33	D2,M13,U4,T6, N16,N8,U8,N11,P17,G17,B10,E17,A8	GND	Input/ Output data I/O GND
FVSS33	J2	GND	GND
AVSS_PLL1, AVSS_PLL2,AVSS_PLL3	H9, J9, K9	GND	PLL GND

Miscellaneous Signals

Pin Name	Ball No	Type	Description
RSTN	K1	I	Global reset (active Low)
PLRTY	C15	I	Select active polarity of the control signals including WEN, REN, WRST, RRST, IE, OE, ROEN and ROINV (total of 8 signals) PLRTY = VDD33, active low. PLRTY = GND, active high. Note: during memory operation, the pin must be permanently connected to VD33 or GND. If PLRTY level is changed during memory operation, memory data is not guaranteed.
XIN	F1	I	Crystal/oscillator input 27 MHz * Minimum crystal frequency accuracy: ±100 ppm TMOD2 pin pull-down to enable XIN pin
XOUT	E1	O	Crystal output
VREF1	N17	A I	Reference voltage input * Please refer to “External decoupling circuit” application note for details
VREF2	L17	A I	Reference voltage input 2 * Please refer to “External decoupling circuit” application note for details
VSSR1	M17	-	Reference voltage ground * Please refer to “External decoupling circuit” application note for details
16EN	D13	I	16-bit bus configuration enable “L” – 32-bit Input and Output bus width (Default) “H” – 16-bit x2 Input and Output bus width
TFEN	C14	I	Two frame mode enable: “L” – Standard FIFO Mode “H” – Two Frame Mode
TEST	G4	I	Test pin (pull-down for normal operation, internal floating)
TMOD0	E3	I	Test pin (pull-down for normal operation, internal floating)
TMOD1	E4	I	Test pin (pull-down for normal operation, internal floating)
TMOD2	F4	I	Test PIN (Pull-down crystal/oscillator input from XIN pin, internal floating)
DLL_CFG[2:0]	D10, C9, D9	I	NC for normal operation (internal pull-down by default), add 10K ohm pull up circuit for option
DRAM_CFG[5:0]	C8,D8,C7,D7,C6,D6	I	NC for normal operation (internal pull-down by default), add 10K ohm pull up circuit for option
NC	A11,C2,C12,C13,D3,D4,D5,D11,D12,D14,E5,F3,F5,F14,G5,G14,H1,H2,H3,H4,H5,H15,H17,J5,K2,M	-	No connect

	3,N3,P3,P4,P6,P7,P9,P10,P12,R3,R5,R6,R7,R8,R9,R10,R11,R12,R14,R15,J4,K4,,K5,L4,L5,M5,C10,C11,D11		

7 Electrical Characteristics

7.1 Absolute Maximum Ratings Under Free-Air Temperature

(These devices are designed to operate within the max/min ratings as specified. Operation beyond these limits may result in permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.)

Parameter		Rating	Unit
VDD33 (VDD33A~H,VD33M,FVDD33)	3.3V I/O Supply Voltage	-0.3 ~ +4.5	V
DVC18/ DVQ18	1.8V Memory Voltage	-0.3 ~ +1.95	V
VDD	1.8V Core Voltage	-0.3 ~ +1.95	V
AVDD1 8_PLL	1.8V PLL Voltage	-0.3 ~ +1.95	V
V_P	Pin Voltage	-0.3 ~ +(VDD33 + 0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +70	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

7.2 Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VDD33=3.3V	I/O Supply Voltage = 3.3V	3.0	3.3	3.6	V
VDD/ DVC18/DVQ18/ AVDD18_PLL	1.8V Core, Memory and PLL Voltage	1.70	1.8	1.95	V
V_{IH}	High Level Input Voltage	0.7VDD33	-	VDD33	V
V_{IL}	Low Level Input Voltage	0	-	0.3VDD33	V

7.3 DC Characteristics

(VDD33 = 3.3V, VDD=DVC18=DVQ18=AVDD_PLL= 1.8V; T_{AMB} = 0 to 70°C)

Parameter		Min	Typ	Max	Unit
150Mhz (-7) version					
I_{DD33}	Operating Current		89		mA
I_{DD18}	Operating Current		407		mA
***** Operating condition: WCLK = RCLK = 150 MHz; Data toggle rate = 20 MHz					
I_{SB33}	Standby Current		13		mA
I_{SB18}	Standby Current		325		mA
***** Standby condition: WCLK = RCLK = 0 MHz					
75Mhz (-13) version					
I_{DD33}	Operating Current		66		mA
I_{DD18}	Operating Current		226		mA
***** Operating condition: WCLK = RCLK = 75 MHz; Data toggle rate = 20 MHz					
I_{SB33}	Standby Current		13		mA
I_{SB18}	Standby Current		180		mA
***** Standby condition: WCLK = RCLK = 0 MHz					
V_{OH}	Hi-level Output Voltage	VDD33-0.4			V
V_{OL}	Lo-level Output Voltage			0.4	V
I_{LI}	Input Leakage Current (No pull-up or pull-down)	-10		+10	µA
I_{LO}	Output Leakage Current (No pull-up or pull-down)	-10		+10	µA
R_L	Input Pull-up/Pull-down Resistance		10		KΩ

7.4 AC Characteristics

(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

Parameter		150 MHZ		75 MHz		Unit
		Min	Max	Min	Max	ns
TWC	WCLK Cycle Time	6.6	-	13.3	-	ns
TWPH	WCLK High Pulse Width	2.6	-	5.3	-	ns
TWPL	WCLK Low Pulse Width	2.6	-	5.3	-	ns
TRC	RCLK Cycle Time	6.6	-	13.3	-	ns
TRPH	RCLK High Pulse Width	2.6	-	5.3	-	ns
TRPL	RCLK Low Pulse Width	2.6	-	5.3	-	ns
TAC	Access Time	3.0	8.0	3.0	9.5	ns
TOH	Output Hold Time	0.6	-	1.0	-	ns
THZ	Output High-Z Setup Time	3.0	8.0	3.0	9.5	ns
TLZ	Output Low-Z Setup Time	1.0	-	1.0	-	ns
TWRS	WRST Setup Time	0.5	-	2.0	-	ns
TWRH	WRST Hold Time	2.5	-	2.5	-	ns
TRRS	RRST Setup Time	0.5	-	2.0	-	ns
TRRH	RRST Hold Time	2.5	-	2.5	-	ns
TDS	Input Data Setup Time	1.5	-	2.0	-	ns
TDH	Input Data Hold Time	2.5	-	2.5	-	ns
TWES	WEN Setup Time	0.5	-	2.0	-	ns
TWEH	WEN Hold Time	2.5	-	2.5	-	ns
TWPW	WEN Pulse Width	3.0	-	4.5	-	ns
TRES	REN Setup Time	0.5	-	2.0	-	ns
TREH	REN Hold Time	2.5	-	2.5	-	ns
TRPW	REN Pulse Width	3.0	-	4.5	-	ns
TIES	IE Setup Time	0.5	-	2.0	-	ns
TIEH	IE Hold Time	2.5	-	2.5	-	ns
TIPW	IE Pulse Width	3.0	-	4.5	-	ns
TOES	OE Setup Time	0.5	-	2.0	-	ns
TOEH	OE Hold Time	2.5	-	2.5	-	ns
TOPW	OE Pulse Width	3.0	-	4.5	-	ns
TTR	Transition Time					ns

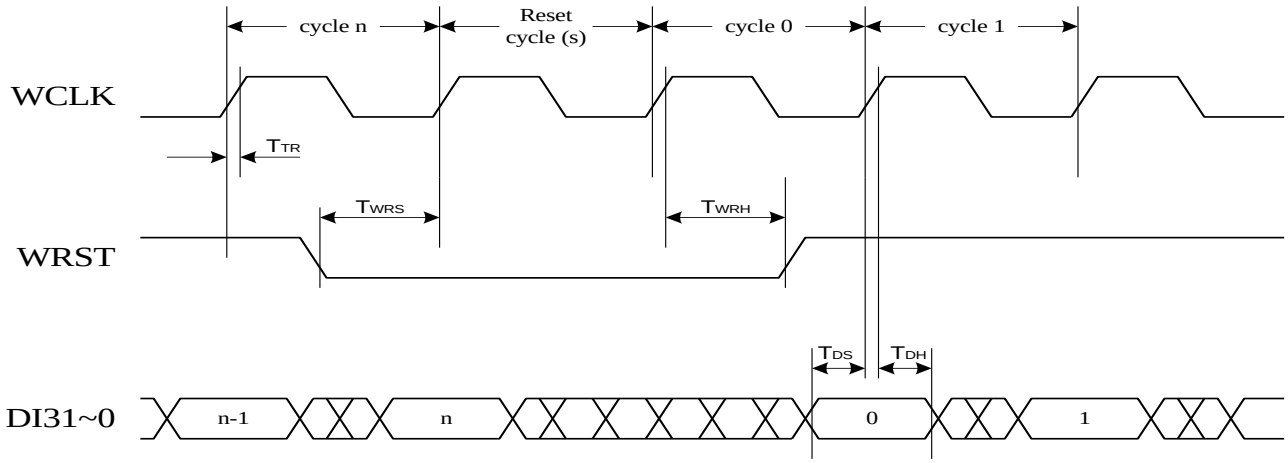
C_I	Input Capacitance					ns
C_O	Output Capacitance					ns

Note: The read address needs to be at least 1,536 cycles after write address to guarantee new data read.

8 TIMING DIAGRAM

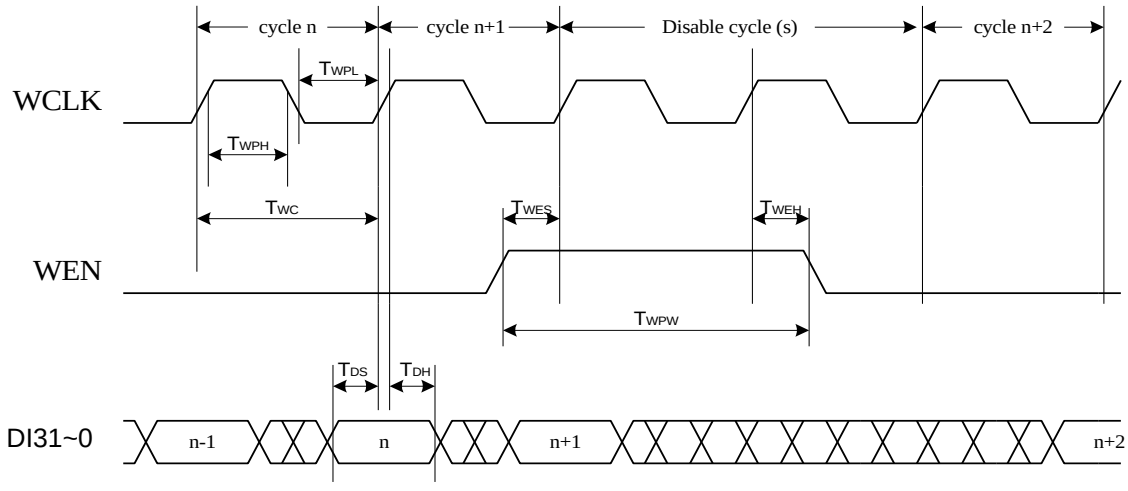
Note: Signals in timing diagram denote the general symbols. In 32-bit data mode, 32-bit data are synchronous with control signals denote “0” accordingly (WCLK0, WE0, RCLK0 and RE0 etc.).
In 16-bit x2 data mode, data bit 0 – 15 are synchronous with control signals denote “0” (WCLK0, WE0, RCLK0 and RE0 etc.) while data bit 16 - 31 are synchronous with control signals denote “1” (WCLK1, WE1, RCLK1 and RE1 etc.) accordingly.

PLRTY = VDD Timing



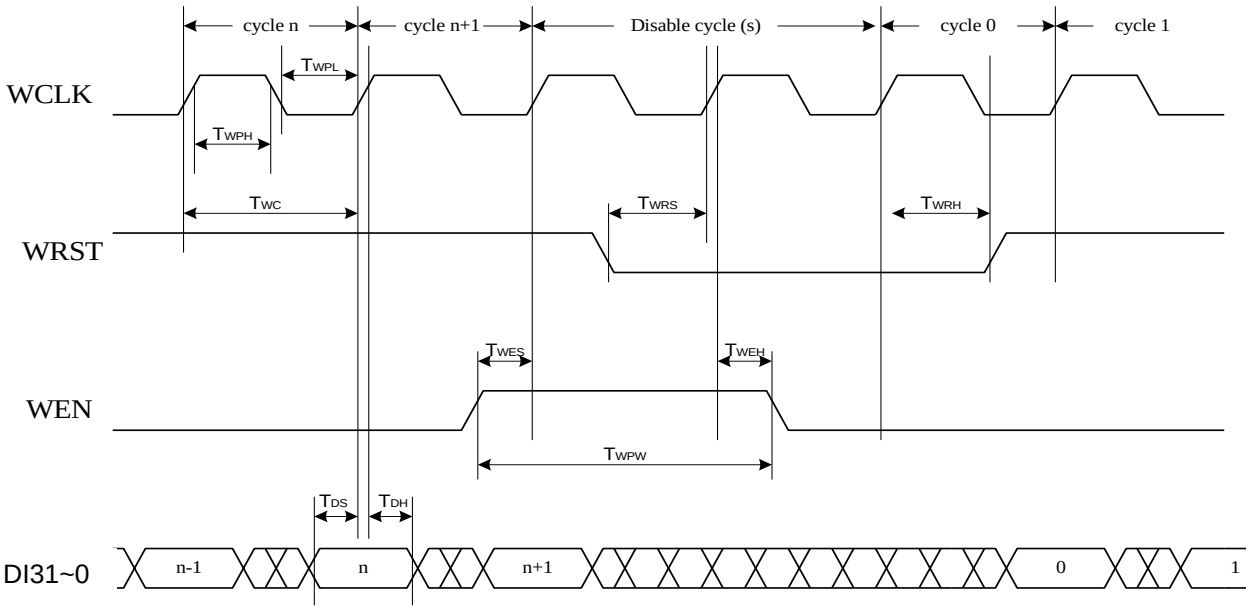
/PLRTY=VDD , WEN= "L" , IE= "L"

Write Cycle Timing (Write Reset)



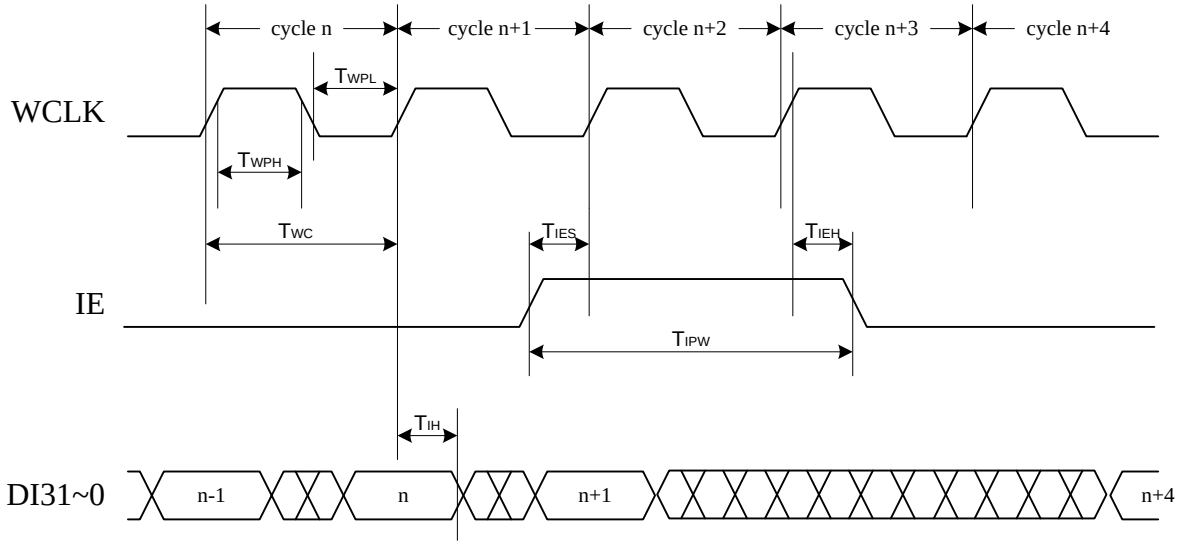
/PLRTY=VDD ,IE="L" ,WRST="H"

Write Cycle Timing (Write Enable)



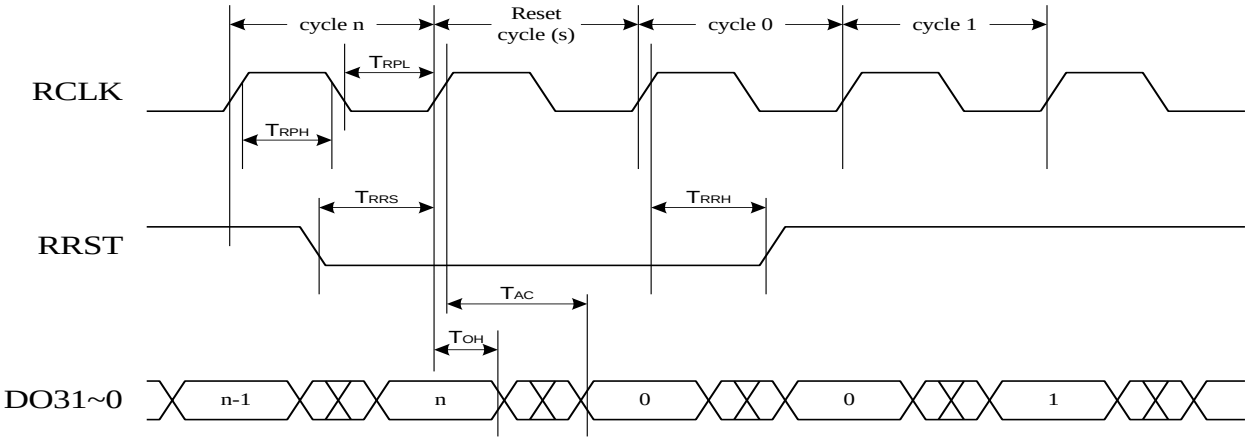
/PLRTY=VDD ,IE="L"

Write Cycle Timing (WEN, WRST)



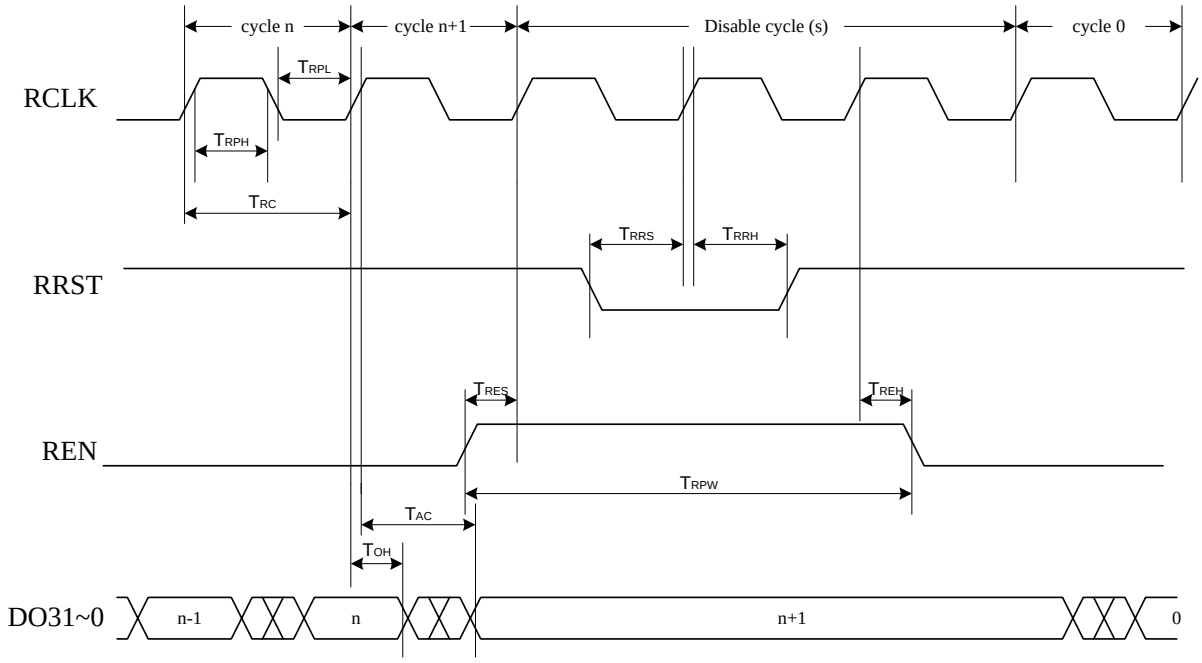
/PLRTY=VDD, WEN="L", WRST="H"

Write Cycle Timing (Input Enable)



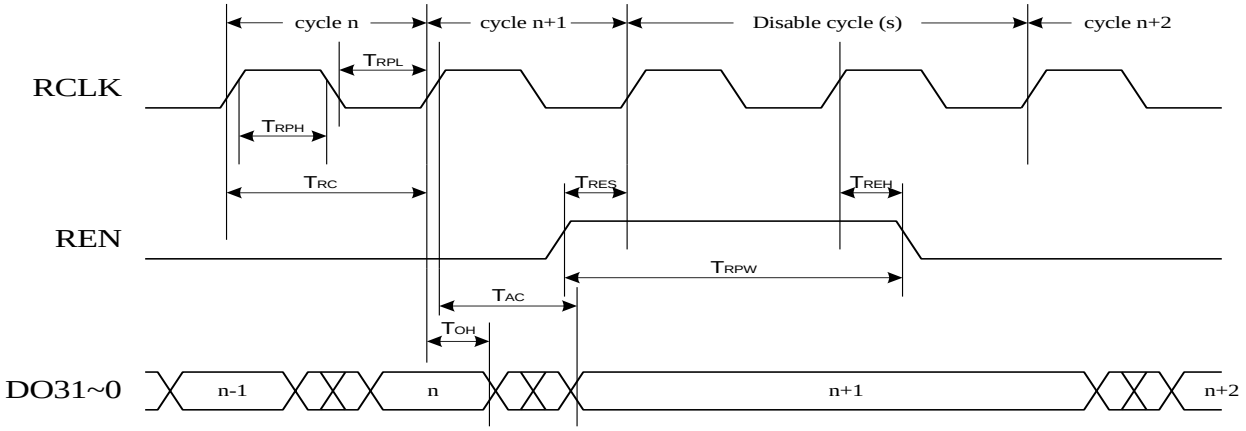
/PLRTY=VDD ,REN= "L" ,OE= "L"

Read Cycle Timing (Read Reset)



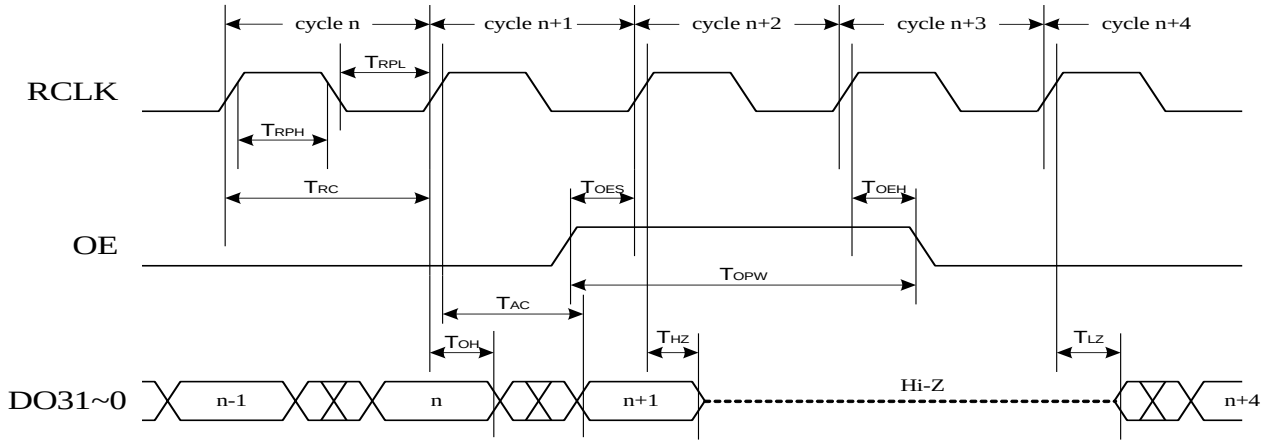
/PLRTY=VDD, OE="L"

Read Cycle Timing (REN, RRST)



/PLRTY=VDD ,OE="L" ,RRST="H"

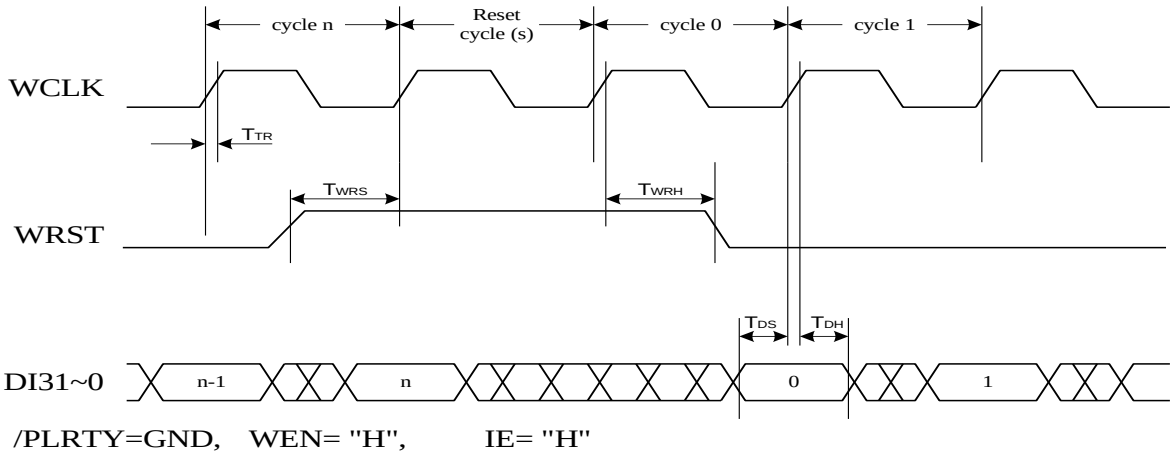
Read Cycle Timing (Read Enable)



/PLRTY=VDD ,REN="L" ,RRST="H"

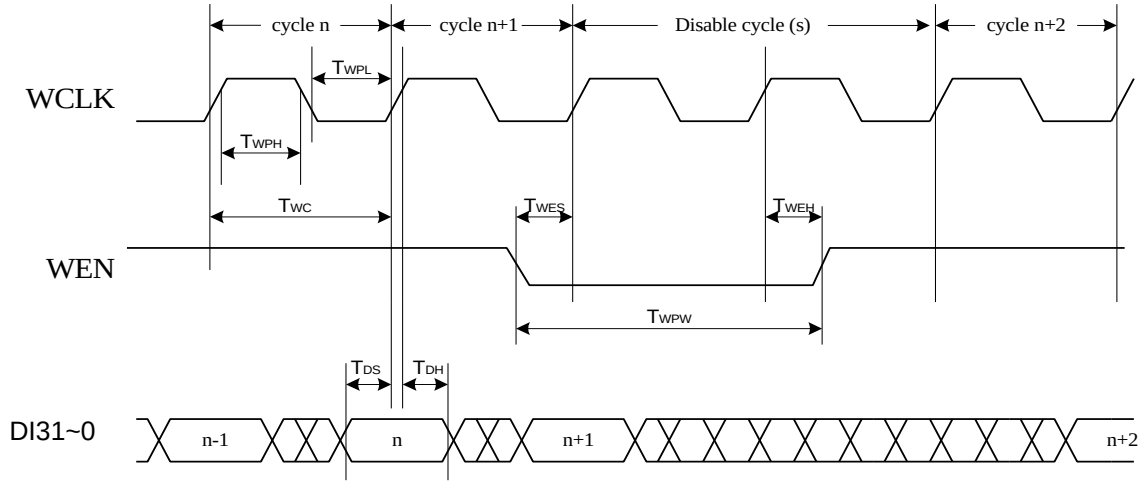
Read Cycle Timing (Output Enable)

PLRTY = GROUND (GND) Timing



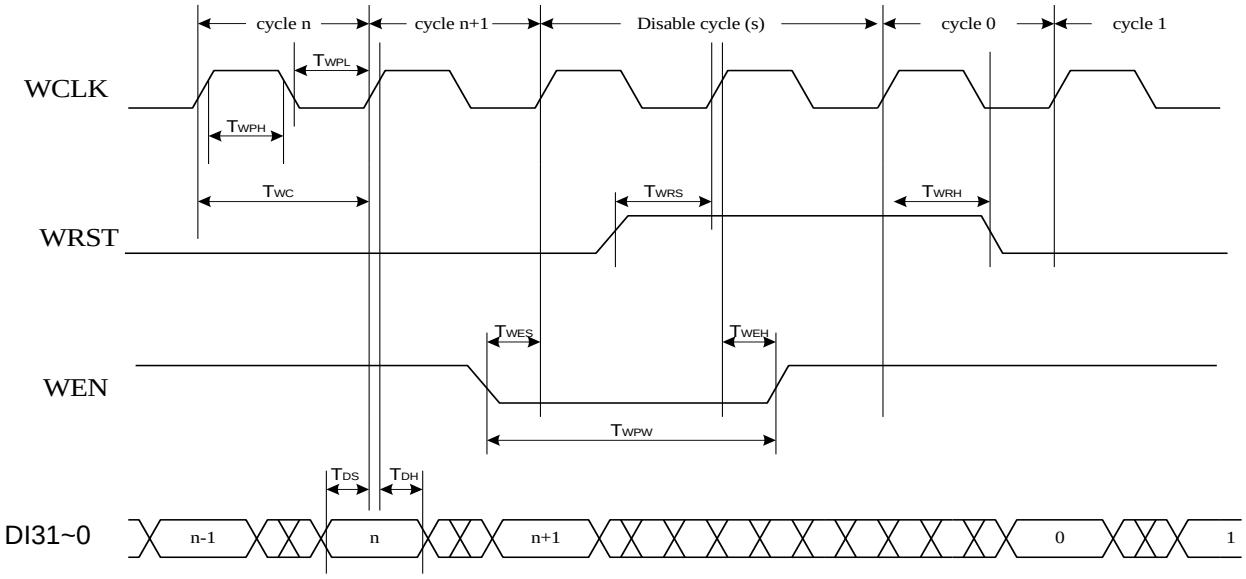
/PLRTY=GND, WEN= "H", IE= "H"

Write Cycle Timing (Write Reset)



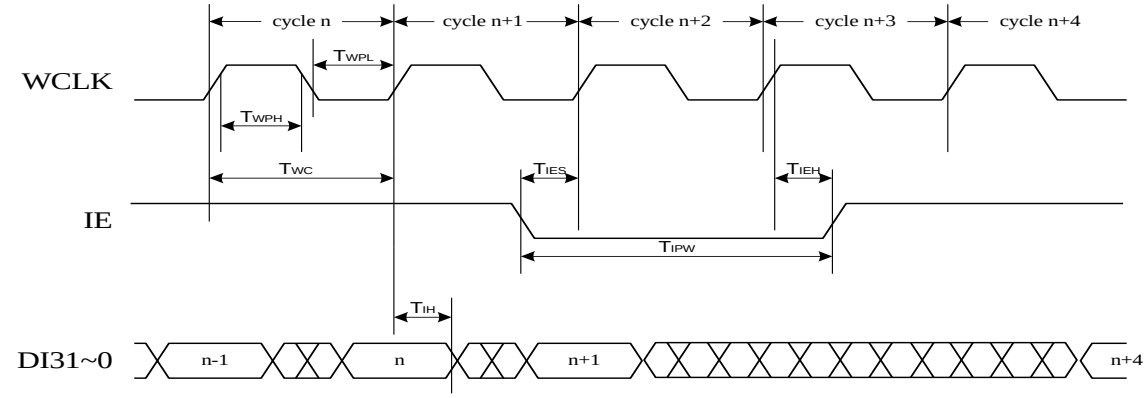
/PLRTY=GND, IE="H", WRST="L"

Write Cycle Timing (Write Enable)



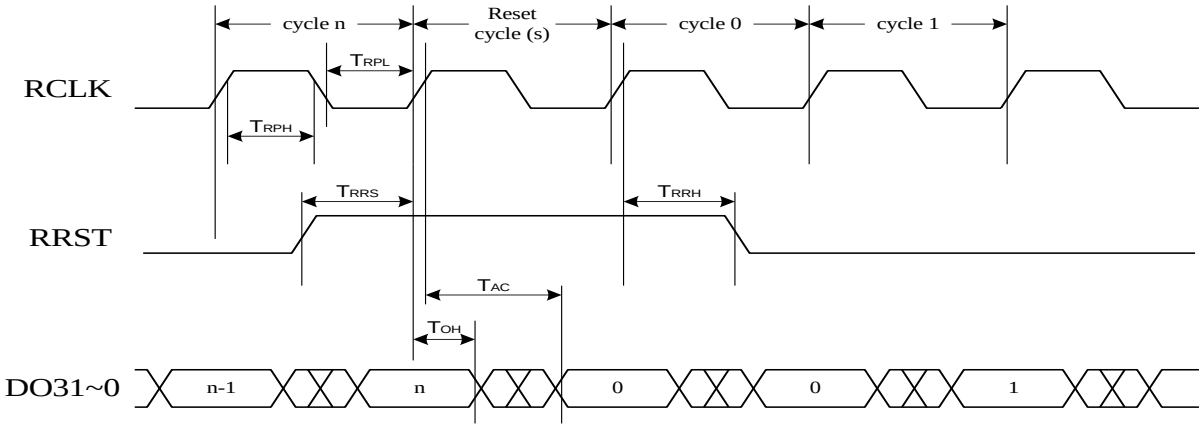
/PLRTY=GND, IE="H"

Write Cycle Timing (WE, WRST)



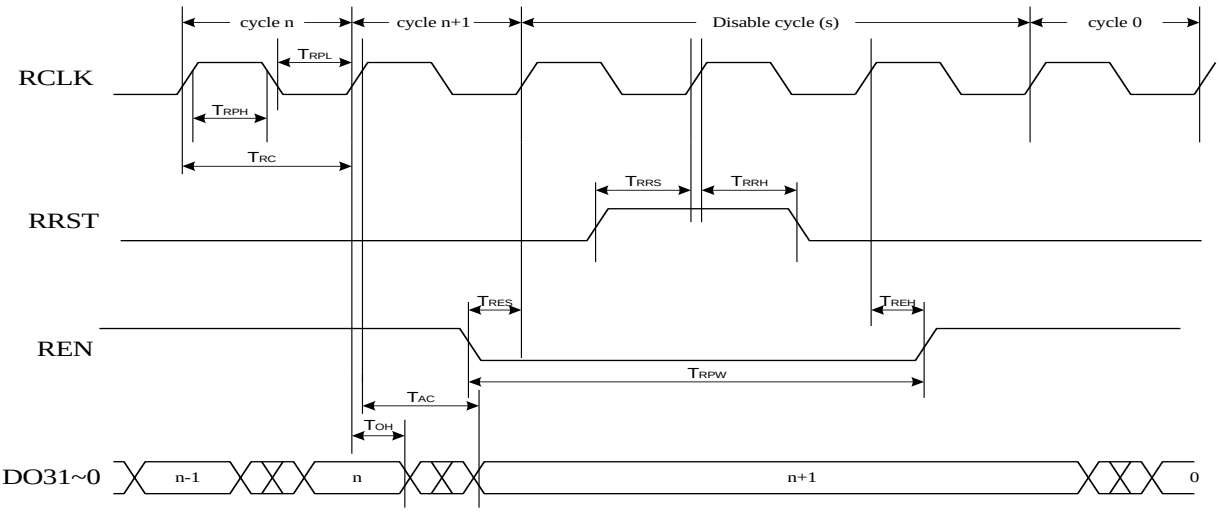
/PLRTY=GND, WEN="H", WRST="L"

Write Cycle Timing (Input Enable)



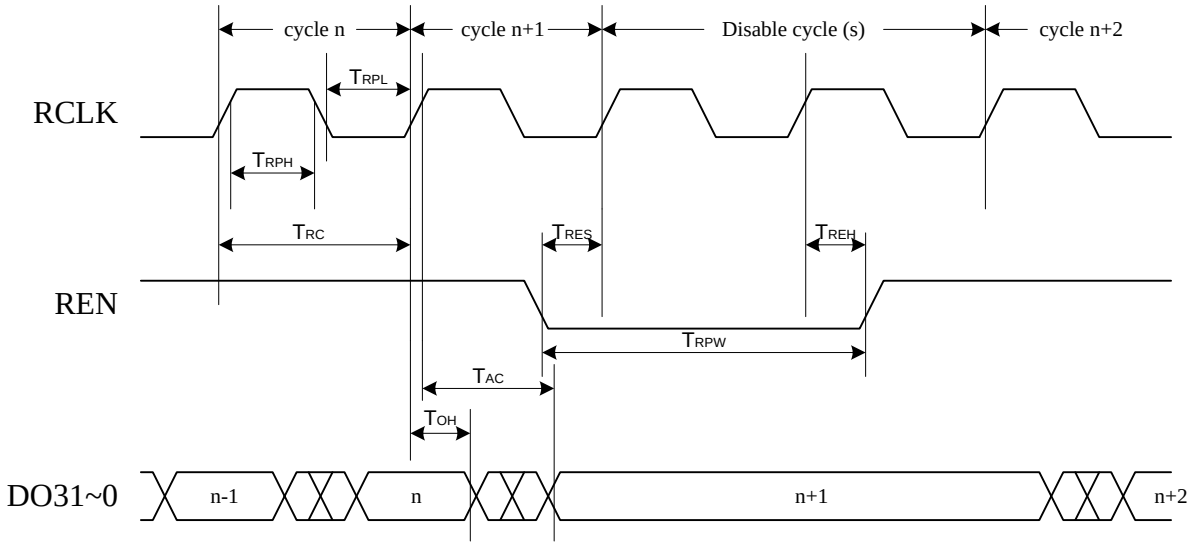
/PLRTY=GND, REN= "H", OE= "H"

Read Cycle Timing (Read Reset)



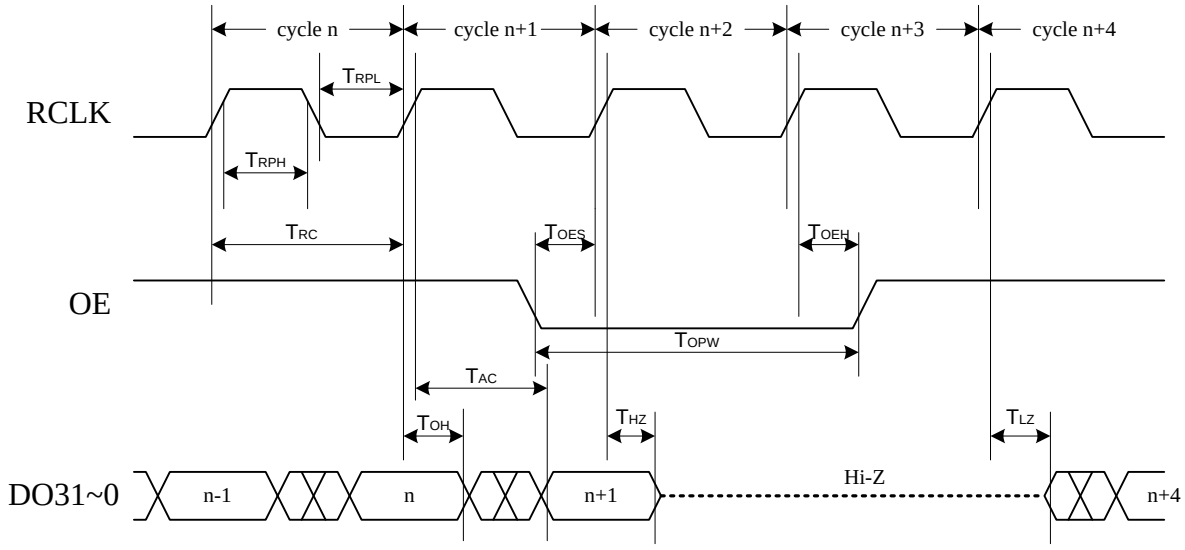
/PLRTY=GND, OE="H"

Read Cycle Timing (REN, RRST)



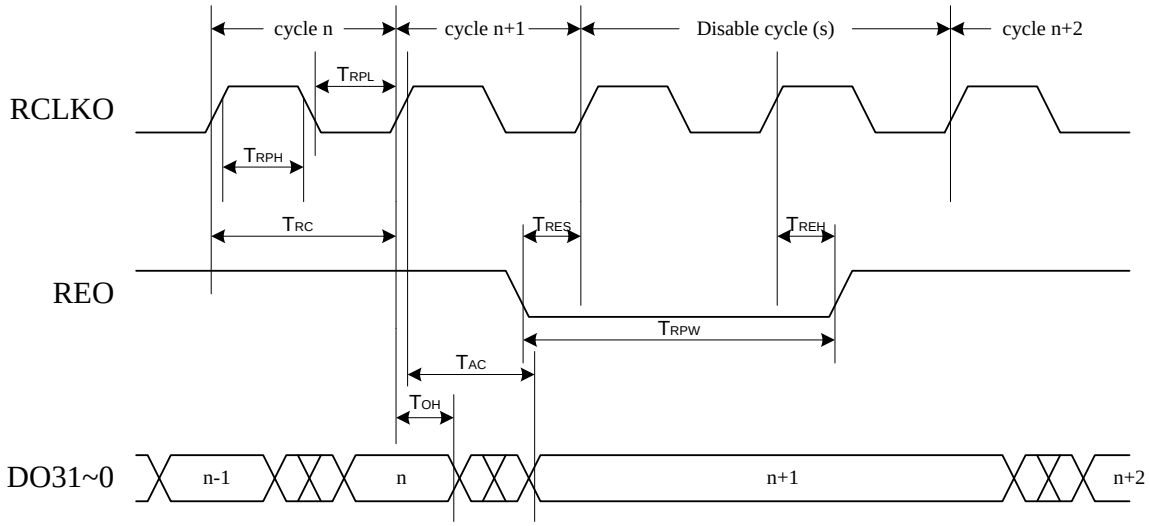
/PLRTY=GND ,OE="H" ,RRST="L"

Read Cycle Timing (Read Enable)



/PLRTY=GND ,REN="H" ,RRST="L"

Read Cycle Timing (Output Enable)



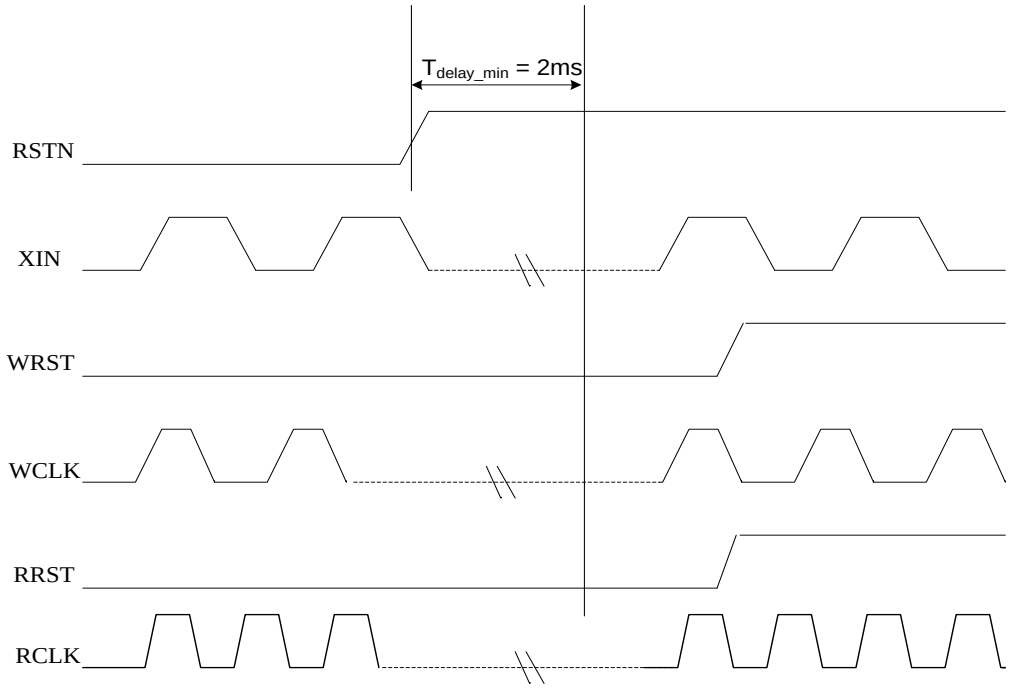
/PLRTY=GND ,OE="H" ,RRST="L"

RCKO Read Cycle Timing (Read Enable)

9 FUNCTION DESCRIPTION

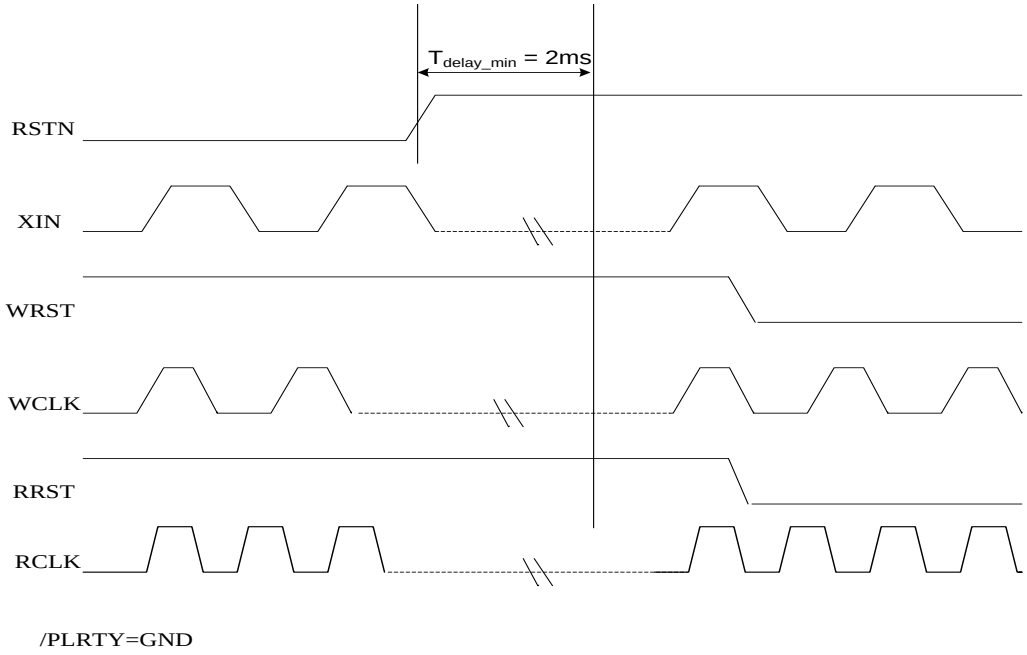
9.1 Power-On-Reset & Initialization

During system power-up, a power-on-reset is required for successful initialization of FIFO internal logic. After deactivation of its reset state, wait for T_{delay_min} (2 ms) before applying any operations to ensure the FIFO is in the normal operating state. Apply a valid reset pulse of WRST and RRST after power-on-reset to guarantee Read/Write operations start at a known address (address point at zero). The following diagrams illustrate global reset and R/W reset timings at power-up with polarity equals VDD and GND



/PLRTY=VDD

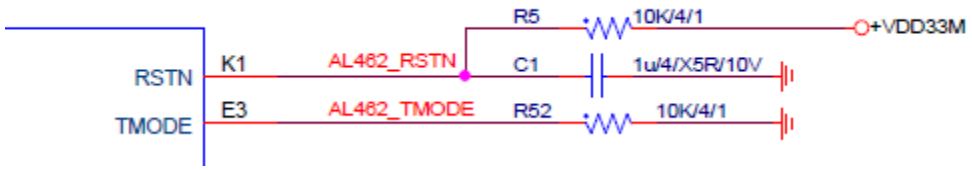
Chip Reset& R/W Reset Timing (Power-on-reset)



/PLRTY=GND

Chip Reset& R/W Reset Timing (Power-on-reset)

Following is a reference RC circuit.



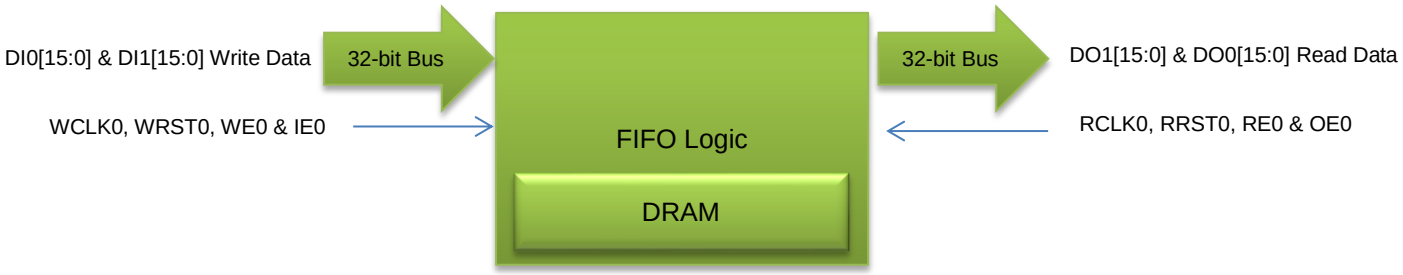
Reset Circuit for RSTN

9.2 FIFO Bus Configurations

FIFO Bus Configurations The FIFO memory can be configured to 32-bit or 16-bit x2 modes and selected by pin 16EN input pin; where Signal 16EN =

- "0" – 32-bit Input and Output bus width (Default)
- "1" – 16-bit x2 Input and Output bus width.

AL462 32-bit Signal Bus I/O



AL462 16-bit x2 Dual Bus I/O

9.3 WRST, RRST Reset Operation

The reset signal can be given at any time regardless of the WEN, REN and OE status. However, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again.

9.4 Control Signals Polarity Select

The AL462 provides the option for operating polarity on controlling signals. With this feature the application design can benefit by matching up the operation polarity between the AL462 and an existing interfacing device without additional glue logic. The operating polarity of control signals WEN, REN, WRST, RRST, IE and OE are controlled by the PLRTY signal. When PLRTY is pulled high, all 6 signals will be active low. When PLRTY is pulled low, all 6 signals will be active high.

9.5 FIFO Write Operation

In the FIFO write operation, 32 bits of write data are input in synchronization with the WCLK clock. The FIFO write operation is determined by WRST, WEN, IE and WCLK signals and the combination of these signals can produce different write results. The PLRTY signal determines the activated polarity of these control signals. The following tables describe the WRITE functions under different operating polarities.

PLRTY = VDD

WRST	WEN	IE	WCLK	Function
L	-	-	↑	Write reset. The write pointer is reset to zero.
H	L	L	↑	Normal Write operation.
H	L	H	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
H	H	-	↑	Write operation stopped. Write address pointer is also stopped.

PLRTY = GND

WRST	WEN	IE	WCLK	Function
H	-	-	↑	Write reset. The write pointer is reset to zero.
L	H	H	↑	Normal Write operation.
L	H	L	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
L	L	-	↑	Write operation stopped. Write address pointer is also stopped.

9.6 FIFO Read Operation

In the FIFO read operation, 32 bits of read data are available in synchronization with the RCLK clock. The access time is stipulated from the rising edge of the RCLK clock. To ensure a valid data read, a minimum of 1.5 Kbyte data write has to occur before any read operations. The FIFO read operation is determined by RRST, REN, OE and RCLK signals; the combination of these signals could produce varying read results. The PLRTY signal could decide the activated polarity of these control signals. The following tables describe the READ functions under different operating polarities.

PLRTY = VDD

RRST	REN	OE	RCLK	Function
L	L	L	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
L	L	H	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
L	H	L	↑	Read address pointer is stopped. Output data is held.

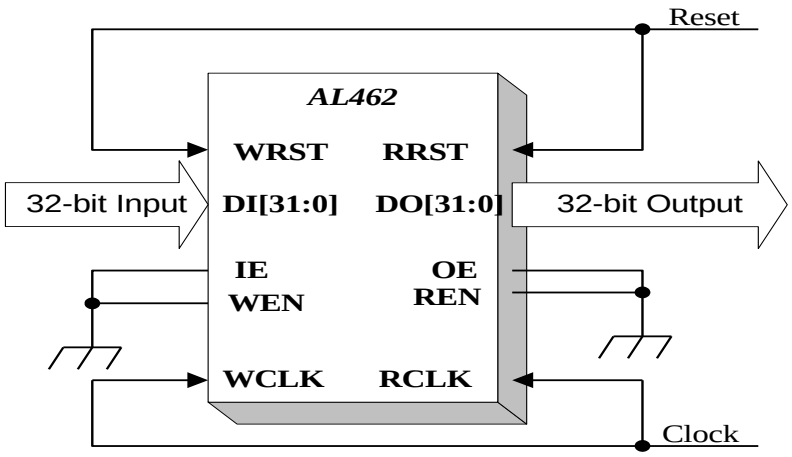
				Read address pointer will be reset to zero and data in the address 0 is output after RE goes low.
L	H	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low.
H	L	L	↑	Normal Read operation.
H	L	H	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
H	H	L	↑	Read address pointer is stopped. Output data is held.
H	H	H	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

PLRTY = GND

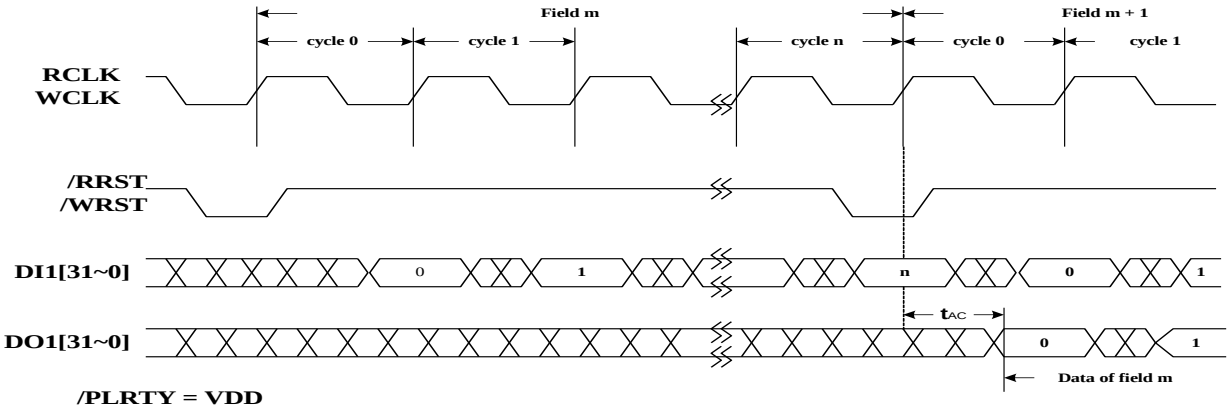
RRST	REN	OE	RCLK	Function
H	H	H	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
H	H	L	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
H	L	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after REN goes low.
H	L	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after REN goes low.
L	H	H	↑	Normal Read operation.
L	H	L	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
L	L	H	↑	Read address pointer is stopped. Output data is held.
L	L	L	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

9.7 One Field Delay Line (The Old Data Read)

As the design shown in the diagram, by applying the reset every 1-field cycle (with the common signal for WRST and RRST) and a constant read/write operation (with all WEN, REN, IE and OE tied to active status), “1 field delay line” timing is shown in the timing chart below. When the difference between the write address and the read address is 0 (the read address and the write address are the same), the old field data are read as shown in the timing chart.



AL462 1 Field Delay Line Diagram



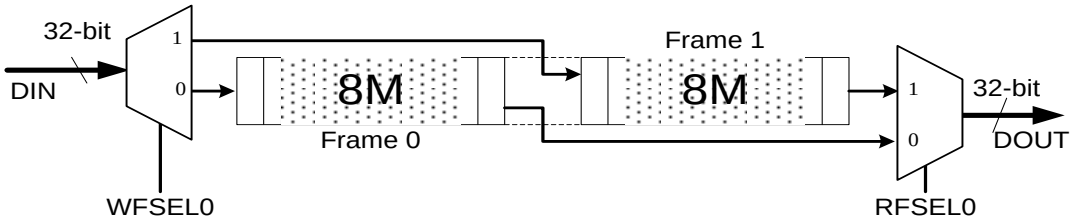
AL462 1 Field Delay Line Timing Diagram

9.8 Two Frame Mode

Two Frame buffering mechanism enables AL462 to store two complete frames simultaneously. This advantage makes it possible to process two separated frames in parallel for enhancing performance. In standard FIFO mode, the whole memory space is utilized as single block for sequential data R/W. Once Two Frame Mode is enabled (TFEN = VDD), AL462 can be configured into two memory blocks. Then the user can use these two separated blocks independently. While data in one frame is being read, the other can be written with a new set of data. The desired Read/Write frame is selected via R/W frame select pins WFSEL & RFSEL. The R/W frame selection and control manipulation are illustrated in the following diagrams.

32-bit Bus Mode 16EN = GROUND (GND)

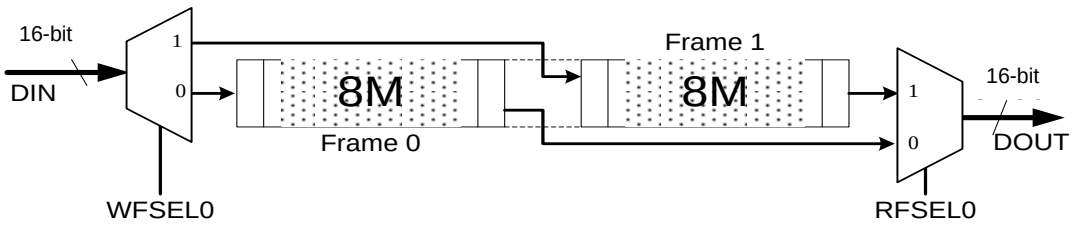
Standard FIFO Mode



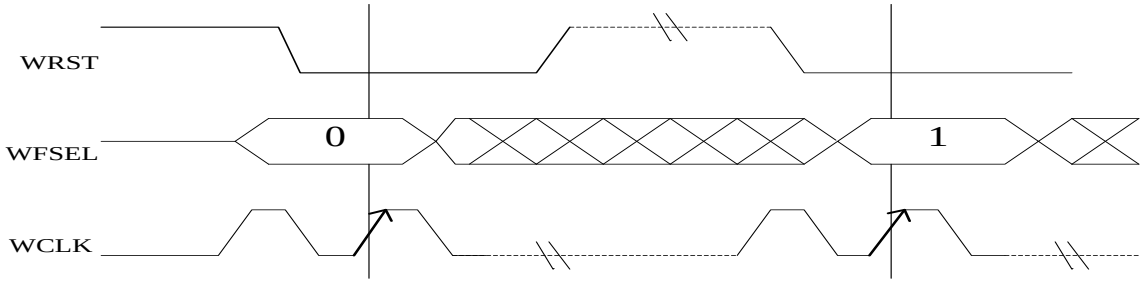
Two Frame Mode

16-bit Bus Mode 16EN = VDD33

Standard FIFO Mode

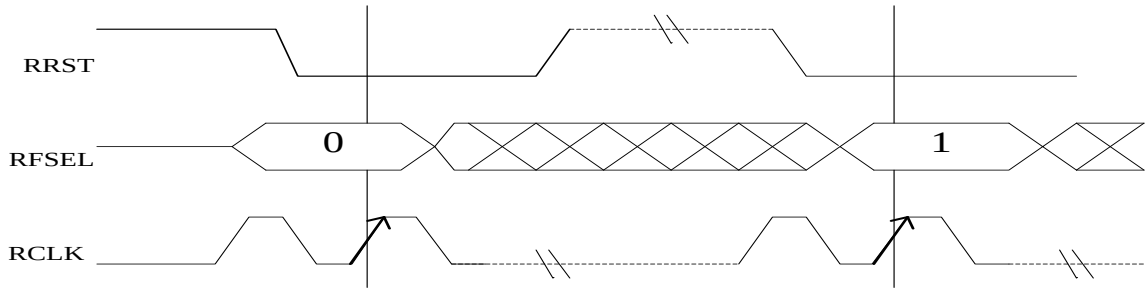


Two Frame Mode



/PLRTY=VDD, TFEN = VDD

Write Frame Select (WFSEL) Timing Diagram

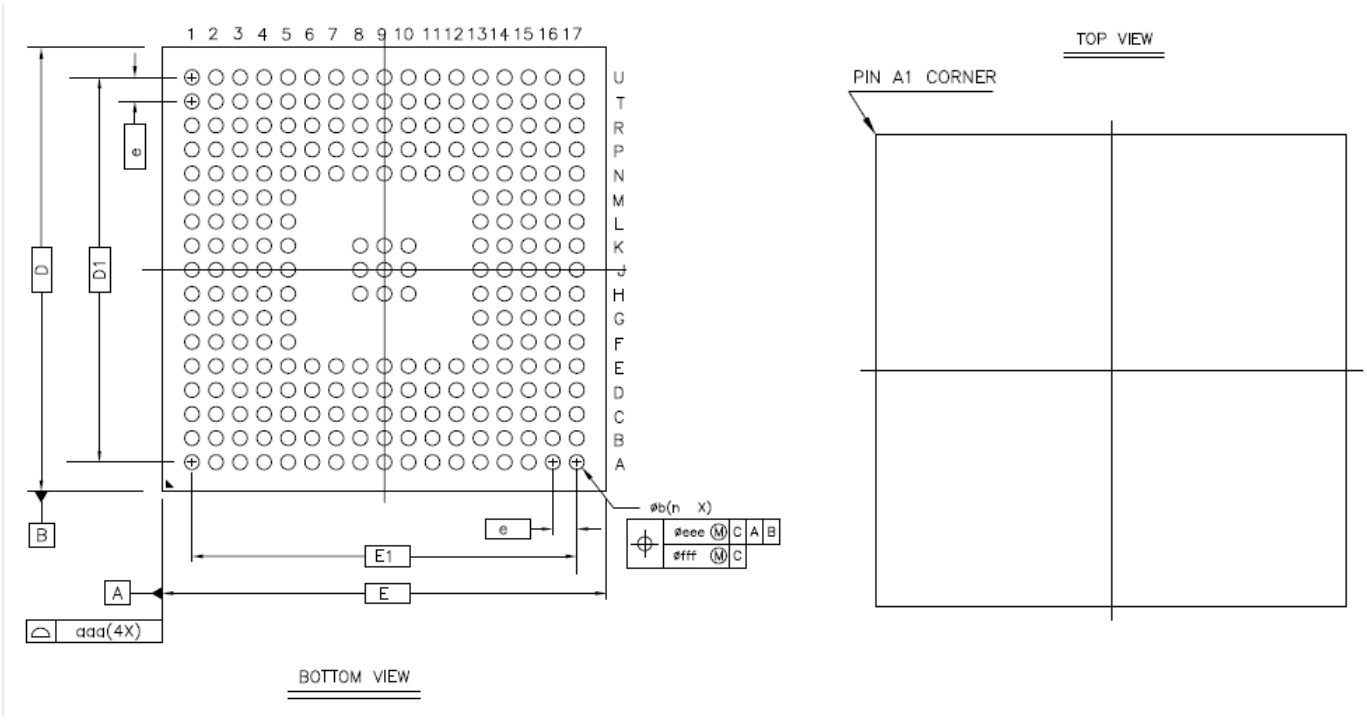


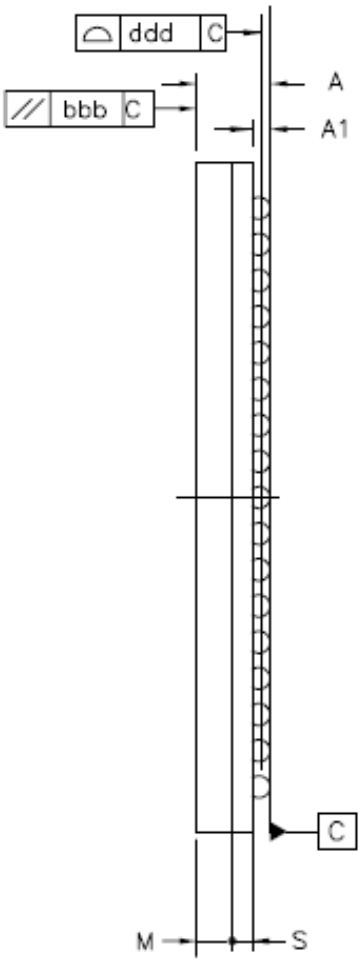
/PLRTY=VDD, TFEN = VDD

Read Frame Select (RFSEL) Timing Diagram

10 MECHNANICAL DRAWING

10.1 249-Ball LFBGA Package





		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			STK LFBGA		
Body Size:	X	E	12.000		
	Y	D	12.000		
Ball Pitch :		e	0.650		
Total Thickness :		A			1.400
Mold Thickness :		M	0.650	Ref.	
Substrate Thickness :		S	0.360	Ref.	
Ball Diameter :			0.400		
Stand Off :		A1	0.270	–	0.370
Ball Width :		b	0.370	–	0.470
Package Edge Tolerance :		aaa	0.150		
Mold Parallelism :		bbb	0.200		
Coplanarity:		ddd	0.120		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	249		
Edge Ball Center to Center :	X	E1	10.400		
	Y	D1	10.400		

ASE ADVANCED SEMICONDUCTOR ENGINEERING, INC.			SCALE		PROJ.	
TITLE			DWG. NO.			REV.
PACKAGE OUTLINE			AAB0XXXX			0
249L STK LFBGA 12 x 12 x1.400			SHEET			SIZE
			1 OF 2			A4
UNIT	TOLERANCE		REFERENCE DOCUMENT			
	DIMENSION	ANGLE				
MM						

11 DESIGN NOTES

11.1 General PCB Design Guideline

The AL462 is available in 249-Ball LFBGA.

Grounding

Analog and digital circuits are separated within the AL462 chip. To minimize system noise and prevent digital system noise from entering the analog portion, a common ground plane for all devices, including the AL462, is recommended. All the connections to the ground plan should have a very short lead. The ground plane should be solid, not cross-hatched.

Power Planes

The analog portion of the AL462 and any associated analog circuitry should have their own power plane, referred to as the analog power plane (AVDD18_PLL1/PLL2/PLL3). The analog power plane should be connected to the digital power plane (VDD18, DVC18 and DVQ18) at a single point through a low resistance ferrite bead.

The digital power plane should provide power to all digital logic on the PCB board, and the analog power plane should provide power to all of the AL462 analog power pins and relevant analog circuitry.

The digital power plane should not be placed under the AL462 chip, the voltage reference or other analog circuitry. Capacitive coupling of digital power supply noise from this layer to the AL462 and its related analog circuitry can degrade signal integrity.

Power Supply Decoupling

Power supply connection pins should be individually decoupled. The decoupling capacitors should be placed as close as possible to the AL462. The ground connection of the capacitor should go straight to the ground plane through a via placed immediately adjacent to the pad. Ideally, the ground connection should be through 2 vias, one placed on either side of the pad. For the best results, use 0.1µF ceramic chip capacitors. Lead lengths should be minimized. The power pins should be connected to the bypass capacitors before being connected to the power planes. 22µF capacitors should also be used between the AL462 power planes and the ground planes to control low-frequency power ripple.

Digital Signal and Clock Interconnect

Digital signals to the AL462 should be isolated as much as possible from other analog circuitry. These signals should not overlap the analog power plane. If this is not possible, coupling can be minimized by routing the digital signal at a 90 degree angle across the analog signals. The 32-bit digital input bus, DI, should have the same trace length; it also applies to DO, the output digital bus. The high frequency clock reference or crystal should be handled carefully. Jitter and noise on the clock will degrade the data integrity. Keep the clock paths to the AL462 as short as possible to reduce the amount of noise picked up.

CONTACT INFORMATION

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