16-CHANNEL, 16-BIT PWM DIMMING LED DRIVER

Description

The AL58263 is a 16-channel constant-current LED driver with 16-bit grayscale Adaptive Pulse Density Modulation (APDM) and supports error diagnostics, power-saving functionality, and current gain control. This distinctive APDM technology abates the non-ideal IOUT distortion due to non-symmetric transient responses and enhances the refresh rate by efficiently separating the frame waveform.

The device operates over a 3V to 5.5V input voltage range, 15V output channel voltage, fast 25MHz DCK input, and delivers up to 55mA of high-accuracy current to each LED string. Each channel's output current can be programmable through a digital interface individually. All channels' output current can be set by one external sensing resistor, along with a 6-bit global current control register.

The AL58263 has built-in diagnostics and LED open/short protection, including error detection. These error results are stored in a register for the MCU to read out.

The AL58263 is available in the TSSOP-24EP (Type A1-B) and wettable flank W-QFN4040-24/SWP (Type A1) packages. The device is specified over the -40°C to +105°C ambient temperature range.

Features

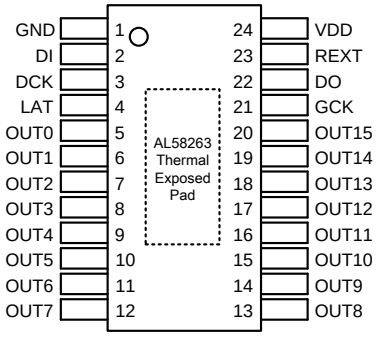
- Input Voltage VDD: 3V to 5.5V
- Output Current Range
  - 2~55mA/5V, 2~35mA/3.3V
  - ±0.1% Output current regulation capability
  - 6-bit global current control: from 12.5% to 200%
- 16 Constant-Current Sink Output Channel
  - 16-bit grayscale resolution with Adaptive Pulse Density Modulation control
  - 15V rated output channels for long LED strings
  - Fast Transient Response – supports external grayscale clock with double edge up to 16MHz
  - ±1.5% (typ.) LED Current accuracy between channels
  - ±3% (typ.) LED Current accuracy between chips
  - Non-scramble waveform for high power LED application
  - Grayscale counter reset selection
  - Grayscale data synchronization selection
- Diagnosis and Protections
  - Error detection includes LED Open, LED Short, Output port leakage, Output short-to-GND, Output short-to-Power and REXT short-to-GND
  - Error detection LEDs on at 0.1mA to avoid any flickering
  - Short detection threshold voltage selection (2/3/4/4.5V)
  - Sleep and 0-data mode to lower down the supply current
  - Pre-overtemperature warning
- 4-Wire Serial Interface (LAT, DI, DO, DCK)
  - 25MHz clock frequency for data transfer
  - EMI reduction grayscale clock
  - Cascaded capability (Max 1,440 devices)
  - External GCK watchdog
  - Stagger outputs delay for EMI reduction
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under a separate datasheet (AL58263Q).**

Pin Assignments

(3D Photo – Not to Scale)

(3D Step file available upon request)

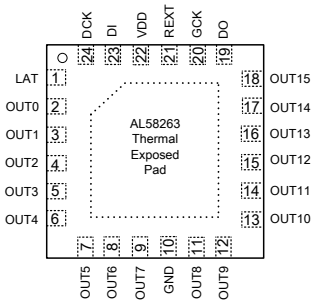
(Top View – Not to Scale)



TSSOP-24EP (Type A1-B)

(3D Step file available upon request)

(Top View – Not to Scale)



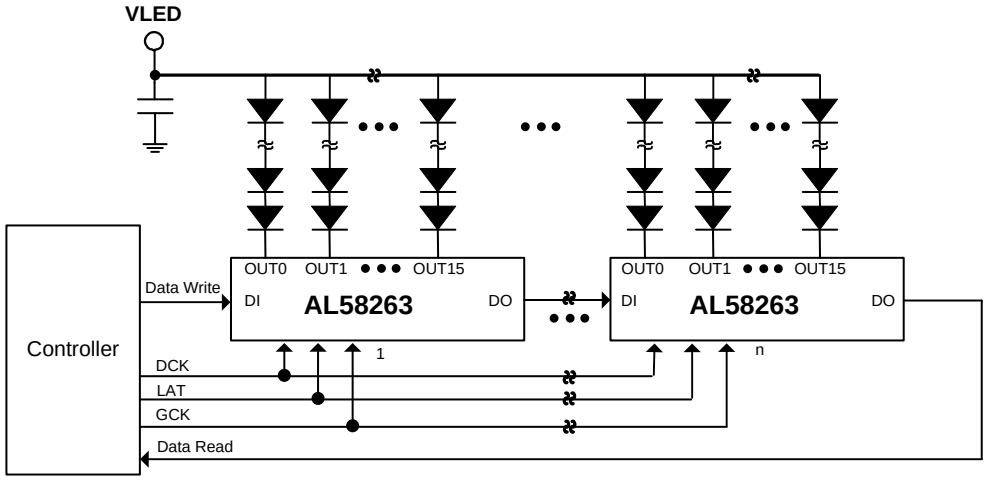
W-QFN4040-24/SWP (Type A1)

Applications

- Indoor and outdoor LED video displays
- Variable message signs (VMS)
- Traffic signs
- Outdoor billboard signage
- LCD display backlighting

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

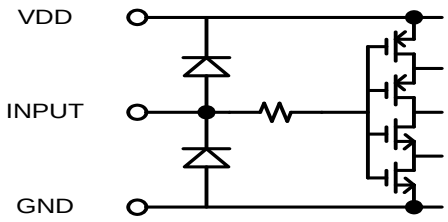


Pin Descriptions

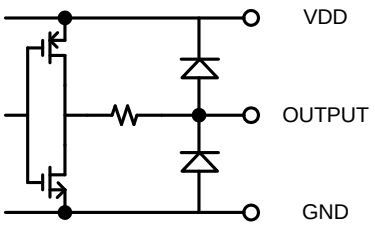
NAME	PIN TSSOP-24EP (Type A1-B)	PIN W-QFN4040-24/SWP (Type A1)	DESCRIPTION
GND	1	10	Ground terminal
DI	2	23	Serial data input terminal.
DCK	3	24	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
LAT	4	1	Input terminal of data strobe and mode setting. Combine DCK with LAT signal to execute the mode control
OUT0 to OUT15	5 to 20	2 to 9, 11 to 18	Sink constant-current outputs (open-drain).
GCK	21	20	External double-edge grayscale clock input for APDM operations
DO	22	19	Serial data output terminal.
REXT	23	21	External resistors connected between REXT and GND for output current value setting.
VDD	24	22	Supply voltage terminal.

Equivalent Circuit of Inputs and Outputs

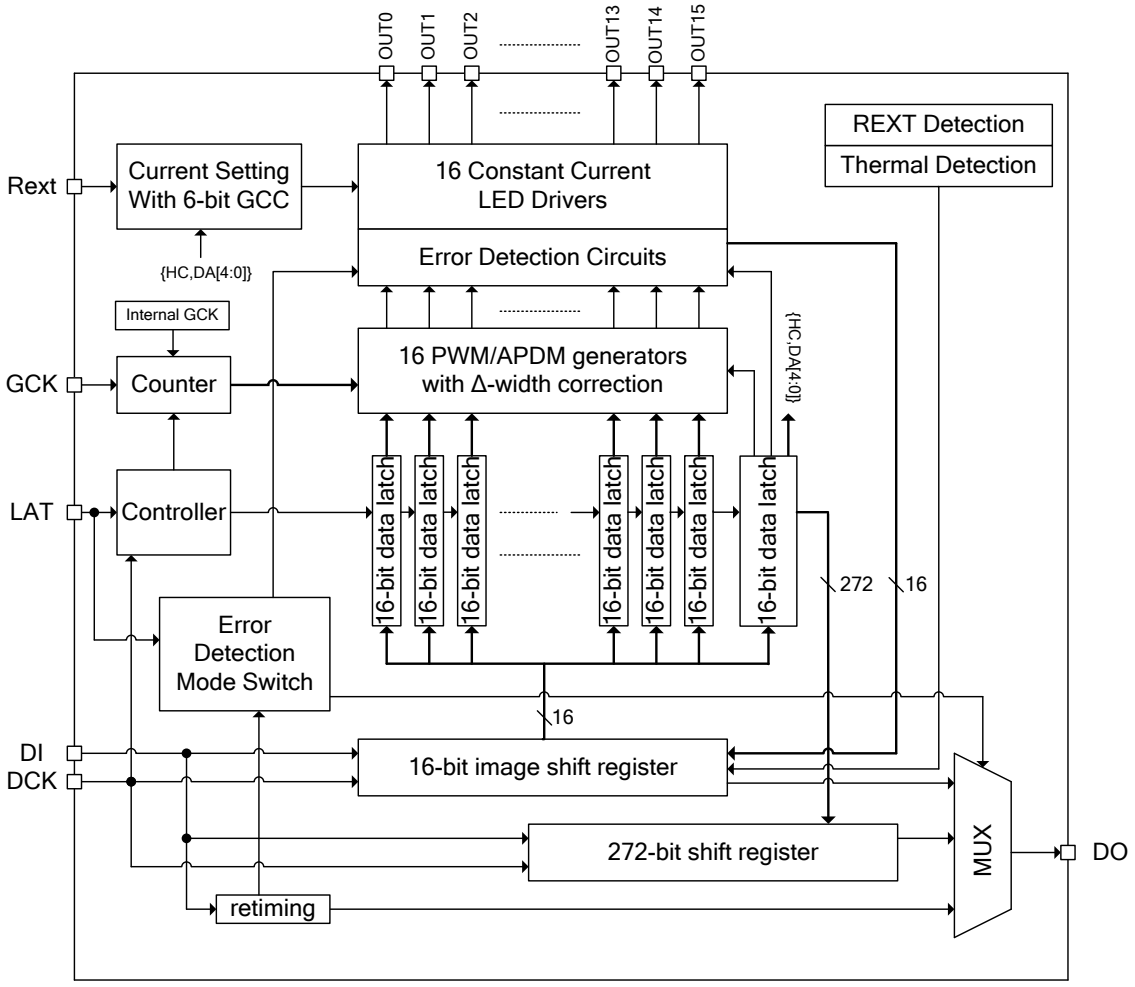
1. DCK, DI, LAT, GCK terminals



2. DO terminal



Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameters	Ratings	Unit
VDD	Supply Voltage	-0.3 ~ 7.0	V
V_{DI}, V_{DCK}, V_{GCK}, V_{LAT}	Input Voltage	-0.3 ~ VDD+0.3	V
IOUT	Output Current	60	mA
VOUT	Output Voltage	-0.3 ~ 16	V
FDCK	Input Clock Frequency	25	MHz
FGCK	Input Grayscale Frequency	16	MHz
IGND	GND Terminal Current	960	mA

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.
(3) Operation at Tj(max) = 150°C may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

ESD Ratings

Symbol	Parameter	Value	Unit
V_{ESD}	Human-Body Model (HBM)	2000	V
	Charged-Device Model (CDM)	750	V

Package Thermal Data (Note 4)

Symbol	Thermal Resistance	Device		Unit
		TSSOP-24EP (Type A1-B)	W-QFN4040-24/SWP (Type A1)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	25.57	31.16	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	14.47	17.25	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	9.57	9.34	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.33	0.41	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.39	9.14	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.21	3.33	°C/W

Note: 4. Test condition: Device mounted on FR-4 PCB (51mm x 51mm 2oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer with maximum area ground plane. For better thermal performance, larger copper pad for heat-sink is needed.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating Supply Voltage	3.0	3.3	5.5	V
I_{OUT}	Output Current (Note 5)	2	—	55	mA
V_{OUT}	Output Voltage	1	—	15	V
T_A	Ambient Temperature (Note 5)	-40	—	+105	°C
T_J	Junction Temperature	-40	—	+125	°C
Tstg	Storage Temperature	-55	—	+150	°C

Note: 5. Dependent on ambient temperature, LED voltage, package thermal limitation, and PCB layout.

Electrical Characteristics (VDD=5.0V @T_A = +25°C, unless otherwise specified.)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 15 V	—	—	0.1	uA
Driving Current (DO)	IOL	VOL = 0.4V	1	3.4	5	mA
	IOH	VOH= VDD-0.4	-5	-3.4	-1	
Output Current Skew (Channel-to-Channel) (Note 6)	dIOUT1	VOUT = 1.0 V Rrext = 560 Ω GCC=101011	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) (Note 7)	dIOUT2		—	±3	±6	%
Output Current Skew (Channel-to-Channel) (Note 6)	dIOUT3	VOUT = 1.0 V Rrext = 7 KΩ GCC=101011	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) (Note 7)	dIOUT4		—	±3	±6	%
Output Voltage Regulation (Note 8)	% / VOUT	Rrext = 560 Ω VOUT = 1 V ~ 3 V	—	±.0.1	±.1	% / V
Supply Voltage Regulation (Note 9)	% / VDD	Rrext = 560 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current (Note 10)	$I_{DD1(off)}$	Rrext = 7 KΩ all outputs turn off	1	2.5	4	mA
	$I_{DD2(on)}$	Rrext = 7 KΩ all outputs turn on	1	2.5	4	
	$I_{DD3(off)}$	Rrext = 560 Ω all outputs turn off	1	5.5	7.5	
	$I_{DD4(on)}$	Rrext = 560 Ω all outputs turn on	1	5.5	7.5	
Thermal alarm temperature	T_{AL}	—	—	+155	—	°C
Thermal alarm temperature hysteresis	T_{AL_HYS}	—	—	+15	—	°C

Notes: 6. Channel-to-channel skew is defined by the formula below:

$$\Delta(\%)=\left[\ \frac{Iout_n}{\frac{(Iout_0+Iout_1+...+Iout_{15})}{16}}-1\ \right]*100\%$$

7. Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%)=\left[\ \left(\frac{\frac{(Iout_0+Iout_1+...+Iout_{15})}{16}-(Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)}\right)\ \right]*100\%$$

8. Output voltage regulation is defined by the formula below:

$$\Delta(\%/V)=\left[\ \frac{Iout_n(@Vout_n=3V)-Iout_n(@Vout_n=1V)}{Iout_n(@Vout_n=3V)}\ \right]*\frac{100\%}{3V-1V}$$

9. Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V)=\left[\ \frac{Iout_n(@V_{DD}=5.5V)-Iout_n(@V_{DD}=3V)}{Iout_n(@Vcc=3V)}\ \right]*\frac{100\%}{5.5V-3V}$$

10. IO excluded.

Electrical Characteristics (VDD=3.3V @T_A = +25°C, unless otherwise specified.)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 15 V	—	—	0.1	uA
Driving Current (DO)	IOL	VOL = 0.4V	1	2.5	5	mA
	IOH	VOH= VDD-0.4	-5	-2.5	-1	
Output Current Skew (Channel-to-Channel) (Note 11)	dIOUT1	VOUT = 1.0 V Rrext = 560 Ω GCC=101011	—	±1.5	±3	%
Output Current Skew (Chip-to-Chip) (Note 12)	dIOUT2		—	±3	±6	%
Output Current Skew (Channel-to-Channel) (Note 11)	dIOUT3	VOUT = 1.0 V Rrext = 7 KΩ GCC=101011	—	±1.5	±3	%
Output Current Skew (Channel-to-Channel) (Note 12)	dIOUT4		—	±3	±6	%
Output Voltage Regulation (Note 13)	% / VOUT	Rrext = 560 Ω VOUT = 1 V ~ 3 V	—	±.0.1	±1	% / V
Supply Voltage Regulation (Note 14)	% / VDD	Rrext = 560 Ω VDD = 3 V ~ 5.5 V	—	±0.7	±1	
Supply Current (Note 15)	$I_{DD1(off)}$	Rrext = 7 KΩ all outputs turn off	1	2.3	4	mA
	$I_{DD2(on)}$	Rrext = 7 KΩ all outputs turn on	1	2.3	4	
	$I_{DD3(off)}$	Rrext = 560 Ω all outputs turn off	1	4.7	7.5	
	$I_{DD4(on)}$	Rrext = 560 Ω all outputs turn on	1	4.7	7.5	
Thermal alarm temperature	T_{AL}	—	—	+155	—	°C
Thermal alarm temperature hysteresis	T_{AL_HYS}	—	—	+15	—	°C

Notes: 11. Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16}} - 1 \right] * 100\%$$

12. Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

13. Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

14. Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

15. IO excluded.

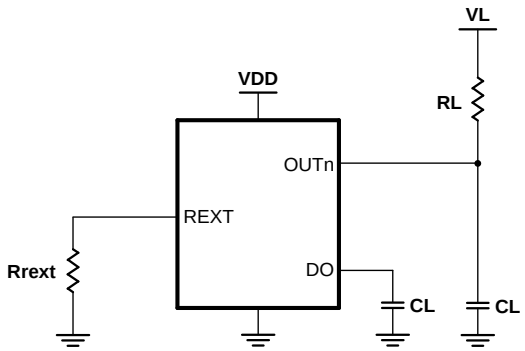
Switching Characteristics (VDD = 5.0V @T_A = +25°C, unless otherwise specified.) (Guarantee by design)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L to ‘H’)	DCK-DO	tpLH3	VIH = VDD VIL = GND Rrext = 560 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	30	35	ns
Propagation Delay (‘H’ to ‘L’)	DCK-DO	tpHL3		—	30	35	
Pulse Duration	LAT	$tw_{(LAT)}$		50	—	—	
	GCK	$tw_{(GCK)}$		20	—	—	
	DCK	$tw_{(DCK)}$		20	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		20	—	—	
	DI	$tsu_{(D)}$		5	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		5	—	—	
Hold Time of Instruction		$th_{(CM)}$		20	—	—	
LED Error Detection Time		Terr1		100	—	—	
Short-to-ground Detection Time		Terr3		160	—	—	
Interval between two command pulses		tpls		230	250	—	
Wake-up time from sleep or 0-data mode		Twake		—	—	4000	us
Data Clock Frequency		F_{DCK}		—	—	25	MHz
Grayscale Clock Frequency (double-edge)		F_{GCK}		—	—	16	

Switching Characteristics (VDD = 3.3V @T_A = +25°C, unless otherwise specified.) (Guarantee by design)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L to ‘H’)	DCK-DO	tpLH3	VIH = VDD VIL = GND Rrext = 560 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	45	55	ns
Propagation Delay (‘H’ to ‘L’)	DCK-DO	tpHL3		—	45	55	
Pulse Duration	LAT	$tw_{(LAT)}$		50	—	—	
	GCK	$tw_{(GCK)}$		20	—	—	
	DCK	$tw_{(DCK)}$		20	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		20	—	—	
	DI	$tsu_{(D)}$		5	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		5	—	—	
Hold Time of Instruction		$th_{(CM)}$		20	—	—	
LED Error Detection Time		Terr1		100	—	—	
Short-to-ground Detection Time		Terr3		180	—	—	
Interval between two command pulses		tpls		230	250	—	
Wake-up time from sleep or 0-data mode		Twake		—	—	4000	us
Data Clock Frequency		F_{DCK}		—	—	15	MHz
Grayscale Clock Frequency (double-edge)		F_{GCK}		—	—	16	

Switching Characteristics Test Circuit

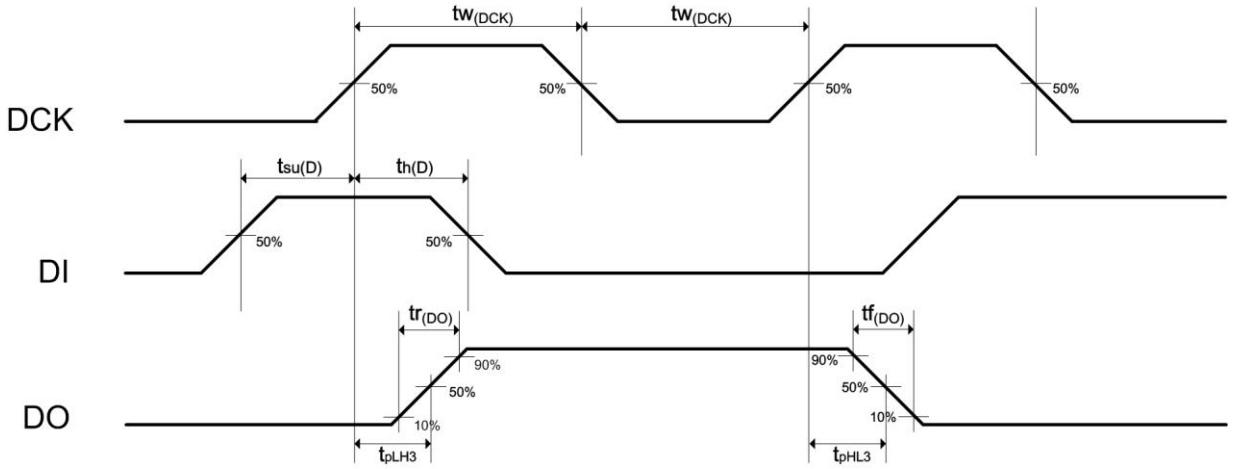


Switching Characteristics Test Circuit

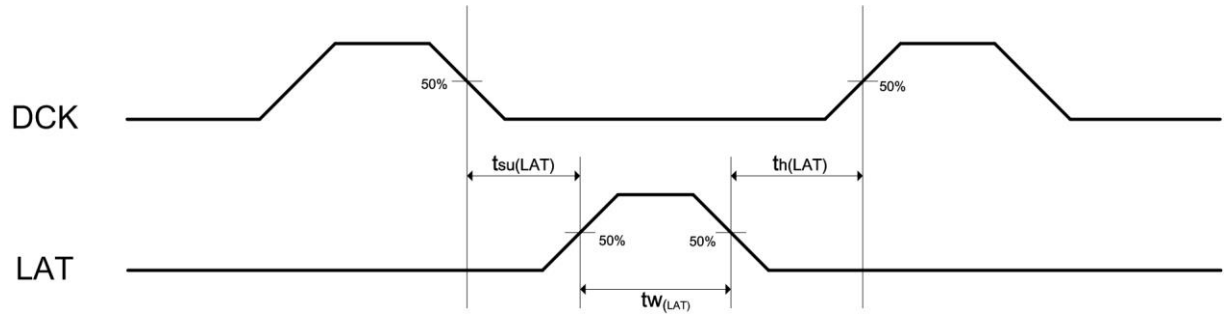
Timing Characteristics (@T_A = +25°C, unless otherwise specified.)

Timing Diagram

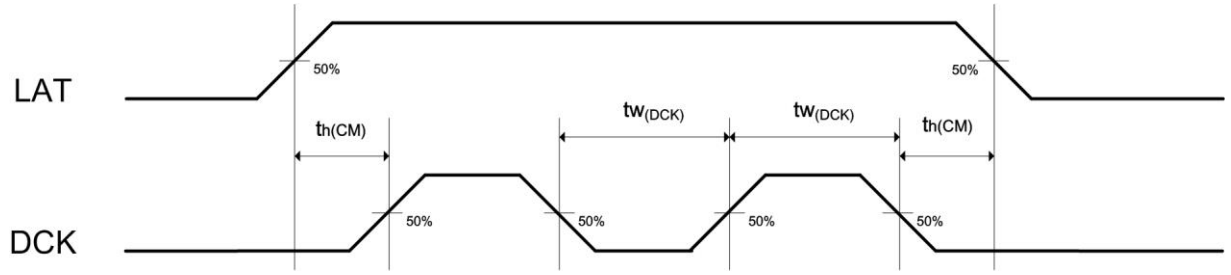
1. DCKI-DI, DO



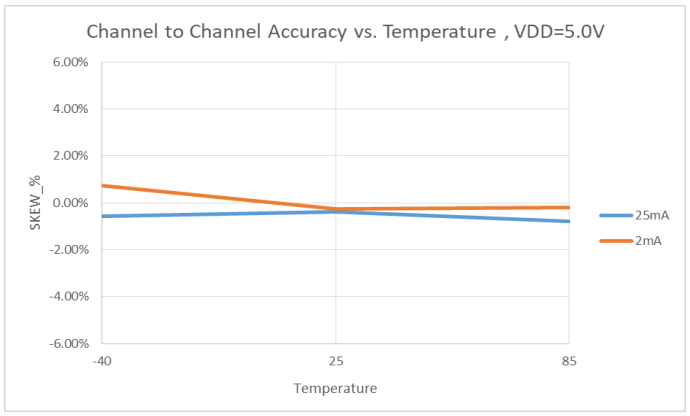
2. GCK-LAT



3. LAT-DCK (Instruction)

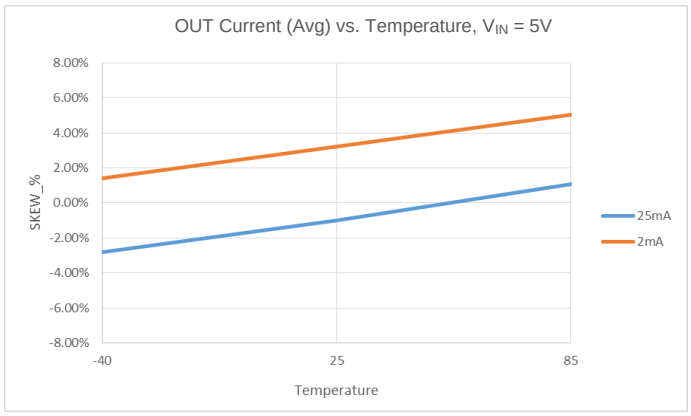


Typical Performance Characteristics (V_{DD} = 5V, -40°C < T_A < +85°C, unless otherwise specified.)



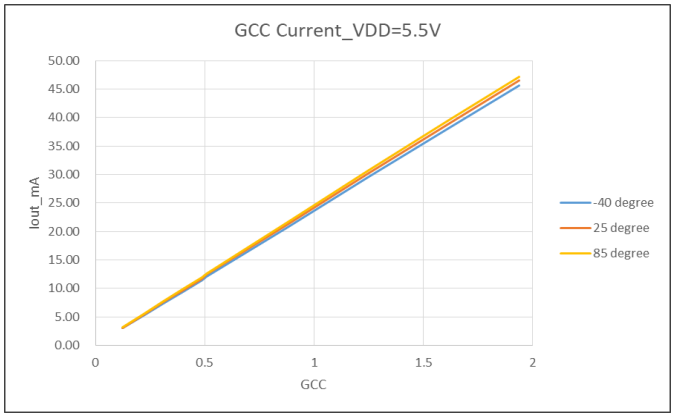
V_{DD} = 5V, I_{OUT} = 25mA, 2mA

Figure 1. Channel to Channel Accuracy vs. Temperature



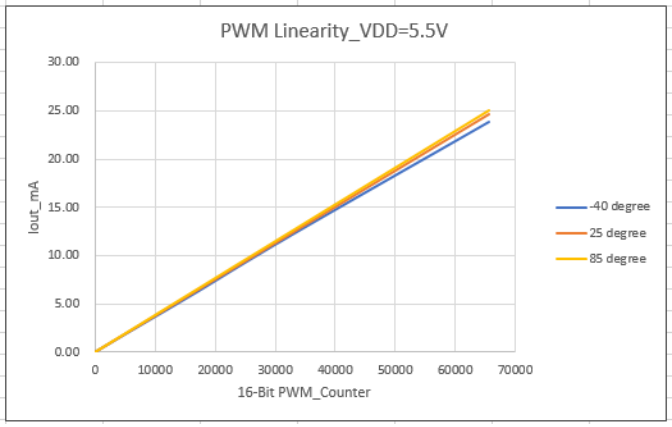
V_{DD} = 5V, I_{OUT} = 25mA, 2mA

Figure 2. Chip to Chip Accuracy vs. Temperature



V_{DD} = 5V, I_{OUT} = 25mA

Figure 3. Gain Control Current vs. Temperature



V_{DD} = 5V, I_{OUT} = 25mA

Figure 4. PWM Linearity vs. Temperature

Functional Descriptions

Fast Transient Response

The AL58263 supports fast transient response times, making high image resolutions possible. The GCK period of 50ns is enough for a complete Vout waveform.

Stagger Outputs Delay

Large in-rush currents will be induced when the system activates all outputs at once. To reduce EMI interference, the AL58263 is designed to have a constant length of delay time (around 16ns) between two output groups. The first group is OUT2n and the second group is OUT2n+1 (n=0~7).

Global Current Control (GCC)

The AL58263 provides 6 bits of global current control (GCC), which can adjust output current by 64 steps.
GCC bits are included in the command data as defined below:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	HC	DA4	DA3	DA2	DA1	DA0	—	—	—	—

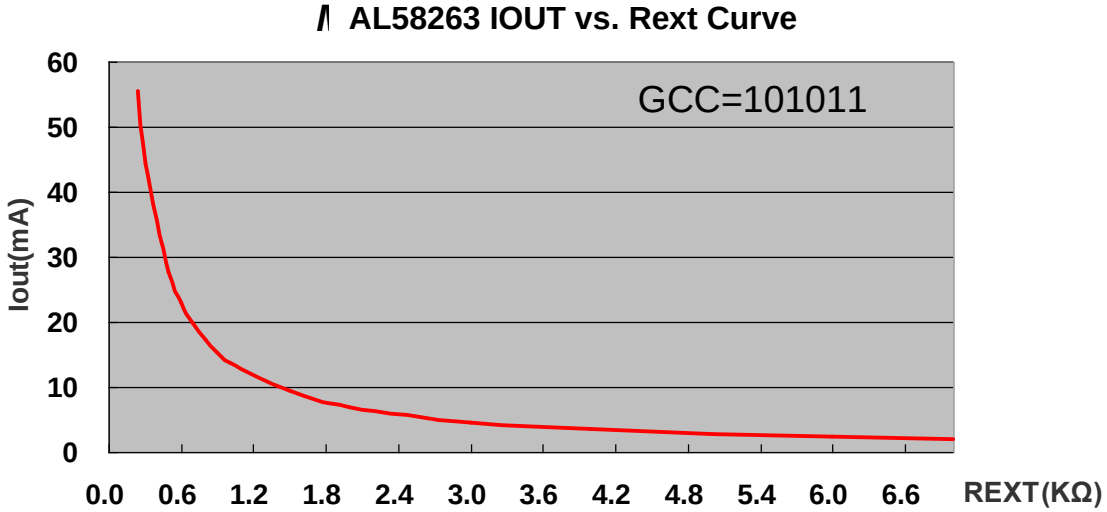
The relationship between the Gain value and GCC bits is described below:
HC=1, Gain ≒ (3 x D + 33) / 65 x (1-0.001 x D), the gain range is from 0.508 to 1.878
HC=0, Gain ≒ (3 x D + 32) / 256 x (1-0.0006 x D), the gain range is from 0.125 to 0.479
Where D = DA4 x 2^4 + DA3 x 2^3 + DA2 x 2^2 + DA1 x 2^1 + DA0 x 2^0
For example, HC=1 and DA[4:0]=11000
D = 1x 2^4 + 1 x 2^3 + 0 x 2^2 + 0 x 2^1 + 0 x 2^0 = 24
Gain ≒ (3 x 24 + 33) / 65 x (1-0.001 x 24) ≒1.577

Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout\ (mA) \fallingdotseq 13.45 / Rext(K\Omega) \times Gain$$

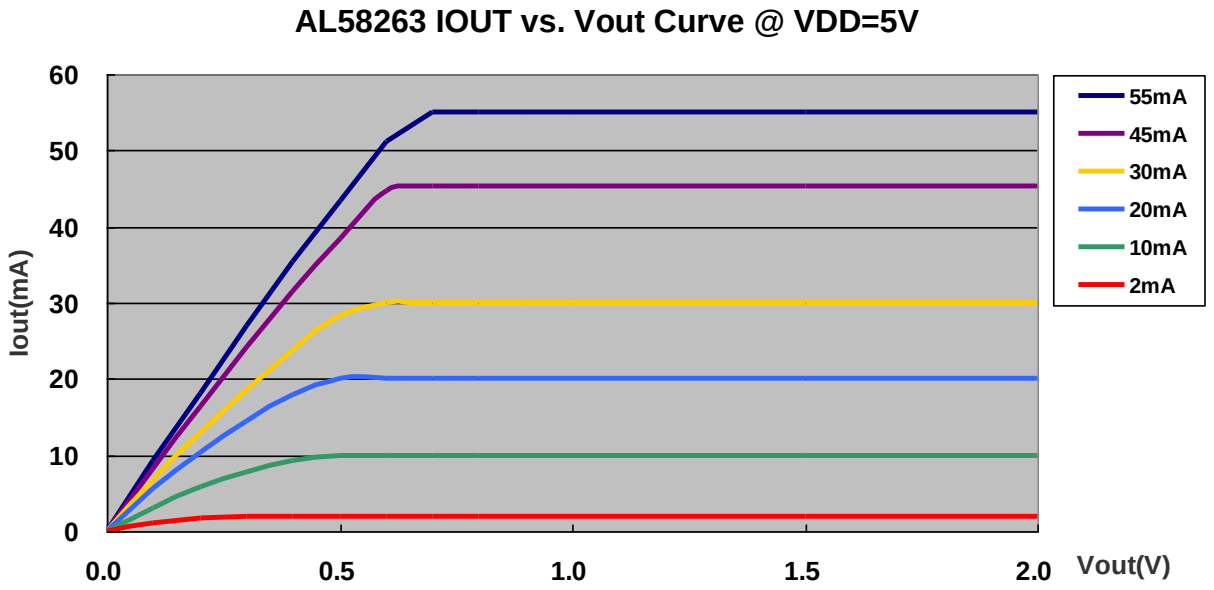
Where Rext is a resistor placed between REXT and GND.
This 13.45 constant center at 10mA may need to be adjusted slightly based on user application and test conditions.
For example, Iout is around 24.12mA when Rrext=560Ω and with GCC=101011.

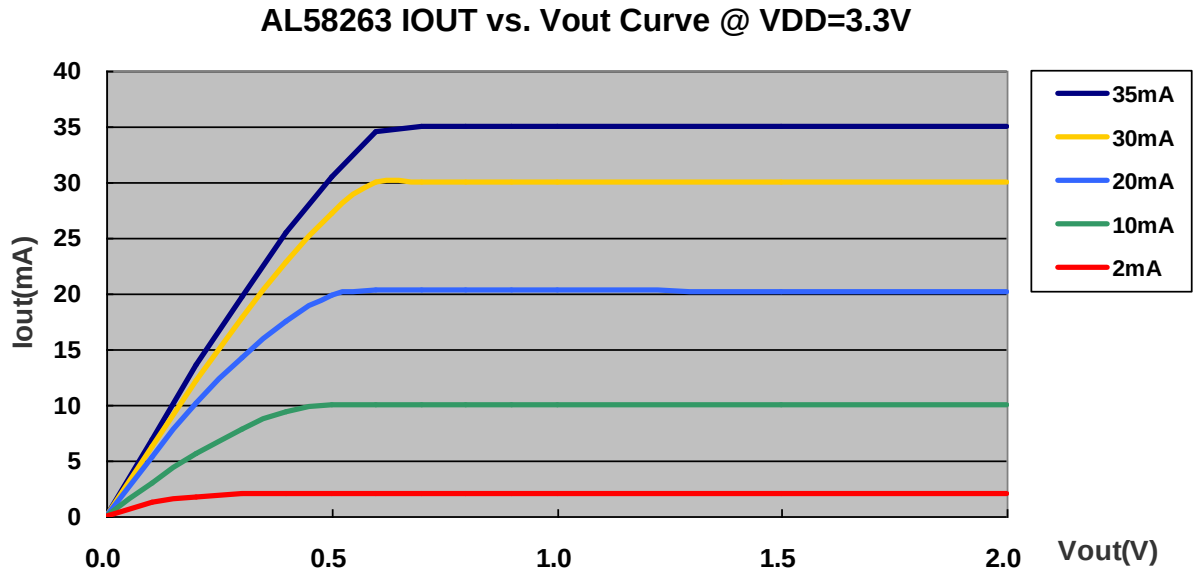


Functional Descriptions (continued)

Constant-Current Output

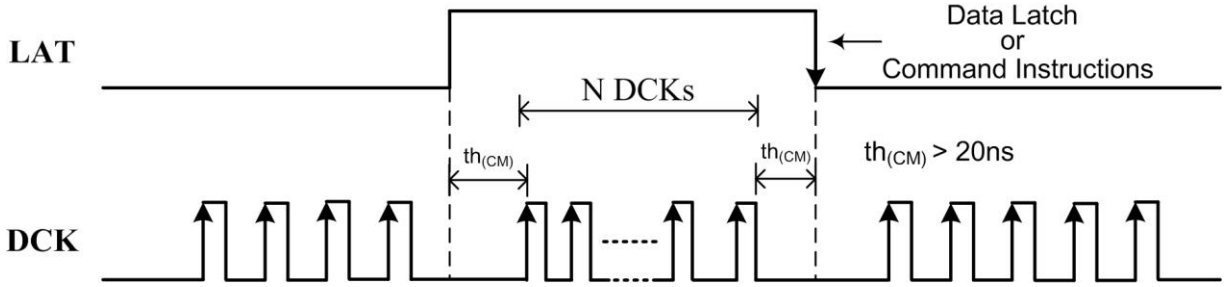
The current characteristics are maintained invariably in the influence of loading voltage. Therefore, the AL58263 can minimize the interference of different LED forward voltages and produce constant current. The following figures illustrate the suitable output voltage that should be determined to keep excellent performance.





Functional Descriptions (continued)

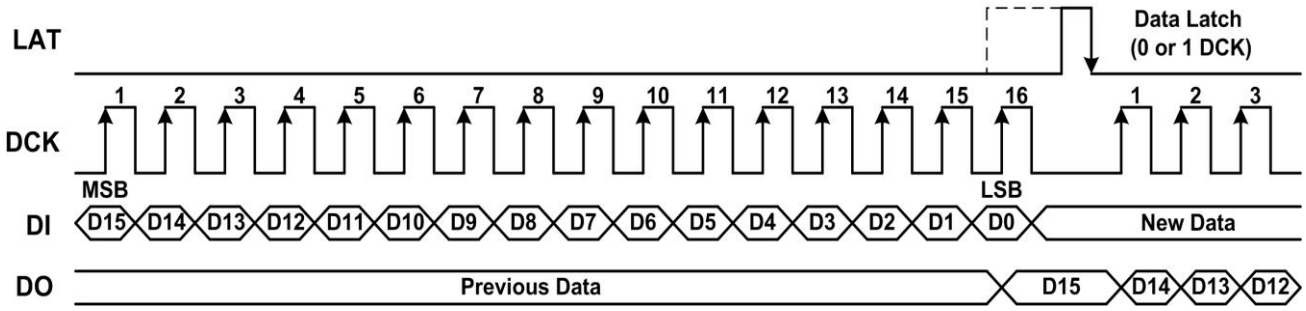
Control Instructions



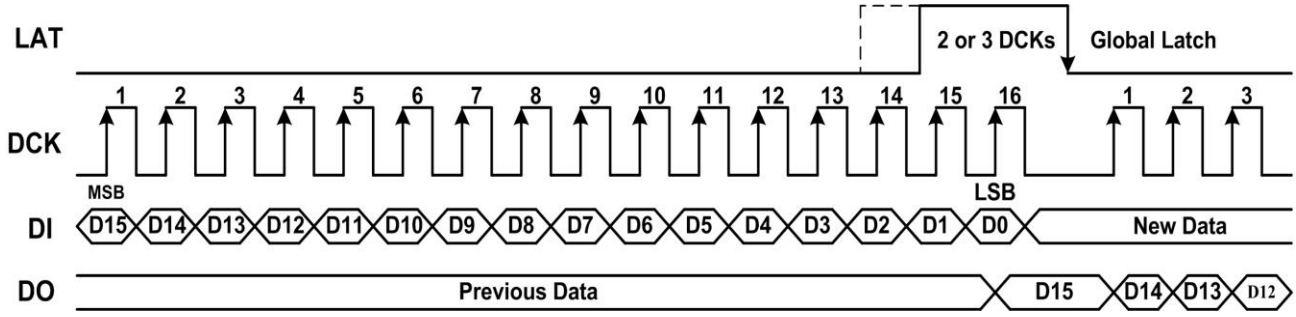
Instruction Name	Number of DCK Pulses when LAT is at High	Function Description
Data Latch	0 or 1	Strobes image data into temporary registers. In this time, constant current outputs are not updated to a new frame data.
Global Latch	2 or 3	Strobes image data from temporary registers into an APDM/PWM generator. In this time, constant current outputs are updated to a new frame data.
Reading Image Data and Command Data	6 or 7	Read out image data and command data from the latch cell to the 272-bit shift registers. And the read data could shift out from DO pin by serial DCK pulses.
Return to Normal Mode	8 or 9	Switch Back from the reading data mode to the normal operating mode.
Writing Command	10 or 11	Strobes command data from the 16-bits shift register into the command latch cell.
Reset APDM/PWM Counter	12 or 13	This instruction will reset APDM/PWM counter to synchronize a new frame if CMD[11]=”H”.

Functional Descriptions (continued)

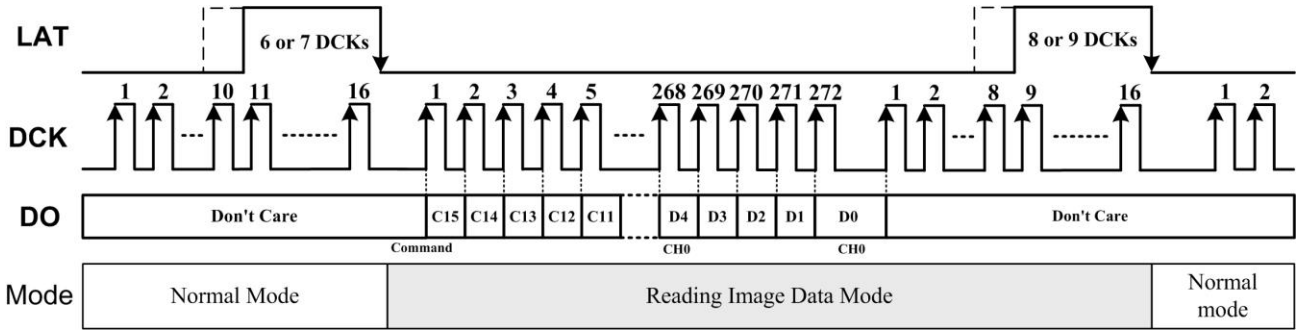
Data Latch



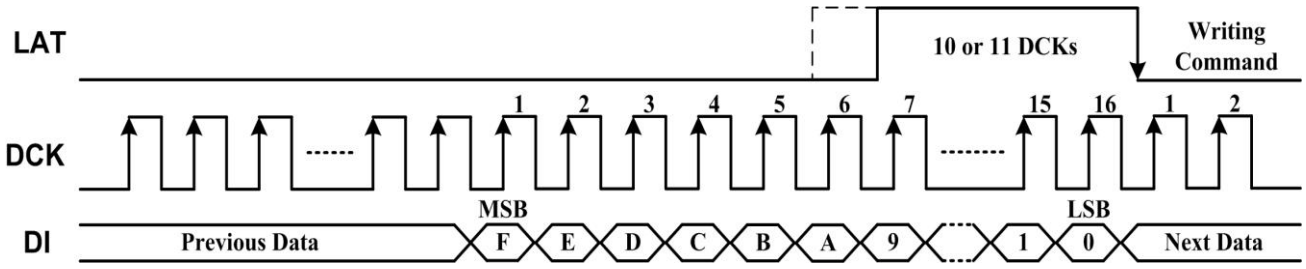
Global Latch



Reading Image Data and Command Data

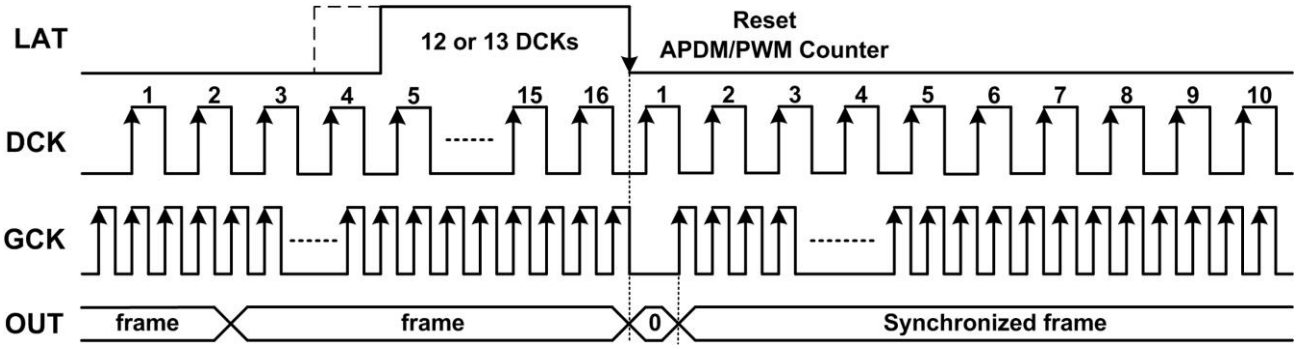


Writing Command

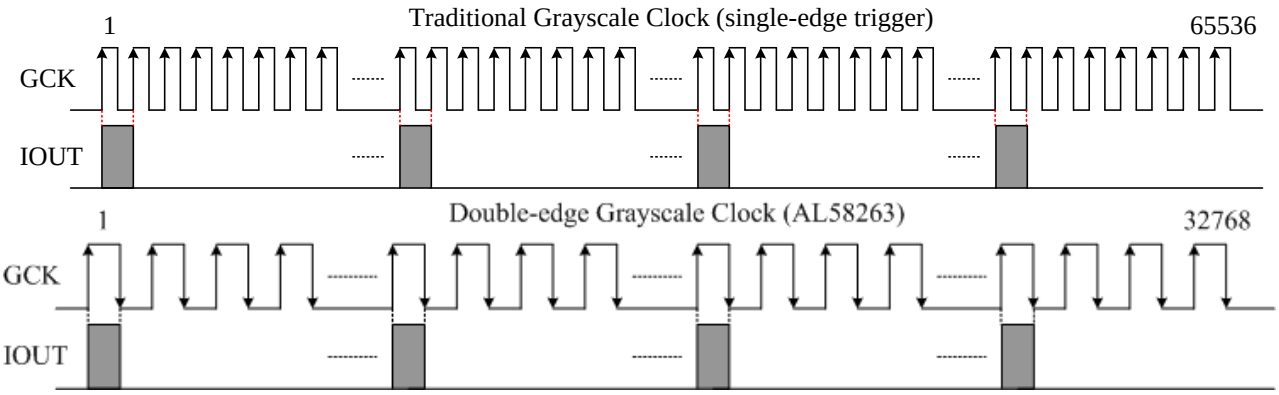


Functional Descriptions (continued)

Reset APDM/PWM Counter (set CMD[11]="1")



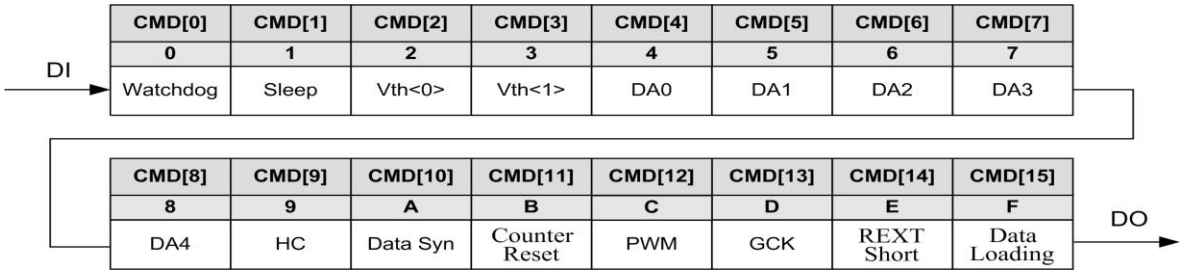
EMI Reduction Grayscale Clock (Double-edge Grayscale Clock)



A whole period of 16 bits of resolution must be composed by 65536 traditional grayscale clocks, as constant current outputs are only triggered at the rising edge of clocks. Therefore, a controller must transmit fast grayscale clocks in order to accomplish a high refresh rate when users adopt traditional PWM chips. The AL58263 supports a specific mode of double-edge grayscale clocks, which triggers both at the rising and falling edges of the clocks. By this approach, a whole period of 16 bits of resolution is composed by only 32768 double-edge grayscale clocks, and the electromagnetic interference decreases substantially due to the slow grayscale clocks.

Functional Descriptions (continued)

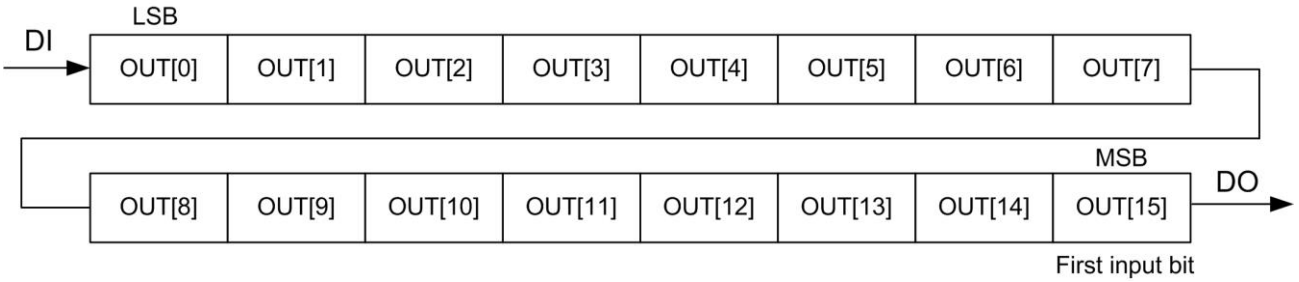
Command Data Format



CMD Bit	Initial Value	Value	Function	Description
CMD[15]	1'b0	1'b0	Mode0	Data transmitting Format: 15 times of data latch + one global latch
		1'b1	Mode1	Data transmitting Format: 16 times of data latch + one global latch
CMD[14]	1'b0	1'b0	Enable	When the voltage of REXT is below 0.15V, all outputs will be forced off.
		1'b1	Disable	Disable
CMD[13]	1'b0	1'b0	External GCK	The GCK signal stems from an external source
		1'b1	Internal GCK	The GCK signal stems from an internal oscillator, 1.5MHz. (When CMD[13]="1",please set CMD[0]="0")
CMD[12]	1'b0	1'b0	APDM mode	Enter the PWM mode to abate the transient loss when AL58263 is as a PWM generator when CMD[12]=1'b0 => APDM mode when CMD[12]=1'b1 => PWM mode
		1'b1	PWM mode	
CMD[11]	1'b0	1'b0	Disable	Disable
		1'b1	Enable	Execute counter reset by inserting 12 or 13 DCKs (rising edge) when LAT keeps at high
CMD[10]	1'b0	1'b0	Auto Synchronization	When the device receives a latch signal, the new frame is updated until the end of old frame
		1'b1	Manual Synchronization	When the device receives a latch signal, the new frame is updated immediately
CMD[9:4]	6'b101011	6'b000000~ 6'b111111	G.C.C	6-bit DA data for global current control (allow 64-step programmable current gain)
CMD[3:2]	2'b00	2'b00 2'b01 2'b10 2'b11	2.0V 3.0V 4.0V 4.5V	Threshold voltage for LED short detection (both at VDD = 5V and 3.3V)
CMD[1]	1'b0	1'b0	Disable	Enter 0-data power saving mode when 16bits PWM data of 16ch are all zeros
		1'b1	Enable	
CMD[0]	1'b0	1'b0	Disable	GCK watchdog All IOUTs will be turned off automatically when GCK keeps high or low level over 30ms. (Result can be read out by "Thermal Detection Mode" or "Rext Detection Mode")
		1'b1	Enable	

Functional Descriptions (continued)

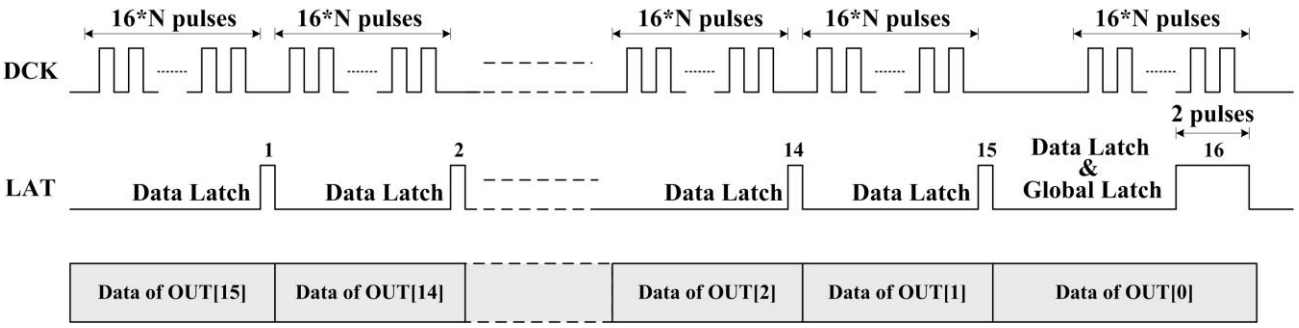
Image Data Format



16 bits of APDM/PWM data are transmitted into the 16-bit shift register, according to the format illustrated above. The first input bit is the most significant bit of each channel.

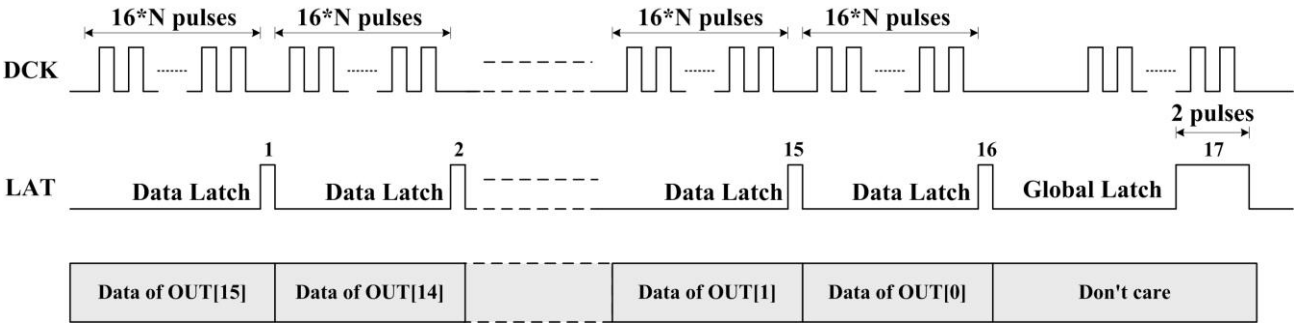
Data Transmitting Protocol

MODE0 (CMD[15]="0")



This data transmitting mode is comprised of 15 data latches and one global latch. The first data latch strobes image data for OUT[15]. The last global latch strobes image data for OUT[0] and loads all the image data of the 16 channels into the APDM/PWM generator. N is the number of devices in series.

MODE1 (CMD[15]="1")

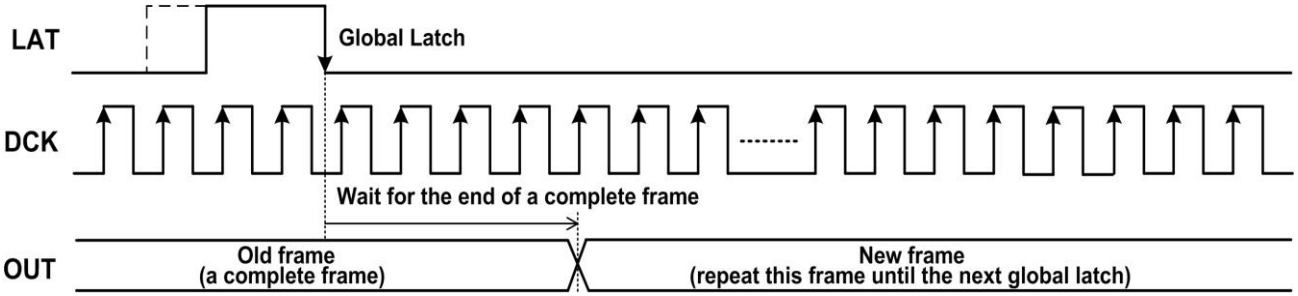


This data transmitting mode is comprised of 16 data latches and one global latch. The first data latch strobes image data for OUT[15]. The last global latch loads all the image data of the 16 channels into the APDM/PWM generator, but does not strobe any image data for output channels. N is the number of devices in series.

Functional Descriptions (continued)

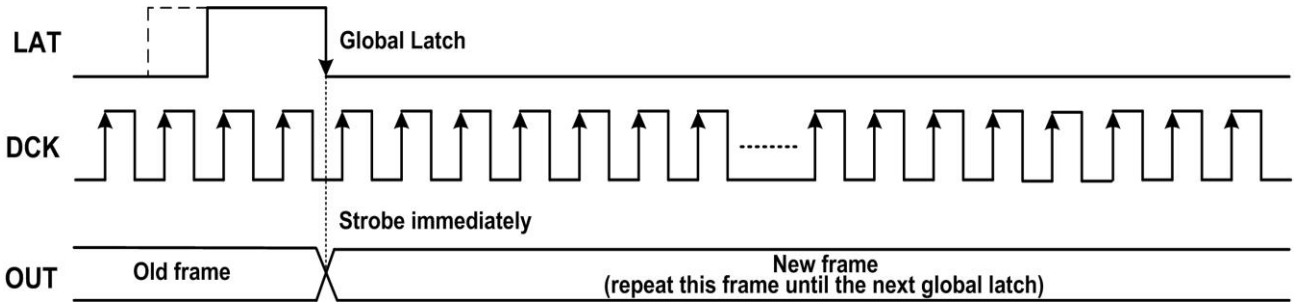
Data Synchronization

Auto Synchronization (CMD[10]="0")



The AL58263 can abate grayscale loss during the frame renewal by using auto synchronization. When the command bit CMD[10] is set to "0", this function can be executed automatically. After a global latch, all OUTs can accomplish a complete frame of old data and then update new frame data. Therefore, each frame maintains a fixed time and assigned grayscale. A controller just provides a free-running GCK for grayscale display in this mode.

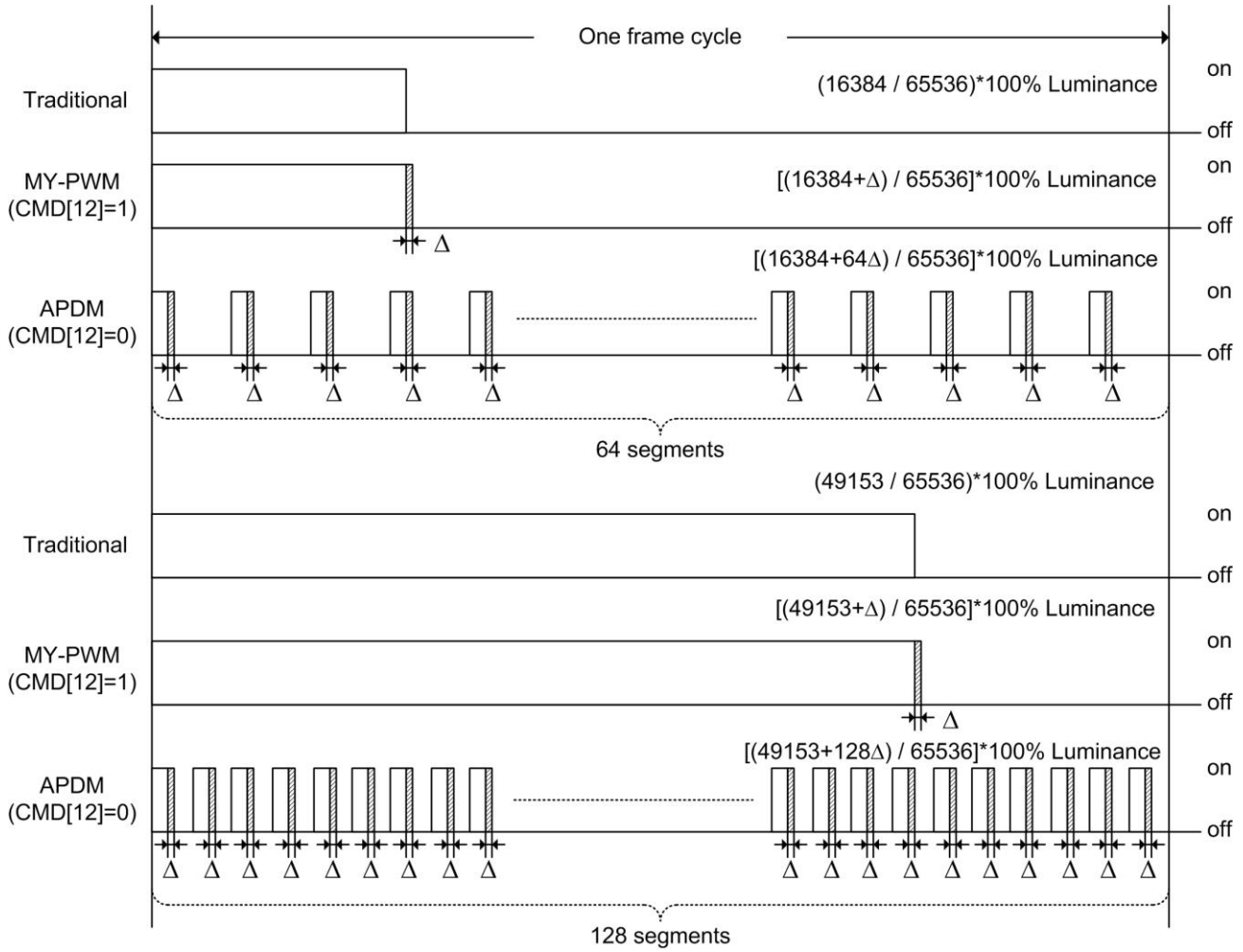
Manual Synchronization (CMD[10]="1")



When the command bit CMD[10] is set to "1", the new frame data can be updated immediately. The old frame may lose a small amount of grayscale due to a non-complete frame time. In this mode, the controller must calculate carefully the number of GCKs in order to synchronize a frame.

Functional Descriptions (continued)

Adaptive Pulse Density Modulation with Δ-Width Correction

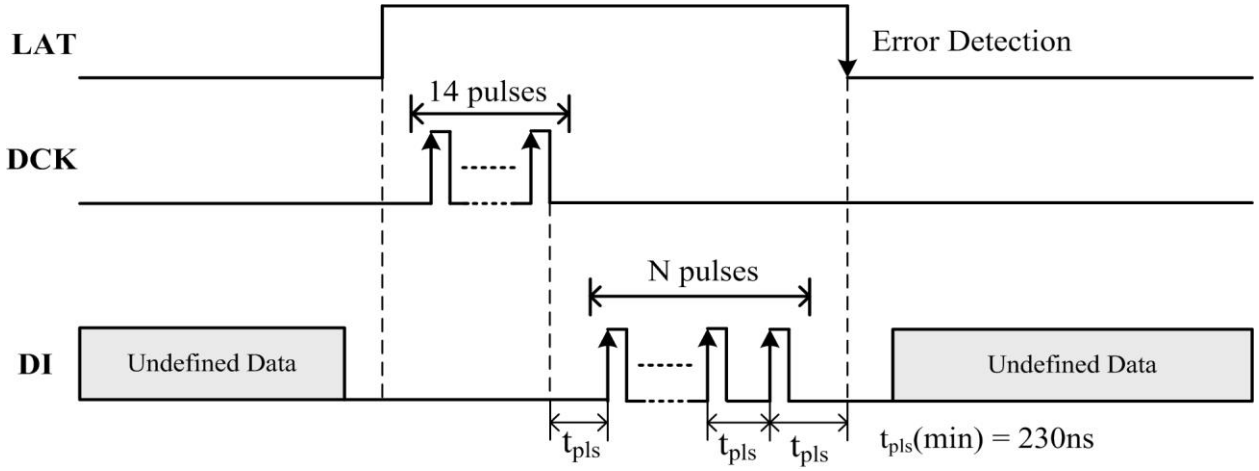


Adaptive Pulse Density Modulation (APDM) is a technique to improve output current waveform distortion and increase visual refresh rate. The adaptive output waveform is determined automatically by the grayscale value. When all outputs operate at high grayscale resolution (grayscale resolution ≧ 50%), the output waveform is divided into 128 segments to increase visual refresh rate. Otherwise, the output waveform is divided into 64 segments at a low grayscale resolution to improve output current waveform distortion. The Δ-width correction (Δ≠0) is used to compensate the non-ideal output current transient response.

When CMD[12]=”0”, the output waveform operates according to APDM.
When CMD[12]=”1”, the output waveform is a form of non-scrambling PWM in order to drive high-power LEDs and decrease transient loss.

Functional Descriptions – Diagnosis and Protections

Error Detection Mode Instructions



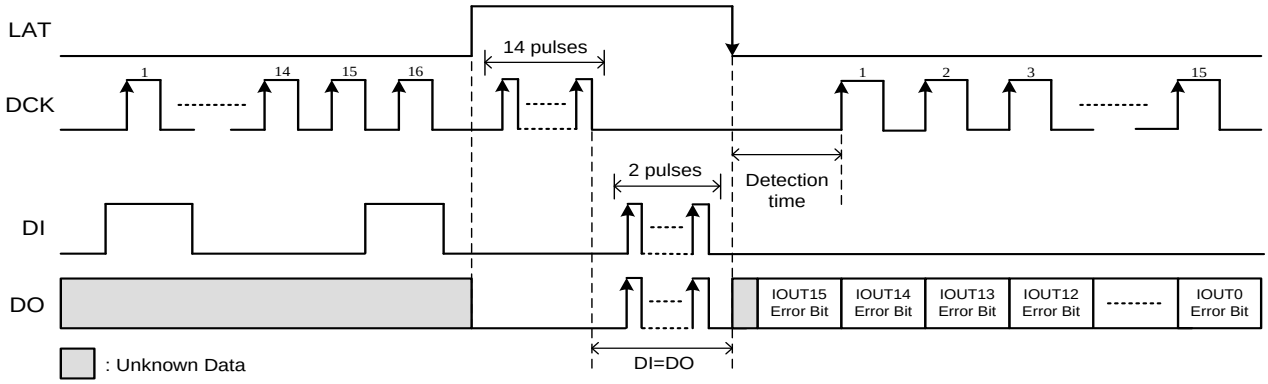
Instruction Name	Number of DI Pulses when LAT is at High	Function Description
LED Open Detection	2	Execute the LED Open Detection no matter what the image data is. The image strobe will occur at the falling edge of LAT signal.
LED Short Detection	4	Execute the LED Short Detection no matter what the image data is. The image strobe will occur at the falling edge of LAT signal.
Short-to-GND Detection	6	Execute the Short-to-GND Detection no matter what the image data is. The device will detect each IOUT pin if short-to-ground or not. The image strobe will occur at the falling edge of LAT signal.
Thermal Detection & Watchdog Result Read Out	8	The device will load thermal detection result and watchdog detection result into the 16th and 1st image shift register by this instruction. The thermal error occurs when the junction temperature is over 155ºC.
LED Smart Detection	10	Execute the LED Smart Detection no matter what the image data is. The device will detect LED Open and LED Short error simultaneously by this instruction. The image strobe will occur at the falling edge of LAT signal.
Sleep Mode	12	This instruction forces the device into Sleep Mode at the falling edge of LAT signal, then keeps GCK=high most internal circuits will shutdown. The device will be activated in the following LAT signal.
REXT Pin Detection & Watchdog Result Read Out	14	The device will load REXT detection result and watchdog detection result into the 16th and 1st image shift register by this instruction. The REXT error occurs when the REXT pin is short-to-GND or above 2.5V.

Functional Descriptions – Diagnosis and Protections (continued)

Error Bit

Error Bit	Symbol	Description
0	Error	When errors, such as open errors, short errors, short-to-GND errors, and thermal errors (PreOTP), are detected in the channel, the error bit, zero, will be loaded into the corresponding image shift register.
1	Normal	In the detecting mode, the bit, one, will be loaded into the corresponding image shift register if the device is under normal operating conditions.

LED Open Error Detection

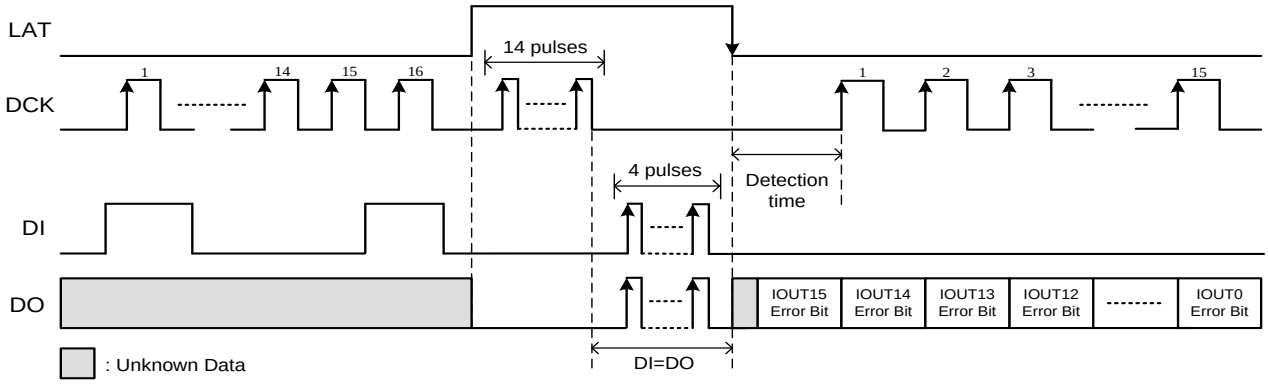


When the LED open error detection instruction is executed, it is necessary to input two DI pulses in Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263 will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of the following DCK.

When the voltage of the IOUT pins is below 0.3V, the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. A retiming DO signal, which is similar to a DI signal, appears when the LAT signal stays in a high level for cascading applications.

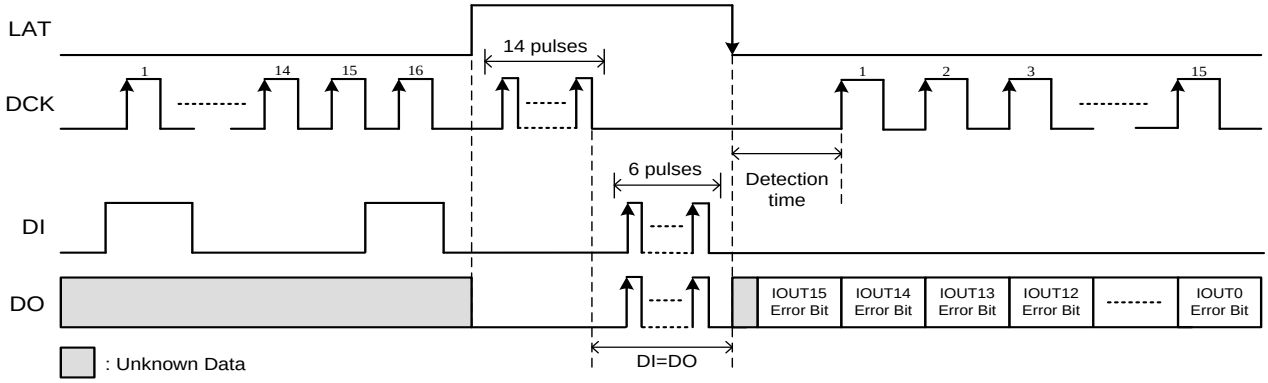
Functional Descriptions – Diagnosis and Protections (continued)

LED Short Error Detection (Output Short-to-Power Included)



When the LED short error detection instruction is executed, it is necessary to input four DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263 will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of the following DCK. When the voltage of the IOUT pins is above the threshold voltage of LED short detection, as determined by CMD[14:13], the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the DCK's rising edge. And a retiming DO signal, which is similar to a DI signal, appears when the LAT signal stays in a high level for cascading applications.

Short-to-GND Error Detection (Output Port Leakage Included)



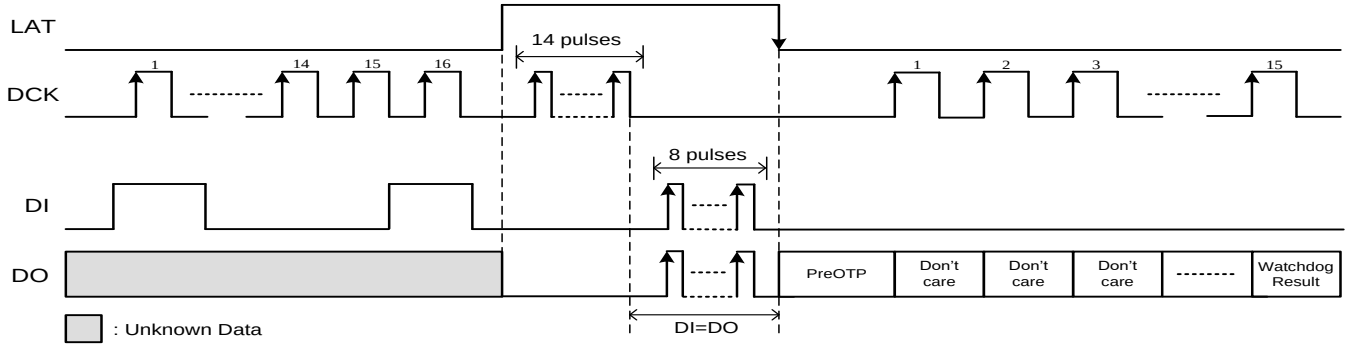
When the short-to-GND error detection instruction is executed, it is necessary to input six DI pulses in Error Detection Mode. No matter what the image latch data is, this instruction forces the output ports of the AL58263 to turn off for error detection. The detection time is defined from the falling edge of LAT to the rising edge of the following DCK.

When the voltage of IOUT pins is below 0.3V, the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the DCK's rising edge . And a retiming DO signal, which is similar to a DI signal, appears when the LAT signal stays in a high level for cascading applications.

Functional Descriptions – Diagnosis and Protections (continued)

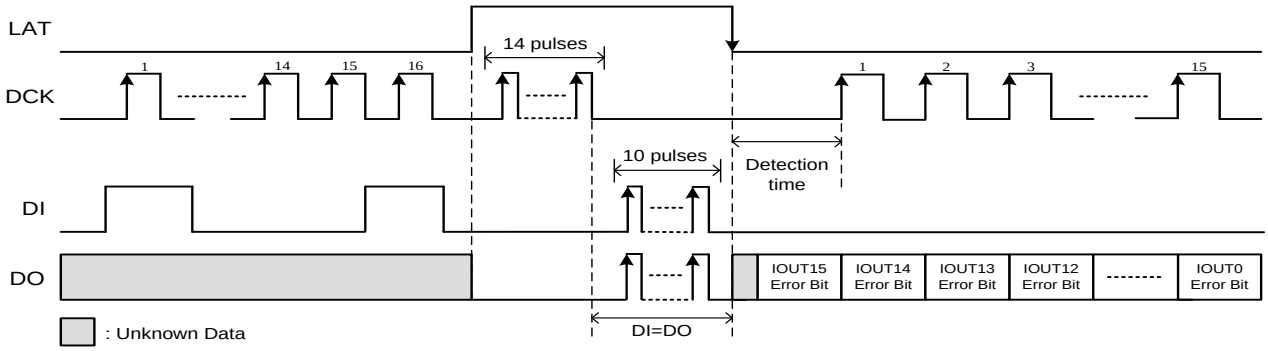
Pre-OTP Warning - Thermal Detection & Watchdog Result Read Out

The AL58263 has a pre-thermal warning threshold of +155°C (typical).



When the thermal detection instruction is executed, it is necessary to input eight DI pulses in Error Detection Mode. The AL58263 will judge of junction temperature by instruction. If the junction temperature is over 155°C, it will lead to thermal error. The device will load the PreOTP and watchdog result into the 16th and 1st image shift register and fill out the other image shift registers with bit code, 1. The error report will be shifted out from the DO pin on the synchronization of the DCK's rising edge . And a retiming DO signal, which is similar to a DI signal, appears when the LAT signal stays in a high level for cascading applications. When CMD[0]=1 and GCK keeps low or high over 30ms, the watchdog result can be "0", otherwise it would be "1".

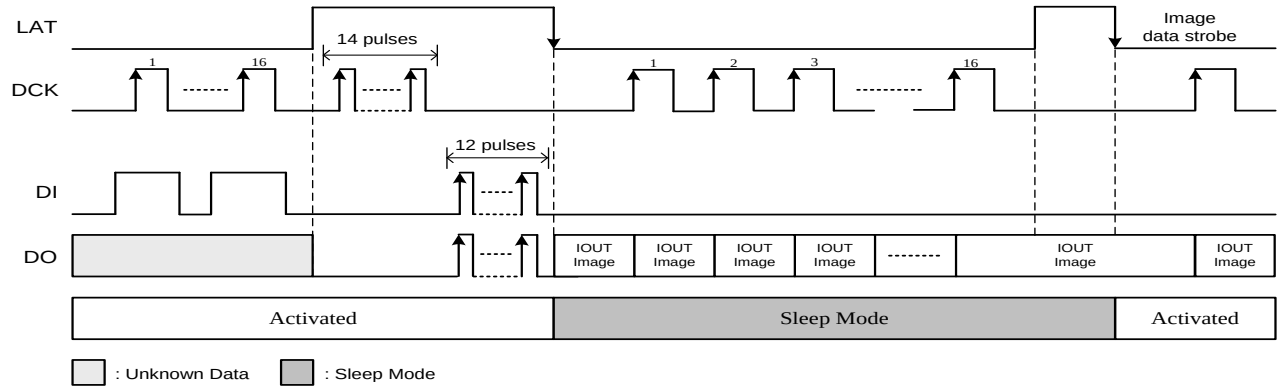
LED Smart Detection



When the LED smart detection instruction is executed, it is necessary to input ten DI pulses in Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263 will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of the following DCK. When the voltage of the IOUT pins is below 0.3V for LED open detection or above the threshold voltage of LED short detection, as determined by CMD[14:13], the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the DCK's rising edge. A retiming DO signal, which is similar to a DI signal, appears when the LAT signal stays in a high level for cascading applications.

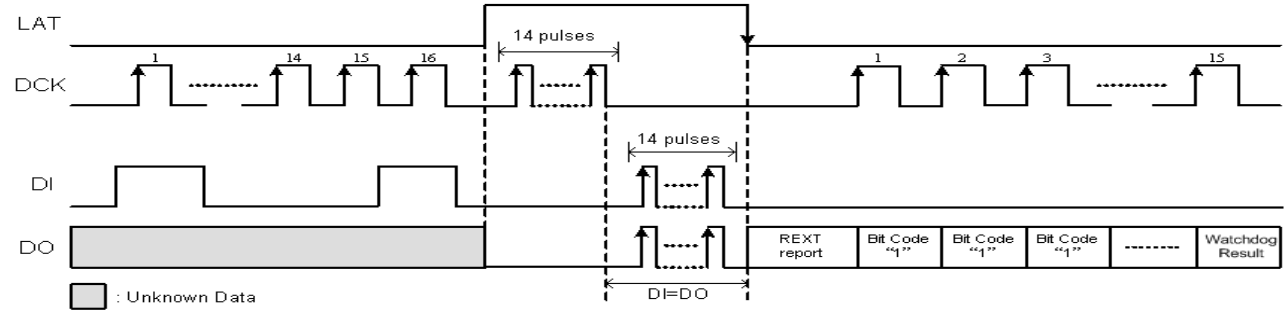
Functional Descriptions – Diagnosis and Protections (continued)

Sleep Mode



To save power, the AL58263 supports sleep mode to turn off most circuits. It is necessary to input twelve pulses in Error Detection Mode to execute this instruction, as well as keeping GCK=high at sleep mode. In this sleep mode, the supply current maintains < 0.1mA because most analog circuits are shutdown, but the digital interface is still activated in order to receive external digital data. Tue AL58263 will enter into sleep mode at the falling edge of this LAT signal and revive at the falling edge of the following LAT signal. The serial image data will be shifted out from the DO pin on the synchronization of the DCK's rising edge. A retiming DO signal, which is similar to aDI signal, appears when the LAT signal stays in a high level for cascading applications.

REXT Detection & Watchdog Result Read Out



When the REXT detection instruction is executed, it is necessary to input fourteen DI pulses in Error Detection Mode. The AL58263 will detect the voltage of the REXT pin by the instructions. If the REXT pin is open or above 2.5V or below 0.15V, it will lead to REXT error. The device will load the REXT report and watchdog the result into the 16th and 1st image shift register, as well as filling out the other image shift registers with bit code, 1. The error report will be shifted out from the DO pin on the synchronization of the DCK's rising edge. A retiming DO signal, which is similar to a DI signal, appears when the LAT signal stays in a high level for cascading applications. When CMD[0]=1 and GCK keeps low or high over 30ms, the watchdog result will be "0", otherwise it will be "1".

Functional Descriptions (continued)

Power Dissipation

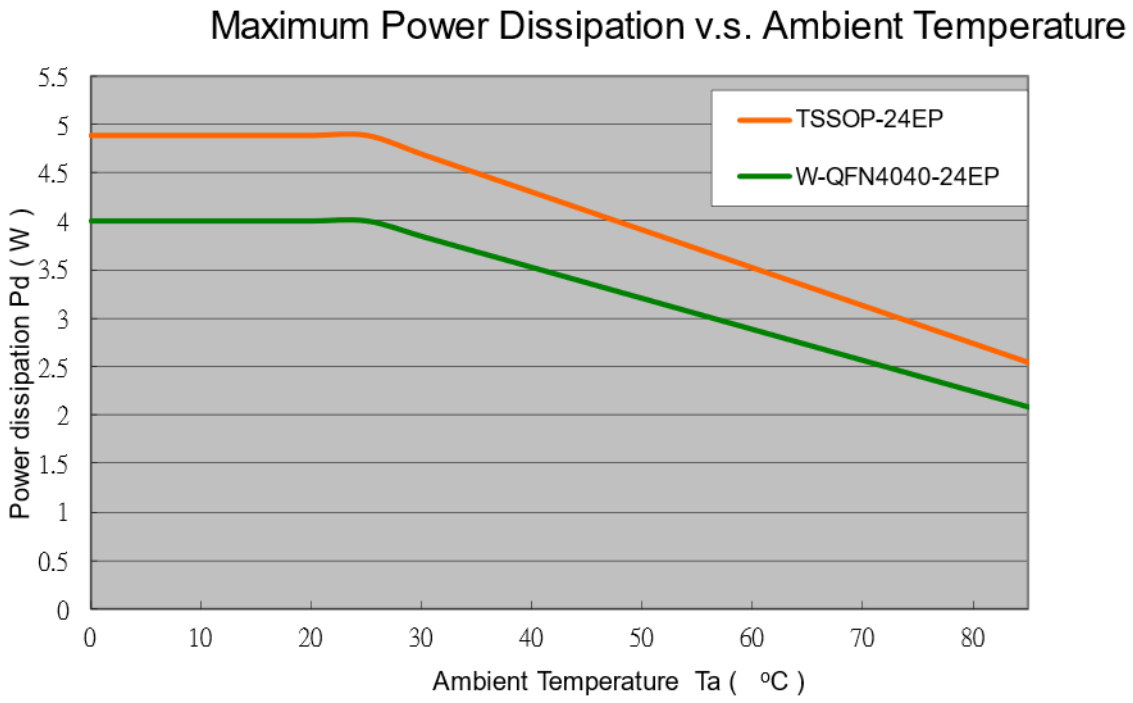
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0)} \times Iout_{(0)} \times Duty_{(0)} + \cdots + Vout_{(N)} \times Iout_{(N)} \times Duty_{(N)}\ ,\ where\ N=1\ to\ 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation, which is determined by package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(^{\circ}C) - Ta(^{\circ}C)}{Rth(j\text{-}a)(^{\circ}C/Watt)}$$

The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the two different packages.

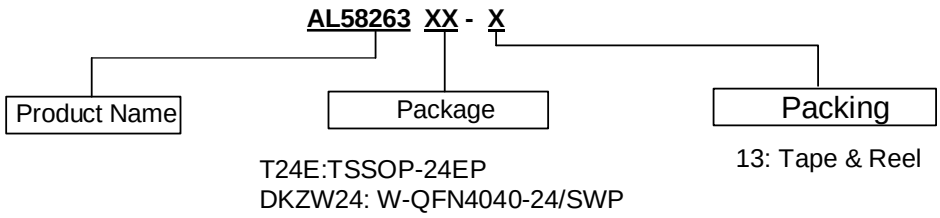


Design Tools (Note 16)

- AL58263EV1, AL58263EV2 Demo Board
- Demo Board Gerber File for PCB Layout Reference
- Design Calculator

Note: 16. Diodes' design tools can be found on our website at https://www.diodes.com/design/tools/.

Ordering Information

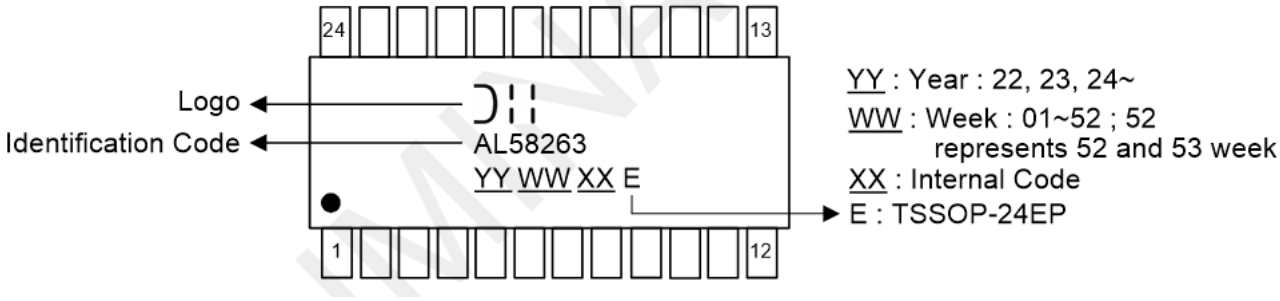


Orderable Part Number	Package	Packing		
		Quantity	Carrier	Part Number Suffix
AL58263T24E-13	TSSOP-24EP (Type A1-B)	2,500	Tape and Reel	-13
AL58263DKZW24-13	W-QFN4040-24/SWP (Type A1)	3,000	Tape and Reel	-13

Marking Information

(1) Package: TSSOP-24EP (Type A1-B)

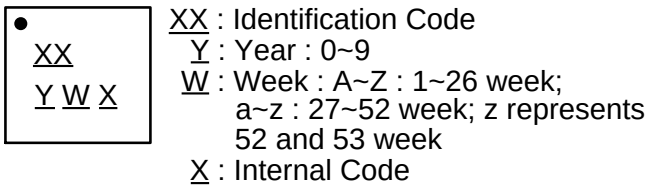
(Top View – Not to Scale)



Orderable Part Number	Package	Identification Code
AL58263T24E-13	TSSOP-24EP (Type A1-B)	AL58263

(2) Package: W-QFN4040-24/SWP (Type A1)

(Top View – Not to Scale)

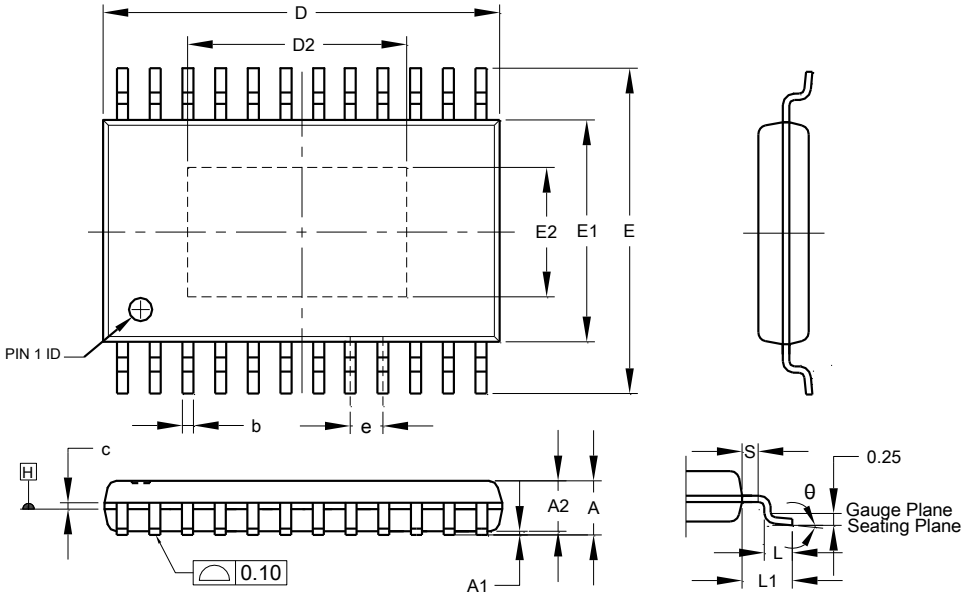


Orderable Part Number	Package	Identification Code
AL58263DKZW24-13	W-QFN4040-24/SWP (Type A1)	J7

Package Outline Dimensions

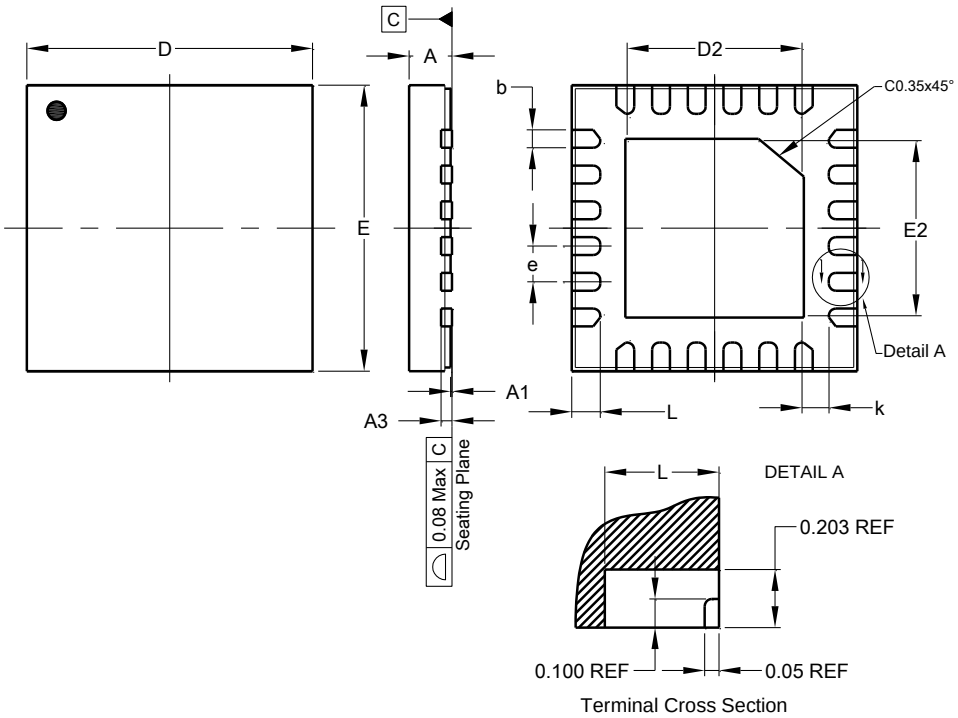
Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-24EP (Type A1-B)



TSSOP-24EP (Type A1-B)			
Dim	**Min**	**Max**	**Typ**
A	--	1.20	--
A1	0.00	0.15	--
A2	0.80	1.05	1.00
b	0.19	0.30	--
c	0.09	0.20	--
D	7.70	7.90	7.80
D2	3.70	4.62	--
E	6.40 BSC		
E1	4.30	4.50	4.40
E2	2.28	2.85	--
e	0.65 BSC		
L	0.45	0.75	060
L1	1.00 REF		
S	0.20	--	--
θ	0°	8°	--
All Dimensions in mm			

W-QFN4040-24/SWP (Type A1)

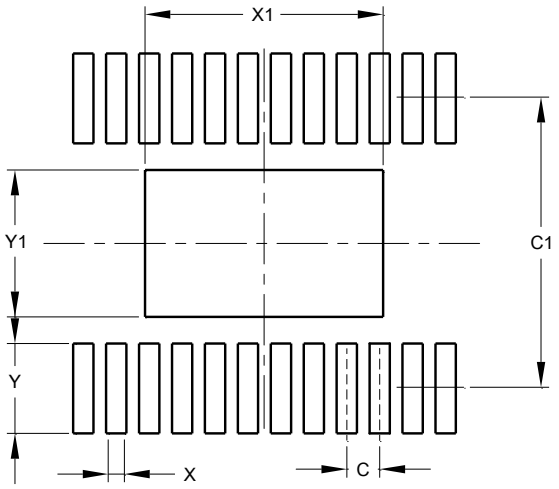


W-QFN4040-24/SWP (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	3.90	4.10	4.00
D2	2.45	2.55	2.50
E	3.90	4.10	4.00
E2	2.45	2.55	2.50
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

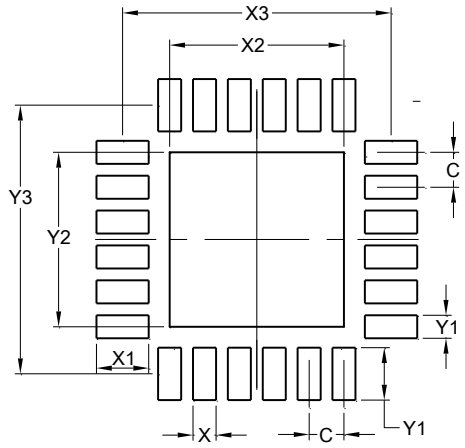
Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-24EP (Type A1-B)



Dimensions	Value (in mm)
C	0.650
C1	5.600
X	0.400
X1	4.225
Y	1.800
Y1	2.640

W-QFN4040-24/SWP (Type A1)



Dimensions	Value
C	0.500
X	0.300
X1	0.750
X2	2.500
X3	3.850
Y	0.750
Y1	0.300
Y2	2.500
Y3	3.850

Tape and Reel Information

Please see https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf for tape and reel details.

Mechanical Data

Package: TSSOP-24EP (Type A1-B)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.096 grams (Approximate)

Package: W-QFN4040-24/SWP (Type A1)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.037 grams (Approximate)

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