ALC3261

(P/N: ALC3261-CG)

FOUR CHANNEL I^{2}S/PCM AUDIO CODEC WITH VOICE DSP

DATASHEET

(China Customer Only)

Rev. 0.91

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

©2012 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC3261 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.9	2012/5/14	First release for China customer
0.91	2012/5/28	

Table of Contents

1. GENERAL DESCRIPTION 1

2. FEATURES 2

3. SYSTEM APPLICATION 3

4. FUNCTION BLOCK AND MIXER PATH 4

4.1. FUNCTION BLOCK 4
4.2. AUDIO MIXER PATH 5
4.3. DIGITAL MIXER PATH 6

5. PIN ASSIGNMENTS 7

6. PIN DESCRIPTIONS 8

6.1. DIGITAL I/O PINS 8
6.2. ANALOG I/O PINS 9
6.3. FILTER/REFERENCE 10
6.4. POWER/GROUND 10

7. FUNCTION DESCRIPTION 11

7.1. POWER 11
7.2. POWER SUPPLY ON/OFF SEQUENCE 12
7.3. RESET 13
7.3.1. Power-On Reset (POR) 13
7.3.2. Software Reset 13
7.4. CLOCKING 14
7.4.1. Phase-Locked Loop 15
7.4.2. I²C and Two I²S/PCM Interface 16
7.5. DIGITAL DATA INTERFACE 17
7.5.1. Two I²S/PCM Interface 17
7.6. AUDIO DATA PATH 20
7.6.1. 2 Analog ADCs with 4-Channel Record Path 20
7.6.2. 4 DACs with 4-Channel Playback Path 21
7.6.3. Mixers 22
7.7. ANALOG AUDIO INPUT PORT 23
7.8. ANALOG AUDIO OUTPUT PORT 24
7.9. DRC AND AGC FUNCTION 26
7.10. SPEAKER AMPLIFIER RATIO GAIN 29
7.11. EQUALIZER BLOCK 30
7.12. I²C CONTROL INTERFACE 31
7.12.1. Address Setting 31
7.12.2. Complete Data Transfer 31
7.13. GPIO, INTERRUPT AND JACK DETECTION 33
7.14. POWER MANAGEMENT 35
7.15. PROGRAMMABLE REGISTER ARRAY 36

8. REGISTERS LIST 37

8.1. REGISTER MAP 37
8.2. MX-00H: S/W RESET & DEVICE ID 39
8.3. MX-01H: SPEAKER OUTPUT CONTROL 40
8.4. MX-02H: HEADPHONE OUTPUT CONTROL 41

8.5. MX-03H: LINE OUTPUT CONTROL 43
8.6. MX-04H: MONO OUTPUT CONTROL 44
8.7. MX-0DH: IN1 INPUT CONTROL 44
8.8. MX-0EH: IN2 INPUT CONTROL 45
8.9. MX-0FH: INL & INR VOLUME CONTROL 46
8.10. MX-19H: DACL1/R1 DIGITAL VOLUME 47
8.11. MX-1AH: DACL2/R2 DIGITAL VOLUME 47
8.12. MX-1BH: DACL2/R2 MUTE/UN-MUTE CONTROL 49
8.13. MX-1CH: STEREO ADC DIGITAL VOLUME CONTROL 49
8.14. MX-1DH: MONO ADC DIGITAL VOLUME CONTROL 50
8.15. MX-1EH: ADC DIGITAL BOOST GAIN CONTROL 52
8.16. MX-27H: STEREO ADC DIGITAL MIXER CONTROL 52
8.17. MX-28H: MONO ADC DIGITAL MIXER CONTROL 53
8.18. MX-29H: STEREO ADC TO DAC DIGITAL MIXER CONTROL 54
8.19. MX-2AH: STEREO DAC DIGITAL MIXER CONTROL 54
8.20. MX-2BH: MONO DAC DIGITAL MIXER CONTROL 55
8.21. MX-2CH: DAC DIGITAL MIXER CONTROL 56
8.22. MX-2DH: VOICE DSP PATH CONTROL 1 57
8.23. MX-2EH: VOICE DSP PATH CONTROL 2 57
8.24. MX-2FH: INTERFACE DAC/ADC DATA CONTROL 58
8.25. MX-3BH: RECMIXL CONTROL 1 58
8.26. MX-3CH: RECMIXL CONTROL 2 59
8.27. MX-3DH: RECMIXR CONTROL 1 60
8.28. MX-3EH: RECMIXR CONTROL 2 61
8.29. MX-45H: HPOMIX CONTROL 62
8.30. MX-46H: SPKMIXL CONTROL 62
8.31. MX-47H: SPKMIXR CONTROL 63
8.32. MX-48H: SPOLMIX CONTROL 64
8.33. MX-49H: SPORMIX CONTROL 65
8.34. MX-4AH: SPOL/RMIX GAIN CONTROL 65
8.35. MX-4CH: MONOMIX CONTROL 66
8.36. MX-4DH: OUTMIXL CONTROL 1 66
8.37. MX-4EH: OUTMIXL CONTROL 2 67
8.38. MX-4FH: OUTMIXL CONTROL 3 68
8.39. MX-50H: OUTMIXR CONTROL 1 69
8.40. MX-51H: OUTMIXR CONTROL 2 70
8.41. MX-52H: OUTMIXR CONTROL 3 71
8.42. MX-53H: LOUTMIX CONTROL 71
8.43. MX-61H: POWER MANAGEMENT CONTROL 1 72
8.44. MX-62H: POWER MANAGEMENT CONTROL 2 73
8.45. MX-63H: POWER MANAGEMENT CONTROL 3 73
8.46. MX-64H: POWER MANAGEMENT CONTROL 4 74
8.47. MX-65H: POWER MANAGEMENT CONTROL 5 75
8.48. MX-66H: POWER MANAGEMENT CONTROL 6 75
8.49. MX-6AH: PRIVATE REGISTER INDEX 76
8.50. MX-6CH: PRIVATE REGISTER DATA 76
8.51. MX-70H: I2S1 DIGITAL INTERFACE CONTROL 76
8.52. MX-71H: I2S2 DIGITAL INTERFACE CONTROL 77
8.53. MX-73H: ADC/DAC CLOCK CONTROL 1 78
8.54. MX-74H: ADC/DAC CLOCK CONTROL 2 79
8.55. MX-75H: DIGITAL MICROPHONE CONTROL 80
8.56. MX-80H: GLOBAL CLOCK CONTROL 81
8.57. MX-81H: PLL CONTROL 1 81
8.58. MX-82H: PLL CONTROL 2 82
8.59. MX-83H: ASRC CONTROL 1 82

8.60. MX-84H: ASRC CONTROL 2 83
8.61. MX-85H: ASRC CONTROL 3 83
8.62. MX-89H: ASRC CONTROL 4 84
8.63. MX-8AH: ASRC CONTROL 5 84
8.64. MX-8CH: CLASS-D AMP OC CONTROL 85
8.65. MX-8DH: CLASS-D AMP OUTPUT CONTROL 85
8.66. MX-8EH: HP AMP CONTROL 85
8.67. MX-92H: SPKVDD DETECTION CONTROL 87
8.68. MX-93H: MICBIAS CONTROL 87
8.69. MX-B0H: EQ CONTROL 1 88
8.70. MX-B1H: EQ CONTROL 2 89
8.71. MX-B4H: DRC/AGC CONTROL 1 90
8.72. MX-B5H: DRC/AGC CONTROL 2 91
8.73. MX-B6H: DRC/AGC CONTROL 3 93
8.74. MX-BBH: JACK DETECTION CONTROL 1 94
8.75. MX-BCH: JACK DETECTION CONTROL 2 95
8.76. MX-BDH: IRQ CONTROL 1 95
8.77. MX-BEH: IRQ CONTROL 2 96
8.78. MX-BFH: GPIO AND INTERNAL STATUS 96
8.79. MX-C0H: GPIO CONTROL 1 97
8.80. MX-C2H: GPIO CONTROL 2 97
8.81. MX-C4H: VOICE DSP CONTROL 1 98
8.82. MX-C5H: VOICE DSP CONTROL 2 98
8.83. MX-C6H: VOICE DSP CONTROL 3 98
8.84. MX-C8H: PROGRAMMABLE REGISTER ARRAY CONTROL 1 99
8.85. MX-C9H: PROGRAMMABLE REGISTER ARRAY CONTROL 2 99
8.86. MX-CAH: PROGRAMMABLE REGISTER ARRAY CONTROL 3 99
8.87. MX-CBH: PROGRAMMABLE REGISTER ARRAY CONTROL 4 100
8.88. MX-CCH: PROGRAMMABLE REGISTER ARRAY CONTROL 5 100
8.89. MX-CFH: SOUNZREAL BASSBACK CONTROL 101
8.90. MX-D9H: SOFT VOLUME & ZCD CONTROL 101
8.91. MX-FAH: GENERAL CONTROL 1 102
8.92. MX-FBH: GENERAL CONTROL 2 103
8.93. PR-3DH: ADC/DAC RESET CONTROL 104
8.94. PR-A0H: EQ LOW PASS FILTER COEFFICIENT (LPF:A1) 104
8.95. PR-A1H: EQ LOW PASS FILTER GAIN (LPF:H0) 105
8.96. PR-A2H: EQ BAND 1 COEFFICIENT (BPF1:A1) 105
8.97. PR-A3H: EQ BAND 1 COEFFICIENT (BPF1:A2) 105
8.98. PR-A4H: EQ BAND 1 GAIN (BPF1:H0) 105
8.99. PR-A5H: EQ BAND 2 COEFFICIENT (BPF2:A1) 106
8.100. PR-A6H: EQ BAND 2 COEFFICIENT (BPF2:A2) 106
8.101. PR-A7H: EQ BAND 2 GAIN (BPF2:H0) 106
8.102. PR-A8H: EQ BAND 3 COEFFICIENT (BPF3:A1) 106
8.103. PR-A9H: EQ BAND 3 COEFFICIENT (BPF3:A2) 107
8.104. PR-AAH: EQ BAND 3 GAIN (BPF3:H0) 107
8.105. PR-ABH: EQ BAND 4 COEFFICIENT (BPF4:A1) 107
8.106. PR-ACH: EQ BAND 4 COEFFICIENT (BPF4:A2) 107
8.107. PR-ADH: EQ BAND 4 GAIN (BPF4:H0) 108
8.108. PR-AEH: EQ HIGH PASS FILTER 1 COEFFICIENT (HPF1:A1) 108
8.109. PR-AFH: EQ HIGH PASS FILTER 1 GAIN (HPF1:H0) 108
8.110. PR-B0H: EQ HIGH PASS FILTER 2 COEFFICIENT (HPF2:A1) 108
8.111. PR-B1H: EQ HIGH PASS FILTER 2 COEFFICIENT (HPF2:A2) 109
8.112. PR-B2H: EQ HIGH PASS FILTER 2 GAIN (HPF2:H0) 109
8.113. MX-FEH: VENDOR ID 109

9. ELECTRICAL CHARACTERISTICS 110

9.1. DC CHARACTERISTICS 110
9.1.1. Absolute Maximum Ratings *110*
9.1.2. Recommended Operating Conditions *110*
9.1.3. Static Characteristics *110*
9.2. ANALOG PERFORMANCE CHARACTERISTICS 111
9.3. SIGNAL TIMING 113
9.3.1. I²C Control Interface *113*
9.3.2. I²S/PCM Interface Master Mode *114*
9.3.3. I²S/PCM Interface Slave Mode *115*

10. APPLICATION CIRCUITS 116

11. MECHANICAL DIMENSIONS 118

12. ORDERING INFORMATION 119

List of Tables

TABLE 1. DIGITAL I/O PINS 8
TABLE 2. ANALOG I/O PINS 9
TABLE 3. FILTER/REFERENCE 10
TABLE 4. POWER/GROUND 10
TABLE 5. POWER SUPPLY FOR BEST PERFORMANCE 11
TABLE 6. POWER SUPPLY CONDITION FOR POWER DOWN LEAKAGE 11
TABLE 7. RESET OPERATION 13
TABLE 8. POWER-ON RESET VOLTAGE 13
TABLE 10. CLOCK SETTING TABLE FOR 48K (UNIT: MHZ) 15
TABLE 11. CLOCK SETTING TABLE FOR 44.1K (UNIT: MHZ) 15
TABLE 12. RATION GAIN TABLE FOR SPKVDD AND AVDD 29
TABLE 14. ADDRESS SETTING (0X38H) 31
TABLE 15. WRITE WORD PROTOCOL 32
TABLE 16. READ WORD PROTOCOL 32
TABLE 17. PROGRAMMABLE REGISTER TABLE 36
TABLE 18. REGISTER MAP 37
TABLE 19. MX-00H: S/W RESET 39
TABLE 20. MX-01H: SPEAKER OUTPUT CONTROL 40
TABLE 21. MX-02H: HEADPHONE OUTPUT CONTROL 41
TABLE 22. MX-03H: LINE OUTPUT CONTROL 43
TABLE 23. MX-04H: MONO OUTPUT CONTROL 44
TABLE 24. MX-0DH: IN1 INPUT CONTROL 44
TABLE 25. MX-0EH: IN2 INPUT CONTROL 45
TABLE 26. MX-0FH: INL & INR VOLUME CONTROL 46
TABLE 27. MX-19H: DACL1/R1 DIGITAL VOLUME 47
TABLE 28. MX-1AH: DACL2/R2 DIGITAL VOLUME 47
TABLE 29. MX-1BH: DACL2/R2 MUTE/UN-MUTE CONTROL 49
TABLE 30. MX-1CH: STEREO ADC DIGITAL VOLUME CONTROL 50
TABLE 31. MX-1DH: MONO ADC DIGITAL VOLUME CONTROL 50
TABLE 32. MX-1EH: ADC DIGITAL BOOST GAIN CONTROL 52
TABLE 33. MX-27H: STEREO ADC DIGITAL MIXER CONTROL 52
TABLE 34. MX-28H: MONO ADC DIGITAL MIXER CONTROL 53
TABLE 35. MX-29H: STEREO ADC TO DAC DIGITAL MIXER CONTROL 54
TABLE 36. MX-2AH: STEREO DAC DIGITAL MIXER CONTROL 54
TABLE 37. MX-2BH: MONO DAC DIGITAL MIXER CONTROL 55
TABLE 38. MX-2CH: DAC DIGITAL MIXER CONTROL 56
TABLE 39. MX-2DH: VOICE DSP PATH CONTROL 1 57
TABLE 40. MX-2EH: VOICE DSP PATH CONTROL 2 57
TABLE 41. MX-2FH: INTERFACE DAC/ADC DATA CONTROL 58
TABLE 42. MX-3BH: RECMIXL CONTROL 1 58
TABLE 43. MX-3CH: RECMIXL CONTROL 2 59
TABLE 44. MX-3DH: RECMIXR CONTROL 1 60
TABLE 45. MX-3EH: RECMIXR CONTROL 2 61
TABLE 46. MX-45H: HPOMIX CONTROL 62
TABLE 47. MX-46H: SPKMIXL CONTROL 62
TABLE 48. MX-47H: SPKMIXR CONTROL 63
TABLE 49. MX-48H: SPOLMIX CONTROL 64
TABLE 50. MX-49H: SPORMIX CONTROL 65
TABLE 51. MX-4AH: SPOL/RMIX GAIN CONTROL 65
TABLE 52. MX-4CH: MONOMIX CONTROL 66
TABLE 53. MX-4DH: OUTMIXL CONTROL 1 66
TABLE 54. MX-4EH: OUTMIXL CONTROL 2 67

TABLE 55. MX-4FH: OUTMIXL CONTROL 3 68
TABLE 56. MX-50H: OUTMIXR CONTROL 1 69
TABLE 57. MX-51H: OUTMIXR CONTROL 2 70
TABLE 58. MX-52H: OUTMIXR CONTROL 3 71
TABLE 59. MX-53H: LOUTMIX CONTROL 71
TABLE 60. MX-61H: POWER MANAGEMENT CONTROL 1 72
TABLE 61. MX-62H: POWER MANAGEMENT CONTROL 2 73
TABLE 62. MX-63H: POWER MANAGEMENT CONTROL 3 73
TABLE 63. MX-64H: POWER MANAGEMENT CONTROL 4 74
TABLE 64. MX-65H: POWER MANAGEMENT CONTROL 5 75
TABLE 65. MX-66H: POWER MANAGEMENT CONTROL 6 75
TABLE 66. MX-6AH: PRIVATE REGISTER INDEX 76
TABLE 67. MX-6CH: PRIVATE REGISTER DATA 76
TABLE 68. MX-70H: I2S1 DIGITAL INTERFACE CONTROL 76
TABLE 69. MX-71H: I2S2 DIGITAL INTERFACE CONTROL 77
TABLE 70. MX-73H: ADC/DAC CLOCK CONTROL 1 78
TABLE 71. MX-74H: ADC/DAC CLOCK CONTROL 2 79
TABLE 72. MX-75H: DIGITAL MICROPHONE CONTROL 80
TABLE 73. MX-80H: GLOBAL CLOCK CONTROL 81
TABLE 74. MX-81H: PLL CONTROL 1 81
TABLE 75. MX-82H: PLL CONTROL 2 82
TABLE 76. MX-83H: ASRC CONTROL 1 82
TABLE 77. MX-84H: ASRC CONTROL 2 83
TABLE 78. MX-85H: ASRC CONTROL 3 83
TABLE 79. MX-89H: ASRC CONTROL 4 84
TABLE 80. MX-8AH: ASRC CONTROL 5 84
TABLE 81. MX-8CH: CLASS-D AMP OC CONTROL 85
TABLE 82. MX-8DH: CLASS-D AMP OUTPUT CONTROL 85
TABLE 83. MX-8EH: HP AMP CONTROL 85
TABLE 84. MX-8FH: HP AMP CONTROL 2 86
TABLE 85. MX-92H: SPKVDD DETECTION CONTROL 87
TABLE 86. MX-93H: MICBIAS CONTROL 87
TABLE 87. MX-B0H: EQ CONTROL 1 88
TABLE 88. MX-B1H: EQ CONTROL 2 89
TABLE 89. MX-B4H: DRC/AGC CONTROL 1 90
TABLE 90. MX-B5H: DRC/AGC CONTROL 2 91
TABLE 91. MX-B6H: DRC/AGC CONTROL 3 93
TABLE 92. MX-BBH: JACK DETECTION CONTROL 1 94
TABLE 93. MX-BCH: JACK DETECTION CONTROL 2 95
TABLE 94. MX-BDH: IRQ CONTROL 1 95
TABLE 95. MX-BEH: IRQ CONTROL 2 96
TABLE 96. MX-BFH: GPIO AND INTERNAL STATUS 96
TABLE 97. MX-C0H: GPIO CONTROL 1 97
TABLE 98. MX-C2H: GPIO CONTROL 2 97
TABLE 99. MX-C4H: VOICE DSP CONTROL 1 98
TABLE 100. MX-C5H: VOICE DSP CONTROL 2 98
TABLE 101. MX-C6H: VOICE DSP CONTROL 3 98
TABLE 102. MX-C8H: PROGRAMMABLE REGISTER ARRAY CONTROL 1 99
TABLE 103. MX-C9H: PROGRAMMABLE REGISTER ARRAY CONTROL 2 99
TABLE 104. MX-CAH: PROGRAMMABLE REGISTER ARRAY CONTROL 3 100
TABLE 105. MX-CBH: PROGRAMMABLE REGISTER ARRAY CONTROL 4 100
TABLE 106. MX-CCH: PROGRAMMABLE REGISTER ARRAY CONTROL 5 100
TABLE 107. MX-CFH: SOUNZREAL BASSBACK CONTROL 101
TABLE 108. MX-D9H: SOFT VOLUME & ZCD CONTROL 101
TABLE 109. MX-FAH: GENERAL CONTROL 1 102

TABLE 110. MX-FBH: GENERAL CONTROL 2 103
TABLE 111. PR-3DH: ADC/DAC RESET CONTROL 104
TABLE 112. PR-A0H: EQ LOW PASS FILTER COEFFICIENT (LPF:A1) 104
TABLE 113. PR-A1H: EQ LOW PASS FILTER GAIN (LPF:H0) 105
TABLE 114. PR-A2H: EQ BAND 1 COEFFICIENT (BPF1:A1) 105
TABLE 115. PR-A3H: EQ BAND 1 COEFFICIENT (BPF1:A2) 105
TABLE 116. PR-A4H: EQ BAND 1 GAIN (BPF1:H0) 105
TABLE 117. PR-A5H: EQ BAND 2 COEFFICIENT (BPF2:A1) 106
TABLE 118. PR-A6H: EQ BAND 2 COEFFICIENT (BPF2:A2) 106
TABLE 119. PR-A7H: EQ BAND 2 GAIN (BPF2:H0) 106
TABLE 120. PR-A8H: EQ BAND 3 COEFFICIENT (BPF3:A1) 106
TABLE 121. PR-A9H: EQ BAND 3 COEFFICIENT (BPF3:A2) 107
TABLE 122. PR-AAH: EQ BAND 3 GAIN (BPF3:H0) 107
TABLE 123. PR-ABH: EQ BAND 4 COEFFICIENT (BPF4:A1) 107
TABLE 124. PR-ACH: EQ BAND 4 COEFFICIENT (BPF4:A2) 107
TABLE 125. PR-ADH: EQ BAND 4 GAIN (BPF4:H0) 108
TABLE 126. PR-AEH: EQ HIGH PASS FILTER 1 COEFFICIENT (HPF1:A1) 108
TABLE 127. PR-AFH: EQ HIGH PASS FILTER 1 GAIN (HPF1:H0) 108
TABLE 128. PR-B0H: EQ HIGH PASS FILTER 2 COEFFICIENT (HPF2:A1) 108
TABLE 129. PR-B1H: EQ HIGH PASS FILTER 2 COEFFICIENT (HPF2:A2) 109
TABLE 130. PR-B2H: EQ HIGH PASS FILTER 2 GAIN (HPF2:H0) 109
TABLE 131. MX-FEH: VENDOR ID 109
TABLE 132. ABSOLUTE MAXIMUM RATINGS 110
TABLE 133. RECOMMENDED OPERATING CONDITIONS 110
TABLE 134. STATIC CHARACTERISTICS 110
TABLE 135. ANALOG PERFORMANCE CHARACTERISTICS 111
TABLE 136. I^2C TIMING 113
TABLE 137. TIMING OF I^2S/PCM MASTER MODE 114
TABLE 138. I^2S/PCM SLAVE MODE TIMING 115
TABLE 139. ORDERING INFORMATION 119

List of Figures

FIGURE 1. BLOCK DIAGRAM 4
FIGURE 2. AUDIO MIXER PATH 5
FIGURE 3. DIGITAL MIXER PATH 6
FIGURE 4. PIN ASSIGNMENTS 7
FIGURE 5. AUDIO CLOCK TREE 14
FIGURE 6. PCM MONO DATA MODE A FORMAT (BCLK POLARITY=0) 17
FIGURE 7. PCM MONO DATA MODE A FORMAT (BCLK POLARITY=1) 17
FIGURE 8. PCM MONO DATA MODE B FORMAT (BCLK POLARITY=0) 18
FIGURE 9. PCM STEREO DATA MODE A FORMAT (BCLK POLARITY=0) 18
FIGURE 10. PCM STEREO DATA MODE B FORMAT (BCLK POLARITY=0) 18
FIGURE 11. I2S DATA FORMAT (BCLK POLARITY=0) 19
FIGURE 12. LEFT-JUSTIFIED DATA FORMAT (BCLK POLARITY=0) 19
FIGURE 13. 4-CHANNEL RECORDING PATH 20
FIGURE 14. 4-CHANNEL PLAYBACK PATH 21
FIGURE 15. SPEAKER OUTPUT MODE – STEREO MODE 24
FIGURE 16. DAC DRC FUNCTION BLOCK 26
FIGURE 17. ADC AGC FUNCTION BLOCK 26
FIGURE 18. DRC/AGC FOR PLAYBACK/RECORDING MODE 27
FIGURE 19. DRC/AGC FOR NOISE GATE MODE 28
FIGURE 20. RATIO GAIN BEHAVIOR FOR SPKVDD AND AVDD 29
FIGURE 21. DATA TRANSFER OVER I2C CONTROL INTERFACE 31
FIGURE 22. GPIO FUNCTION BLOCK 33
FIGURE 23. IRQ FUNCTION BLOCK 34
FIGURE 24. JD SOURCE SELECTION 34
FIGURE 25. POWER MANAGEMENT 35
FIGURE 28. I2C CONTROL INTERFACE 113
FIGURE 29. TIMING OF I2S/PCM MASTER MODE 114
FIGURE 30. I2S/PCM SLAVE MODE TIMING 115
FIGURE 32. PACKAGE DIMENSION 118

1. General Description

The ALC3261 is a low power, dual I^2S interface, 4 channels DAC and 2 channel ADC Audio Codec with a optimized Voice DSP integrated. The primary I2S interface connects to system host chip and its secondary I^2S interface can perform as input or output device connected to external processor, blue tooth device or wireless transceiver.

ALC3261 is a highly integration of audio subsystem chip, including two stereo DACs with 100dB SNR, one stereo ADC with 94dB SNR, stereo Class-D speaker amplifiers provides 1.5W per channel into 8Ω or 2.5W per channel into 4Ω with a 5V supply with excellent PSRR and low EMI, a mono differential earpiece amplifier is also provided, providing output from any DAC or Analog-in.

The ALC3261 features an extra low power cap-free headphone amplifier. It consumes only less than 10mW power during playback, providing tablet system longer battery life under headphone listening mode.

The integrated DRC (Dynamic Range Controller) and parametric Equalizer provides further digital sound processing capability of audio playback paths. The DRC in ALC3261 continuously monitors the DAC output level. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. It ensures the maximum/consistent signal amplitude without producing audio clipping and speaker damage. The parametric Equalizer contains 7 independent filters with programmable gain, center frequency and bandwidth to tailor the frequency characteristics of embedded speaker system according to user preferences.

ALC3261 embedded a low power wideband voice DSP. This optimized voice DSP provides excellent noise suppression, echo cancellation and beam forming performance. It combines 8 kHz and 16 kHz sampling rate and 75MIPS digital signal processing capability to achieve high fidelity and non-stationary wideband performance.

2. Features

- Two Stereo Digital-to-Analog Converters with 100dBA SNR
- One Stereo Analog-to-Digital Converter with 94dBA SNR
- Differential analog microphone inputs with boost pre-amplifiers and low noise microphone bias
  - +20/+24/+30/+35/+40/+44/+50/+52 dB microphone boost gain
  - MIC input to ADC with 50dB boost gain, SNR > 66dBA and THD+N < -65dB
  - Adjustable microphone reference voltage (0.9*MICVDD or 0.75*MICVDD)
- Stereo line level input
  - Line level input to ADC with 0dB gain, SNR >= 94dBA, THD+N <= -83dB
- Stereo line level output
  - ADC to line level output with 0dB gain, SNR >= 100dBA, THD+N <= -86dB
- Stereo/Mono BTL (Bridge-Tied-Load) Class-D amplifier
  - 650mW/CH (SPKVDD=3.6V, THD+N < = 1%, 8Ω Load)
  - 500mW/CH (SPKVDD=3.6V, THD+N < = 0.1%, 8Ω Load)
  - 1.2W/CH (SPKVDD=5.0V, THD+N < = 1%, 8Ω Load)
  - 2.5W/CH (SPKVDD=5.0V, THD+N < = 10%, 4Ω Load)
  - 2.1W/CH (SPKVDD=5.0V, THD+N < = 1%, 4Ω Load)
  - Auto speaker ratio gain for SPKVDD = 3.3V ~ 5.0V
- Stereo Cap-Free headphone amplifier with extra low power consumption for playback
  - 20mW/CH (AVDD=CPVDD=1.8V, THD+N <= -80dB, 16Ω Load)
  - Playback power consumption <= 10mW (AVDD=VBVDD=CPVDD=1.8V, 16Ω, With I2S Clock, Playback Silence)
  - Playback power consumption <= 13mW (AVDD=VBVDD=CPVDD=1.8V, 16Ω, With I2S Clock, Playback 1mW/channel to 32Ω headphone)
- Mono differential receiver amplifier
  - 50mW/CH (AVDD=CPVDD=1.8V, THD+N <= -70dB, 16Ω Load, BTL mode)
- Audio jack insert detection
- Inside PLL can receiver wide range clock input
- Two 24bit/8kHz ~ 192kHz I^2S/PCM interface for each mono DAC and stereo DAC
- Two 24bit/8kHz ~ 192kHz I^2S/PCM interface for stereo ADC
- I^2C control interface
- Two digital microphone interfaces supported
- Asynchronous sample rate converter (ASRC) for each interface
- Programmable register table with two sequencers
- 7-bands parametric equalizer (EQ) for DAC path or ADC path
- Enhanced DRC(Dynamic Range Control)/AGC(Auto Gain Control) with compression function for DAC path or ADC path
- Zero detection and soft volume for pop noise suppression
- Speaker amplifier DC term self-test function for speaker protection
- Voice Processing
  - Noise Reduction
  - Beam Forming with Stereo Microphone
  - Far Field Pick-Up Technology

3. System Application

- Smart Phones
- Tablet

4. Function Block and Mixer Path

4.1. Function Block

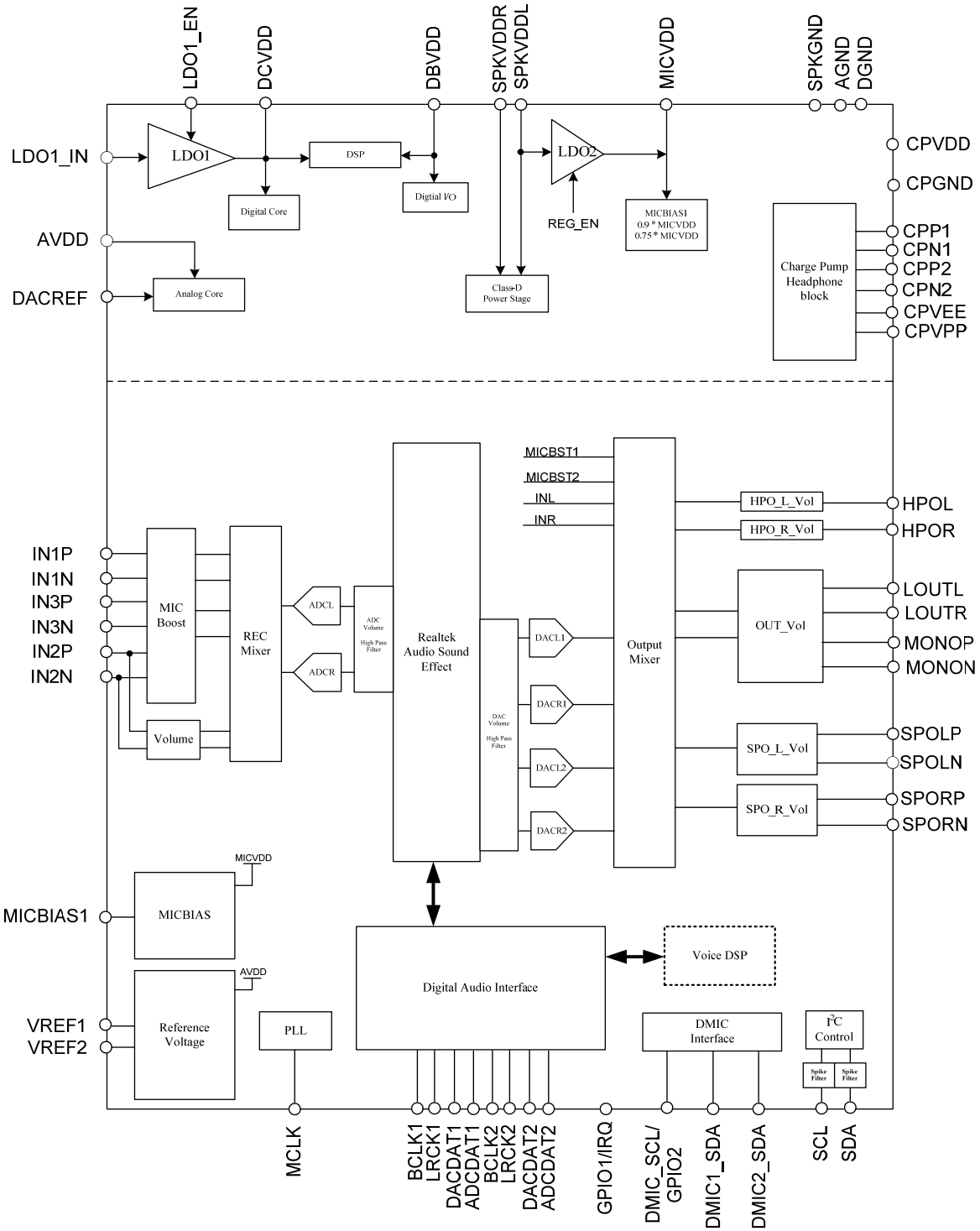


Figure 1. Block Diagram

4.2. Audio Mixer Path

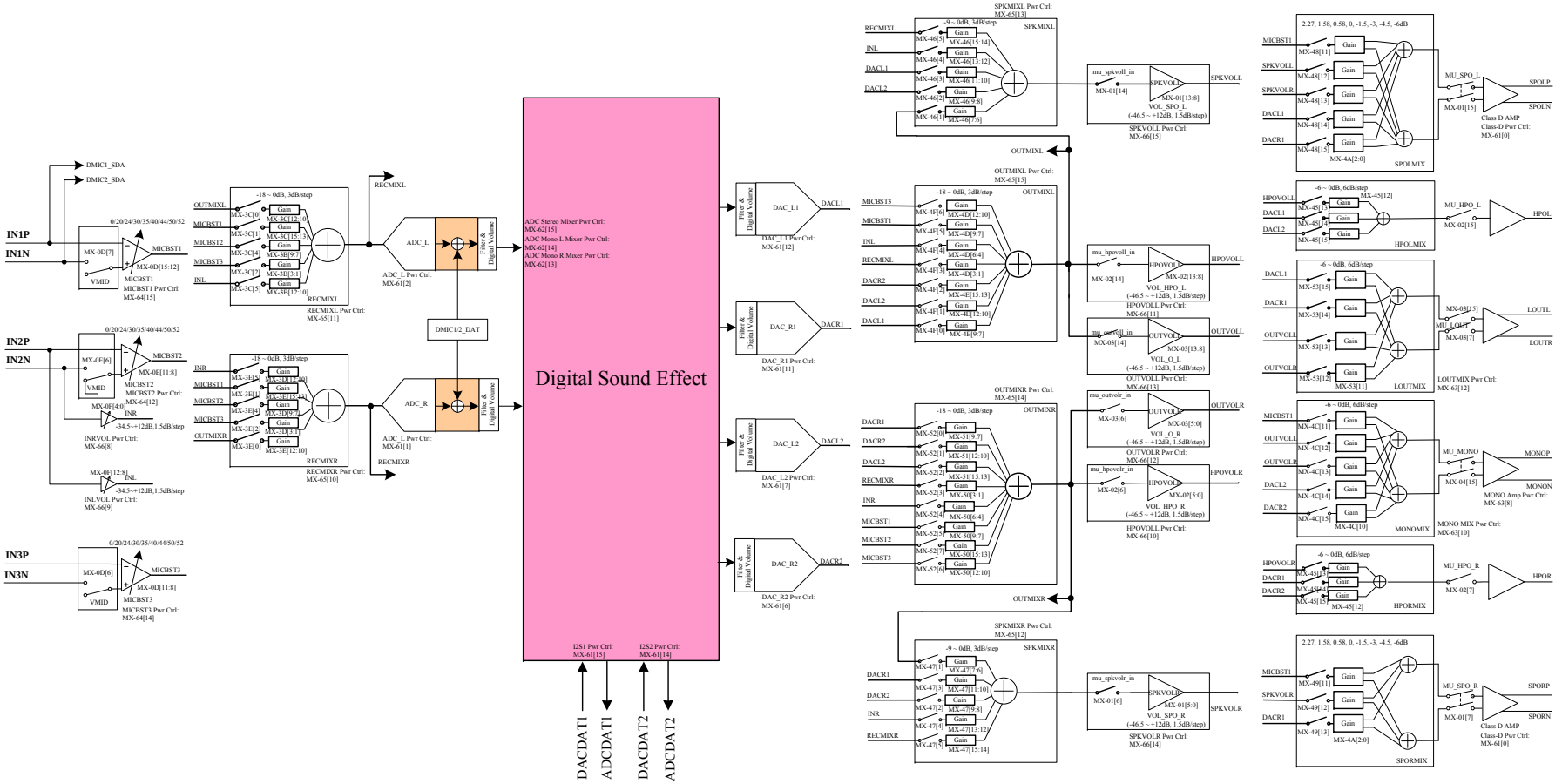


Figure 2. Audio Mixer Path

4.3. Digital Mixer Path

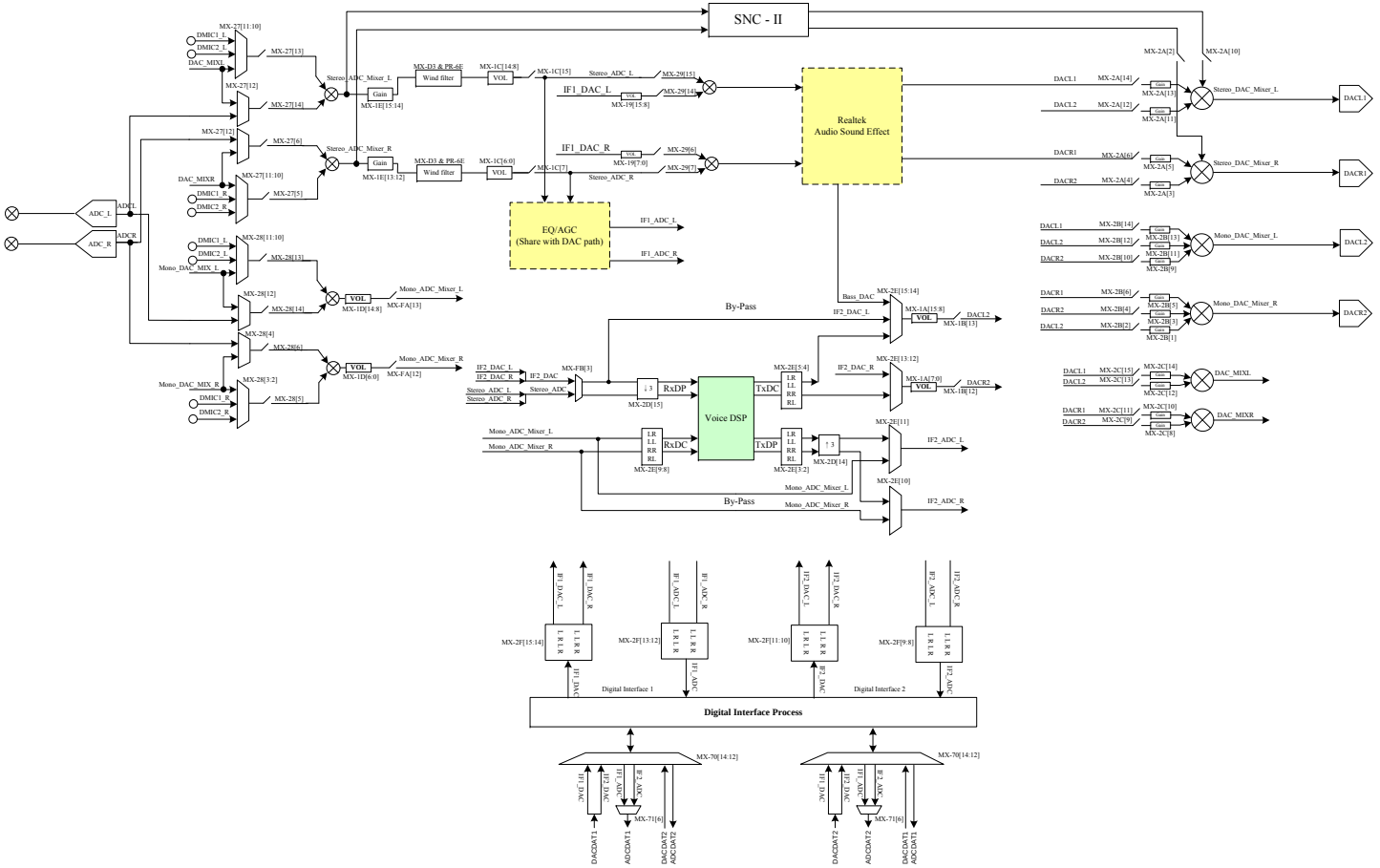


Figure 3. Digital Mixer Path

5. Pin Assignments

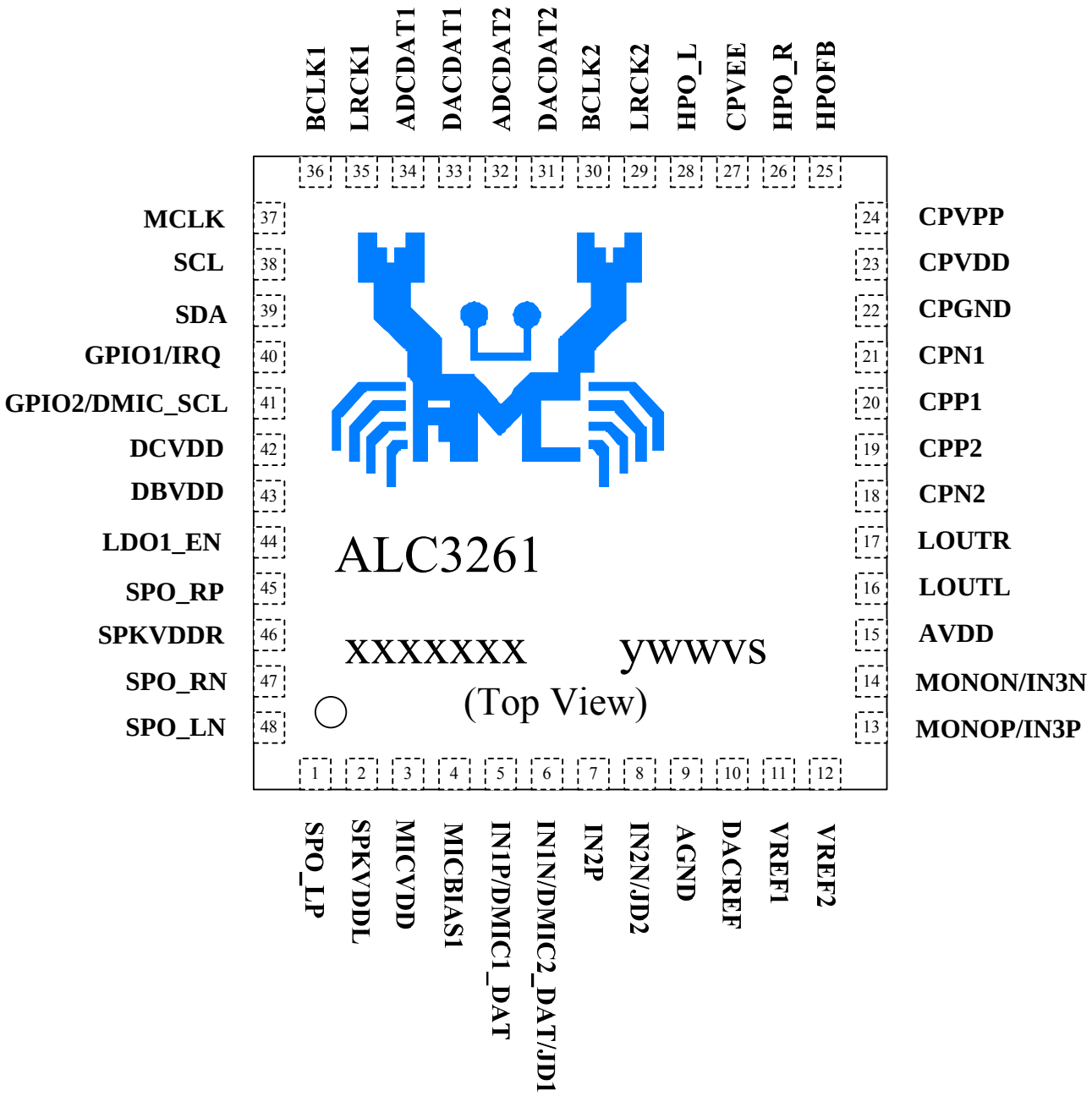


Figure 4. Pin Assignments

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
DACDAT1	I	33	First I2S interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
ADCDAT1	O	34	First I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK1	I/O	36	First I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
LRCK1	I/O	35	First I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
DACDAT2	I	31	Second I2S interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
ADCDAT2	O	32	Second I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK2	I/O	30	Second I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
LRCK2	I/O	29	Second I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
SDA	I/O	39	I2C interface serial data	Open drain structure
SCL	I	38	I2C interface clock input	Schmitt trigger
MCLK	I	37	I2S interface master clock input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
GPIO1/IRQ	I/O	40	General purpose input and output Interrupt output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger
DMIC_SCL	O	41	Digital microphone clock output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
LDO1_EN	I	44	LDO1 enable control for digital core power (Low: Disable; High: Enable)	Input threshold: V_{IL} = 0.65*DBVDD V_{IH} = 0.35*DBVDD
				Total: 14 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LOUTR	O	17	Line output type (single-end output) Right channel	Analog output
LOUTL	O	16	Line output type (single-end output) Left channel	Analog output
IN2P	I	7	Positive differential input for microphone 2 Left channel line input	Analog input
IN2N/JD2	I	8	Negative differential input for microphone 2 Right channel line input Second jack detection pin	Analog input JD threshold: V_{IL} = 0.2V V_{IH} = 1.2V
IN1P/DMIC_DAT	I	5	Positive differential input for microphone 1 First digital microphone data input	Analog input Digital input
IN1N/JD1	I	6	Negative differential input for microphone 1 First jack detection pin	Analog input Digital input JD threshold: V_{IL} = 0.2V V_{IH} = 1.2V
HPO_R	O	26	Headphone amplifier output Right channel	Analog output
HPO_L	O	28	Headphone amplifier output Left channel	Analog output
SPO_LP	O	1	Speaker amplifier output Left differential positive output channel	Analog output
SPO_LN	O	48	Speaker amplifier output Left differential negative output channel	Analog output
SPO_RP	O	45	Speaker amplifier output Right differential positive output channel	Analog output
SPO_RN	O	47	Speaker amplifier output Right differential negative output channel	Analog output
MONOP/IN3P	I/O	13	Mono output with driving capability Differential positive output channel Positive differential input for microphone 3	Analog output Analog input
MONON/IN3N	I/O	14	Mono output with driving capability Differential negative output channel Negative differential input for microphone 3	Analog output Analog input
				Total: 14 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
MICBIAS1	O	4	Bias voltage output for microphone	Programmable analog DC output
VREF1	O	11	First internal reference voltage	4.7uF capacitor to analog ground
VREF2	O	12	Second internal reference voltage	4.7uF capacitor to analog ground
HPOFB	-	25	Headphone reference ground	Headphone ground
CPN1	-	21	First charge pump bucket capacitor	2.2uf capacitor to CPP1
CPP1	-	20	First charge pump bucket capacitor	2.2uf capacitor to CPN1
CPN2	-	18	Second charge pump bucket capacitor	2.2uf capacitor to CPP2
CPP2	-	19	Second charge pump bucket capacitor	2.2uf capacitor to CPN2
				Total: 8 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
MICVDD	P	3	MICBIAS power	3.0V ~ 3.3V (default=3.3V)
AVDD	P	15	Analog power	1.71V ~ 1.9V (default=1.8V)
DACREF	P	10	Analog power	1.71V ~ 1.9V (default=1.8V)
AGND	P	9	Analog ground	
CPVDD	P	23	Charge pump power	1.71V ~ 1.9V (default=1.8V)
CPGND	P	22	Charge pump ground	
CPVEE	P	27	Charge pump negative voltage output	2.2uf capacitor to analog ground
CPVPP	P	24	Charge pump positive voltage output	2.2uf capacitor to analog ground
DCVDD	P	42	Digital core power	1.1V~1.3V (default=open if LDO1_EN is pulled high to DBVDD , or connected to external 1.2V if LDO1_EN is pulled low.)
DBVDD	P	43	Digital I/O power	1.71V~3.3V (default=1.8V)
SPKVDDL	P	2	Speaker AMP power for left channel	3.0V~5.0V (default=5.0V or 3.3V)
SPKVDDR	P	46	Speaker AMP power for right channel	3.0V~5.0V (default=5.0V or 3.3V)
SPKGND/ DGND	P	49*	Speaker AMP ground Digital ground	Exposed-Pad
				Total: 12 Pins

7. Function Description

7.1. Power

There are different power types in ALC3261. DBVDD is for digital I/O power, DCVDD is for digital core power, AVDD/DACREF is for analog power, CPVDD is for charge pump power, MICVDD is for MICBIAS power and SPKVDD is for speaker amplifier power.

The power supplier limit condition are DBVDD ≧ DCVDD and SPKVDD ≧ MICVDD > AVDD = DACREF = CPVDD, AVDD ≧ DCVDD, and for the best performance, our design setting is shown as below.

Table 5. Power Supply for Best Performance

Power	DBVDD	DCVDD	AVDD	DACREF	CPVDD	MICVDD	SPKVDD
Setting	1.8V	1.2V	1.8V	1.8V	1.8V	3.3V	5.0V

To prevent all power down leakage, there are two settings for power supply. At these conditions, the leakage will be smaller. First setting is to power on all power pin. Second setting is to only power on SPKVDD and others are removed. The detail setting is shown as following table.

Table 6. Power Supply Condition for Power Down Leakage

Power	DBVDD	DCVDD	AVDD	DACREF	CPVDD	MICVDD	SPKVDD
Setting-1	Supplied	Supplied	Supplied	Supplied	Supplied	Supplied	Supplied
Setting-2	N/A	N/A	N/A	N/A	N/A	N/A	Supplied

7.2. Power Supply On/Off Sequence

To prevent pop noise or other side effect and make sure function work normally. We recommend power supply on/off sequence as below:

Power On Sequence: (Sequentially turn-on power pins)

1. Pull LDO1_EN pin (Pin#44) to DGND (digital ground)
2. SPKVDD power supply on
3. DCVDD power supply on (This step is required if DCVDD is supplied by external 1.2V power. This step and Step 5 are exclusive.)
4. DBVDD/AVDD/DACREF/CPVDD power supply on
5. Pull LDO1_EN pin (Pin#44) to DBVDD (This step is required if DCVDD is generated by internal LDO. This step and Step 3 are exclusive. If DCVDD is supplied by external 1.2V, LDO1_EN must be pulled low.)
6. MICVDD power supply on (This step is required if MICVDD is supplied by external power)
7. Software starts to initialize ALC3261

Power Off Sequence: (Sequentially turn off power pins)

1. Power down all Codec function (Write 0x0000'h to register MX-00'h)
2. Pull LDO1_EN pin (Pin#44) to DGND (If internal LDO is used to generate DCVDD)
3. MICVDD power supply off (If MICVDD is supplied by external power)
4. DBVDD/AVDD/DACREF/CPVDD power supply off
5. DCVDD power supply off (If DCVDD is supplied by external power)
6. SPKVDD power supply off

7.3. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 7. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write MX-00h	Reset all registers to default values except some specify control registers and logic.

7.3.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC3261 (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 8. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	-	0.8	-	V
V_{POR_OFF}	-	0.52	-	V

Note:
1.V_{POR_OFF} must be below V_{POR_ON}
2. $T^oC = 25^oC$
3. When DCVDD is supplied 1.2V

7.3.2. Software Reset

When MX-00h is wrote, all registers become to default value.

7.4. Clocking

The system clock of ALC3261 can be selected from MCLK or PLL. MCLK is always provided externally while the reference clock of PLL can be selected from MCLK, BCLK1/2. The driver should arrange the clock of each block and setup each divider.

The Clk_sys_i2s1=256*Fs provides clocks into stereo DAC/ADC filter that can be selected from MCLK or PLL. Refer to Figure 5. Audio SYSCLK
The Clk_sys_i2s2=256*Fs provides clocks into mono DAC/ADC filter that can be selected from MCLK, PLL, refer to Figure 5. Audio SYSCLK

When enable ASRC (Asynchronous Sample Rate Converter) function, the clock sources from MCLK and BCLK1 (or BCLK2) are allowed to be asynchronous. The Realtek ASRC technology can ensure data accuracy and keep audio performance under clock source asynchronous.

When ALC3261 at master mode, the clock source from MCLK will be divided and be sent to external device. The ratio of BCLK and LRCK can set by register – MX-73.

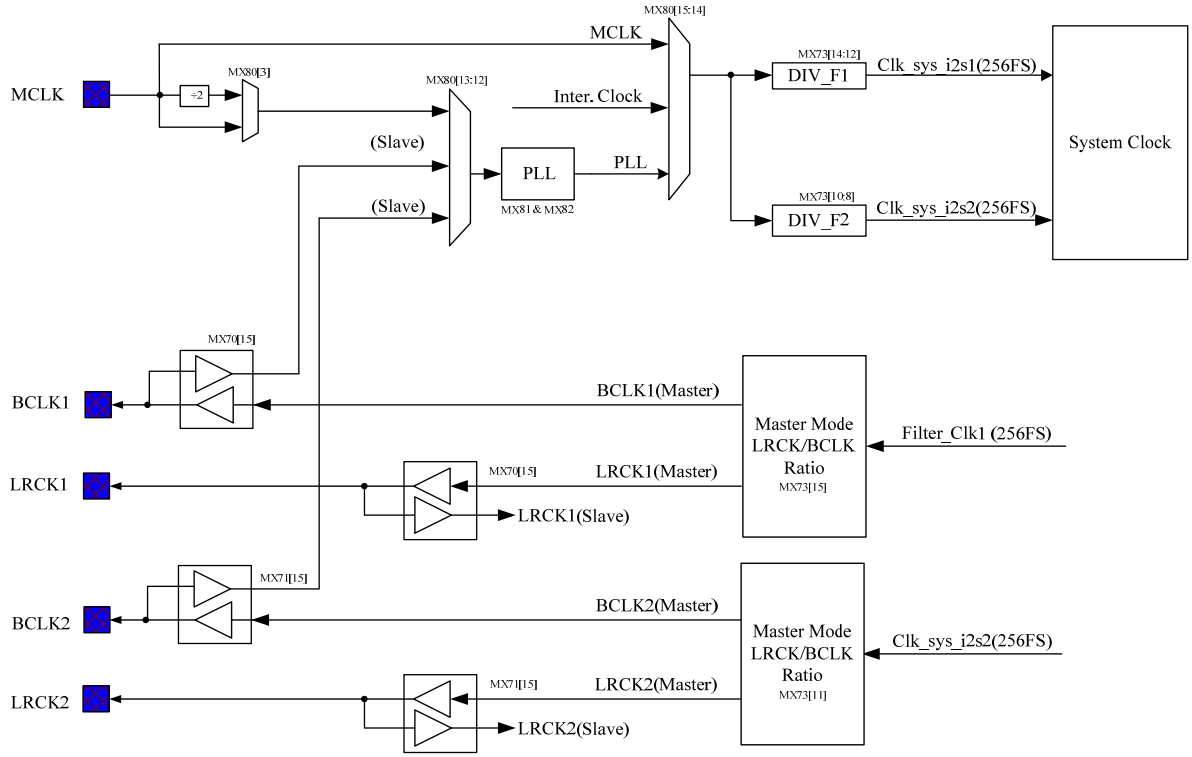


Figure 5. Audio Clock Tree

7.4.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. The source of the PLL can be set to MCLK, BCLK1 or BCLK2 by setting register.

The S/W driver can set up the PLL to output a frequency to match the requirement of system clock.

The PLL transmit formula as below:

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 10. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6
24	39	8	98.4	2	24.6

Table 11. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632
24	62	15	90.352	2	22.588

7.4.2. I²C and Two I²S/PCM Interface

The ALC3261 supports I²C for the digital control interface, and has two I²S/PCM for digital data interface. These two I²S/PCM audio digital interfaces are used to send data to 4 DACs or to receive data from a stereo ADC. These two I²S/PCM audio digital interfaces can be configured to Master mode or Slave mode.

Master Mode

Under master mode, BCLK and LRCK are configured as output. If I2S SYSCLK is selected from MCLK source, sel_sysclk1 (MX-80[15:14]) should set as 00'b. If selected from PLL output, sel_sysclk1 should set as 01'b. PLL's source is suggested to provide frequency from 2.048MHz to 40MHz. The driver should set each divider (MX-73 and MX-89) to arrange the clock distribution. Refer to Figure5. Audio Clock Tree, for details.

Slave Mode

Under slave mode BCLK and LRCK are configured as input. The SYSCLK can be input from MCLK, and BCLK can be synchronous or asynchronous to MCLK. If the SYSCLK is selected from BCLK, the internal PLL should generate 256*FS by BCLK. And the driver should set each divider to arrange the clock distribution. Refer to Figure5. Audio Clock Tree, for details.

7.5. Digital Data Interface

7.5.1. Two I²S/PCM Interface

The two I2S/PCM interface can be configured as master mode or slave mode. Three audio data formats are supported:

- PCM mode
- Left justified mode
- I²S mode

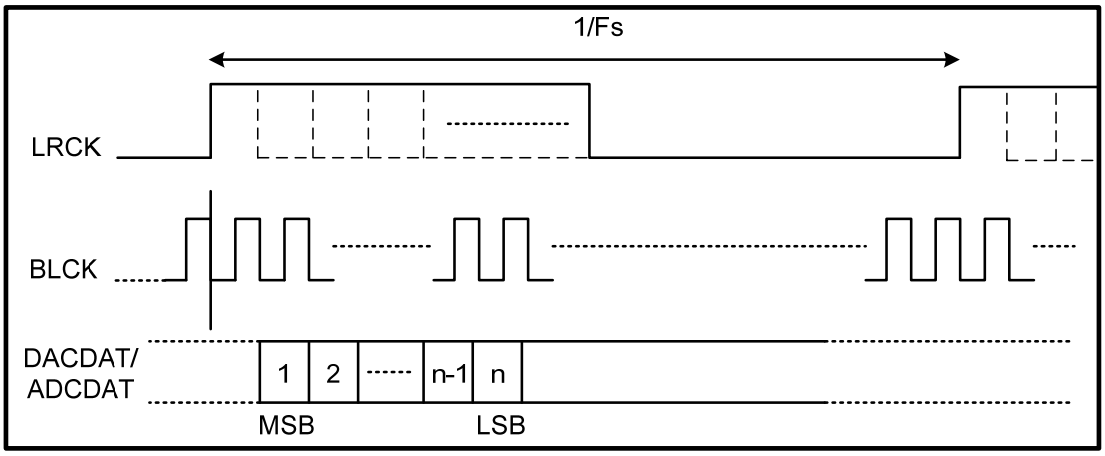


Figure 6. PCM MONO Data Mode A Format (BCLK POLARITY=0)

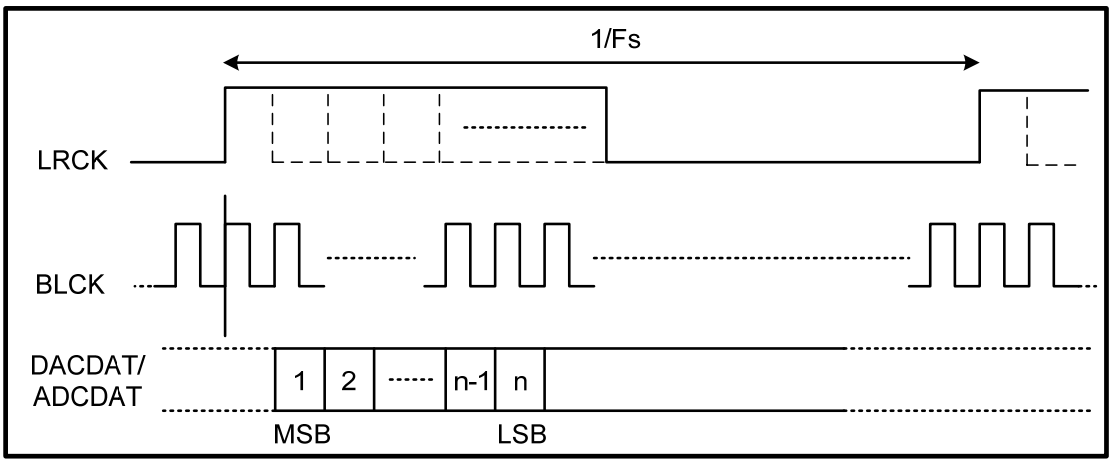


Figure 7. PCM MONO Data Mode A Format (BCLK POLARITY=1)

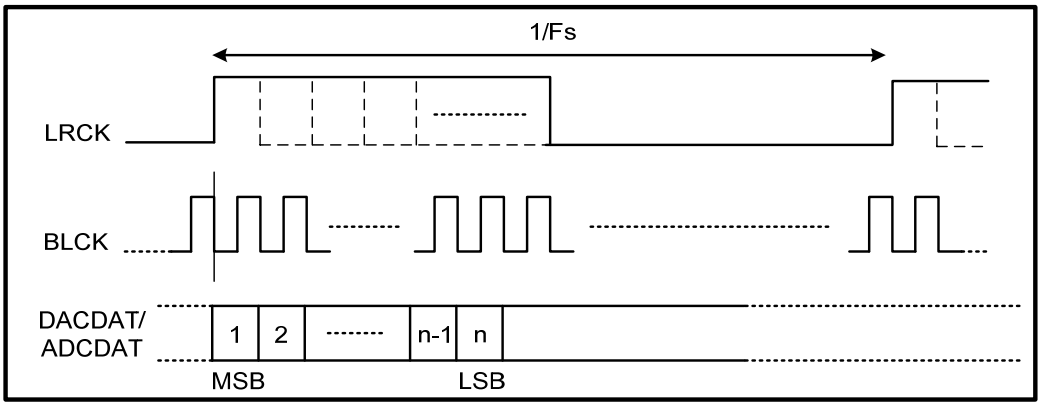


Figure 8. PCM MONO Data Mode B Format (BCLK POLARITY=0)

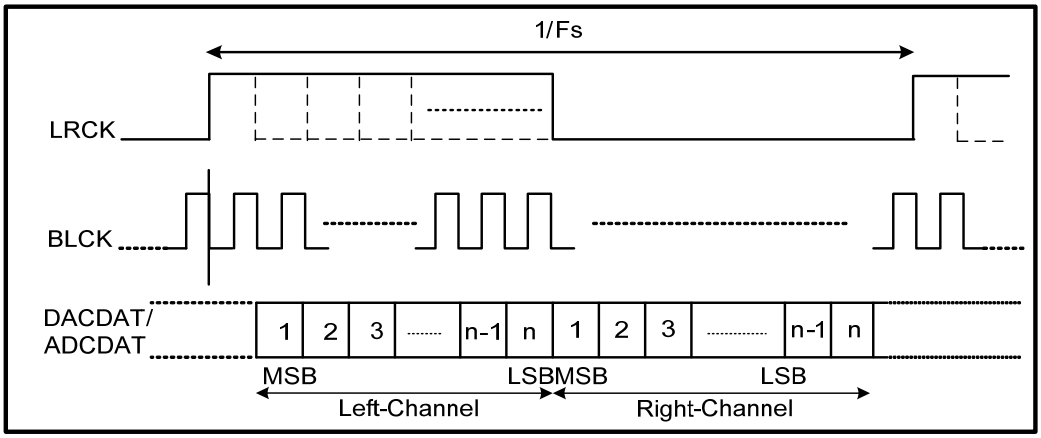


Figure 9. PCM Stereo Data Mode A Format (BCLK POLARITY=0)

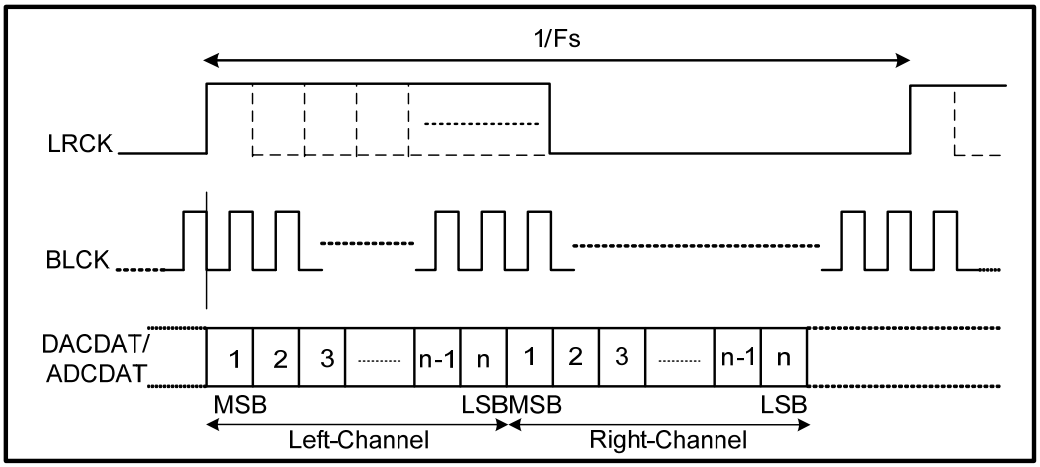


Figure 10. PCM Stereo Data Mode B Format (BCLK POLARITY=0)

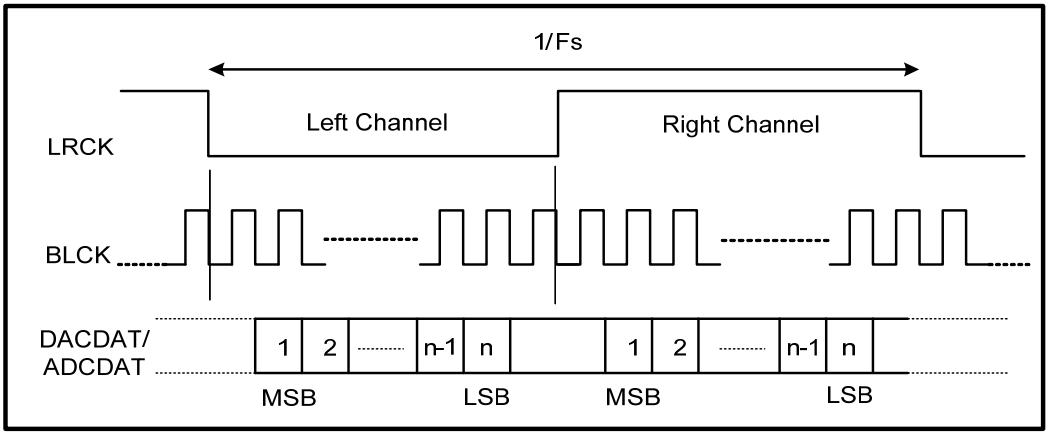


Figure 11. I²S Data Format (BCLK POLARITY=0)

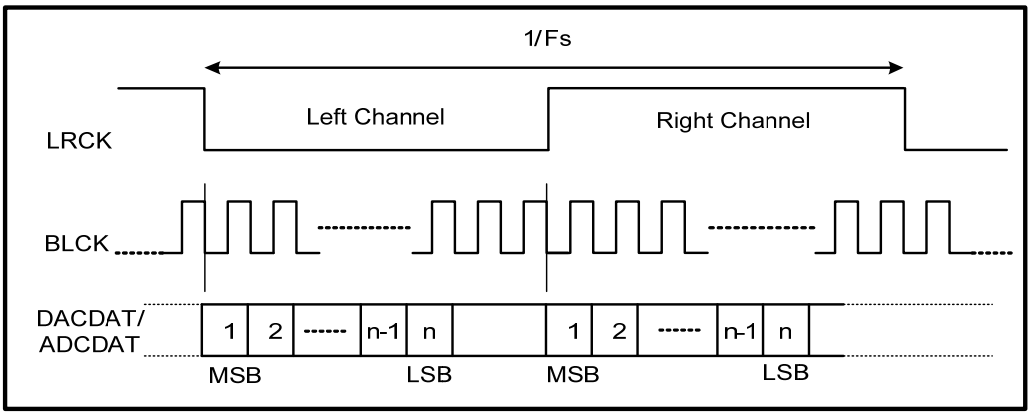


Figure 12. Left-Justified Data Format (BCLK POLARITY=0)

7.6. Audio Data Path

The ALC3261 provides 4-channel analog DACs for playback and 2-channel analog ADCs for recording.

7.6.1. 2 Analog ADCs with 4-Channel Record Path

There are two analog ADCs and with up to 4-channel recording path. You can use two analog microphones pass to analog ADCs and two digital microphones to reach 4-channel recording. Or use two digital microphone interfaces to reach 4-channel recording. These 4-channel data need to pass to 2-I2S interface, maybe two channels for one I2S interface or mono channel for one I2S interface.

The full scale input of analog ADC is around 0.55Vrms. In order to save power, the left and right analog ADC can be powered down separately by setting pow_adc_l (MX-61[2]) and pow_adc_r (MX-61[1]). And the volume control of the stereo ADC is also separately controlled by ad_gain_l (MX-1C[14:8]) and ad_gain_r (MX-1C[6:0]).

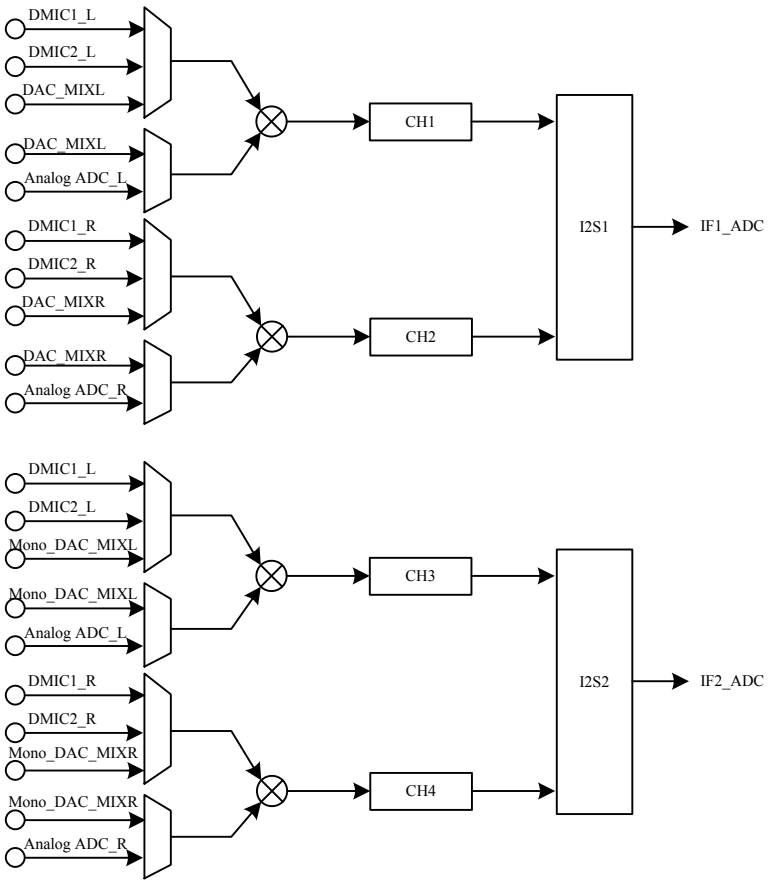


Figure 13. 4-Channel Recording Path

7.6.2. 4 DACs with 4-Channel Playback Path

There are four analog DACs and with up to 4-channel playback path. Two I2S interfaces provide four channels data to analog DACs. And analog DAC can output audio signal to speaker output, headphone output, mono output or line output.

The full scale output of analog DAC is around 1Vrms at line output port. In order to save power, the four analog DACs can be powered down separately by setting pow_dac_l_1 (MX-61[12]), pow_dac_r_1 (MX-61[11]), pow_dac_l_2 (MX-61[7]) and pow_dac_r_2 (MX-61[6]). And the digital volume control of the four DACs are also separately controlled by vol_dac1_l (MX-19[15:8]), vol_dac1_r (MX-19[7:0]), vol_mono_dacl (MX-1A[15:8] and vol_mono_dacr (MX-1A[7:0]).

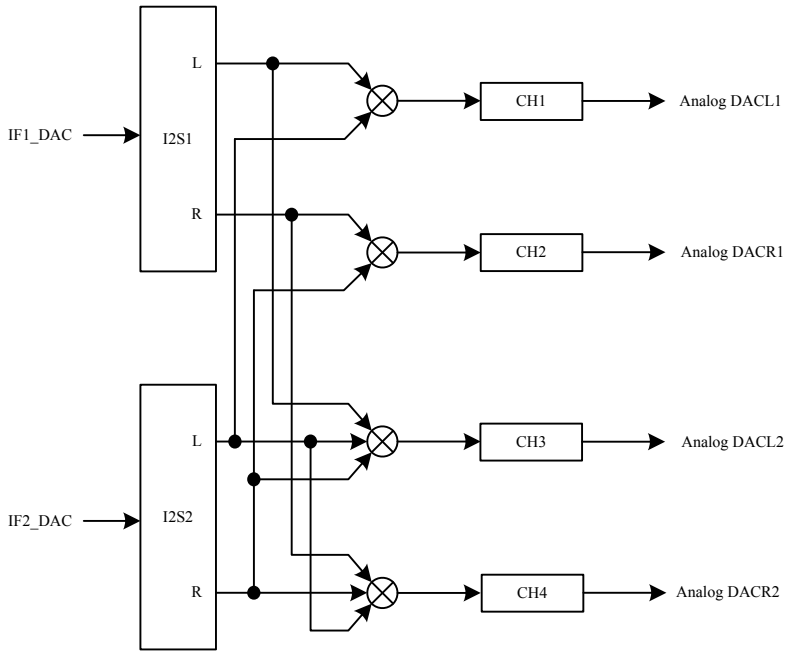


Figure 14. 4-Channel Playback Path

7.6.3. Mixers

The ALC3261 has digital and analog mixers build-in.

- **Output mixer - OUTMIXL/R**

  The stereo analog mixer can do mixing for DAC output and analog input. The mixer output is mainly for headphone output and line output. Each input path has it's mute control to the mixer block in MX-4D ~ MX-52. pow_outmixl and pow_outmixr can be used to power on/off OUTMIXL/R

- **Speaker mixer – SPKMIXL/R**

  The stereo analog mixer can do mixing for OUTMIX output, DAC output and analog input. The mixer output is for speaker output. Each input path has it's mute control to the mixer block in MX-46 and MX-47. pow_spkmixl and pow_spkmixr can be used to power on/off SPKMIXL/R.

- **Speaker_Out mixer – SPOMIXL/R**

  The stereo analog mixer can do mixing for from speaker volume, DAC and analog input. The mixer output is direct to speaker output. Each input path has it's mute control to the mixer block in MX-48 and MX-49.

- **LINE_Out mixer – LOUTMIX**

  The stereo analog mixer can do mixing for analog input and DAC output. The mixer output is for line-out output for drive external amplifier. Each input has individual mute control to the mixer block in MX-53. pow_lout can be used to power on/off LOUTMIX.

- **Record mixer – RECMIXL/R**

  The stereo analog mixer can do mixing for analog input and OUTMIX output. The mixer output is for ADC input. Each input path has it's mute control to the mixer block in MX-3B ~ MX-3E. pow_recmixl and pow_recmixr can be used to power on/off RECMIXL/R.

- **HP mixer – HPOMIXL/R**

  The stereo analog mixer can do mixing for headphone volume and DAC output. The mixer output directly output to external headphone device. Each input path has it's mute control to the mixer block in MX-45.

- **Digital mixer**

  There are ten digital mixers in ALC3261. Four digital mixers are assigned for ADC recording. These four mixers can mix analog line input, analog microphone input and digital microphone input then output to I2S interface to other device. Another four digital mixers are assigned DAC playback. These mixers can mix digital data from I2S interface or ADC data from external analog signal. The mixed data is output to analog DAC and output port to drive external device. The other two mixers are use for DA-AD processing. The incoming data from two I2S interfaces (DACDAT) uses these two mixers to do mixing and output to I2S interface (ADCDAT).

7.7. Analog Audio Input Port

The ALC3261 has two types analog input ports: microphone input and line input.

- **IN1P/N**

  The IN1P/N is a microphone type input port. The input port can be configured to differential input or single-ended input by MX-0D[7]. The microphone input port has its microphone bias and microphone boost. The low noise microphone bias can improve recording performance and enhance recording quality. Build-in short current detection scheme can be used for switch detection. Multi-steps microphone boost gain set by sel_bst1 (MX-0D[15:12]) is easy to use for microphone application. Pow_bst1 can be used to power down the MIC1 boost and pow_micbias1 can be used to power down the microphone bias 1.

- **IN2P/N**

  The IN2P/N is a dual type input port: microphone input and line input. Microphone input can be configured to differential input or single-ended input by MX-0E[6]. Multi-steps microphone boost gain set by sel_bst2 (MX-0E[11:8]) is easy to use for microphone application. Pow_bst2 can be used to power down the MIC2 boost. As line input, it has volume control for tuning by MX-0F[12:8] and MX-0F[4:0].

- **IN3P/N**

  The IN3P/N is a microphone input. The microphone input can be configured to differential input or single-ended input by MX-0D[6]. Multi-steps microphone boost gain set by sel_bst3 (MX-0D[11:8]) is easy to use for microphone application. Pow_bst3 can be used to power down the MIC3 boost.

7.8. Analog Audio Output Port

The ALC3261 supports four type output ports:

- **SPO_L/R_P/N**

  The speaker output of ALC3261 is a stereo BTL output with Class-D type amplifier.
  The power of speaker amplifier is an individual power pin and higher than AVDD. So the input and output of speaker amplifier has a gain ratio to enlarge or reduce the income analog signal. The gain ratio setting can be controlled by fbgain_clsd (MX-8D[15:12]).
  The input source of the speaker output port can be selected from analog input, SPKVOL, DAC output by setting MX-48/49.
  The front stage of speaker output has gain control and volume control. For gain control, the range is from 0dB to -9dB and controlled by MX-46/47. For volume control, the range is from +12dB to -46.5dB with 1.5dB/step controlled by MX-01.
  The pow_spo_voll (MX-66[15]) and pow_spo_volr (MX-66[14]) can be used to power on/off SPKVOLL and SPKVOLR. The pow_clsd (MX-61[0]) can be used to power on/off SPO_L/R_P/N.

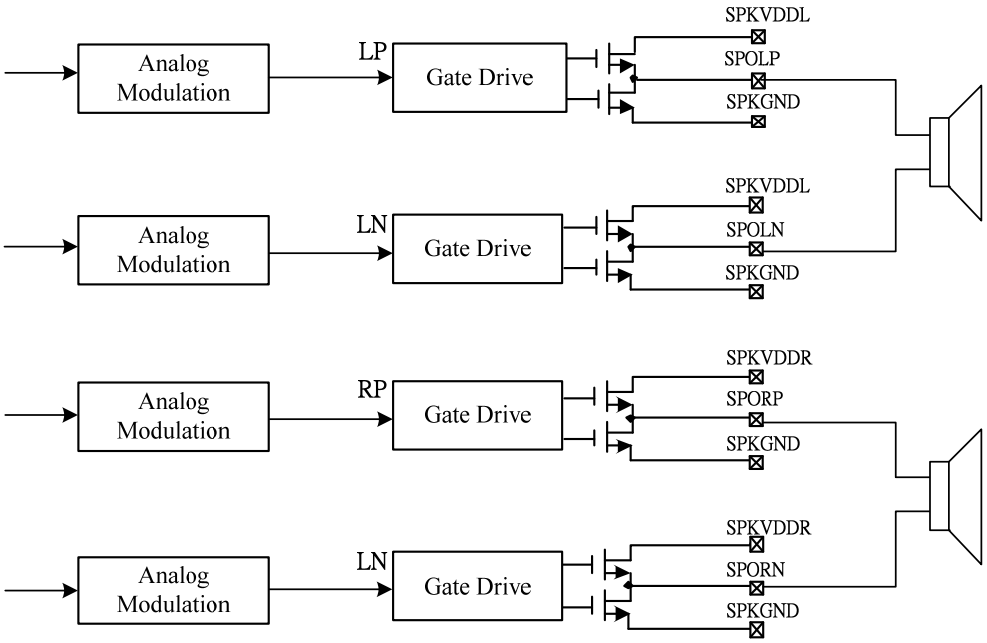


Figure 15. Speaker Output Mode – Stereo Mode

- **HPO_L/R**

  The headphone output of ALC3261 is a stereo output with cap-free type headphone amplifier. It does not need to connect external capacitor and can connect to earphone device directly. The headphone output source can mix from output mixer (OUTMIX) or DAC by setting MX-45. The front stage of headphone output has volume control and gain control. The volume range is from +12dB to -46.5dB with 1.5dB/step by MX-02.
  En_l_hp and en_r_hp (MX-63[7/6]) can be used to power on/off Headphone Amplifier, and pow_hpo_voll and pow_hpo_volr (MX-66[11/10]) can be used to power on/off headphone volume control. In addition, pow_pump_hp (MX-8E[3]) can be used to power on/off charge pump circuit for Headphone Amplifier.

- **MONO_P/N**

  The mono output is a differential output with Class-AB type amplifier. The mono output source can be mixed from analog input, OUTVOL and DAC output by setting MX-4C[15:11]. The front stage of mono output has gain control for attenuation, the gain control is 0dB or -6dB by MX-4C[10].

- **Line_OUT_L/R**

  The output type is line type output. The output is a stereo single ended output. The input can be selected from OUTVOL or DAC output by setting MX-53[15:12]. The front stage of LOUT output has gain control for attenuation. The gain control is 0dB or -6dB by MX-53[11].

7.9. DRC and AGC Function

The Dynamic Range Controller (DRC) dynamically adjusts the input signal and let the output signal achieve the target level. The ALC3261 supports playback DRC for DAC path, and the DRC can also be used as AGC(Auto Gain Controller) for ADC path. The control register is at MX-B4[15:14]. The function block is shown as below. The signal input pass through the Pre-Gain first, then DRC volume and Post-Gain then output. The Pre-Gain is use to enlarge the input signal. The DRC volume is use to attenuate the signal after detected by DRC. The Post-Gain is use to fine tune the signal after pass DRC tuning.

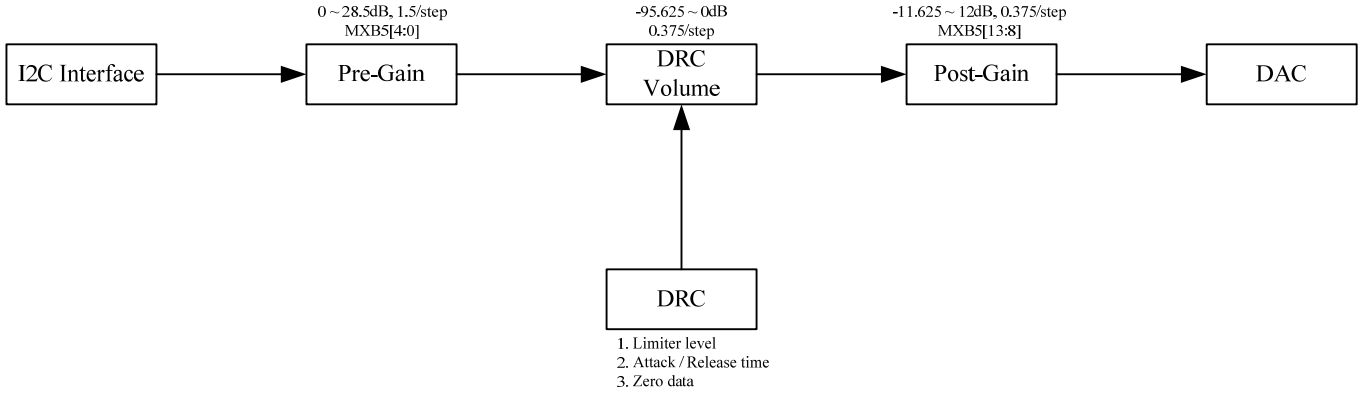


Figure 16. DAC DRC Function Block

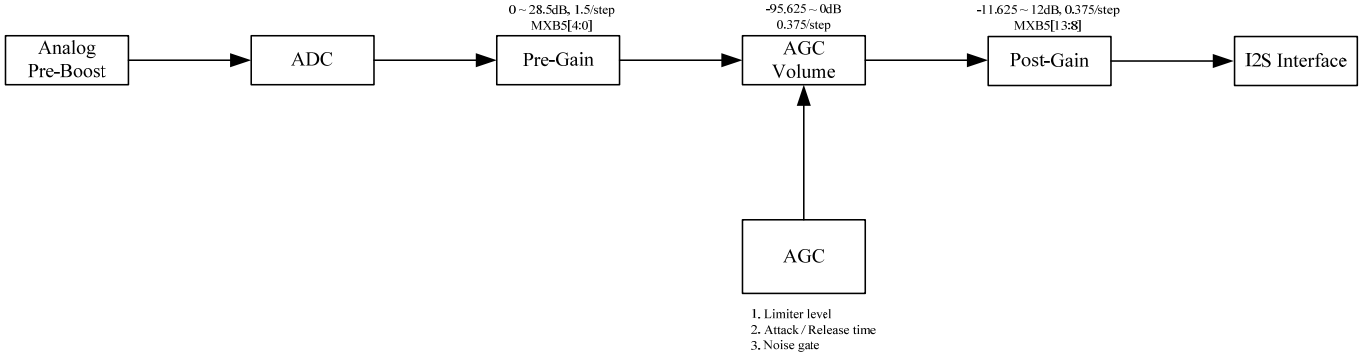


Figure 17. ADC AGC Function Block

Playback/Recording Mode:

For DAC playback or ADC recording mode, when the input signal exceeds target threshold, the signal will decrease "DRC/AGC Digital Volume" (0.375dB/step at every zero-crossing) until drop to target level then keep the digital volume. When input signal is below the target threshold, the signal will step-up "DRC/AGC Digital Volume" (0.375dB/step every zero-crossing) until return to original level. If want to return to the target level, need to set the pre-gain to achieve.

Fine tune parameters:

- Limiter Threshold: 0 ~ -46.5dB, 1.5dB/step, MX-B6[11:7]
- Attack Rate: T=(4*2^n)/sample rate, n = MX-B4[12:8]
- Recovery Rate: T=(4*2^n)/sample rate, n = MX-B4[4:0]

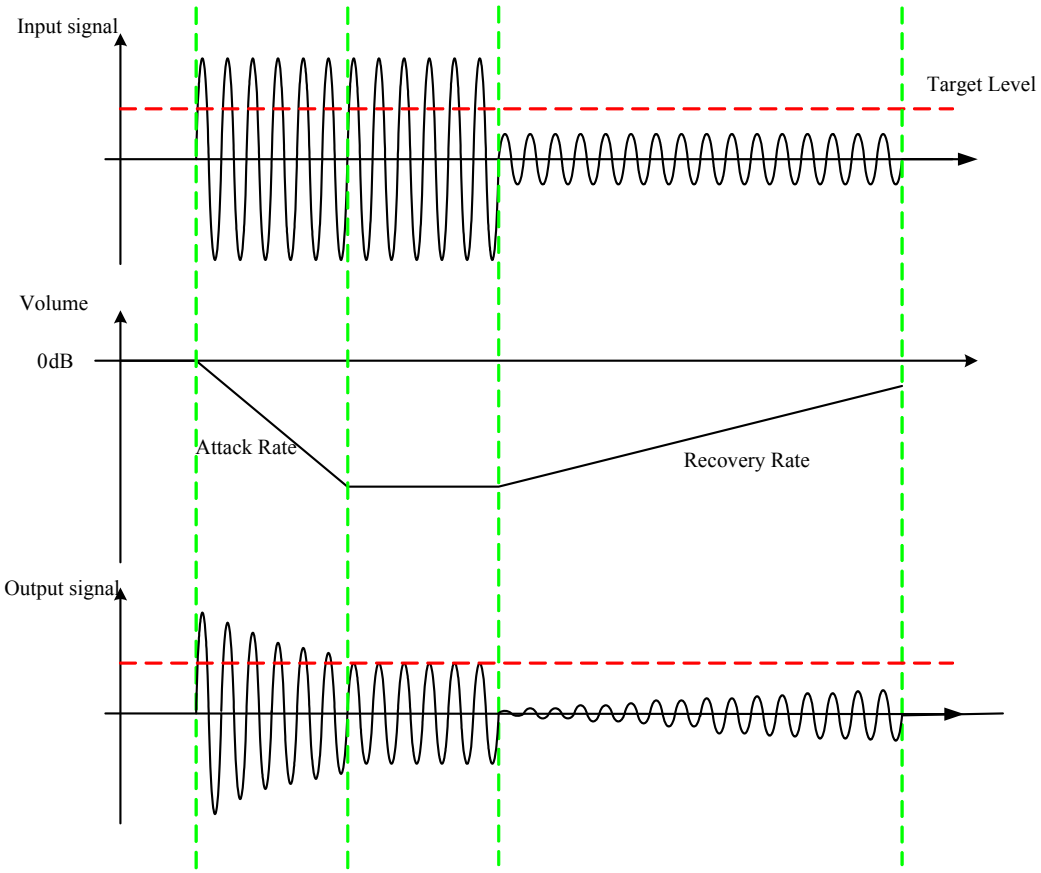


Figure 18. DRC/AGC for Playback/Recording Mode

Noise Gate Mode:

The Noise Gate Function is use to reduce the noise floor for DAC path or ADC path. When input signal is below noise gate level, the input signal will be reduced by DRC/AGC volume in order to suppress the background noise. The reducing level can be set by register. And when input signal is above noise gate, the input signal will be boosted to target level.

Fine tune parameters:

- Noise Gate Threshold: -36 ~ -82.5dB, 1.5dB/step, MX-B6[4:0]
- Noise Gate Attack Rate: T=(4*2^n)/sample rate, n = PR-06[4:0]
- Noise Gate Recovery Rate: T=(4*2^n)/sample rate, n = PR-02[12:8]
- Reducing Noise Level: 0 ~ 45dB, 3dB/step, MX-B6[15:12]

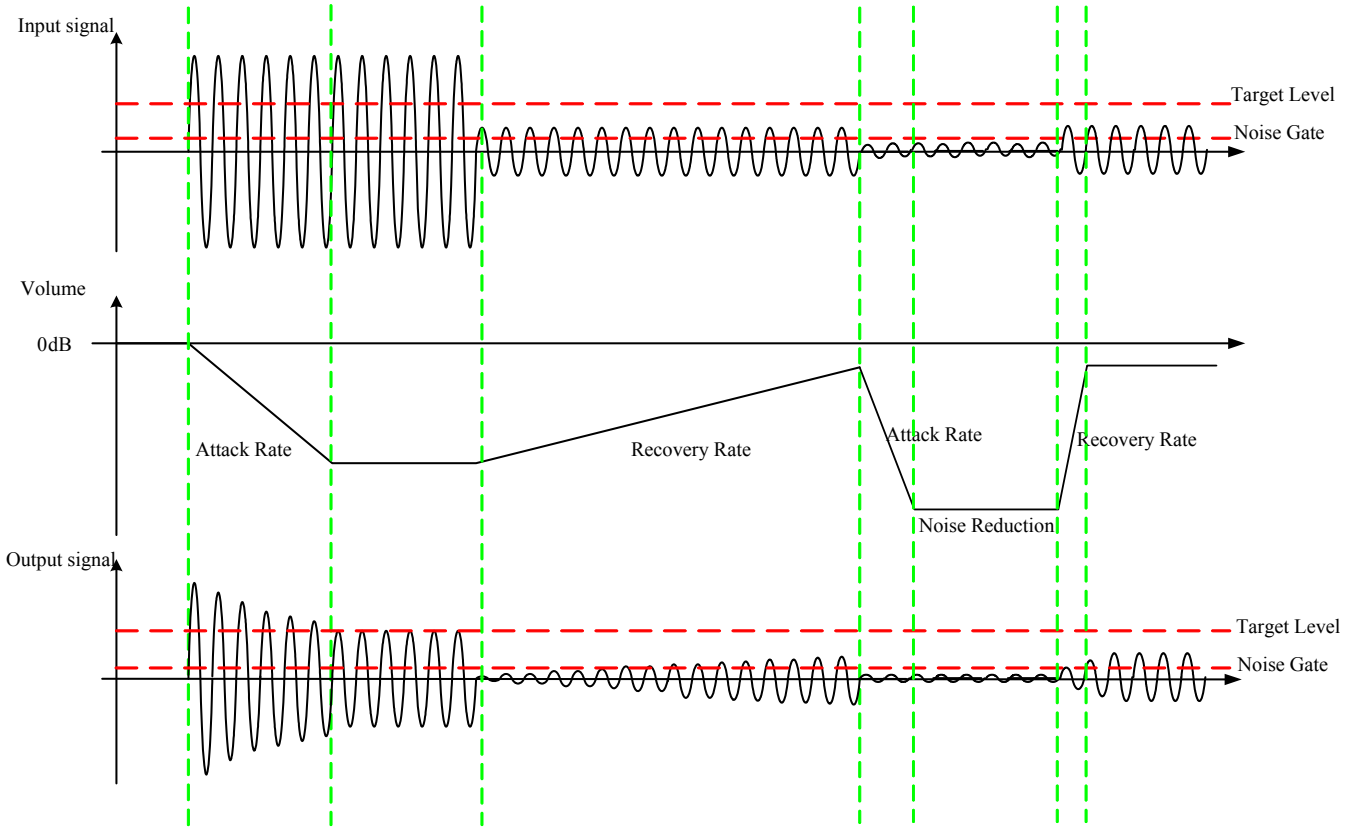


Figure 19. DRC/AGC for Noise Gate Mode

7.10. Speaker Amplifier Ratio Gain

Owing to speaker power (SPKVDD) and analog power (AVDD) are under different power domain. And normally the speaker power is higher than analog power. So the audio input signal needs to be boosted or reduced by a gain then output from speaker amplifier. When SPKVDD is dropping, the gain needs to be reduced to prevent the signal is clipping. And when SPKVDD is rising, the gain need to be boosted to prevent the signal is too small.

Table 12. Ration Gain Table for SPKVDD and AVDD

	AVDD = 1.8V	AC + DC Ratio Gain	Register Setting MX-8D[15:12]
SPKVDD	3.0 V	1.94	0000'b, 1.94x
	3.3 V	2.0	0001'b, 2.00x
	3.5 V	2.11	0010'b, 2.11x
	3.6 V	2.22	0011'b, 2.20x
	3.8 V	2.33	0100'b, 2.33x
	4.0 V	2.44	0101'b, 2.44x
	4.2 V	2.55	0110'b, 2.55x
	4.4 V	2.66	0111'b, 2.66x
	4.6 V	2.77	1000'b, 2.77x
	4.8 V	3.0	1001'b, 3.00x
	5.0 V	3.3	1010'b, 3.30x

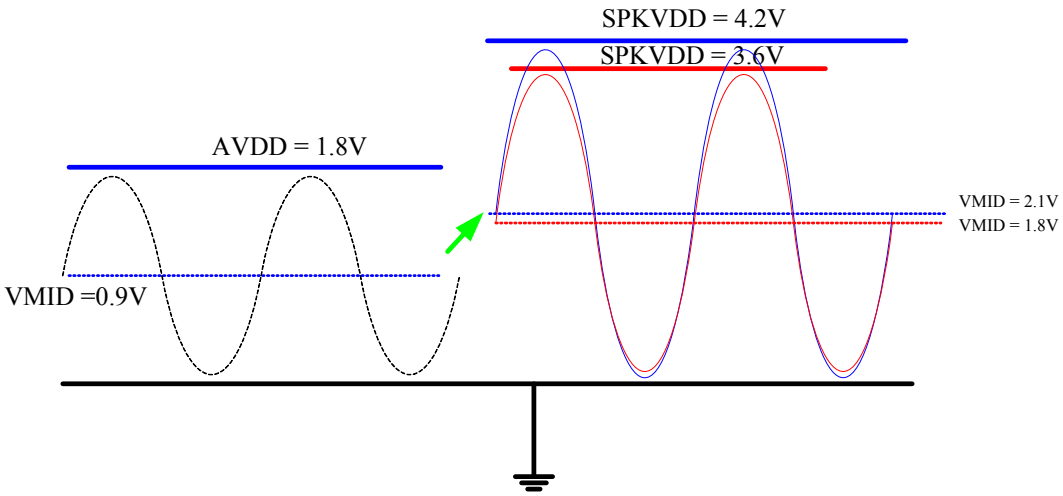


Figure 20. Ratio Gain Behavior for SPKVDD and AVDD

7.11. Equalizer Block

The equalizer block cascades 7 bands of equalizer to tailor the frequency characteristics of embedded speaker system according to user preferences and to emulate environment sound. The 7 bands equalizer includes two high pass filter, four band pass filter and one low pass filter. One high pass filter cascaded in the front end is used to drop low frequency tone, The tone has a large amplitude and may damage a mini speaker. The high pass filter can be used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength. Four bands of bi-quad band pass filters are used to emulate environment sounds, e.g., 'Pub', 'Live', 'Rock',… etc.. The gain, center frequency and bandwidth of each filter are all programmable.

7.12. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400KHz rate and SDA data is a open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

7.12.1. Address Setting

Table 14. Address Setting (0x38h)

(MSB)			BIT				(LSB)
0	0	1	1	1	0	0	R/W

7.12.2. Complete Data Transfer

Data Transfer over I²C Control Interface

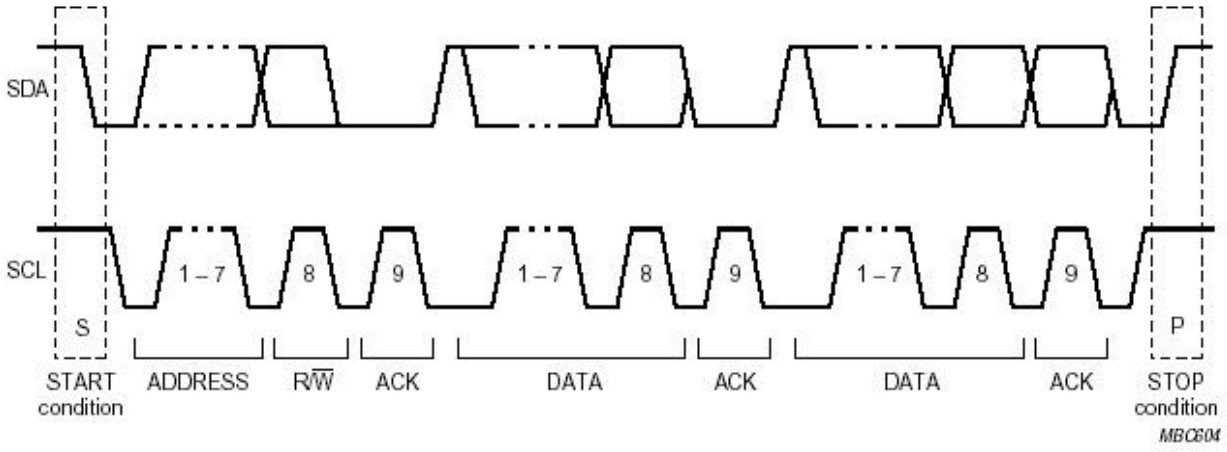
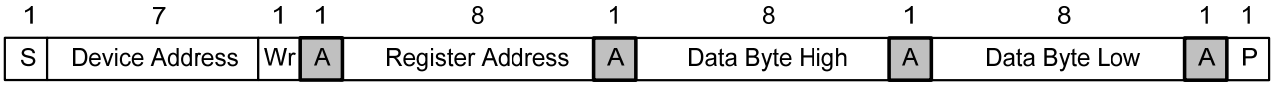


Figure 21. Data Transfer Over I²C Control Interface

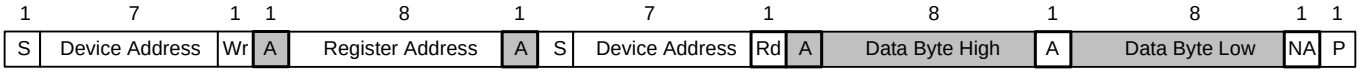
Write WORD Protocol

Table 15. Write WORD Protocol



Read WORD Protocol

Table 16. Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

7.13. GPIO, Interrupt and Jack Detection

The ALC3261 supports two GPIOs – GPIO1/GPIO2. These two GPIOs are multi-function pins. GPIO1 can be configured to GPIO or IRQ output by MX-C0[15]. GPIO2 can be configured to GPIO or DMIC clock output by MX-C0[14]. These two GPIOs can also be configured to jack detection pins. For jack detection purpose, it needs switch GPIO to input pin. Basically, ALC3261 has dedicated jack detection pins – JD1 and JD2. The JD1 and JD2 share pins with IN1N and IN2N.

For GPIO function, the GPIO can be configured to input or output. For input type, the internal circuit can read pin status and report to register table. For output type, the internal circuit can drive this pin to high or low to control external device. In GPIO function, the pin polarity can be controlled by register at output type.

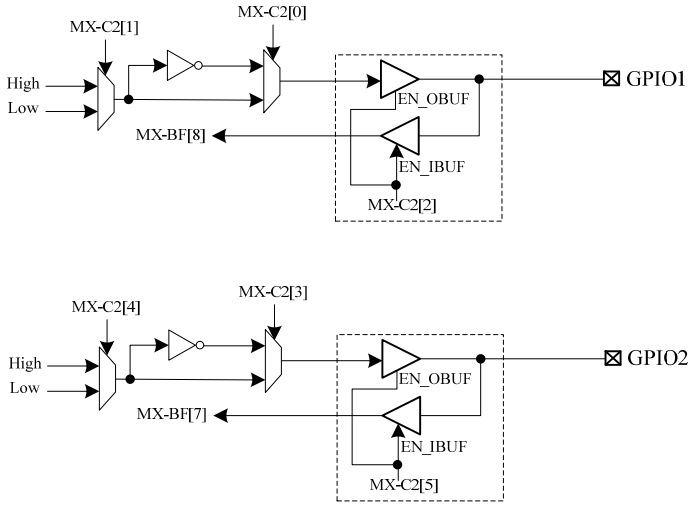


Figure 22. GPIO Function Block

For IRQ function, the IRQ output source can be selected from JD Status, JD2 Status, Over-Temperature Status and MICBIAS1 Over-Current Status. When either status is trigged, the GPIO will output a flag as interrupt signal.

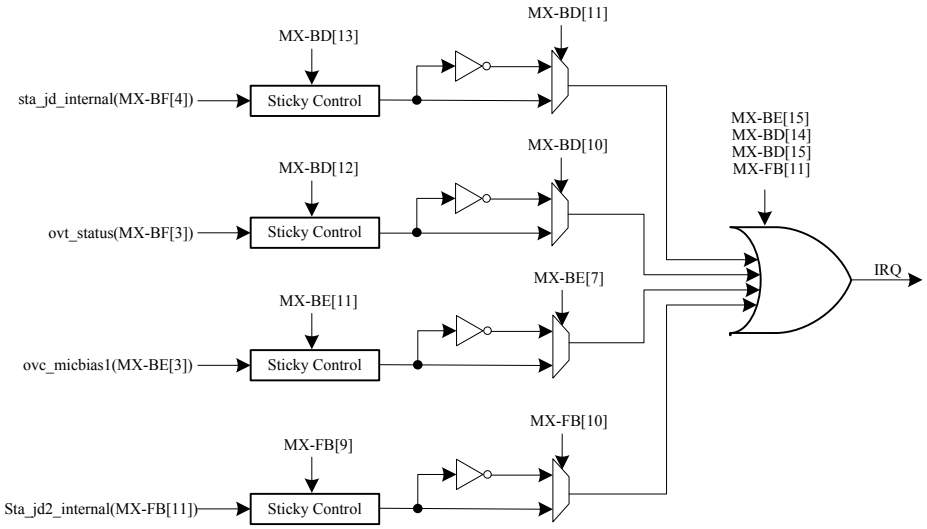


Figure 23. IRQ Function Block

For jack detection function, there are four pins to be jack detect pins, GPIO1, GPIO2, JD1 (share with IN1N) and JD2 (share with IN2N). The jack detect function can be used to turn-on or turn-off the related output ports. When jack detect pin is trigged, the selected output ports will be turn-on or turn-off.

The MICBIAS supports short detection function. When MICBIAS circuit is short, MICBIAS circuit will generate an over-current flag. The flag can generate an interrupt signal to notice host and let S/W do follow-up processings.

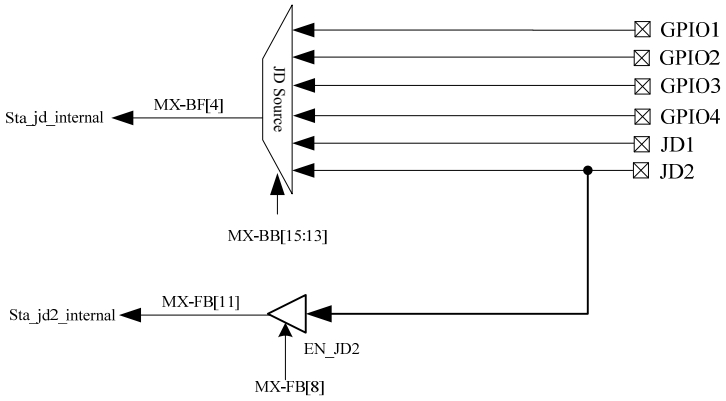


Figure 24. JD Source Selection

7.14. Power Management

ALC3261 detailed Power Management control registers are supported in MX-61h, 62h, 63h, 64h and 65h. Each particular block will only be active when each bit MX-61h, 62h, 63h, 64h, and 65h is set to enable.

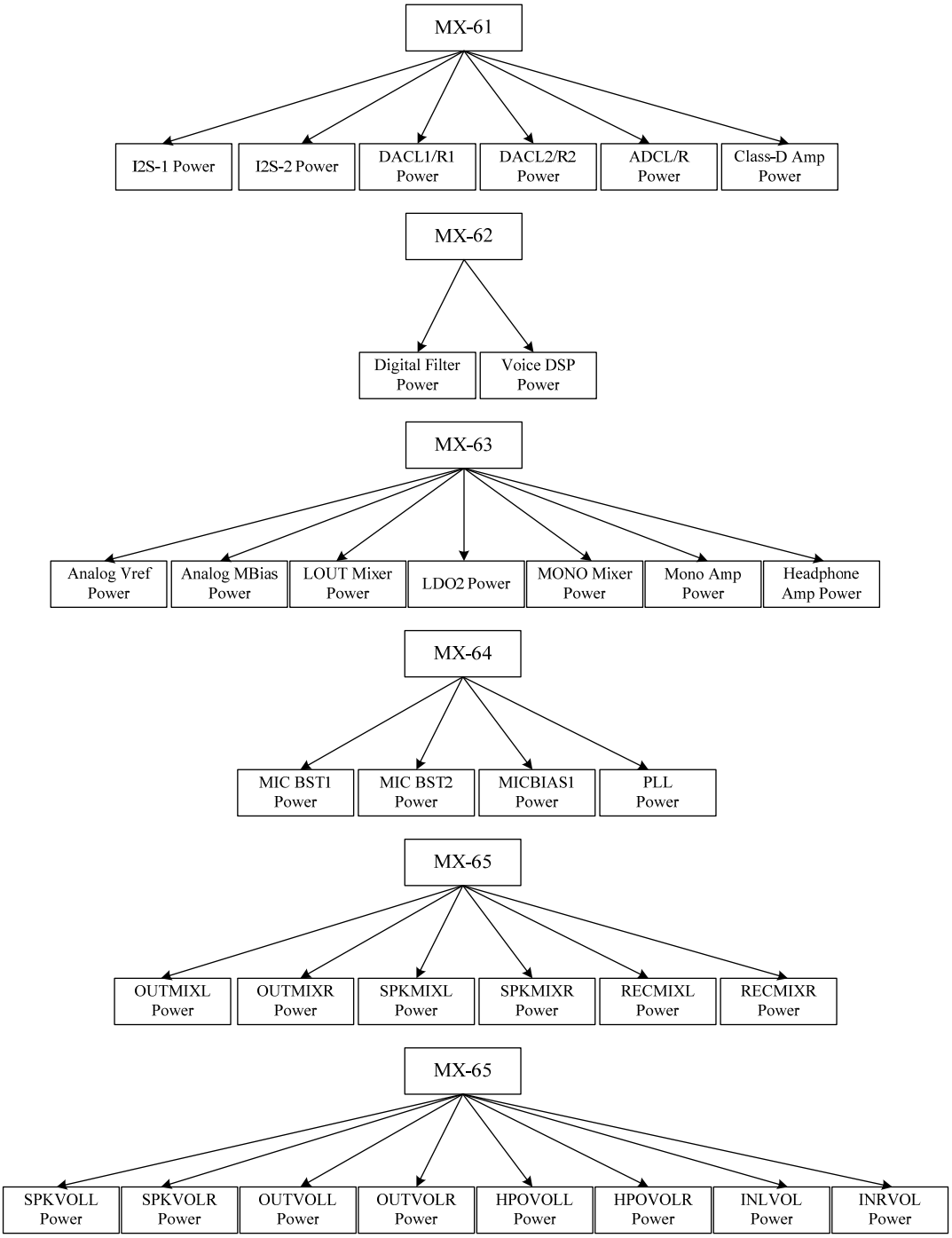


Figure 25. Power Management

7.15. Programmable Register Array

The Programmable Register Array is used for continuing executing register set by one register command. These registers are need to program first. There are 16-sequences register settings can be set. For each sequence, can fill in MX type registers, PR type register or time delay (100us ~ 100ms). These 16-sequences registers can be divided to two sequencers. The start point and end point for each sequencer can be set from sequence-0 to sequence-15. For example, you can program sequencer-1 to execute sequence-0 to sequence-10 and sequencer-2 to execute sequence-11 to sequence-15 or program sequencer-1 to execute sequence -6 to sequence -15 and sequencer-2 to execute sequence -0 to sequence -5.

The Table 17 shown as programmable register table with two sequencers.

Table 17. Programmable Register Table

Sequencer (1-bit)		Sequences (4-bit)	Delay Time (8-bit)	Register Level (1-bit)	Register Index (8-bit)	Register Data (16-bit)
1	Start	0000'b	-	x	xx	xxxx
	-	0001'b	xx	-	-	-
	-	0010'b	-	x	xx	xxxx
	-	0011'b	xx	-	-	-
	-	0100'b	-	x	xx	xxxx
	-	0101'b	xx	-	-	-
	End	0110'b	-	x	xx	xxxx
2	Start	0111'b	xx	-	-	-
	-	1000'b	-	x	xx	xxxx
	-	1001'b	xx	-	-	-
	-	1010'b	-	x	xx	xxxx
	-	1011'b	xx	-	-	-
	-	1100'b	-	x	xx	xxxx
	-	1101'b	xx	-	-	-
	-	1110'b	-	x	xx	xxxx
	End	1111'b	xx	-	-	-

Settings Procedures:

1. Set Programmable Register Table
   => Set register level (MX-C8[9])/register index (MX-C8[7:0])/register data (MX-C9) for each sequence (MX-C8[15:12])
   => Set delay time (MX-CA[15:8]) for each sequence (MX-C8[15:12])
   => Set start point (MX-CB[11:8]/MX-CC[11:8]) and end point (MX-CB[3:0]/MX-CC[3:0]) for each sequencer
2. Enable Programmable Register Function (MX-CA[7])
3. Execute Sequencer-1/2
   => Sequencer-1 (MX-CA[6])
   => Sequencer-2 (MX-CA[5])
4. Check Sequencer-1/2 finished or not?
   => Sequencer-1 (MX-C8[11])

=> Sequencer-2 (MX-C8[10])

8. Registers List

ALC3261 register map as shown as following and accessing unimplemented registers, will return a 0.

8.1. Register Map

Table 18. Register Map

Type	Name	Description	Register Address	Reset State
Reset	S/W Reset	S/W Reset & Device ID	MX-00h	0x0006'h
I/O	SPKOUT	Speaker Output Volume & Mute/Un-Mute	MX-01h	0xC8C8'h
	HPOUT	Headphone Output Volume & Mute/Un-Mute	MX-02h	0xC8C8'h
	LOUT	Line Output Volume & Mute/Un-Mute	MX-03h	0xC8C8'h
	MONOOUT	MONO Output Mute/Un-Mute	MX-04h	0x8000'h
	IN1	IN1 Mode and Gain Boost Control	MX-0Dh	0x0000'h
	IN2	IN2 Mode and Gain Boost Control	MX-0Eh	0x0000'h
	INL/INR	INL/INR Volume Control	MX-0Fh	0x0808'h
Digital Gain/Volume	DACL1/R1	DACL1/R1 Digital Volume Control	MX-19h	0xAFAF'h
	DACL2/R2-1	DACL2/R2 Digital Volume Control	MX-1Ah	0xAFAF'h
	DACL2/R2-2	DACL2/R2 Digital Mute/Un-Mute Control	MX-1Bh	0x0000'h
	ADCL/R-1	ADCL/R Digital Volume & Mute/Un-Mute Control	MX-1Ch	0x2F2F'h
	ADCL/R-2	ADCL/R Digital Path Volume Control	MX-1Dh	0x2F2F'h
	ADCL/R-3	ADC Boost Gain for DMIC	MX-1Eh	0x0000'h
Digital Mixer	ADC-1	ADC Stereo Digital Mixer Control	MX-27h	0x7060'h
	ADC-2	ADC Mono Digital Mixer Control	MX-28h	0x7070'h
	ADC-3	ADC to DAC Digital Mixer Control	MX-29h	0x8080'h
	DAC-1	DAC Stereo Digital Mixer Control	MX-2Ah	0x5454'h
	DAC-2	DAC Mono Digital Mixer Control	MX-2Bh	0x5454'h
	DAC-3	DAC Stereo to Mono Mixer Control	MX-2Ch	0xAA00'h
	Voice DSP-1	Voice DSP Path Control-1	MX-2Dh	0x0000'h
	Voice DSP-2	Voice DSP Path Control-2	MX-2Eh	0xA000'h
	Copy Mode	ADC/DAC Data Copy Mode Control	MX-2Fh	0x0000'h
Input Mixer	RECMIXL-1	RECMIXL Gain Control	MX-3Bh	0x0000'h
	RECMIXL-2	RECMIXL Gain & Selection Control	MX-3Ch	0x007F'h
	RECMIXR-1	RECMIXR Gain Control	MX-3Dh	0x0000'h
	RECMIXR-2	RECMIXR Gain & Selection Control	MX-3Eh	0x007F'h
Output Mixer	HPOMIX	HPOMIX Gain & Selection Control	MX-45h	0xE000'h
	SPKMIXL	SPKMIXL Gain & Selection Control	MX-46h	0x003E'h
	SPKMIXR	SPKMIXR Gain & Selection Control	MX-47h	0x003E'h
	SPOMIXL	SPOMIXL Selection Comtrol	MX-48h	0xF800'h
	SPOMIXR	SPOMIXR Selection Control	MX-49h	0x3800'h
	SPOMIXL/R	SPOMIXL/R Gain Control	MX-4Ah	0x0004'h
	MONOMIX	MONOMIX Gain & Selection Control	MX-4Ch	0xFC00'h
	OUTMIXL-1	OUTMIXL Gain Control-1	MX-4Dh	0x0000'h
	OUTMIXL-2	OUTMIXL Gain Control-2	MX-4Eh	0x0000'h
	OUTMIXL-3	OUTMIXL Selection Control	MX-4Fh	0x01FF'h
	OUTMIXR-1	OUTMIXR Gain Control-1	MX-50h	0x0000'h
	OUTMIXR-2	OUTMIXR Gain Control-2	MX-51h	0x0000'h
	OUTMIXR-3	OUTMIXR Selection Control	MX-52h	0x01FF'h
	LOUTMIX	LOUTMIX Gain & Selection Control	MX-53h	0xF000'h

Type	Name	Description	Register Address	Reset State
Power Management	Management-1	I2S & DAC & ADC & Class-D Power Control	MX-61h	0x0000'h
	Management-2	Digital Filter Power Control	MX-62h	0x0000'h
	Management-3	VREF & MBias & LOUTMIX & Mono & HP & LDO2 Power Control	MX-63h	0x00C0'h
	Management-4	MICBST & MICBIAS Power Control	MX-64h	0x0000'h
	Management-5	OUTMIX & SPKMIX & RECMIX Power Control	MX-65h	0x0000'h
	Management-6	SPOVOL & OUTVOL & HPOVOL & INVOL Power Control	MX-66h	0x0000'h
PR Register	PR Index	PR Register Index	MX-6Ah	0x0000'h
	PR Data	PR Register Data	Mx-6Ch	0x0000'h
Digital Interface	I2S1 Port Ctrl	I2S-1 Interface Control	MX-70h	0x8000'h
	I2S2 Port Ctrl	I2S-2 Interface Control	MX-71h	0x8000'h
	ADC/DAC Clock-1	ADC/DAC Clock Control-1	MX-73h	0x1110'h
	ADC/DAC Clock-2	ADC/DAC Clock Control-2	MX-74h	0x0C00'h
Digital MIC	DMIC	Digital Microphone Control	MX-75h	0x1D00'h
Global Clock	Global Clock	Global Clock Control	MX-80h	0x0000'h
	PLL-1	PLL Control-1	MX-81h	0x0000'h
	PLL-2	PLL Control-2	MX-82h	0x0000'h
	ASRC-1	ASRC Control-1	MX-83h	0x0000'h
	ASRC-2	ASRC Control-2	MX-84h	0x0000'h
	ASRC-3	ASRC Control-3	MX-85h	0x0008'h
	ASRC-6	ASRC Control-4	MX-89h	0x0000'h
	ASRC-7	ASRC Control-5	MX-8Ah	0x0000'h
SPK Amp	Class-D	Class-D OC Control	MX-8Ch	0x0228'h
	Class-D	Class-D Ratio Gain & Mode Control	MX-8Dh	0xA800'h
HP Amp	HP	HP Output De-Pop Control	MX-8Eh	0x0004'h
SPK Amp	PV Detection	SPKVDD Detection Control	MX-92h	0x0000'h
MICBIAS	MICBIAS	MICBIAS Control	MX-93h	0x3000'h
EQ	EQ-1	EQ Control-1	MX-B0h	0x2000'h
	EQ-2	EQ Control-2	MX-B1h	0x0000'h
	EQ-Parameter	EQ Low Pass Filter – a1	PR-A0h	0x1C10'h
	EQ-Parameter	EQ Low Pass Filter – H0	PR-A1h	0x01F4'h
	EQ-Parameter	EQ Band Pass Filter 1 – a1	PR-A2h	0xC5E9'h
	EQ-Parameter	EQ Band Pass Filter 1 – a2	PR-A3h	0x1A98'h
	EQ-Parameter	EQ Band Pass Filter 1 – H0	PR-A4h	0x1D2C'h
	EQ-Parameter	EQ Band Pass Filter 2 – a1	PR-A5h	0xC882'h
	EQ-Parameter	EQ Band Pass Filter 2 – a2	PR-A6h	0x1C10'h
	EQ-Parameter	EQ Band Pass Filter 2 – H0	PR-A7h	0x01F4'h
	EQ-Parameter	EQ Band Pass Filter 3 – a1	PR-A8h	0xE904'h
	EQ-Parameter	EQ Band Pass Filter 3 – a2	PR-A9h	0x1C10'h
	EQ-Parameter	EQ Band Pass Filter 3 – H0	PR-AAh	0x01F4'h
	EQ-Parameter	EQ Band Pass Filter 4 – a1	PR-ABh	0xE904'h
	EQ-Parameter	EQ Band Pass Filter 4 – a2	PR-ACh	0x1C10'h
	EQ-Parameter	EQ Band Pass Filter 4 – H0	PR-ADh	0x01F4'h
	EQ-Parameter	EQ High Pass Filter 1 – a1	PR-AEh	0x1C10'h

Type	Name	Description	Register Address	Reset State
	EQ-Parameter	EQ High Pass Filter 1 – H0	PR-AFh	0x01F4'h
	EQ-Parameter	EQ High Pass Filter 2 – a1	PR-B0h	0x2000'h
	EQ-Parameter	EQ High Pass Filter 2 – a2	PR-B1h	0x0000'h
	EQ-Parameter	EQ High Pass Filter 2 – H0	PR-B2h	0x2000'h
DRC/AGC	DRC/AGC-1	DRC/AGC Control-1	MX-B4h	0x2206'h
	DRC/AGC-2	DRC/AGC Control-2	MX-B5h	0x1F00'h
	DRC/AGC-3	DRC/AGC Control-3	MX-B6h	0x0000'h
SNC	SNC-1	SNC Control-1	MX-B8h	0x034B'h
	SNC-2	SNC Control-2	MX-B9h	0x0066'h
	SNC-3	SNC Control-3	MX-BAh	0x000B'h
Jack Detection	JD-1	Jack Detection Control-1	MX-BBh	0x0000'h
	JD-2	Jack Detection Control-2	MX-BCh	0x0000'h
IRQ	IRQ-1	IRQ Control-1	MX-BDh	0x0000'h
	IRQ-2	IRQ Control-2	MX-BEh	0x0000'h
Flag Status	Status	GPIO & Internal Status	MX-BFh	0x0000'h
GPIO	GPIO-1	GPIO Control-1	MX-C0h	0x0400'h
	GPIO-2	GPIO Control-2	MX-C2h	0x0000'h
Voice DSP	DSP R/W	Voice DSP Access Control - Address	MX-C4h	0x0000'h
	DSP R/W	Voice DSP Access Control - Data	MX-C5h	0x0000'h
	DSP Ctrl	Voice DSP Control	MX-C6h	0x2000'h
Register Array	Control-1	Register Array Control-1	MX-C8h	0x0000'h
	Control-2	Register Array Control-2	MX-C9h	0x0000'h
	Control-3	Register Array Control-3	MX-CAh	0x0000'h
	Control-4	Register Array Control-4	MX-CBh	0x0000'h
	Control-5	Register Array Control-5	MX-CCh	0x0000'h
SVOL & ZCD	SVOL & ZCD	Soft Volume and ZCD Control	MX-D9h	0x0809'h
General Control		General Control 1	MX-FAh	0x3400'h
		General Control 2	MX-FBh	0x0000'h
		ADC/DAC RESET Control	PR-3D	0x2400'h
Vendor ID	ID	Vendor ID	MX-FEh	0x10EC'h

8.2. MX-00h: S/W Reset & Device ID

Default: 0006'h

Table 19. MX-00h: S/W Reset

Port Name	Bits	Read/Write	Reset State	Description
Reserved	15:0	R	0'h	Reserved
Device_id	2:1	R	3'h	ALC3261
Reserved	0	R	0'h	Reserved

Note: Writes to this register will reset all registers to their default values.

8.3. MX-01h: Speaker Output Control

Default: C8C8’h

Table 20. MX-01h: Speaker Output Control

Port Name	Bits	Read/Write	Reset State	Description
mu_spo_l	15	R/W	1’h	Mute Control for Left Speaker Output Port (SPOLP/LN) 0’b: Un-Mute 1’b: Mute
Mu_spkvoll_in	14	R/W	1’h	Mute Control for Left Speaker Volume Channel (SPKVOLL) 0’b: Un-Mute 1’b: Mute
vol_spol	13:8	R/W	8’h	Left Speaker Channel Volume Control (SPKVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step
mu_spo_r	7	R/W	1’h	Mute Control for Right Speaker Output Port (SPORP/RN) 0’b: Un-Mute 1’b: Mute
Mu_spkvolr_in	6	R/W	1’h	Mute Control for Right Speaker Volume Channel (SPKVOLR) 0’b: Un-Mute 1’b: Mute
Vol_spor	5:0	R/W	8’h	Right Speaker Channel Volume Control (SPKVOLR) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42

5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.4. MX-02h: Headphone Output Control

Default: C8C8’h

Table 21. MX-02h: Headphone Output Control

Name	Bits	Read/Write	Reset State	Description
mu_hpo_l	15	R/W	1’h	Mute Control for Left Headphone Output Port (HPOL) 0’b: Un-Mute 1’b: Mute
Mu_hpovoll_in	14	R/W	1’h	Mute Control for Left Headphone Volume Channel (HPOVOLL) 0’b: Un-Mute 1’b: Mute
vol_hpol	13:8	R/W	8’h	Left Headphone Channel Volume Control (HPOVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step
mu_hpo_r	7	R/W	1’h	Mute Control Right Headphone Output Port (HPOR) 0’b: Un-Mute 1’b: Mute

Name	Bits	Read/Write	Reset State	Description
Mu_hpovolr_in	6	R/W	1'h	Mute Control for Right Headphone Volume Channel (HPOVOLR) 0'b: Un-Mute 1'b: Mute
Vol_hpor	5:0	R/W	8'h	Right Headphone Channel Volume Control (HPOVOLR)❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.5. MX-03h: LINE Output Control

Default: C8C8’h

Table 22. MX-03h: LINE Output Control

Name	Bits	Read/Write	Reset State	Description
Mu_lout_l	15	R/W	1’h	Mute Control for Left Line Output Port(LOUTL) 0’b: Un-Mute 1’b: Mute
Mu_outvoll_in	14	R/W	1’h	Mute Control for Left Output Volume Channel (OUTVOLL) 0’b: Un-Mute 1’b: Mute
Vol_outl	13:8	R/W	08’h	Left Output Volume Control (OUTVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step
Mu_lout_r	7	R/W	1’h	Mute Control for Right Line Output Port (LOUTR) 0’b: Un-Mute 1’b: Mute
Mu_outvolr_in	6	R/W	1’h	Mute Control for Right Output Volume Channel (OUTVOLR) 0’b: Un-Mute 1’b: Mute
Vol_outr	5:0	R/W	08’h	Right Output Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			

10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.6. MX-04h: MONO Output Control

Default: 8000'h

Table 23. MX-04h: MONO Output Control

Name	Bits	Read/Write	Reset State	Description
mu_mono	15	R/W	1'h	Mute Control for MONO Output Port 0'b: Un-Mute 1'b: Mute
reserved	14:0	R	0'h	Reserved

8.7. MX-0Dh: IN1 Input Control

Default: 0000'h

Table 24. MX-0Dh: IN1 Input Control

Name	Bits	Read/Write	Reset State	Description
Sel_bst1	15:12	R/W	0'h	IN1 Boost Control (BST1) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved

Name	Bits	Read/Write	Reset State	Description
Sel_bst3	11:8	R/W	0'h	IN3 Boost Control (BST3) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved
En_in1_df	7	R/W	0'h	IN1 Input Mode Control 0'b: Single Ended Mode 1'b: Differential Mode
En_in3_df	6	R/W	0'h	IN3 Input Mode Control 0'b: Single Ended Mode 1'b: Differential Mode
reserved	5:0	R/W	0'h	Reserved

8.8. MX-0Eh: IN2 Input Control

Default: 0000'h

Table 25. MX-0Eh: IN2 Input Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R/W	0'h	Reserved
Sel_bst2	11:8	R/W	0'h	IN2 Boost Control (BST2) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved
Reserved	7	R	0'h	Reserved
En_in2_df	6	R/W	0'h	IN2 Input Mode Control 0'b: Single Ended Mode 1'b: Differential Mode
Reserved	5:0	R	0'h	Reserved

8.9. MX-0Fh: INL & INR Volume Control

Default: 0808’h

Table 26. MX-0Fh: INL & INR Volume Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0’h	Reserved
Vol_inl	12:8	R/W	8’h	INL Channel Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 1F’h: -34.5dB, with 1.5dB/step
Reserved	7:5	R	0’h	Reserved
Vol_inr	4:0	R/W	8’h	INR Channel Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 1F’h: -34.5dB, with 1.5dB/step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12
1	1	10.5	17	11	-13.5
2	2	9	18	12	-15
3	3	7.5	19	13	-16.5
4	4	6	20	14	-18
5	5	4.5	21	15	-19.5
6	6	3	22	16	-21
7	7	1.5	23	17	-22.5
8	8	0	24	18	-24
9	9	-1.5	25	19	-25.5
10	A	-3	26	1A	-27
11	B	-4.5	27	1B	-28.5
12	C	-6	28	1C	-30
13	D	-7.5	29	1D	-31.5
14	E	-9	30	1E	-33
15	F	-10.5	31	1F	-34.5

8.10. MX-19h: DACL1/R1 Digital Volume

Default: AFAF'h

Table 27. MX-19h: DACL1/R1 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac1_l	15:8	R/W	AF'h	DAC1 Left Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac1_r	7:0	R/W	AF'h	DAC1 Right Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

8.11. MX-1Ah: DACL2/R2 Digital Volume

Default: AFAF'h

Table 28. MX-1Ah: DACL2/R2 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac2_l	15:8	R/W	AF'h	DAC2 Left Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac2_r	7:0	R/W	AF'h	DAC2 Right Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.625	53	35	-45.75	106	6A	-25.875	159	9F	-6	212	D4	
1	1	-65.25	54	36	-45.375	107	6B	-25.5	160	A0	-5.625	213	D5	
2	2	-64.875	55	37	-45	108	6C	-25.125	161	A1	-5.25	214	D6	
3	3	-64.5	56	38	-44.625	109	6D	-24.75	162	A2	-4.875	215	D7	
4	4	-64.125	57	39	-44.25	110	6E	-24.375	163	A3	-4.5	216	D8	
5	5	-63.75	58	3A	-43.875	111	6F	-24	164	A4	-4.125	217	D9	

6	6	-63.375	59	3B	-43.5	112	70	-23.625	165	A5	-3.75	218	DA	
7	7	-63	60	3C	-43.125	113	71	-23.25	166	A6	-3.375	219	DB	
8	8	-62.625	61	3D	-42.75	114	72	-22.875	167	A7	-3	220	DC	
9	9	-62.25	62	3E	-42.375	115	73	-22.5	168	A8	-2.625	221	DD	
10	A	-61.875	63	3F	-42	116	74	-22.125	169	A9	-2.25	222	DE	
11	B	-61.5	64	40	-41.625	117	75	-21.75	170	AA	-1.875	223	DF	
12	C	-61.125	65	41	-41.25	118	76	-21.375	171	AB	-1.5	224	E0	
13	D	-60.75	66	42	-40.875	119	77	-21	172	AC	-1.125	225	E1	
14	E	-60.375	67	43	-40.5	120	78	-20.625	173	AD	-0.75	226	E2	
15	F	-60	68	44	-40.125	121	79	-20.25	174	AE	-0.375	227	E3	
16	10	-59.625	69	45	-39.75	122	7A	-19.875	175	AF	0	228	E4	
17	11	-59.25	70	46	-39.375	123	7B	-19.5	176	B0		229	E5	
18	12	-58.875	71	47	-39	124	7C	-19.125	177	B1		230	E6	
19	13	-58.5	72	48	-38.625	125	7D	-18.75	178	B2		231	E7	
20	14	-58.125	73	49	-38.25	126	7E	-18.375	179	B3		232	E8	
21	15	-57.75	74	4A	-37.875	127	7F	-18	180	B4		233	E9	
22	16	-57.375	75	4B	-37.5	128	80	-17.625	181	B5		234	EA	
23	17	-57	76	4C	-37.125	129	81	-17.25	182	B6		235	EB	
24	18	-56.625	77	4D	-36.75	130	82	-16.875	183	B7		236	EC	
25	19	-56.25	78	4E	-36.375	131	83	-16.5	184	B8		237	ED	
26	1A	-55.875	79	4F	-36	132	84	-16.125	185	B9		238	EE	
27	1B	-55.5	80	50	-35.625	133	85	-15.75	186	BA		239	EF	
28	1C	-55.125	81	51	-35.25	134	86	-15.375	187	BB		240	F0	
29	1D	-54.75	82	52	-34.875	135	87	-15	188	BC		241	F1	
30	1E	-54.375	83	53	-34.5	136	88	-14.625	189	BD		242	F2	
31	1F	-54	84	54	-34.125	137	89	-14.25	190	BE		243	F3	
32	20	-53.625	85	55	-33.75	138	8A	-13.875	191	BF		244	F4	
33	21	-53.25	86	56	-33.375	139	8B	-13.5	192	C0		245	F5	
34	22	-52.875	87	57	-33	140	8C	-13.125	193	C1		246	F6	
35	23	-52.5	88	58	-32.625	141	8D	-12.75	194	C2		247	F7	
36	24	-52.125	89	59	-32.25	142	8E	-12.375	195	C3		248	F8	
37	25	-51.75	90	5A	-31.875	143	8F	-12	196	C4		249	F9	
38	26	-51.375	91	5B	-31.5	144	90	-11.625	197	C5		250	FA	
39	27	-51	92	5C	-31.125	145	91	-11.25	198	C6		251	FB	
40	28	-50.625	93	5D	-30.75	146	92	-10.875	199	C7		252	FC	
41	29	-50.25	94	5E	-30.375	147	93	-10.5	200	C8		253	FD	

42	2A	-49.875	95	5F	-30	148	94	-10.125	201	C9		254	FE	
43	2B	-49.5	96	60	-29.625	149	95	-9.75	202	CA		255	FF	
44	2C	-49.125	97	61	-29.25	150	96	-9.375	203	CB				
45	2D	-48.75	98	62	-28.875	151	97	-9	204	CC				
46	2E	-48.375	99	63	-28.5	152	98	-8.625	205	CD				
47	2F	-48	100	64	-28.125	153	99	-8.25	206	CE				
48	30	-47.625	101	65	-27.75	154	9A	-7.875	207	CF				
49	31	-47.25	102	66	-27.375	155	9B	-7.5	208	D0				
50	32	-46.875	103	67	-27	156	9C	-7.125	209	D1				
51	33	-46.5	104	68	-26.625	157	9D	-6.75	210	D2				
52	34	-46.125	105	69	-26.25	158	9E	-6.375	211	D3				

8.12. MX-1Bh: DACL2/R2 Mute/Un-Mute Control

Default: 0000’h

Table 29. MX-1Bh: DACL2/R2 Mute/Un-Mute Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
Mu_dac2_l	13	R/W	0’h	Mute Control for Left DAC2 Volume 0’b: Un-Mute 1’b: Mute
Mu_dac2_r	12	R/W	0’h	Mute Control for Right DAC2 Volume 0’b: Un-Mute 1’b: Mute
reserved	11:0	R	0’h	Reserved

8.13. MX-1Ch: Stereo ADC Digital Volume Control

Default: 2F2F’h

Table 30. MX-1Ch: Stereo ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Mu_adc_vol_l	15	R/W	0'h	Mute Control for Stereo ADC Left Volume Channel 0'b: Un-Mute 1'b: Mute
Ad_gain_l	14:8	R/W	2F'h	Stereo ADC Left Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Mu_adc_vol_r	7	R/W	0'h	Mute Control for Stereo ADC Right Volume Channel 0'b: Un-Mute 1'b: Mute
Ad_gain_r	6:0	R/W	2F'h	Stereo ADC Right Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

8.14. MX-1Dh: Mono ADC Digital Volume Control

Default: 2F2F'h

Table 31. MX-1Dh: Mono ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
Mono_ad_gain_l	14:8	R/W	2F'h	Mono ADC Left Channel Volume Control ❶ 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
reserved	7	R	0'h	Reserved

Mono_ad_gain_r	6:0	R/W	2F'h	Mono ADC Right Channel Volume Control ❶ 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25
14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625
15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375
17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125
19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875
21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

8.15. MX-1Eh: ADC Digital Boost Gain Control

Default: 0000'h

Table 32. MX-1Eh: ADC Digital Boost Gain Control

Name	Bits	Read/Write	Reset State	Description
Ad_boost_gain_l	15:14	R/W	0'h	ADC Left Channel Digital Boost Gain 00'b: 0dB 01'b: 12dB 10'b: 24dB 11'b: 36dB
Ad_boost_gain_r	13:12	R/W	0'h	ADC Right Channel Digital Boost Gain 00'b: 0dB 01'b: 12dB 10'b: 24dB 11'b: 36dB
reserved	11:0	R/W	0'h	Reserved

8.16. MX-27h: Stereo ADC Digital Mixer Control

Default: 7060'h

Table 33. MX-27h: Stereo ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	reserved
mu_stereo_adcl1	14	R/W	1'h	Mute Control for Stereo ADC1 Left Channel 0'b: Un-Mute 1'b: Mute
mu_stereo_adcl2	13	R/W	1'h	Mute Control for Stereo ADC2 Left Channel 0'b: Un-Mute 1'b: Mute
sel_stereo_adc1	12	R/W	1'h	Select Control for Stereo ADC1 Source 0'b: DAC_MIXL/ DAC_MIXR 1'b: ADCL/ADCR
sel_stereo_adc2	11:10	R/W	0'h	Select Control for Stereo ADC2 Source 00'b: DMIC_L1/ DMIC_R1 01'b: DMIC_L2/ DMIC_R2 10'b: DAC_MIXL/ DAC_MIXR 11'b: Reserved
reserved	9:7	R	0'h	Reserved
mu_stereo_adcr1	6	R/W	1'h	Mute Control for Stereo ADC1 Right Channel 0'b: Un-Mute 1'b: Mute

mu_stereo_adcr2	5	R/W	1'h	Mute Control for Stereo ADC2 Right Channel 0'b: Un-Mute 1'b: Mute
reserved	4:0	R	0'h	reserved

8.17. MX-28h: Mono ADC Digital Mixer Control

Default: 7070'h

Table 34. MX-28h: Mono ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	reserved
mu_mono_adcl1	14	R/W	1'h	Mute Control for Mono ADC1 Left Channel 0'b: Un-Mute 1'b: Mute
mu_mono_adcl2	13	R/W	1'h	Mute Control for Mono ADC2 Left Channel 0'b: Un-Mute 1'b: Mute
sel_mono_adcl1	12	R/W	1'h	Select Control for Mono ADC1 Left Channel Source 0'b: Mono_DAC_Mixer_L 1'b: ADCL
sel_mono_adcl2	11:10	R/W	0'h	Select Control for Mono ADC2 Left Channel Source 00'b: DMIC_L1 01'b: DMIC_L2 10'b: Mono_DAC_Mixer_L 11'b: Reserved
reserved	9:7	R	0'h	reserved
mu_mono_adcr1	6	R/W	1'h	Mute Control for Mono ADC1 Right Channel 0'b: Un-Mute 1'b: Mute
mu_mono_adcr2	5	R/W	1'h	Mute Control for Mono ADC2 Right Channel 0'b: Un-Mute 1'b: Mute
sel_mono_adcr1	4	R/W	1'h	Select Control for Mono ADC1 Right Channel Source 0'b: Mono_DAC_Mixer_R 1'b: ADCR
sel_mono_adcr2	3:2	R/W	0'h	Select Control for Mono ADC2 Right Channel Source 00'b: DMIC_R1 01'b: DMIC_R2 10'b: Mono_DAC_Mixer_R 11'b: Reserved
reserved	1:0	R	0'h	Reserved

8.18. MX-29h: Stereo ADC to DAC Digital Mixer Control

Default: 8080’h

Table 35. MX-29h: Stereo ADC to DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
mu_stereo_adc_mixer_l	15	R/W	1’h	Mute Control for Stereo ADC Left Channel to DAC 0’b: Un-Mute 1’b: Mute
mu_if1_dac_l	14	R/W	0’h	Mute Control for I2S-1 to DAC Left Channel 0’b: Un-Mute 1’b: Mute
reserved	13:8	R	0’h	Reserved
mu_stereo_adc_mixer_r	7	R/W	1’h	Mute Control for Stereo ADC Right Channel to DAC 0’b: Un-Mute 1’b: Mute
mu_if1_dac_r	6	R/W	0’h	Mute Control for I2S-1 to DAC Right Channel 0’b: Un-Mute 1’b: Mute
reserved	5:0	R	0’h	reserved

8.19. MX-2Ah: Stereo DAC Digital Mixer Control

Default: 5454’h

Table 36. MX-2Ah: Stereo DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	reserved
mu_stereo_dacl1	14	R/W	1’h	Mute Control for DACL1 to Stereo DAC Left Mixer 0’b: Un-Mute 1’b: Mute
gain_dacl1_to_stereo_l	13	R/W	0’h	Gain Control for DACL1 to Stereo DAC Left Mixer 0’b: 0dB 1’b: -6dB
mu_stereo_dacl2	12	R/W	1’h	Mute Control for DACL2 to Stereo DAC Left Mixer 0’b: Un-Mute 1’b: Mute
gain_dacl2_to_stereo_l	11	R/W	0’h	Gain Control for DACL2 to Stereo DAC Left Mixer 0’b: 0dB 1’b: -6dB
mu_snc_to_dac_l	10	R/W	1’h	Mute Control for SNC Function to Stereo DAC Left Mixer 0’b: Un-Mute 1’b: Mute
reserved	9:7	R	0’h	reserved
mu_stereo_dacr1	6	R/W	1’h	Mute Control for DACR1 to Stereo DAC Right Mixer 0’b: Un-Mute 1’b: Mute

Name	Bits	Read/Write	Reset State	Description
gain_dacr1_to_stereo_r	5	R/W	0'h	Gain Control for DACR1 to Stereo DAC Right Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dacr2	4	R/W	1'h	Mute Control for DACR2 to Stereo DAC Right Mixer 0'b: Un-Mute 1'b: Mute
gain_dacr2_to_stereo_r	3	R/W	0'h	Gain Control for DACR2 to Stereo DAC Right Mixer 0'b: 0dB 1'b: -6dB
mu_snc_to_dac_r	2	R/W	1'h	Mute Control for SNC Function to Stereo DAC Right Mixer 0'b: Un-Mute 1'b: Mute
reserved	1:0	R	0'h	reserved

8.20. MX-2Bh: Mono DAC Digital Mixer Control

Default: 5454'h

Table 37. MX-2Bh: Mono DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
mu_mono_l_dacl1	14	R/W	1'h	Mute Control for DACL1 to Mono DAC Mixer 0'b: Un-Mute 1'b: Mute
gain_mono_l_dacl1	13	R/W	0'h	Gain Control for DACL1 to Mono DAC Mixer 0'b: 0dB 1'b: -6dB
mu_mono_l_dacl2	12	R/W	1'h	Mute Control for DACL2 to Mono DAC Mixer 0'b: Un-Mute 1'b: Mute
gain_mono_l_dacl2	11	R/W	0'h	Gain Control for DACL2 to Mono DAC Mixer 0'b: 0dB 1'b: -6dB
mu_mono_l_dacr2	10	R/W	1'h	Mute Control for DACR2 to Mono DAC Mixer 0'b: Un-Mute 1'b: Mute
gain_mono_l_dacr2	9	R/W	0'h	Gain Control for DACR2 to Mono DAC Mixer 0'b: 0dB 1'b: -6dB
reserved	8:7	R	0'h	Reserved
mu_mono_r_dacr1	6	R/W	1'h	Mute Control for DACR1 to Mono DAC Mixer 0'b: Un-Mute 1'b: Mute
gain_mono_r_dacr1	5	R/W	0'h	Gain Control for DACR1 to Mono DAC Mixer 0'b: 0dB 1'b: -6dB

Name	Bits	Read/Write	Reset State	Description
mu_mono_r_dacr2	4	R/W	1'h	Mute Control for DACR2 to Mono DAC Mixer 0'b: Un-Mute 1'b: Mute
gain_mono_r_dacr2	3	R/W	0'h	Gain Control for DACR2 to Mono DAC Mixer 0'b: 0dB 1'b: -6dB
mu_mono_r_dacl2	2	R/W	1'h	Mute Control for DACL2 to Mono DAC Mixer 0'b: Un-Mute 1'b: Mute
gain_mono_r_dacl2	1	R/W	0'h	Gain Control for DACL2 to Mono DAC Mixer 0'b: 0dB 1'b: -6dB
reserved	0	R	0'h	reserved

8.21. MX-2Ch: DAC Digital Mixer Control

Default: AA00'h

Table 38. MX-2Ch: DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
mu_dacl1_to_dacl	15	R/W	1'h	Mute Control for DACL1 to DACMIXL 0'b: Un-Mute 1'b: Mute
gain_dacl1_to_dacl	14	R/W	0'h	Gain Control for DACL1 to DACMIXL 0'b: 0dB 1'b: -6dB
mu_dacl2_to_dacl	13	R/W	1'h	Mute Control for DACL2 to DACMIXL 0'b: Un-Mute 1'b: Mute
gain_dacl2_to_dacl	12	R/W	0'h	Gain Control for DACL2 to DACMIXL 0'b: 0dB 1'b: -6dB
mu_dacr1_to_dacr	11	R/W	1'h	Mute Control for DACR1 to DACMIXR 0'b: Un-Mute 1'b: Mute
gain_dacr1_to_dacr	10	R/W	0'h	Gain Control for DACR1 to DACMIXR 0'b: 0dB 1'b: -6dB
mu_dacr2_to_dacr	9	R/W	1'h	Mute Control for DACR2 to DACMIXR 0'b: Un-Mute 1'b: Mute
gain_dacr2_to_dacr	8	R/W	0'h	Gain Control for DACR2 to DACMIXR 0'b: 0dB 1'b: -6dB
reserved	7:0	R	0'h	reserved

8.22. MX-2Dh: Voice DSP Path Control 1

Default: 0000'h

Table 39. MX-2Dh: Voice DSP Path Control 1

Name	Bits	Read/Write	Reset State	Description
sel_src_to_rxdp	15	R/W	0'h	Select the Sample Rate Converter(SRC) for RxDP 0'b: Normal 1'b: Divided by 3
sel_src_to_txdp	14	R/W	0'h	Select the Sample Rate Converter(SRC) for Interface2 0'b: Normal 1'b: Multiplied by 3
reserved	13:0	R	0'h	reserved

8.23. MX-2Eh: Voice DSP Path Control 2

Default: A000'h

Table 40. MX-2Eh: Voice DSP Path Control 2

Name	Bits	Read/Write	Reset State	Description
sel_dacl2	15:14	R/W	2'h	Select Control for DACL2 00'b: IF2_DAC_L (By pass DSP) 01'b: Reserved 10'b: TxDC 11'b: Bass L/R
sel_dacr2	13:12	R/W	2'h	Select Control for DACR2 00'b: IF2_DAC_R (By pass DSP) 01'b: Reserved 10'b: TxDC 11'b: reserved
sel_if2_adc_l	11	R/W	0'h	Select Control for I2S2 ADC Left Channel 0'b: TxDP 1'b: Mono ADC Mixer L(By pass DSP)
sel_if2_adc_r	10	R/W	0'h	Select Control for I2S2 ADC Right Channel 0'b: TxDP 1'b: Mono ADC Mixer R(By pass DSP)
sel_rxdc_data	9:8	R/W	0'h	Select Control for RxDC Input Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel
Reserved	7:6	R	0'h	Reserved
sel_txdc_data	5:4	R/W	0'h	Select Control for TxDC Input Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel

Name	Bits	Read/Write	Reset State	Description
sel_txdp_data	3:2	R/W	0'h	Select Control for TxDP Input Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel
reserved	1:0	R	0'h	reserved

8.24. MX-2Fh: Interface DAC/ADC Data Control

Default: 0000'h

Table 41. MX-2Fh: Interface DAC/ADC Data Control

Name	Bits	Read/Write	Reset State	Description
sel_if1_dac_data	15:14	R/W	0'h	Select Control for I2S1 DACDAT Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel
sel_if1_adc_data	13:12	R/W	0'h	Select Control for I2S1 ADCDAT Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel
sel_if2_dac_data	11:10	R/W	0'h	Select Control for I2S2 DACDAT Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel
sel_if2_adc_data	9:8	R/W	0'h	Select Control for I2S2 ADCDAT Data 00'b: Normal 01'b: Swap 10'b: Left Channel Copy to Right Channel 11'b: Right Channel Copy to Left Channel
reserved	7:0	R	0'h	reserved

8.25. MX-3Bh: RECMIXL Control 1

Default: 0000'h

Table 42. MX-3Bh: RECMIXL Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0'h	reserved

Name	Bits	Read/Write	Reset State	Description
Gain_inl_recmixl	12:10	R/W	0'h	Gain Control for INL to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
Gain_bst2_recmixl	9:7	R/W	0'h	Gain Control for BST2 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
reserved	6:4	R/W	0'h	reserved
Gain_bst3_recmixl	3:1	R/W	0'h	Gain Control for BST3 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
reserved	0	R	0'h	reserved

8.26. MX-3Ch: RECMIXL Control 2

Default: 007F'h

Table 43. MX-3Ch: RECMIXL Control 2

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_recmixl	15:13	R/W	0'h	Gain Control for BST1 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB

Name	Bits	Read/Write	Reset State	Description
Gain_outmixl_recmixl	12:10	R/W	0'h	Gain Control for OUTMIXL to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
reserved	9:6	R	0'h	reserved
Mu_inl_rexmixl	5	R/W	1'h	Mute Control for INL to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst2_recmixl	4	R/W	1'h	Mute Control for BST2 to RECMIXL 0'b: Un-Mute 1'b: Mute
reserved	3	R/W	1'h	reserved
Mu_bst3_recmixl	2	R/W	1'h	Mute Control for BST3 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst1_recmixl	1	R/W	1'h	Mute Control for BST1 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_outmixl_recmixl	0	R/W	1'h	Mute Control for OUTMIXL to RECMIXL 0'b: Un-Mute 1'b: Mute

8.27. MX-3Dh: RECMIXR Control 1

Default: 0000'h

Table 44. MX-3Dh: RECMIXR Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R/W	0'h	Reserved
Gain_inr_recmixr	12:10	R/W	0'h	Gain Control for INR to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB

Name	Bits	Read/Write	Reset State	Description
Gain_bst2_recmixr	9:7	R/W	0'h	Gain Control for BST2 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
reserved	6:4	R/W	0'h	Reserved
Gain_bst3_recmixr	3:1	R/W	0'h	Gain Control for BST3 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
reserved	0	R/W	0'h	Reserved

8.28. MX-3Eh: RECMIXR Control 2

Default: 007F'h

Table 45. MX-3Eh: RECMIXR Control 2

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_recmixr	15:13	R/W	0'h	Gain Control for BST1 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
Gain_outmixr_recmixr	12:10	R/W	0'h	Gain Control for OUTMIXR to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB
reserved	9:6	R	0'h	reserved
Mu_inr_rexmixr	5	R/W	1'h	Mute Control for INR to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst2_recmixr	4	R/W	1'h	Mute Control for BST2 to RECMIXR 0'b: Un-Mute 1'b: Mute
Reserved	3	R/W	1'h	reserved

Name	Bits	Read/Write	Reset State	Description
Mu_bst3_recmixr	2	R/W	1'h	Mute Control for BST3 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst1_recmixr	1	R/W	1'h	Mute Control for BST1 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_outmixr_recmixr	0	R/W	1'h	Mute Control for OUTMIXR to RECMIXR 0'b: Un-Mute 1'b: Mute

8.29. MX-45h: HPOMIX Control

Default: E000'h

Table 46. MX-45h: HPOMIX Control

Name	Bits	Read/Write	Reset State	Description
mu_dac2_hpomix	15	R/W	1'h	Mute Control for DAC2 to HPOMIX 0'b: Un-Mute 1'b: Mute
mu_dac1_hpomix	14	R/W	1'h	Mute Control for DAC1 to HPOMIX 0'b: Un-Mute 1'b: Mute
mu_hpovol_hpomix	13	R/W	1'h	Mute Control for HPOVOL to HPOMIX 0'b: Un-Mute 1'b: Mute
Gain_hpomix	12	R/W	0'h	Gain Control for HPOMIX 0'b: 0dB 1'b: -6dB
Reserved	11:0	R	0'h	reserved

8.30. MX-46h: SPKMIXL Control

Default: 003E'h

Table 47. MX-46h: SPKMIXL Control

Name	Bits	Read/Write	Reset State	Description
gain_recmixl_spkmixl	15:14	R/W	0'h	Gain Control for RECMIXL to SPKMIXL 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB

Name	Bits	Read/Write	Reset State	Description
Gain_inl_spkmixl	13:12	R/W	0'h	Gain Control for INL to SPKMIXL 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Gain_dacl1_spkmixl	11:10	R/W	0'h	Gain Control for DACL1 to SPKMIXL 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Gain_dacl2_spkmixl	9:8	R/W	0'h	Gain Control for DACL2 to SPKMIXL 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Gain_outmixl_spkmixl	7:6	R/W	0'h	Gain Control for OUTMIXL to SPKMIXL 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Mu_recmix1_spkmixl	5	R/W	1'h	Mute Control for RECMIXL to SPKMIXL 0'b: Un-Mute 1'b: Mute
Mu_inl_spkmixl	4	R/W	1'h	Mute Control for INL to SPKMIXL 0'b: Un-Mute 1'b: Mute
Mu_dacl1_spkmixl	3	R/W	1'h	Mute Control for DACL1 to SPKMIXL 0'b: Un-Mute 1'b: Mute
Mu_dacl2_spkmixl	2	R/W	1'h	Mute Control for DACL2 to SPKMIXL 0'b: Un-Mute 1'b: Mute
Mu_outmixl_spkmixl	1	R/W	1'h	Mute Control for OUTMIXL to SPKMIXL 0'b: Un-Mute 1'b: Mute
Reserved	0	R	0'h	Reserved

8.31. MX-47h: SPKMIXR Control

Default: 003E'h

Table 48. MX-47h: SPKMIXR Control

Name	Bits	Read/Write	Reset State	Description
gain_recmixr_spkmixr	15:14	R/W	0'h	Gain Control for RECMIXR to SPKMIXR 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB

Name	Bits	Read/Write	Reset State	Description
Gain_inr_spkmixr	13:12	R/W	0'h	Gain Control for INR to SPKMIXR 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Gain_dacr1_spkmixr	11:10	R/W	0'h	Gain Control for DACR1 to SPKMIXR 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Gain_dacr2_spkmixr	9:8	R/W	0'h	Gain Control for DACR2 to SPKMIXR 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Gain_outmixr_spkmixr	7:6	R/W	0'h	Gain Control for OUTMIXR to SPKMIXR 00'b: 0dB 01'b: -3dB 10'b: -6dB 11'b: -9dB
Mu_recmixr_spkmixr	5	R/W	1'h	Mute Control for RECMIXR to SPKMIXR 0'b: Un-Mute 1'b: Mute
Mu_inr_spkmixr	4	R/W	1'h	Mute Control for INR to SPKMIXR 0'b: Un-Mute 1'b: Mute
Mu_dacr1_spkmixr	3	R/W	1'h	Mute Control for DACR1 to SPKMIXR 0'b: Un-Mute 1'b: Mute
Mu_dacr2_spkmixr	2	R/W	1'h	Mute Control for DACR2 to SPKMIXR 0'b: Un-Mute 1'b: Mute
Mu_outmixr_spkmixr	1	R/W	1'h	Mute Control for OUTMIXR to SPKMIXR 0'b: Un-Mute 1'b: Mute
Reserved	0	R	0'h	Reserved

8.32. MX-48h: SPOLMIX Control

Default: F800'h

Table 49. MX-48h: SPOLMIX Control

Name	Bits	Read/Write	Reset State	Description
Mu_dacr1_spolmix	15	R/W	1'h	Mute Control for DACR1 to SPOLMIX 0'b: Un-Mute 1'b: Mute
Mu_dacl1_spolmix	14	R/W	1'h	Mute Control for DACL1 to SPOLMIX 0'b: Un-Mute 1'b: Mute

Name	Bits	Read/Write	Reset State	Description
Mu_spkvolr_spolmix	13	R/W	1'h	Mute Control for SPKVOLR to SPOLMIX 0'b: Un-Mute 1'b: Mute
Mu_spkvoll_spolmix	12	R/W	1'h	Mute Control for SPKVOLL to SPOLMIX 0'b: Un-Mute 1'b: Mute
Mu_bst1_spolmix	11	R/W	1'h	Mute Control for BST1 to SPOLMIX 0'b: Un-Mute 1'b: Mute
reserved	10:0	R	0'h	Reserved

8.33. MX-49h: SPORMIX Control

Default: 3800'h

Table 50. MX-49h: SPORMIX Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
Mu_dacr1_spormix	13	R/W	1'h	Mute Control for DACR1 to SPORMIX 0'b: Un-Mute 1'b: Mute
Mu_spkvolr_spormix	12	R/W	1'h	Mute Control for SPKVOLR to SPORMIX 0'b: Un-Mute 1'b: Mute
Mu_bst1_spormix	11	R/W	1'h	Mute Control for BST1 to SPORMIX 0'b: Un-Mute 1'b: Mute
reserved	10:0	R	0'h	Reserved

8.34. MX-4Ah: SPOL/RMIX Gain Control

Default: 0004'h

Table 51. MX-4Ah: SPOL/RMIX Gain Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:3	R	0'h	Reserved
Spk_gain_clsd	2:0	R/W	4'h	Gain Control for SPOL/RMIX 000'b: -6dB (0.50x) 001'b: -4.5dB (0.60x) 010'b: -3dB (0.71x) 011'b: -1.5dB (0.84x) 100'b: 0dB (1.0x) 101'b: 0.83dB (1.1x) 110'b: 1.58dB (1.2x) 111'b: 2.28dB (1.3x)

8.35. MX-4Ch: MONOMIX Control

Default: FC00’h

Table 52. MX-4Ch: MONOMIX Control

Name	Bits	Read/Write	Reset State	Description
Mu_dacr2_monomix	15	R/W	1’h	Mute Control for DACR2 to MONOMIX 0’b: Un-Mute 1’b: Mute
Mu_dacl2_monomix	14	R/W	1’h	Mute Control for DACL2 to MONOMIX 0’b: Un-Mute 1’b: Mute
Mu_outvolr_monomix	13	R/W	1’h	Mute Control for OUTVOLR to MONOMIX 0’b: Un-Mute 1’b: Mute
Mu_outvoll_monomix	12	R/W	1’h	Mute Control for OUTVOLL to MONOMIX 0’b: Un-Mute 1’b: Mute
Mu_bst1_monomix	11	R/W	1’h	Mute Control for BST1 to MONOMIX 0’b: Un-Mute 1’b: Mute
Gain_mono	10	R/W	1’h	Gain Control for MONOMIX 0’b: 0dB 1’b: -6dB
reserved	9:0	R	0’h	Reserved

8.36. MX-4Dh: OUTMIXL Control 1

Default: 0000’h

Table 53. MX-4Dh: OUTMIXL Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R/W	0’h	Reserved
Gain_bst3_outmixl	12:10	R/W	0’h	Gain Control for BST3 to OUTMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_outmixl	9:7	R/W	0'h	Gain Control for BST1 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_inl_outmixl	6:4	R/W	0'h	Gain Control for INL to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_recmixl_outmixl	3:1	R/W	0'h	Gain Control for RECMIXL to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Reserved	0	R	0'h	reserved

8.37. MX-4Eh: OUTMIXL Control 2

Default: 0000'h

Table 54. MX-4Eh: OUTMIXL Control 2

Name	Bits	Read/Write	Reset State	Description
Gain_dacr2_outmixl	15:13	R/W	0'h	Gain Control for DACR2 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved

Name	Bits	Read/Write	Reset State	Description
Gain_dacl2_outmixl	12:10	R/W	0'h	Gain Control for DACL2 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_dacl1_outmixl	9:7	R/W	0'h	Gain Control for DACL1 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
reserved	6:0	R	0'h	Reserved

8.38. MX-4Fh: OUTMIXL Control 3

Default: 01FF'h

Table 55. MX-4Fh: OUTMIXL Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:7	R	7'h	Reserved
Mu_bst3_outmixl	6	R/W	1'h	Mute Control for BST3 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst1_outmixl	5	R/W	1'h	Mute Control for BST1 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_inl_outmixl	4	R/W	1'h	Mute Control for INL to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_recmixl_outmixl	3	R/W	1'h	Mute Control for RECMIXL to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_dacr2_outmixl	2	R/W	1'h	Mute Control for DACR2 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_dacl2_outmixl	1	R/W	1'h	Mute Control for DACL2 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_dacl1_outmixl	0	R/W	1'h	Mute Control for DACL1 to OUTMIXL 0'b: Un-Mute 1'b: Mute

8.39. MX-50h: OUTMIXR Control 1

Default: 0000’h

Table 56. MX-50h: OUTMIXR Control 1

Name	Bits	Read/Write	Reset State	Description
Gain_bst2_outmixr	15:13	R/W	0’h	Gain Control for BST2 to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_bst3_outmixr	12:10	R/W	0’h	Gain Control for BST3 to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_bst1_outmixr	9:7	R/W	0’h	Gain Control for BST1 to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_inr_outmixr	6:4	R/W	0’h	Gain Control for INR to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved

Name	Bits	Read/Write	Reset State	Description
Gain_recmixr_outmixr	3:1	R/W	0'h	Gain Control for RECMIXR to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
reserved	0	R	0'h	Reserved

8.40. MX-51h: OUTMIXR Control 2

Default: 0000'h

Table 57. MX-51h: OUTMIXR Control 2

Name	Bits	Read/Write	Reset State	Description
Gain_dacl2_outmixr	15:13	R/W	0'h	Gain Control for DACL2 to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_dacr2_outmixr	12:10	R/W	0'h	Gain Control for DACR2 to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_dacr1_outmixr	9:7	R/W	0'h	Gain Control for DACR1 to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
reserved	6:0	R	0'h	Reserved

8.41. MX-52h: OUTMIXR Control 3

Default: 01FF'h

Table 58. MX-52h: OUTMIXR Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R/W	1'h	Reserved
Mu_bst2_outmixr	7	R/W	1'h	Mute Control for BST2 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst3_outmixr	6	R/W	1'h	Mute Control for BST3 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst1_outmixr	5	R/W	1'h	Mute Control for BST1 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_inr_outmixr	4	R/W	1'h	Mute Control for INR to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_recmixr_outmixr	3	R/W	1'h	Mute Control for RECMIXR to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_dacr2_outmixr	2	R/W	1'h	Mute Control for DACR2 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_dacl2_outmixr	1	R/W	1'h	Mute Control for DACL2 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_dacr1_outmixr	0	R/W	1'h	Mute Control for DACR1 to OUTMIXR 0'b: Un-Mute 1'b: Mute

8.42. MX-53h: LOUTMIX Control

Default: F000'h

Table 59. MX-53h: LOUTMIX Control

Name	Bits	Read/Write	Reset State	Description
Mu_dacl1_lout	15	R/W	1'h	Mute Control for DACL1 to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_dacr1_lout	14	R/W	1'h	Mute Control for DACR1 to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_outvoll_lout	13	R/W	1'h	Mute Control for OUTVOLL to LOUTMIX 0'b: Un-Mute 1'b: Mute

Name	Bits	Read/Write	Reset State	Description
Mu_outvolr_lout	12	R/W	1'h	Mute Control for OUTVOLR to LOUTMIX 0'b: Un-Mute 1'b: Mute
Gain_lout	11	R/W	0'h	Gain Control for LOUTMIX 0'b: 0dB 1'b: -6dB
reserved	10:0	R/W	0'h	Reserved

8.43. MX-61h: Power Management Control 1

Default: 0000'h

Table 60. MX-61h: Power Management Control 1

Name	Bits	Read/Write	Reset State	Description
En_i2s1	15	R/W	0'h	I2S1 Digital Interface Power Control 0'b: Power Down 1'b: Power On
En_i2s2	14	R/W	0'h	I2S2 Digital Interface Power Control 0'b: Power Down 1'b: Power On
reserved	13	R/W	0'h	Reserved
Pow_dac_l_1	12	R/W	0'h	Analog DACL1 Power Control 0'b: Power Down 1'b: Power On
Pow_dac_r_1	11	R/W	0'h	Analog DACR1 Power Control 0'b: Power Down 1'b: Power On
reserved	10:8	R	0'h	Reserved
Pow_dac_l_2	7	R/W	0'h	Analog DACL2 Power Control 0'b: Power Down 1'b: Power On
Pow_dac_r_2	6	R/W	0'h	Analog DACR2 Power Control 0'b: Power Down 1'b: Power On
reserved	5:3	R	0'h	Reserved
Pow_adc_l	2	R/W	0'h	Analog ADCL Power Control 0'b: Power Down 1'b: Power On
Pow_adc_r	1	R/W	0'h	Analog ADCR Power Control 0'b: Power Down 1'b: Power On
Pow_clsd	0	R/W	0'h	Class-D Amp Power Control 0'b: Power Down 1'b: Power On

8.44. MX-62h: Power Management Control 2

Default: 0000’h

Table 61. MX-62h: Power Management Control 2

Name	Bits	Read/Write	Reset State	Description
Pow_adc_stereo_filter	15	R/W	0’h	Stereo ADC Digital Filter Power Control 0’b: Power Down 1’b: Power On
Pow_adc_monol_filter	14	R/W	0’h	Mono ADC_L Digital Filter Power Control 0’b: Power Down 1’b: Power On
Pow_adc_monor_filter	13	R/W	0’h	Mono ADC_R Digital Filter Power Control 0’b: Power Down 1’b: Power On
Pow_i2s_dsp	12	R/W	0’h	I2S Interface for DSP Power Control 0’b: Power Down 1’b: Power On
reserved	11:0	R	0’h	Reserved

8.45. MX-63h: Power Management Control 3

Default: 00C0’h

Table 62. MX-63h: Power Management Control 3

Name	Bits	Read/Write	Reset State	Description
Pow_vref1	15	R/W	0’h	VREF1 Power Control 0’b: Power Down 1’b: Power On
En_fastb1	14	R/W	0’h	VREF1 Fast Mode Control 0’b: Fast VREF 1’b: Slow VREF, (For good analog performance)
Pow_main_bias	13	R/W	0’h	MBIAS Power Control 0’b: Power Down 1’b: Power On
Pow_lout	12	R/W	0’h	LOUTMIX Power Control 0’b: Power Down 1’b: Power On
Pow_bg_bias	11	R/W	0’h	MBIAS Bandgap Power Control 0’b: Power Down 1’b: Power On
Pow_mono	10	R/W	0’h	MONOMIX Power Control 0’b: Power Down 1’b: Power On
reserved	9	R	0’h	Reserved
En_amp_mono	8	R/W	0’h	Mono Amp Power Control 0’b: Power Down 1’b: Power On

Name	Bits	Read/Write	Reset State	Description
En_l_hp	7	R/W	1'h	Left Headphone Amp Power Control 0'b: Power Down 1'b: Power On
En_r_hp	6	R/W	1'h	Right Headphone Amp Power Control 0'b: Power Down 1'b: Power On
En_amp_hp	5	R/W	0'h	Improve HP Amp Driving 0'b: Disable 1'b: Enable
Pow_vref2	4	R/W	0'h	VREF2 Power Control 0'b: Power Down 1'b: Power On
En_fastb2	3	R/W	0'h	VREF2 Fast Mode Control 0'b: Fast VREF 1'b: Slow VREF, (For good analog performance)
Pow_ldo2	2	R/W	0'h	LDO2 Power Control 0'b: Power Down 1'b: Power On
reserved	1:0	R	0'h	Reserved

8.46. MX-64h: Power Management Control 4

Default: 0000'h

Table 63. MX-64h: Power Management Control 4

Name	Bits	Read/Write	Reset State	Description
Pow_bst1	15	R/W	0'h	MIC BST1 Power Control 0'b: Power Down 1'b: Power On
Pow_bst3	14	R/W	0'h	MIC BST3 Power Control 0'b: Power Down 1'b: Power On
reserved	13	R/W	0'h	reserved
Pow_bst2	12	R/W	0'h	MIC BST2 Power Control 0'b: Power Down 1'b: Power On
Pow_micbias1	11	R/W	0'h	MICBIAS1 Power Control 0'b: Power Down 1'b: Power On
reserved	10	R/W	0'h	reserved
Pow_pll	9	R/W	0'h	PLL Power Control 0'b: Power Down 1'b: Power On
reserved	8:0	R	0'h	Reserved

8.47. MX-65h: Power Management Control 5

Default: 0000’h

Table 64. MX-65h: Power Management Control 5

Name	Bits	Read/Write	Reset State	Description
Pow_outmixl	15	R/W	0’h	OUTMIXL Power Control 0’b: Power Down 1’b: Power On
Pow_outmixr	14	R/W	0’h	OUTMIXR Power Control 0’b: Power Down 1’b: Power On
Pow_spkmixl	13	R/W	0’h	SPKMIXL Power Control 0’b: Power Down 1’b: Power On
Pow_spkmixr	12	R/W	0’h	SPKMIXR Power Control 0’b: Power Down 1’b: Power On
Pow_recmixl	11	R/W	0’h	RECMIXL Power Control 0’b: Power Down 1’b: Power On
Pow_recmixr	10	R/W	0’h	RECMIXR Power Control 0’b: Power Down 1’b: Power On
reserved	9:0	R	0’h	Reserved

8.48. MX-66h: Power Management Control 6

Default: 0000’h

Table 65. MX-66h: Power Management Control 6

Name	Bits	Read/Write	Reset State	Description
Pow_spkvoll	15	R/W	0’h	SPKVOLL Power Control 0’b: Power Down 1’b: Power On
Pow_spkvolr	14	R/W	0’h	SPKVOLR power Control 0’b: Power Down 1’b: Power On
Pow_outvoll	13	R/W	0’h	OUTVOLL Power Control 0’b: Power Down 1’b: Power On
Pow_outvolr	12	R/W	0’h	OUTVOLR Power Control 0’b: Power Down 1’b: Power On
Pow_hpovoll	11	R/W	0’h	HPOVOLL Power Control 0’b: Power Down 1’b: Power On

Name	Bits	Read/Write	Reset State	Description
Pow_hpovolr	10	R/W	0'h	HPOVOLR Power Control 0'b: Power Down 1'b: Power On
Pow_inlvol	9	R/W	0'h	INLVOL Power Control 0'b: Power Down 1'b: Power On
Pow_inrvol	8	R/W	0'h	INRVOL Power Control 0'b: Power Down 1'b: Power On
reserved	7:0	R	0'h	Reserved

8.49. MX-6Ah: Private Register Index

Default: 0000'h

Table 66. MX-6Ah: Private Register Index

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R	0'h	reserved
Pr_index	7:0	R/W	0'h	PR Register Index

8.50. MX-6Ch: Private Register Data

Default: 0000'h

Table 67. MX-6Ch: Private Register Data

Name	Bits	Read/Write	Reset State	Description
Pr_data	15:0	R/W	0'h	PR Register Data

8.51. MX-70h: I2S1 Digital Interface Control

Default: 8000'h

Table 68. MX-70h: I2S1 Digital Interface Control

Name	Bits	Read/Write	Reset State	Description
Sel_i2s1_ms	15	R/W	0'h	I2S1 Digital Interface Mode Control 0'b: Master Mode 1'b: Slave Mode

Name	Bits	Read/Write	Reset State	Description
Sel_i2s1_in	14:12	R/W	0'h	I2S Digital Interface Input Port Selection Control 000'b: I2S1 <= BCLK1/LRCK1/DACDAT1/ADCDAT1 I2S2 <= BCLK2/LRCK2/DACDAT2/ADCDAT2 101'b: I2S1 <= BCLK2/LRCK2/DACDAT2/ADCDAT2 I2S2 <= BCLK1/LRCK1/DACDAT1/ADCDAT1 110'b: I2S1 <= BCLK1/LRCK1/DACDAT1/ADCDAT1 I2S2 <= BCLK1/LRCK1/DACDAT1/ADCDAT1 111'b: I2S1 <= BCLK2/LRCK2/DACDAT2/ADCDAT2 I2S2 <= BCLK2/LRCK2/DACDAT2/ADCDAT2 Others: Reserved
en_i2s1_out_comp	11:10	R/W	0'h	I2S1 Output Data Compress (For ADCDAT1 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s1_in_comp	9:8	R/W	0'h	I2S1 Input Data Compress (For DACDAT1 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
Inv_i2s1_bclk	7	R/W	0'h	I2S1 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	6:4	R	0'h	Reserved
sel_i2s1_len	3:2	R/W	0'h	I2S1 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
sel_i2s1_format	1:0	R/W	0'h	I2S1 PCM Data Format Selection 00'b: I^2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

8.52. MX-71h: I2S2 Digital Interface Control

Default: 8000'h

Table 69. MX-71h: I2S2 Digital Interface Control

Name	Bits	Read/Write	Reset State	Description
Sel_i2s2_ms	15	R/W	0'h	I2S2 Digital Interface Mode Control 0'b: Master Mode 1'b: Slave Mode
reserved	14:12	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
en_i2s2_out_comp	11:10	R/W	0'h	I2S2 Output Data Compress (For ADCDAT2 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s2_in_comp	9:8	R/W	0'h	I2S2 Input Data Compress (For DACDAT2 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
inv_i2s2_bclk	7	R/W	0'h	I2S2 BCLK Polarity Control 0'b: Normal 1'b: Invert
sel_sdi	6	R/W	0'h	When MX-70[14:12]=6'h or 7'h, Select ADCDAT1/2 Output Source MX-70[14:12]=0x6'h: 0'b: ADCDAT1 is From IF1_ADC 1'b: ADCDAT1 is From IF2_ADC MX-70[14:12]=0x7'h: 0'b: ADCDAT2 is From IF1_ADC 1'b: ADCDAT2 is From IF2_ADC
reserved	5:4	R	0'h	Reserved
sel_i2s2_len	3:2	R/W	0'h	I2S2 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
sel_i2s2_format	1:0	R/W	0'h	I2S2 PCM Data Format Selection 00'b: I^2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

8.53. MX-73h: ADC/DAC Clock Control 1

Default: 1114'h

Table 70. MX-73h: ADC/DAC Clock Control 1

Name	Bits	Read/Write	Reset State	Description
sel_i2s_bclk_ms1	15	R/W	0'h	I2S1 Master Mode Clock Relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)

Name	Bits	Read/Write	Reset State	Description
sel_i2s_pre_div1	14:12	R/W	1'h	I2S Clock Pre-Divider 1 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
sel_i2s_bclk_ms2	11	R/W	0'h	I2S2 Master Mode Clock Relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)
sel_i2s_pre_div2	10:8	R/W	1'h	I2S Pre-Divider 2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
reserved	7:4	R/W	1'h	Reserved
sel_dac_osr	3:2	R/W	1'h	Stereo DAC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 16Fs
sel_adc_osr	1:0	R/W	0'h	Stereo ADC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 16Fs

8.54. MX-74h: ADC/DAC Clock Control 2

Default: 0C00'h

Table 71. MX-74h: ADC/DAC Clock Control 2

Name	Bits	Read/Write	Reset State	Description
sel_da_osr_mono_l	15:14	R/W	0'h	Mono DACL Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 16Fs
sel_da_osr_mono_r	13:12	R/W	0'h	Mono DACR Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 16Fs

Name	Bits	Read/Write	Reset State	Description
reserved	11:0	R/W	C00’h	Reserved

8.55. MX-75h: Digital Microphone Control

Default: 1D00’h

Table 72. MX-75h: Digital Microphone Control

Name	Bits	Read/Write	Reset State	Description
en_dmic1	15	R/W	0’h	Enable DMIC1 Interface 0’b: Disable 1’b: Enable (Output DMIC clock)
en_dmic2	14	R/W	0’h	Enable DMIC2 Interface 0’b: Disable 1’b: Enable (Output DMIC clock)
sel_dmic1_l_edge	13	R/W	0’h	DMIC1 Left Channel Source Control 0’b: Latch from falling edge 1’b: Latch from rising edge
sel_dmic1_r_edge	12	R/W	1’h	DMIC1 Right Channel Source Control 0’b: Latch from falling edge 1’b: Latch from rising edge
reserved	11:10	R/W	3’h	Reserved
sel_dmic2_l_edge	9	R/W	0’h	DMIC2 Left Channel Source Control 0’b: Latch from falling edge 1’b: Latch from rising edge
sel_dmic2_r_edge	8	R/W	1’h	DMIC2 Right Channel Source Control 0’b: Latch from falling edge 1’b: Latch from rising edge
sel_dmic_clk	7:5	R/W	0’h	DMIC Clock Rate Control 000’b: 256*fs/2 001’b: 256*fs/3 010’b: 256*fs/4 011’b: 256*fs/6 100’b: 256*fs/8 101’b: 256*fs/12
reserved	4:0	R	0’h	Reserved

8.56. MX-80h: Global Clock Control

Default: 0000’h

Table 73. MX-80h: Global Clock Control

Name	Bits	Read/Write	Reset State	Description
sel_sysclk1	15:14	R/W	0’h	System Clock Source MUX Control 00’b: MCLK 01’b: PLL 10’b: Reserved 11’b: Reserved
sel_pll_sour	13:12	R/W	0’h	PLL Source Selection 00’b: From MCLK 01’b: From BCLK1 10’b: From BCLK2 11’b: Reserved
reserved	11:4	R	0’h	Reserved
sel_pll_pre_div	3	R/W	0’h	PLL Pre-Divider 0’b: ÷ 1 1’b: ÷ 2
reserved	2:0	R	0’h	Reserved

8.57. MX-81h: PLL Control 1

Default: 0000’h

Table 74. MX-81h: PLL Control 1

Name	Bits	Read/Write	Reset State	Description
Pll_n_code	15:7	R/W	0’h	PLL N[8:0] Code 000000000’b: Div 2 000000001’b: Div 3 … 111111111’b: Div 513
Reserved	6:5	R	0’h	Reserved
Pll_k_code	4:0	R/W	0’h	PLL K[4:0] Code 00000’b: Div 2 00001’b: Div 3 … 11111’b: Div 33

8.58. MX-82h: PLL Control 2

Default: 0000’h

Table 75. MX-82h: PLL Control 2

Name	Bits	Read/Write	Reset State	Description
Pll_m_code	15:12	R/W	0’h	PLL M[3:0] Code 0000’b: Div 2 0001’b: Div 3 … 1111’b: Div 17
Pll_m_bypass	11	R/W	0’h	Bypass PLL M Code 0’b : No bypass 1’b : Bypass
Reserved	10:0	R	0’h	Reserved

8.59. MX-83h: ASRC Control 1

Default: 0000’h

Table 76. MX-83h: ASRC Control 1

Name	Bits	Read/Write	Reset State	Description
sel_stereo_asrc	15	R/W	0’h	Mode Select Control for Stereo Filter 0’b : Normal Mode 1’b : ASRC1 Mode
sel_mono_asrc	14	R/W	0’h	Select Control for Mono Filter 0’b : Clk_i2s2_filter 1’b : (Clk_i2s2_filter) / 3
reserved	13	R/W	0’h	Reserved
sel_i2s2_filter	12	R/W	0’h	Select Control for Clk_i2s2_filter 0’b : Normal Mode 1’b : ASRC2 Mode
reserved	11:10	R/W	0’h	Reserved
sel_dmic1_mode	9	R/W	0’h	Select Control for ASRC Mode in DMIC1 Function 0’b : Normal Mode 1’b : ASRC Mode
sel_dmic2_mode	8	R/W	0’h	Select Control for ASRC Mode in DMIC2 Function 0’b : Normal Mode 1’b : ASRC Mode
reserved	7:0	R	0’h	Reserved

8.60. MX-84h: ASRC Control 2

Default: 0000’h

Table 77. MX-84h: ASRC Control 2

Name	Bits	Read/Write	Reset State	Description
sel_mono_da_l_mode	15	R/W	0’h	Select Control for DA_L Mono Filter 0’b: Normal Mode 1’b: ASRC Mode
sel_mono_da_r_mode	14	R/W	0’h	Select Control for DA_R Mono Filter 0’b: Normal Mode 1’b: ASRC Mode
sel_mono_ad_l_mode	13	R/W	0’h	Select Control for AD_L Mono Filter 0’b: Normal Mode 1’b: ASRC Mode
sel_mono_ad_r_mode	12	R/W	0’h	Select Control for AD_R Mono Filter 0’b: Normal Mode 1’b: ASRC Mode
sel_adc_mode	11	R/W	0’h	Select Control for ADC Stereo Filter 0’b: Normal Mode 1’b: ASRC Mode
reserved	10:6	R/W	0’h	Reserved
sel_stereo_dac_mode	5	R/W	0’h	Select Control for DAC Stereo Filter 0’b : Normal Mode 1’b : ASRC Mode
En_i2s1_asrcin_auto_det	4	R/W	0’h	Automatically Detect I2S1 Input Sample Rate 0’b : Disable 1’b : Enable
En_i2s2_asrcin_auto_det	3	R/W	0’h	Automatically Detect I2S2 Input Sample Rate 0’b : Disable 1’b : Enable
reserved	2	R/W	0’h	Reserved
Sel_asrcin_256fs_sys	1:0	R/W	0’h	Select for Pre-System Clock 00’b: 512*48k 01’b: 1024*48k 10’b: 2048*48k 11’b: Reserved

8.61. MX-85h: ASRC Control 3

Default: 0008’h

Table 78. MX-85h: ASRC Control 3

Name	Bits	Read/Write	Reset State	Description
I2s1_asrcin_fsi_rate_manual	15:12	R/W	0’h	Set I2S1 Input Sample Rate 0’h: 48K 1’h: 96k 2’h: 192k 3’h: 32K 4’h: 48K 5’h: 96k 6’h: 192k 7’h: 32K 8’h: 48K 9’h: 96k A’h: 192k B’h: reserve C’h: 22.05K D’h: reserve E’h: 11.025K F’h: reserve

Name	Bits	Read/Write	Reset State	Description
I2s2_asrcin_fsi_rate_manual	11:8	R/W	0'h	Set I2S2 Input Sample Rate 0'h: 48K 1'h: 96k 2'h: 192k 3'h: 32K 4'h: 48K 5'h: 96k 6'h: 192k 7'h: 32K 8'h: 48K 9'h: 96k A'h: 192k B'h: reserve C'h: 22.05K D'h: reserve E'h: 11.025K F'h: reserve
reserved	7:0	R/W	0'h	Reserved

8.62. MX-89h: ASRC Control 4

Default: 0000'h

Table 79. MX-89h: ASRC Control 4

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
i2s1_track_prediv	14:12	R/W	0'h	Set I2S1 Clock Division for Stereo Filter 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16
reserved	11	R	0'h	Reserved
i2s2_track_prediv	10:8	R/W	0'h	Set I2S2 Clock Division for Mono Filter 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16
reserved	7:0	R/W	0'h	Reserved

8.63. MX-8Ah: ASRC Control 5

Default: 0000'h

Table 80. MX-8Ah: ASRC Control 5

Name	Bits	Read/Write	Reset State	Description
asrcin_fsi1_rate	15:12	R	0'h	I2S1 Sample Rate Detection 0000'b: 48k, 44.1k, 32k 0001'b: 96k, 88.2k 0010'b: 192k, 176.4k 0100'b: 24k, 22.05k, 16k 0110'b: 12k, 11.025k, 8k
asrcin_fsi2_rate	11:8	R	0'h	I2S2 Sample Rate Detection 0000'b: 48k, 44.1k, 32k 0001'b: 96k, 88.2k 0010'b: 192k, 176.4k 0100'b: 24k, 22.05k, 16k 0110'b: 12k, 11.025k, 8k
reserved	7:0	R	0'h	Reserved

8.64. MX-8Ch: Class-D Amp OC Control

Default: 0228’h

Table 81. MX-8Ch: Class-D Amp OC Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:10	R	0’h	Reserved
Pow_ocp_clsd	9	R/W	1’h	Class-D Amp Over-Current Sensor Power Control 0’b: Power Down 1’b: Power On
Autopd_clsd	8	R/W	0’h	Class-D Amp Auto Power Down Control When OC 0’b: Disable 1’b: Enable
reserved	7:0	R/W	28’h	Reserved

8.65. MX-8Dh: Class-D Amp Output Control

Default: A800’h

Table 82. MX-8Dh: Class-D Amp Output Control

Name	Bits	Read/Write	Reset State	Description
fbgain_clsd	15:12	R/W	A’h	Class-D Amp AC+DC Ratio Gain Control 1010’b: 3.30 × 1001’b: 3.00 × 1000’b: 2.77× 0111’b: 2.66× 0110’b: 2.55× 0101’b: 2.44× 0100’b: 2.33× 0011’b: 2.22× 0010’b: 2.11× 0001’b: 2.00× 0000’b: 1.94×
reserved	11:0	R/W	800’h	Reserved

8.66. MX-8Eh: HP Amp Control

Default: 0004’h

Table 83. MX-8Eh: HP Amp Control

Name	Bits	Read/Write	Reset State	Description
Smttrig_hp	15	R/W	0’h	Enable Softgen Trigger for Soft Mute Depop 0’b: Disable 1’b: Enable
reserved	14:10	R/W	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
En_smt_l_hp	9	R/W	0'h	Enable HP_L Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
En_smt_r_hp	8	R/W	0'h	Enable HP_R Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
Pdn_hp	7	R/W	0'h	Capless Depop Power Down Control 0'b: Disbale 1'b: Enable
Softgen_rstn	6	R/W	0'h	Reset Softgen to Initialize SOFTP=1 0'b: Disbale 1'b: Reset
Softgen_rstp	5	R/W	0'h	Reset Softgen to Initialize SOFTP=0 0'b: Disbale 1'b: Reset
En_out_hp	4	R/W	0'h	Enable Headphone Output 0'b: Disable 1'b: Enable
Pow_pump_hp	3	R/W	0'h	Charge Pump Power Control 0'b: Power Down 1'b: Power On
En_softgen_hp	2	R/W	1'h	Power On Soft Generator 0'b: Power down 1'b: Power on
reserved	1	R/W	0'h	Reserved
Pow_capless	0	R/W	0'h	HP Amp All Power On Control 0'b: Power Down 1'b: Power On

8.67. MX-8Fh: HP Amp Control 2

Default: 1100'h

Table 84. MX-8Fh: HP Amp Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
Depop_mode_hp	13	R/W	0'h	Select HP Depop Mode 0'b: Depop mode 1 1'b: Depop mode 2
reserved	12:7	R/W	22'h	Reserved
En_depop_mode1	6	R/W	0'h	HP Depop Mode 1 Control 0'b: Disbale 1'b: Enable
reserved	5:0	R/W	0'h	Reserved

8.68. MX-92h: SPKVDD Detection Control

Default: 0000’h

Table 85. MX-92h: SPKVDD Detection Control

Name	Bits	Read/Write	Reset State	Description
en_spk_auto_ratio	15	R/W	0’h	Enable SPKVDD Detection 0’b: Disable 1’b: Enable
en_spk_auto_gain	14	R/W	0’h	Enable Speaker Amp Auto Ratio Gain Control ❶ (Digital will mapping ratio gain table by SPKVDD detection) 0’b: Disable 1’b: Enable
reserved	13:0	R	0’h	Reserved

❶ AC Ratio Gain would be:

Ratio Gain Table (ACVDD with SPKVDD)				
ACVDD	**SPKVDD**	**Voltage Detected Code**	**AC+DC Ratio Gain**	**FBGAIN[3:0]**
1.8V	<3.0V	0000	1.94	0000
	3.0V ~ 3.3V	0001	1.94	0000
	3.3V ~ 3.5V	0010	2	0001
	3.5V ~ 3.6V	0011	2.11	0010
	3.6V ~ 3.8V	0100	2.22	0011
	3.8V ~ 4.0V	0101	2.33	0100
	4.0V ~ 4.2V	0110	2.44	0101
	4.2V ~ 4.4V	0111	2.55	0110
	4.4V ~ 4.6V	1000	2.66	0111
	4.6V ~ 4.8V	1001	2.77	1000
	4.8V ~ 5V	1010	3.00	1001
	>5V	1011	3.30	1010

8.69. MX-93h: MICBIAS Control

Default: 3000’h

Table 86. MX-93h: MICBIAS Control

Name	Bits	Read/Write	Reset State	Description
Sel_micbias1	15	R/W	0’h	MICBIAS1 Output Voltage Control 0’b: 0.9 * MICVDD 1’b: 0.75 * MICVDD
reserved	14:12	R/W	3’h	Reserved
Pow_mic1_ovcd	11	R/W	0’h	MICBIAS1 Short Current Detector Control 0’b: Disable 1’b: Enable

Name	Bits	Read/Write	Reset State	Description
Mic1_ovcd_th_sel	10:9	R/W	0'h	MICBIAS1 Short Current Detector Threshold 00'b: 600uA 01'b: 1500uA 1x'b: 2000uA Note: tolerance is 200uA
reserved	8:0	R/W	0'h	reserved

8.70. MX-B0h: EQ Control 1

Default: 2000'h

Table 87. MX-B0h: EQ Control 1

Name	Bits	Read/Write	Reset State	Description
eq_sour	15	R/W	0'h	EQ Path Control 0'b: DAC path 1'b: ADC path
eq_para_update	14	R/W	0'h	EQ Parameter Update Control 0'b: No action 1'b: Update parameter
reserved	13:7	R/W	40'h	Reserved
sta_hpf2	6	R	0'h	EQ High Pass Filter (HPF2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_hpf1	5	R	0'h	EQ High Pass Filter (HPF1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf4	4	R	0'h	EQ Band-4 (BP4) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf3	3	R	0'h	EQ Band-3 (BP3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf2	2	R	0'h	EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

Name	Bits	Read/Write	Reset State	Description
sta_bpf1	1	R	0'h	EQ Band-1 (BP1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_lpf	0	R	0'h	EQ Low Pass Filter (LPF) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

8.71. MX-B1h: EQ Control 2

Default: 0000'h

Table 88. MX-B1h: EQ Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:9	R	0'h	Reserved
reg_typ_hpf_en	8	R/W	0'h	EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
reg_typ_lpf_en	7	R/W	0'h	EQ Low Pass Filter Mode Control 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
en_hpf2	6	R/W	0'h	EQ High Pass 2nd Butterworth Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
en_hpf1	5	R/W	0'h	EQ High Pass Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
en_bpf4	4	R/W	0'h	EQ Band-4 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_bpf3	3	R/W	0'h	EQ Band-3 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_bpf2	2	R/W	0'h	EQ Band-2 (BP2) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_bpf1	1	R/W	0'h	EQ Band-1 (BP1) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_lpf	0	R/W	0'h	EQ Low Pass Filter (LPF) Filter Control. 0'b: Disabled and reset 1'b: Enabled.

8.72. MX-B4h: DRC/AGC Control 1

Default: 2206’h

Table 89. MX-B4h: DRC/AGC Control 1

Name	Bits	Read/Write	Reset State	Description
sel_drc_agc	15:14	R/W	0’h	DRC/AGC Enable 00’b: Disable DRC/AGC 01’b: Enable DRC to DAC Path 10’b: Disable DRC/AGC 11’b: Enable AGC to ADC Path
update_drc_agc_para m	13	R	1’h	Update DRC/AGC Parameter Write 1’b to update all DRC/AGC parameter
sel_drc_agc_atk	12:8	R/W	2’h	Select DRC/AGC attack rate (0.375dB/TU)❶ 00’h: 83 uSec 01’h: 0.167 mSec … 10’h: 5.46 Sec Others: Reserved
Drc_agc_rate_sel	7:5	R/W	0’h	DRC/AGC Rate Control for Sample Rate Change❸ 001’b: 48kHz 010’b: 96kHz 011’b: 192kHz 101’b: 44.1kHz 110’b: 88.2kHz 111’b: 176.4kHz Others: Reserved
sel_rc_rate	4:0	R/W	6’h	Select DRC/AGC recovery rate (0.375dB/TU)❷ 00’h: 83 uSec 01’h: 0.167 mSec … 10’h: 5.46 Sec Others: Reserved

❶ attack time=(4*2^n)/Sample_Rate, n=MX-B4[12:8], default=0.33mS
❷ recovery time=(4*2^n)/Sample_Rate, n= MX-B4 [4:0], default=5.3mS
❸ When change I2S’s sample rate, the DRC/AGC rate control is need to be changed same with I2S’s sample rate. When change the DRC/AGC rate, the parameter of DRC/AGC isn’t need be modified.
When I2S’s sample rate is below 48kHz, that need to set the DRC/AGC rate to 48kHz and re-calculate the DRC/AGC’s parameter by I2S’s sample rate.

8.73. MX-B5h: DRC/AGC Control 2

Default: 1F00’h

Table 90. MX-B5h: DRC/AGC Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
sel_drc_agc_post_bst	13:8	R/W	1f’h	DRC/AGC Digital Post-Boost Gain (0.375dB/step)❶ 00’h= -11.625dB …….. 3F’h= 12dB Others: Reserved
En_drc_agc_compress	7	R/W	0’h	DRC Compression Function Control 0’b: Disable 1’b: Enable
Sel_ratio	6:5	R/W	0’h	DRC Compression Ratio Selection 00’b: 1:1 01’b: 1:2 10’b: 1:3 11’b: 1:4
sel_drc_agc_pre_bst	4:0	R/W	0’h	DRC/AGC Digital Pre-Boost GAin (1.5dB/step)❷ 00’h= 0dB 01’h= 1.5dB 02’h= 3dB 03’h= 4.5dB …….. 13’h= 28.5dBFS Others: Reserved

❶Gain table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-11.625	16	10	-5.625	32	20	0.375	48	30	6.375	64	40	
1	1	-11.25	17	11	-5.25	33	21	0.75	49	31	6.75	65	41	
2	2	-10.875	18	12	-4.875	34	22	1.125	50	32	7.125	66	42	
3	3	-10.5	19	13	-4.5	35	23	1.5	51	33	7.5	67	43	
4	4	-10.125	20	14	-4.125	36	24	1.875	52	34	7.875	68	44	
5	5	-9.75	21	15	-3.75	37	25	2.25	53	35	8.25	69	45	

6	6	-9.375	22	16	-3.375	38	26	2.625	54	36	8.625	70	46	
7	7	-9	23	17	-3	39	27	3	55	37	9	71	47	
8	8	-8.625	24	18	-2.625	40	28	3.375	56	38	9.375	72	48	
9	9	-8.25	25	19	-2.25	41	29	3.75	57	39	9.75	73	49	
10	A	-7.875	26	1A	-1.875	42	2A	4.125	58	3A	10.125	74	4A	
11	B	-7.5	27	1B	-1.5	43	2B	4.5	59	3B	10.5	75	4B	
12	C	-7.125	28	1C	-1.125	44	2C	4.875	60	3C	10.875	76	4C	
13	D	-6.75	29	1D	-0.75	45	2D	5.25	61	3D	11.25			
14	E	-6.375	30	1E	-0.375	46	2E	5.625	62	3E	11.625			
15	F	-6	31	1F	0	47	2F	6	63	3F	12			

❷

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	0	16	10	24
1	1	1.5	17	11	25.5
2	2	3	18	12	27
3	3	4.5	19	13	28.5
4	4	6	20	14	
5	5	7.5	21	15	
6	6	9	22	16	
7	7	10.5	23	17	
8	8	12	24	18	
9	9	13.5	25	19	
10	A	15	26	1A	
11	B	16.5	27	1B	
12	C	18	28	1C	
13	D	19.5	29	1D	
14	E	21	30	1E	
15	F	22.5	31	1F	

8.74. MX-B6h: DRC/AGC Control 3

Default: 0000’h

Table 91. MX-B6h: DRC/AGC Control 3

Name	Bits	Read/Write	Reset State	Description
Noise_gate_boost	15:12	R/W	0’h	Select Compensation Gain When Signal is Below Noise Gate 0’h: 0dB 1’h: 3dB 2’h: 6dB … E’h: 42dB F’h: 45dB
sel_drc_agc_thmax	11:7	R/W	0’h	DRC/AGC Limiter Level (1.5dB/step) 00’h= 0dBFS 01’h= -1.5dBFS 02’h= -3dBFS 03’h= -4.5dBFS … 1F’h= -46.5dBFS
en_drc_agc_noise_gate	6	R/W	0’h	Enable Noise Gate function 0’b: Diaable 1’b: Enable
En_drc_agc_noise_gate_hold	5	R/W	0’h	Enable Noise Gate Hold Data Function 0’b: Disable 1’b: Enable
sel_drc_agc_noise_th	4:0	R/W	0’h	Noise Gate Threshold (-1.5dB/step) 00’h: -36dBFS 01’h: -375dBFS …….. 1F’h: -82.5 dBFS

8.75. MX-BBh: Jack Detection Control 1

Default: 0000’h

Table 92. MX-BBh: Jack Detection Control 1

Name	Bits	Read/Write	Reset State	Description
sel_jd_source	15:13	R/W	0’h	Jack Detect Selection 000’b: OFF 001’b: GPIO1 010’b: JD1 and enable IN1N pin share 011’b: JD2 and enable IN2N pin share 100’b: GPIO2 Others: Reserved
reserved	12	R	0’h	Reserved
en_jd_hpo	11	R/W	0’h	Enable Jack Detect Trigger HPOUT 0’b: Disable 1’b: Enable
polarity_jd_tri_hpo	10	R/W	0’h	Select Jack Detect Polarity Trigger HPOUT 0’b: Low trigger 1’b: High trigger
en_jd_spo_l	9	R/W	0’h	Enable Jack Detect Trigger SPK_OUT_LP/LN 0’b: Disable 1’b: Enable
polarity_jd_tri_spo_l	8	R/W	0’h	Select Jack Detect Polarity Trigger SPO_LP/LN 0’b: Low trigger 1’b: High trigger
en_jd_spo_r	7	R/W	0’h	Enable Jack Detect Trigger SPO_RP/RN 0’b: Disable 1’b: Enable
polarity_jd_tri_spo_r	6	R/W	0’h	Select Jack Detect Polarity Trigger SPO_RP/RN 0’b: Low trigger 1’b: High trigger
en_jd_mono	5	R/W	0’h	Enable Jack Detect Trigger MONOOUT 0’b: Disable 1’b: Enable
polarity_jd_tri_mono	4	R/W	0’h	Select Jack Detect Polarity Trigger MONOOUT 0’b: Low trigger 1’b: High trigger
en_jd_lout	3	R/W	0’h	Enable Jack Detect Trigger LOUT 0’b: Disable 1’b: Enable
polarity_jd_tri_lout	2	R/W	0’h	Select Jack Detect Polarity Trigger LOUT 0’b: Low trigger 1’b: High trigger
reserved	1:0	R/W	0’h	reserved

8.76. MX-BCh: Jack Detection Control 2

Default: 0000’h

Table 93. MX-BCh: Jack Detection Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:6	R	0’h	Reserved
en_snc_det	5:4	R/W	0’h	Select Detection Source for SNC On/Off Mode 00’b: Disable 01’b: From MICBIAS1 Over-Current (sta_micbias1_ovcd) 10’b: Reserved 11’b: From JD (sta_jd_internal)
polarity_snc_det	3	R/W	0’h	Select SNC Detection Polarity Trigger for SNC On/Off Mode 0’b: Low trigger 1’b: High trigger
En_sncmon_det	2:1	R/W	0’h	Enable Detection Source for SNC Monitor Mode 00’b: Disable 01’b: From MICBIAS1 Over-Current (sta_micbias1_ovcd) 10’b: Reserved 11’b: From JD (sta_jd_internal)
polarity_sncmon_det	0	R/W	0’h	Select SNCMON Detection Polarity Trigger for SNC Monitor Mode 0: Low trigger 1: High trigger

8.77. MX-BDh: IRQ Control 1

Default: 0000’h

Table 94. MX-BDh: IRQ Control 1

Name	Bits	Read/Write	Reset State	Description
en_irq_jd	15	R/W	0’h	IRQ Output Source Configure of Jack Detection Status 0’b: Disable 1’b: Enable
en_irq_ovtd	14	R/W	0’h	IRQ Output Source Configure of Over Temperature Status 0’b: Disable 1’b: Enable
en_jd_sticky	13	R/W	0’h	Sticky Control for Jack Detect 0’b: Disable 1’b: Enable
en_ovt_sticky	12	R/W	0’h	Sticky Control for Over Temperature 0’b: Disable 1’b: Enable
inv_jd	11	R/W	0’h	Jack Detection Status Polarity 0’b: Normal 1’b: Output Invert

Name	Bits	Read/Write	Reset State	Description
inv_ovtd	10	R/W	0'h	Over Temperature Status Polarity 0'b: Normal 1'b: Output Invert
reserved	9:0	R	0'h	Reserved

8.78. MX-BEh: IRQ Control 2

Default: 0000'h

Table 95. MX-BEh: IRQ Control 2

Name	Bits	Read/Write	Reset State	Description
en_irq_micbias1_ovcd	15	R/W	0'h	IRQ Output Source Configure of MICBIAS1 Over Current Status 0'b: Disable 1'b: Enable
reserved	14:12	R/W	0'h	Reserved
en_micbias1_ovcd_sticky	11	R/W	0'h	Sticky Control for MICBIAS1 Over Current 0'b: Disable 1'b: Enable
reserved	10:8	R/W	0'h	Reserved
inv_micbias1_ovcd	7	R/W	0'h	MICBIAS1 over current status polarity 0'b: Normal 1'b: Output Invert
reserved	6:4	R	0'h	Reserved
Ovc_micbias1	3	R	0'h	MICBIAS1 Over Current Status Read: return status of each status pin Write: Write '0' to clear stick bit
Reserved	2:0	R	0'h	Reserved

8.79. MX-BFh: GPIO and Internal Status

Default: 0000'h

Table 96. MX-BFh: GPIO and Internal Status

Name	Bits	Read/Write	Reset State	Description
reserved	15:9	R	0'h	Reserved
sta_gpio1	8	R	0'h	GPIO1 Pin Status Read: return status of each GPIO pin
sta_gpio2	7	R	0'h	GPIO2 Pin Status Read: return status of each GPIO pin
reserved	6:5	R	0'h	reserved
sta_jd_internal	4	R	0'h	JD Status Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit

Name	Bits	Read/Write	Reset State	Description
ovt_status	3	R	0'h	Over Temperature Status❶ Read: return status of each status pin Write: Write '0' to clear stick bit
reserved	2:1	R	0'h	Reserved
sta_ovcd	0	R	0'h	Speaker amplifier over current status Read: return status of each status pin

8.80. MX-C0h: GPIO Control 1

Default: 0400'h

Table 97. MX-C0h: GPIO Control 1

Name	Bits	Read/Write	Reset State	Description
sel_gpio1_type	15	R/W	0'h	GPIO1 Pin Function Select 0'b: GPIO1 1'b: IRQ output
sel_gpio2_type	14	R/W	0'h	GPIO2 Pin Function Select 0'b: GPIO2 1'b: DMIC1_SCL
reserved	13:0	R/W	400'h	Reserved

8.81. MX-C2h: GPIO Control 2

Default: 0000'h

Table 98. MX-C2h: GPIO Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:6	R/W	0'h	Reserved
sel_gpio2	5	R/W	0'h	GPIO2 Pin Configuration 0'b: Input 1'b: Output
sel_gpio2_logic	4	R/W	0'h	GPIO2 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio2	3	R/W	0'h	GPIO2 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio1	2	R/W	0'h	GPIO1 Pin Configuration 0'b: Input 1'b: Output
sel_gpio1_logic	1	R/W	0'h	GPIO1 Output Pin Control 0'b: Drive Low 1'b: Drive High

Name	Bits	Read/Write	Reset State	Description
inv_gpio1	0	R/W	0'h	GPIO1 Pin Polarity 0'b: Normal 1'b: Output Invert

8.82. MX-C4h: Voice DSP Control 1

Default: 0000'h

Table 99. MX-C4h: Voice DSP Control 1

Name	Bits	Read/Write	Reset State	Description
Aec_addr	15:0	R/W	0'h	Voice DSP Register Address

8.83. MX-C5h: Voice DSP Control 2

Default: 0000'h

Table 100. MX-C5h: Voice DSP Control 2

Name	Bits	Read/Write	Reset State	Description
Aec_data	15:0	R/W	0'h	Voice DSP Register Data

8.84. MX-C6h: Voice DSP Control 3

Default: 2000'h

Table 101. MX-C6h: Voice DSP Control 3

Name	Bits	Read/Write	Reset State	Description
Aec_busy	15	R	0'h	Voice DSP I2C Busy Flag 0'b: Normal 1'b: Busy
reserved	14	R/W	0'h	reserved
fm34_clk_sel	13:12	R/W	2'h	Voice DSP Clock Source Select 00'b: 12.288MHz (Internal I2C SCL = 384KHz) 01'b: 6.144MHz (Internal I2C SCL = 192KHz) 10'b: 3.072MHz (Internal I2C SCL = 96KHz) 11'b: 2.048MHz (Internal I2C SCL = 64KHz)
f_pdb	11	R/W	0'h	Power Down Control for Voice DSP 0'b: Power Down 1'b: Power On
f_prst	10	R/W	0'h	Reset Control for Voice DSP 0'b: Reset 1'b: Normal

Name	Bits	Read/Write	Reset State	Description
aec_read	9	R/W	0'h	Voice DSP Read Enable 0'b: Disable 1'b: Enable
aec_write	8	R/W	0'h	Voice DSP Write Enable 0'b: Disable 1'b: Enable
reserved	7:0	R/W	0'h	Reserved

8.85. MX-C8h: Programmable Register Array Control 1

Default: 0000'h

Table 102. MX-C8h: Programmable Register Array Control 1

Name	Bits	Read/Write	Reset State	Description
sequencer	15:12	R/W	0'h	Register Sequencer 0 ~ 16
sta_seq1_ready	11	R	0'h	The Processing Status of Sequence-1 0'b: Sequence-1 is running 1'b: Sequence-1 is finished
sta_seq2_ready	10	R	0'h	The Processing Status of Sequence-2 0'b: Sequence-2 is running 1'b: Sequence-2 is finished
reg_level	9	R/W	0'h	Register Level Selection 0'b: MX register 1'b: PR register
sequence_write	8	R/W	0'h	Write Sequences to Programmable Table Write "1" to execute, then clear to "0"
reg_index	7:0	R/W	00'h	Register Index 00'h ~ FF'h

8.86. MX-C9h: Programmable Register Array Control 2

Default: 0000'h

Table 103. MX-C9h: Programmable Register Array Control 2

Name	Bits	Read/Write	Reset State	Description
Reg_data	15:0	R/W	0'h	Register Data 0000'h ~ FFFF'h

8.87. MX-CAh: Programmable Register Array Control 3

Default: 0000'h

Table 104. MX-CAh: Programmable Register Array Control 3

Name	Bits	Read/Write	Reset State	Description
sequence_delay	15:8	R/W	00'h	Delay Time Between the Sequencer 00'h: No delay time, delay function off 01'h ~ FF'h (100us ~ 100ms)
pro_reg_en	7	R/W	0'h	Control The Programmable Register 0'b: Disable 1'b: Enable
sequence_run_1	6	R	0'h	Run Sequence-1 from Programmable Table Write "1" to execute, then clear to "0" 0'b: Normal 1'b: Write
sequence_run_2	5	R	0'h	Run Sequence-2 from Programmable Table Write "1" to execute, then clear to "0" 0'b: Normal 1'b: Write
reserved	4:0	R	0'h	Reserved

8.88. MX-CBh: Programmable Register Array Control 4

Default: 0000'h

Table 105. MX-CBh: Programmable Register Array Control 4

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0'h	Reserved
sequence_1_start	11:8	R/W	00'h	Start for Sequence-1 00'h ~ 15'h
reserved	7:4	R	0'h	Reserved
sequence_1_end	3:0	R/W	00'h	End for Sequence-1 00'h ~ 15'h

8.89. MX-CCh: Programmable Register Array Control 5

Default: 0000'h

Table 106. MX-CCh: Programmable Register Array Control 5

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0'h	Reserved
sequence_2_start	11:8	R/W	00'h	Start for Sequence-2 00'h ~ 15'h
reserved	7:4	R	0'h	Reserved
sequence_2_end	3:0	R/W	00'h	End for Sequence-2 00'h ~ 15'h

8.90. MX-CFh: SounzReal BassBack Control

Default: 0013’h

Table 107. MX-CFh: SounzReal BassBack Control

Name	Bits	Read/Write	Reset State	Description
En_bb	15	R/W	0’h	Enable BassBack Function 0’b: Disable 1’b: Enable
Sel_bb_coef	14:12	R/W	0’h	Select Control for BassBack Coefficient Type 000’b: Type A 001’b: Type B 010’b: Type C 011’b: Type D 1xx’b: Reserved
Reserved	11:6	R	0’h	Reserved
Bb_boost_gain	5:0	R/W	13’h	Select Control BassBack Boost Gain 000001’b: 1.5dB 000010’b: 3dB …… 010011’b: 24dB …… 011111’b: 42dB, with 1.5dB/Step

8.91. MX-D9h: Soft Volume & ZCD Control

Default: 0809’h

Table 108. MX-D9h: Soft Volume & ZCD Control

Name	Bits	Read/Write	Reset State	Description
en_softvol	15	R/W	0’h	Digital Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_spo_svol	14	R/W	0’h	SPOVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_o_svol	13	R/W	0’h	OUTVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_hpo_svol	12	R/W	0’h	HPOVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_zcd_digital	11	R/W	1’h	Digital Volume Zero Crossing Detection Control 0’b: Disable 1’b: Enable
pow_zcd	10	R/W	0’h	Power On Zero Crossing 0’b: Power Down 1’b: Power On

Name	Bits	Read/Write	Reset State	Description
En_zcd_recmixl	9	R/W	0'h	RECMIXL Mute/Un-Mute ZCD Control 0'b: Disable 1'b: Enable
En_zcd_recmixr	8	R/W	0'h	RECMIXR Mute/Un-Mute ZCD Control 0'b: Disable 1'b: Enable
En_zcd_spkmixl	7	R/W	0'h	SPKMIXL Mute/Un-Mute ZCD Control 0'b: Disable 1'b: Enable
En_zcd_spkmixr	6	R/W	0'h	SPKMIXR Mute/Un-Mute ZCD Control 0'b: Disable 1'b: Enable
En_zcd_outmixl	5	R/W	0'h	OUTMIXL Mute/Un-Mute ZCD Control 0'b: Disable 1'b: Enable
En_zcd_outmixr	4	R/W	0'h	OUTMIXR Mute/Un-Mute ZCD Control 0'b: Disable 1'b: Enable
sel_svol	3:0	R/W	9'h	Soft Volume Change Delay Time 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved Note: SVSYNC=1/Fs, Step:-1.5dBFS

8.92. MX-FAh: General Control 1

Default: 3400'h

Table 109. MX-FAh: General Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R/W	0'h	Reserved
En_lout_df	14	R/W	0'h	Enable Differential Output for LOUT 0'b: Disable 1'b: Enable LOUTL => LOUTL LOUTR => (inv)LOUTR
Mu_mono_adc_vol_l	13	R/W	1'h	Digital Mute Control for Mono Left ADC Filter to I2S 0'b: Un-Mute 1'b: Mute

Name	Bits	Read/Write	Reset State	Description
Mu_mono_adc_vol_r	12	R/W	1'h	Digital Mute Control for Mono Right ADC Filter to I2S 0'b: Un-Mute 1'b: Mute
Reserved	11:10	R/W	1'h	Reserved
En_in1_se	9	R/W	0'h	IN1 Single-End Input Control 0'b: Disable 1'b: Enable
En_in2_se	8	R/W	0'h	IN2 Single-End Input Control 0'b: Disable 1'b: Enable
Reserved	7	R/W	0'h	Reserved
Sel_clk_ad_src	6	R/W	0'h	Clock Select for Stereo ADC 0'b: Normal mode 1'b: Asynchronous mode
Sel_clk_ad_src_mono_l	5	R/W	0'h	Clock Select for Left Mono ADC 0'b: Normal mode 1'b: Asynchronous mode
Sel_clk_ad_src_mono_r	4	R/W	0'h	Clock Select for Right Mono ADC 0'b: Normal mode 1'b: Asynchronous mode
reserved	3:1	R/W	0'h	Reserved
Digital_gate_ctrl	0'h	R/W	0'h	I2S Clock Gating Control 0'b: Gating input clock 0'b: Enable input clock

8.93. MX-FBh: General Control 2

Default: 0000'h

Table 110. MX-FBh: General Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R/W	0'h	Reserved
En_irq_jd2	12	R/W	0'h	IRQ Output Source Configuration for JD2 0'b: Disable 1'b: Enable
Sta_jd2_internal	11	R	0'h	JD2 Status Read: Return status of JD2 Write: Write '0' to clean sticky bit
Inv_jd2	10	R/W	0'h	JD2 Status Polarity 0'b: Normal 1'b: Output Invert
En_jd2_sticky	9	R/W	0'h	Sticky Control for JD2 0'b: Disable 1'b: Enable
En_jd2	8	R/W	0'h	Enable JD2 Function for Extra JD Status 0'b: Disable 1'b: Enable
Reserved	7:6	R/W	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
	5:4	R/W	0’h	For DSP Interface I2S Format Control 00’b: Disable 01’b: 19.2MHz/50FS/48kHz 10’b: 19.2MHz/50FS/16kHz 11’b: 19.2MHz/50FS/8kHz
Sel_rxdp	3	R/W	0’h	Voice DSP RXDP Source Selection 0’b: From IF2_ADC 1’b: From Stereo_ADC
	2	R/W	0’h	I2S1 Format Control (19.2MHz/50FS/48kHz) 0’b: Disable 1’b: Enable
	1	R/W	0’h	I2S2 Format Control (19.2MHz/50FS/48kHz) 0’b: Disable 1’b: Enable
Reserved	0	R/W	0’h	Reserved

8.94. PR-3Dh: ADC/DAC RESET Control

Default: 2400’h

Table 111. PR-3Dh: ADC/DAC RESET Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R/W	1’h	Reserved
En_ckgen_adc	12	R/W	0’h	Enable ADC Clock Generator 0’b: Disable 1’b: Enable
Reserved	11:10	R/W	1’h	Reserved
En_ckgen_dac	9	R/W	0’h	Enable DAC Clock Generator 0’b: Disable 1’b: Enable
Reserved	8:0	R/W	0’h	Reserved

8.95. PR-A0h: EQ Low Pass Filter Coefficient (LPF:a1)

Default: 1C10’h

Table 112. PR-A0h: EQ Low Pass Filter Coefficient (LPF:a1)

Name	Bits	Read/Write	Reset State	Description
lpf_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.96. PR-A1h: EQ Low Pass Filter Gain (LPF:H0)

Default: 01F4'h

Table 113. PR-A1h: EQ Low Pass Filter Gain (LPF:H0)

Name	Bits	Read/Write	Reset State	Description
lpf_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.97. PR-A2h: EQ Band 1 Coefficient (BPF1:a1)

Default: C5E9'h

Table 114. PR-A2h: EQ Band 1 Coefficient (BPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf1_a1	15:0	R/W	C5E9'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.98. PR-A3h: EQ Band 1 Coefficient (BPF1:a2)

Default: 1A98'h

Table 115. PR-A3h: EQ Band 1 Coefficient (BPF1:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf1_a2	15:0	R/W	1A98'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.99. PR-A4h: EQ Band 1 Gain (BPF1:H0)

Default: 1D2C'h

Table 116. PR-A4h: EQ Band 1 Gain (BPF1:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf1_h0	15:0	R/W	1D2C'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.100. PR-A5h: EQ Band 2 Coefficient (BPF2:a1)

Default: C882'h

Table 117. PR-A5h: EQ Band 2 Coefficient (BPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a1	15:0	R/W	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.101. PR-A6h: EQ Band 2 Coefficient (BPF2:a2)

Default: 1C10'h

Table 118. PR-A6h: EQ Band 2 Coefficient (BPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a2	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.102. PR-A7h: EQ Band 2 Gain (BPF2:H0)

Default: 01F4'h

Table 119. PR-A7h: EQ Band 2 Gain (BPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf2_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.103. PR-A8h: EQ Band 3 Coefficient (BPF3:a1)

Default: E904'h

Table 120. PR-A8h: EQ Band 3 Coefficient (BPF3:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.104. PR-A9h: EQ Band 3 Coefficient (BPF3:a2)

Default: 1C10’h

Table 121. PR-A9h: EQ Band 3 Coefficient (BPF3:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.105. PR-AAh: EQ Band 3 Gain (BPF3:H0)

Default: 01F4’h

Table 122. PR-AAh: EQ Band 3 Gain (BPF3:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf3_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.106. PR-ABh: EQ Band 4 Coefficient (BPF4:a1)

Default: E904’h

Table 123. PR-ABh: EQ Band 4 Coefficient (BPF4:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.107. PR-ACh: EQ Band 4 Coefficient (BPF4:a2)

Default: 1C10’h

Table 124. PR-ACh: EQ Band 4 Coefficient (BPF4:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.108. PR-ADh: EQ Band 4 Gain (BPF4:H0)

Default: 01F4'h

Table 125. PR-ADh: EQ Band 4 Gain (BPF4:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf4_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.109. PR-AEh: EQ High Pass Filter 1 Coefficient (HPF1:a1)

Default: 1C10'h

Table 126. PR-AEh: EQ High Pass Filter 1 Coefficient (HPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf1_a1	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.110. PR-AFh: EQ High Pass Filter 1 Gain (HPF1:H0)

Default: 01F4'h

Table 127. PR-AFh: EQ High Pass Filter 1 Gain (HPF1:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf1_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.111. PR-B0h: EQ High Pass Filter 2 Coefficient (HPF2:a1)

Default: 2000'h

Table 128. PR-B0h: EQ High Pass Filter 2 Coefficient (HPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a1	15:0	R/W	2000'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.112. PR-B1h: EQ High Pass Filter 2 Coefficient (HPF2:a2)

Default: 0000’h

Table 129. PR-B1h: EQ High Pass Filter 2 Coefficient (HPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.113. PR-B2h: EQ High Pass Filter 2 Gain (HPF2:H0)

Default: 2000’h

Table 130. PR-B2h: EQ High Pass Filter 2 Gain (HPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf2_h0	15:0	R/W	2000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.114. MX-FEh: Vendor ID

Default: 10EC’h

Table 131. MX-FEh: Vendor ID

Name	Bits	Read/Write	Reset State	Description
Vendor_id	15:0	R	10EC’h	Vendor ID

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 132. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	1.4	V
Analog	AVDD	-0.3	-	1.98	V
Analog	DACREF	-0.3	-	1.98	V
Headphone	CPVDD	-0.3	-	1.98	V
Micbias	MICVDD	-0.3	-	3.63	V
Speaker	SPKVDD	-0.3	-	7[1]	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

Note 1: SPKVDD=5V with 3.5% duty cycle Power bouncing up to SPKVDD=7V is acceptable.

9.1.2. Recommended Operating Conditions

Table 133. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.71	1.8	3.6	V
Digital Core	DCVDD	1.1	1.2	1.3	V
Analog	AVDD	1.71	1.8	1.9	V
Analog	DACREF	1.71	1.8	1.9	V
Headphone	CPVDD	1.71	1.8	1.9	V
Micbias	MICVDD	3.0	3.3	3.6	V
Speaker	SPKVDD[1]	3.0	3.6/5.0	5.5	V

Note 1: A 10µF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin.

9.1.3. Static Characteristics

Table 134. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Output Buffer High Drive Current	-	0.6	1.8	4.3	mA
Output Buffer Low Drive Current	-	0.7	2.1	4.8	mA
Input Buffer Pull-Up Resistor	-	55	110	270	KΩ
Input Buffer Pull-Down Resistor	-	63	130	300	KΩ

Note: DBVDD=1.8V, DCVDD=1.2V, $T_{ambient}$=40°C.

9.2. Analog Performance Characteristics

Table 135. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs (Single-ended)	-	0.6	-	Vrms
MIC Inputs (Single-ended)	-	0.6	-	Vrms
MIC Inputs (Differential)	-	1.2	-	Vrms
Full Scale Output Voltage				
Line Outputs (Single-ended)	-	1.0	-	Vrms
Line Outputs (Differential)	-	1.0	-	Vrms
Headphone Amplifiers Outputs (For 10KOhm Load)	-	1.0	-	Vrms
Headphone Amplifiers Outputs (For 16Ohm Load)		0.7		Vrms
Speaker Amplifiers Outputs (SPKVDD=5.0V with 4Ω Load, 1% THD+N)		2.9		Vrms
S/N Ratio				
Stereo DAC Direct to HP_L/R with 32Ohm	-	100	102	dBA
Stereo DAC Direct to SPK_OUT with 8Ohm/5V (Differential)	-	95		dBA
Line_In to Stereo ADC with 0dB (Single-end)		94	95	dBA
MIC_In to Stereo ADC with 0dB (Differential or Single-end)		94	95	dBA
MIC_In to Stereo ADC with 20dB and MICBIAS (Differential or Single-end)		89		dBA
MIC_In to Stereo ADC with 40dB and MICBIAS (Differential or Single-end)		78		dBA
MIC_In to Stereo ADC with 50dB and MICBIAS (Differential or Single-end)		68		dBA
Total Harmonic Distortion + Noise				
DAC Direct to HP_L/R with 16Ohm				
Po = 20mW/CH		-81	-83	dB
DAC Direct to HP_L/R with 10KOhm				
-3dBFS		-86		dB
DAC Direct to MONO_P/N with 16Ohm				
Po = 50mW/CH		-70		dB
Po = 60mW/CH		-65		dB
DAC Direct to SPK_OUT (Differential)				
Po=1.2W (5V/8Ohm)		<1		%
Po=2.1W (5V/4Ohm)		<1		%
Po=920mW (4.2V/8Ohm)		<1		%
Po=650mW (3.6V/8Ohm)		<1		%
Line_In to Stereo ADC with 0dB (Single-end)		-83		dB
MIC_In to Stereo ADC with 0dB (Differential or Single-end)		-83		dB
MIC_In to Stereo ADC with 20dB and MICBIAS (Differential or		-81		dB

Parameter	Min	Typ	Max	Units
Single-end)				
MIC_In to Stereo ADC with 40dB and MICBIAS (Differential or Single-end)		-74		dB
MIC_In to Stereo ADC with 50dB and MICBIAS (Differential or Single-end)		-65		dB
PSRR (Vripple=100mV, <=1KHz)				
DAC to Headphone Amplifier		60		dB
DAC to BTL Speaker Amplifier		65		dB
MIC/LINE_IN to ADC		60		dB
BTL Speaker Amplifier Efficiency				
(f_{IN}=1kHz, 4Ω Load, SPKVDD=5.0V, Output Power=2.8W, with LC filter, L=33uH and C=1uF)				
Class-D (Stereo Mode)	-	88	-	%
Power Consumption (Slave I2S Mode, 24-bit, SR: 44.1KHz)				
P_power down (No Clock Input)		<150		uW
P_playback (Stereo DAC to HP_OUT with 16 Ohm Load, With Clock, play silence)		<= 5		mW
P_playback (Stereo DAC to HP_OUT with 16 Ohm Load, With Clock, Po=1mW/CH)		<= 13		mW
P_playback (Stereo DAC to SPK_OUT with 8 Ohm Load, With Clock, play silence)		< 19		mW
P_record (LINE_IN to Stereo ADC, With Clock)		< 8		mW
Power Down Current				
I_{DDA} (Analog Block)	-	-	10	µA
I_{DDD} (Digital Block)	-	-	30	µA
MICBIAS1 Output Voltage				
Setting 1	-	0.9*MICVDD	-	V
Setting 2	-	0.75*MICVDD	-	V
MICBIAS1 Drive Current				
MICBIAS = 0.9*LDO2_O	-	4	-	mA

Note: Standard test conditions:
$T_{ambient}$=25°C
DBVDD=1.8V
DCVDD=1.2V
AVDD=1.8V
MICVDD=3.3V
CPVDD=1.8V
SPKVDD=5.0V or 4.2V or 3.6V.
1kHz input sine wave; PCM Sampling frequency=48kHz; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation
dBA: with A-Weighting

9.3. Signal Timing

9.3.1. I²C Control Interface

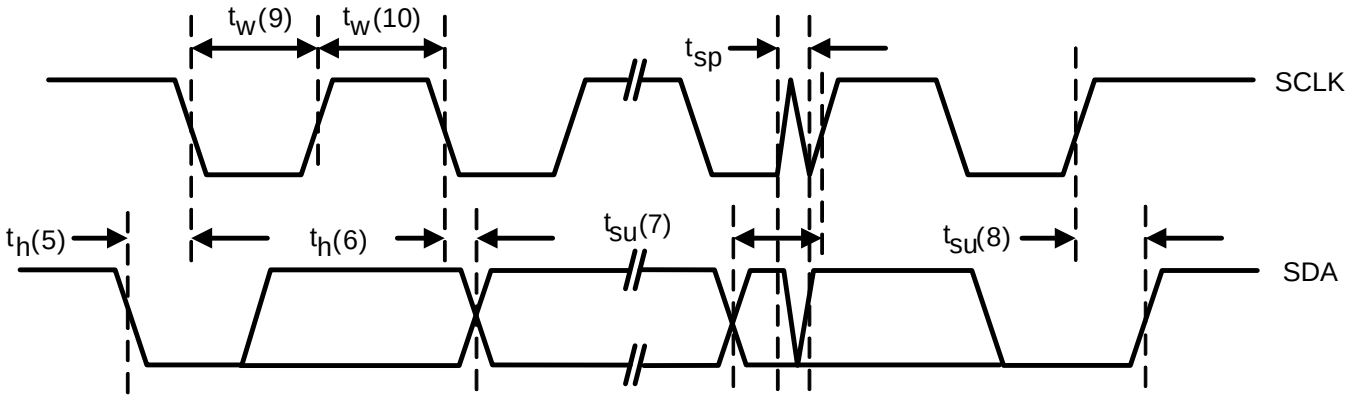


Figure 28. I²C Control Interface

Table 136. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	F	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

9.3.2. I²S/PCM Interface Master Mode

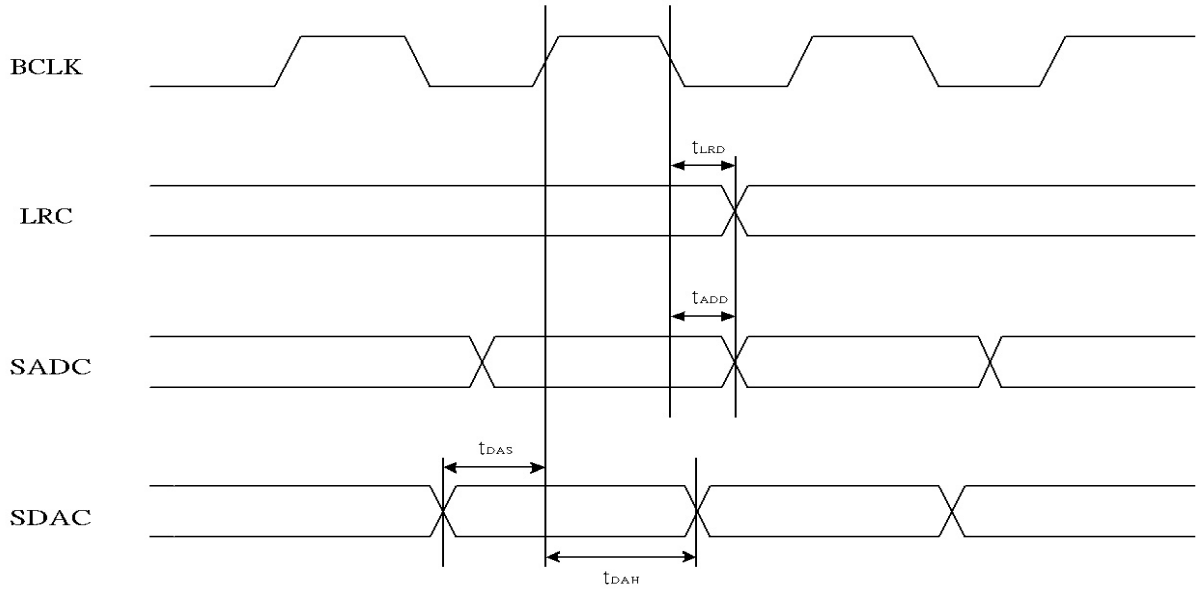


Figure 29. Timing of I²S/PCM Master Mode

Table 137. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

9.3.3. I²S/PCM Interface Slave Mode

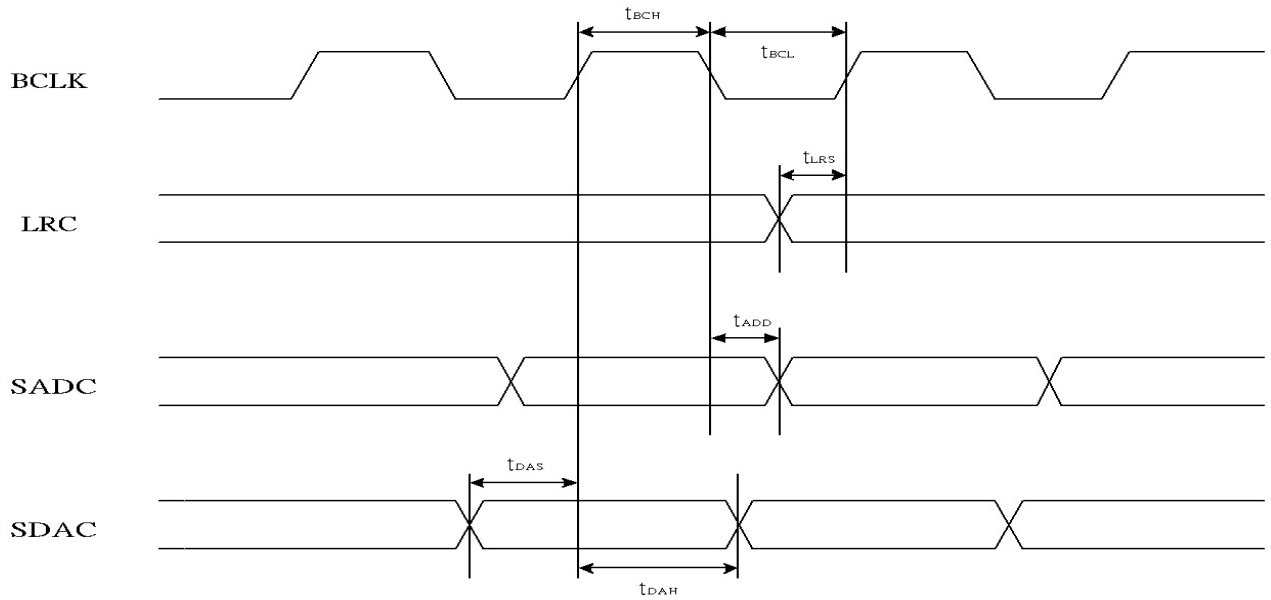
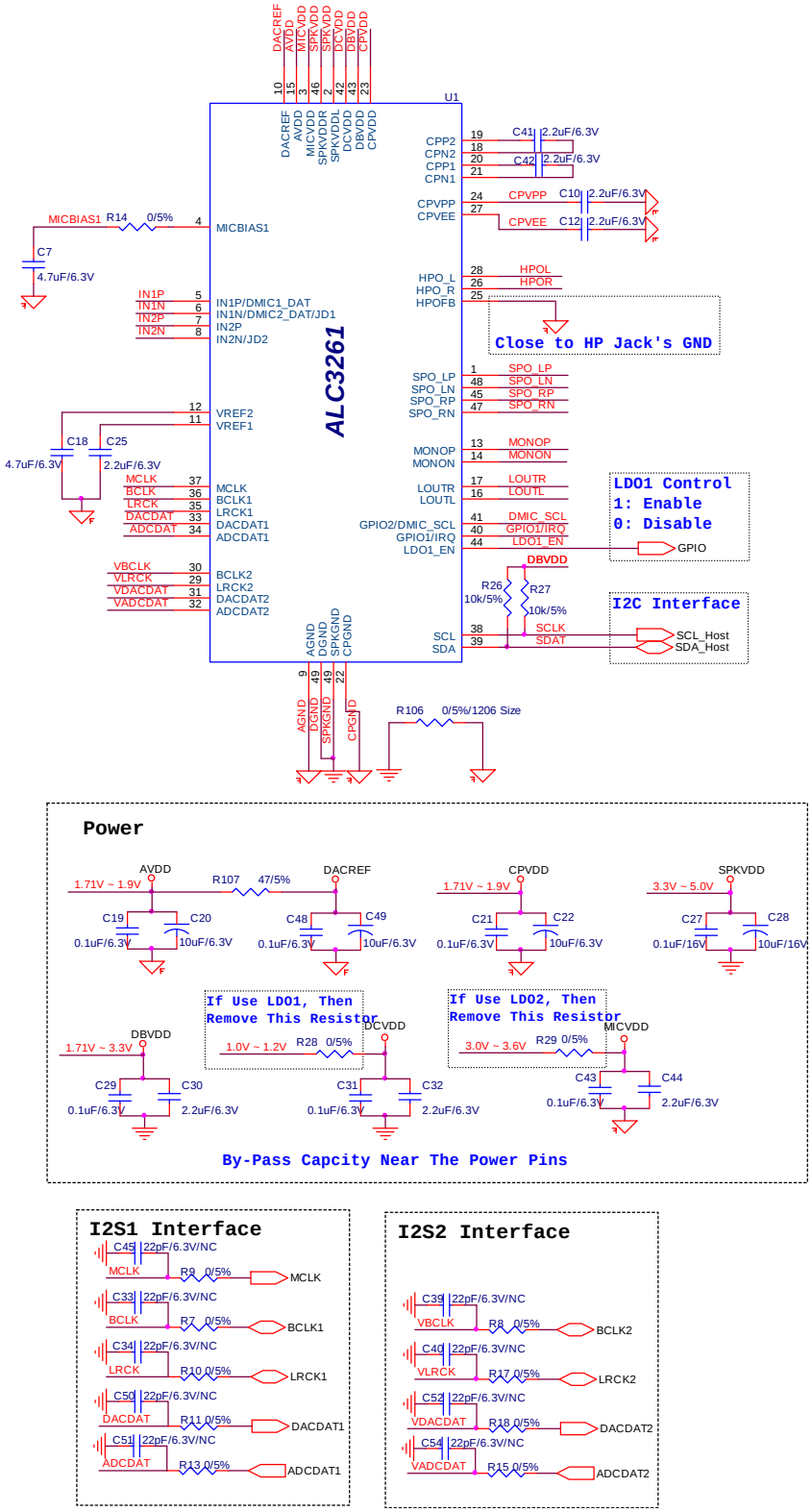


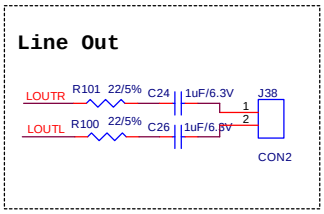
Figure 30. I²S/PCM Slave Mode Timing

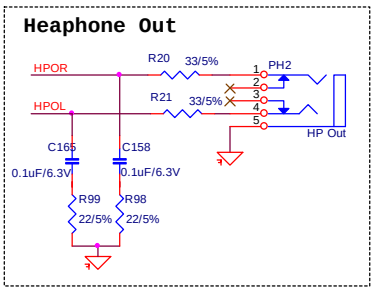
Table 138. I²S/PCM Slave Mode Timing

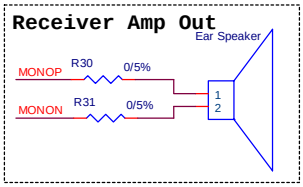
Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

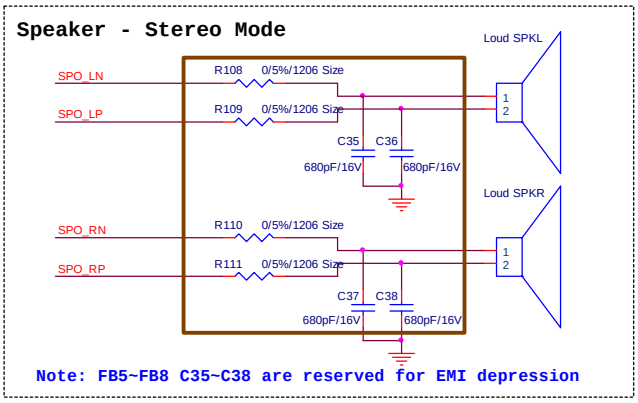
10. Application Circuits

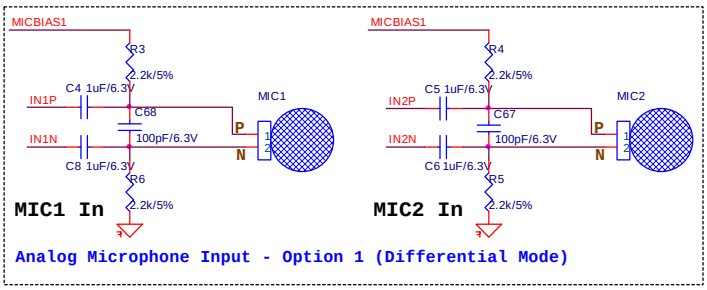


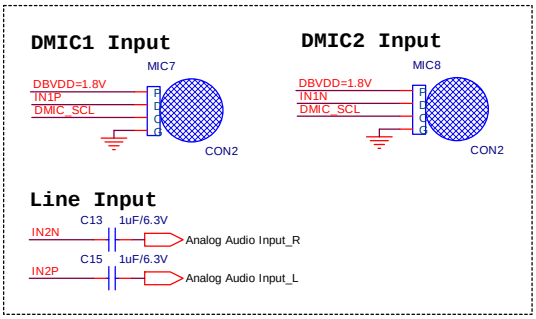

Line Out
LOUTR
R101 22/5%
C24 1uF/6.3V
LOUTL
R100 22/5%
C26 1uF/6.3V
J38
CON2

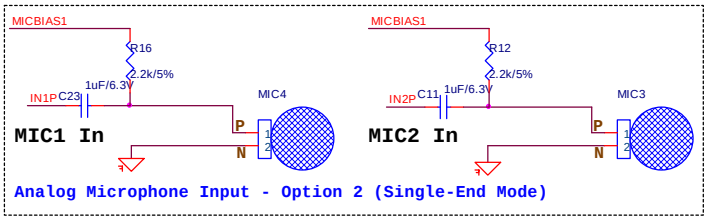

Heaphone Out
HPOR
HPOL
R20 33/5%
R21 33/5%
PH2
HP Out
C165 0.1uF/6.3V
C158 0.1uF/6.3V
R99 22/5%
R98 22/5%


Receiver Amp Out
Ear Speaker
MONOP
R30 0/5%
MONON
R31 0/5%


Speaker - Stereo Mode
Loud SPKL
Loud SPKR
SPO_LN
SPO_LP
SPO_RN
SPO_RP
R108 0/5%/1206 Size
R109 0/5%/1206 Size
R110 0/5%/1206 Size
R111 0/5%/1206 Size
C35 680pF/16V
C36 680pF/16V
C37 680pF/16V
C38 680pF/16V
Note: FB5~FB8 C35~C38 are reserved for EMI depression

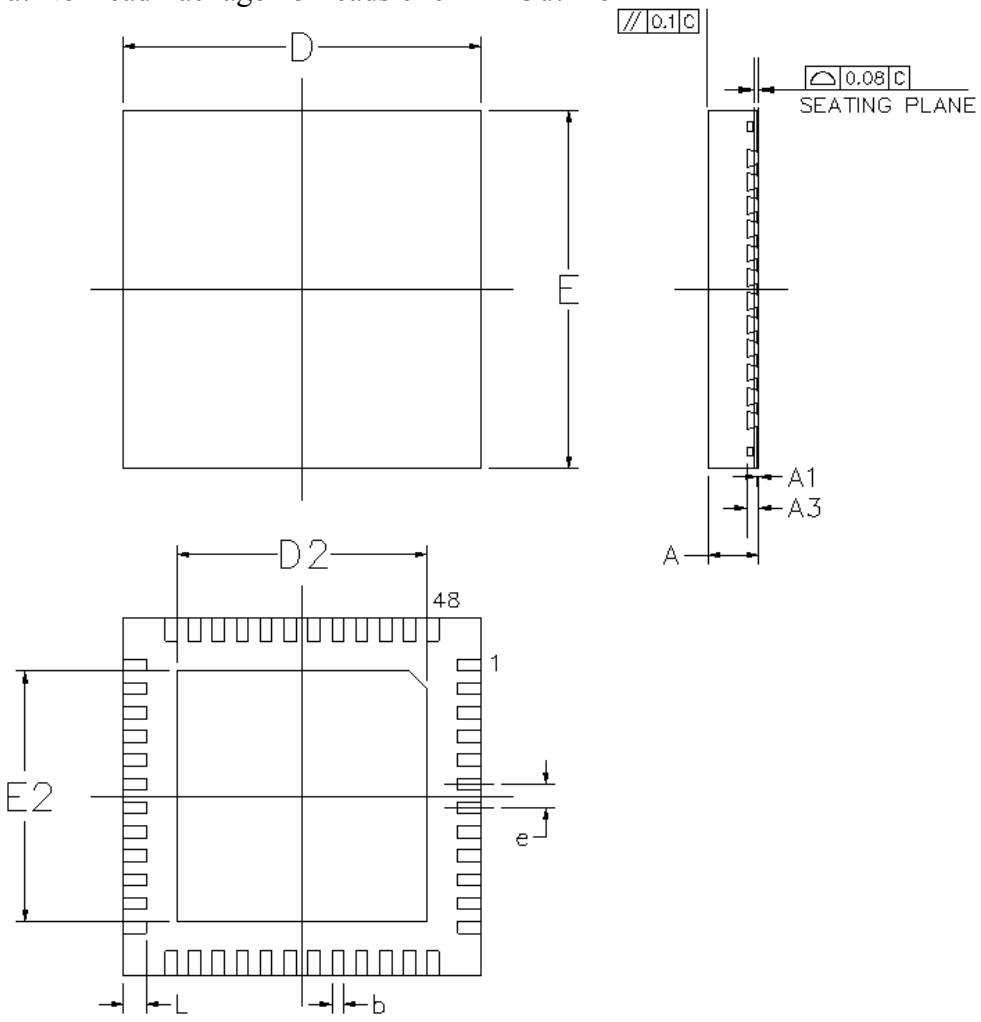

MICBIAS1
R3 2.2k/5%
C4 1uF/6.3V
IN1P
C68 100pF/6.3V
IN1N
C8 1uF/6.3V
R6 2.2k/5%
MIC1
MIC1 In
R4 2.2k/5%
C5 1uF/6.3V
IN2P
C67 100pF/6.3V
IN2N
C6 1uF/6.3V
R5 2.2k/5%
MIC2
MIC2 In
Analog Microphone Input - Option 1 (Differential Mode)


DMIC1 Input
MIC7
DBVDD=1.8V
IN1P
DMIC_SCL
CON2
DMIC2 Input
MIC8
DBVDD=1.8V
IN1N
DMIC_SCL
CON2
Line Input
IN2N
C13 1uF/6.3V
Analog Audio Input_R
IN2P
C15 1uF/6.3V
Analog Audio Input_L


MICBIAS1
R16 2.2k/5%
IN1P
C23 1uF/6.3V
MIC1 In
MIC4
R12 2.2k/5%
IN2P
C11 1uF/6.3V
MIC2 In
MIC3
Analog Microphone Input - Option 2 (Single-End Mode)

11. Mechanical Dimensions

Plastic Quad Flat No-Lead Package 48 Leads 6x6mm^2 Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes··

1. CONTROLLING DIMENSION·· MILLIMETER(mm).
2. REFERENCE DOCUMENTL·· JEDEC MO-220.

Figure 32. Package Dimension

12. Ordering Information

Table 139. Ordering Information

Part Number	Package	Status
ALC3261-CG	48-Pin QFN (6mm x 6mm) in 'Green' Package (Tray)	Mass Production
ALC3261-CGT	48-Pin QFN (6mm x 6mm) in 'Green' Package (Tape & Reel)	Mass Production

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com