ALC5620

I^2C + I^2S Audio Codec

Preliminary Datasheet

Rev. 3.4
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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC5620 Audio CODEC chip.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

.Revision History

Revision	Release Date	Summary
1.0	2006/09/16	Preliminary
2.0	2007/01/09	Update Register List
3.0	2007/03/01	Update Register List
3.1	2007/03/12	Update to package diagram
3.2	2007/03/19	Update to Audio mixer path
3.3	2007/04/20	1. Modify Max. of SPKVDD=5V and Output max. power of Speaker=1W
3.4	2007/05/02	1. Add Verf pull up Resistor

Table of Contents

1. General Description

The ALC5620 provides Dual channels Hi-Fi CODEC for playback and Dual channels ADC for record via I2S interface. In addition, an Independant Voice DAC is provided with PCM interface for bluetooth application.

This chip support ClassAB/ClassD configurable Speak output which can provide up to 1W and Headphone output which can provide up to 31.25mW. Each block of the chip can be power down to save power.

1.1 Features

- Digital-to-Analog Converter with 90dB SNR and –85dB THD+N.
- Analog-to-Digital Converter with 85dB SNR and –80dB THD+N.
- One analog stereo inputs, LINE-IN
- One analog mono single ended or differential inputs, PHONE and PHONEN input
- Stereo, mono single ended or differential analog microphone inputs, with boost pre-amplifiers. (+20/+30/+40dB)
- BTL (Bridge-Tied Load) Max. output with on chip 1W speaker driver (SPKVDD=5V, 8Ω load)
- Stereo headphone output with on chip 45mW headphone driver (HPVDD=3.3V, 16Ω load)
- 25mW SE or 75mW BTL mono output support (AVDD=3.3V, 32Ω load)
- Microphone switch detection
- Integrate 16-bit I2S/PCM interface voice DAC for blue-tooth and other external devices
- Power management and enhanced power saving.
- Support digital 5 bands equalizer (EQ)
- Support digital spatial sound and pseudo stereo effect
- Support pop noise suppression
- Inside PLL can receive wide range of clock input (Digital IO power > 1.8V)
- Both digital power supplies from 1.8V to 3.6V, speaker amplifier power supplies from 2.3V to 4.2V
- Analog power, headphone power supplies from 2.3V to 3.6V
- 48-pin QFN package

1.2 Applications

- Tablet PC system
- GPS or Multi-Media phone
- Smart phone applications

2. Function Block Diagrams

2.1 Function Block

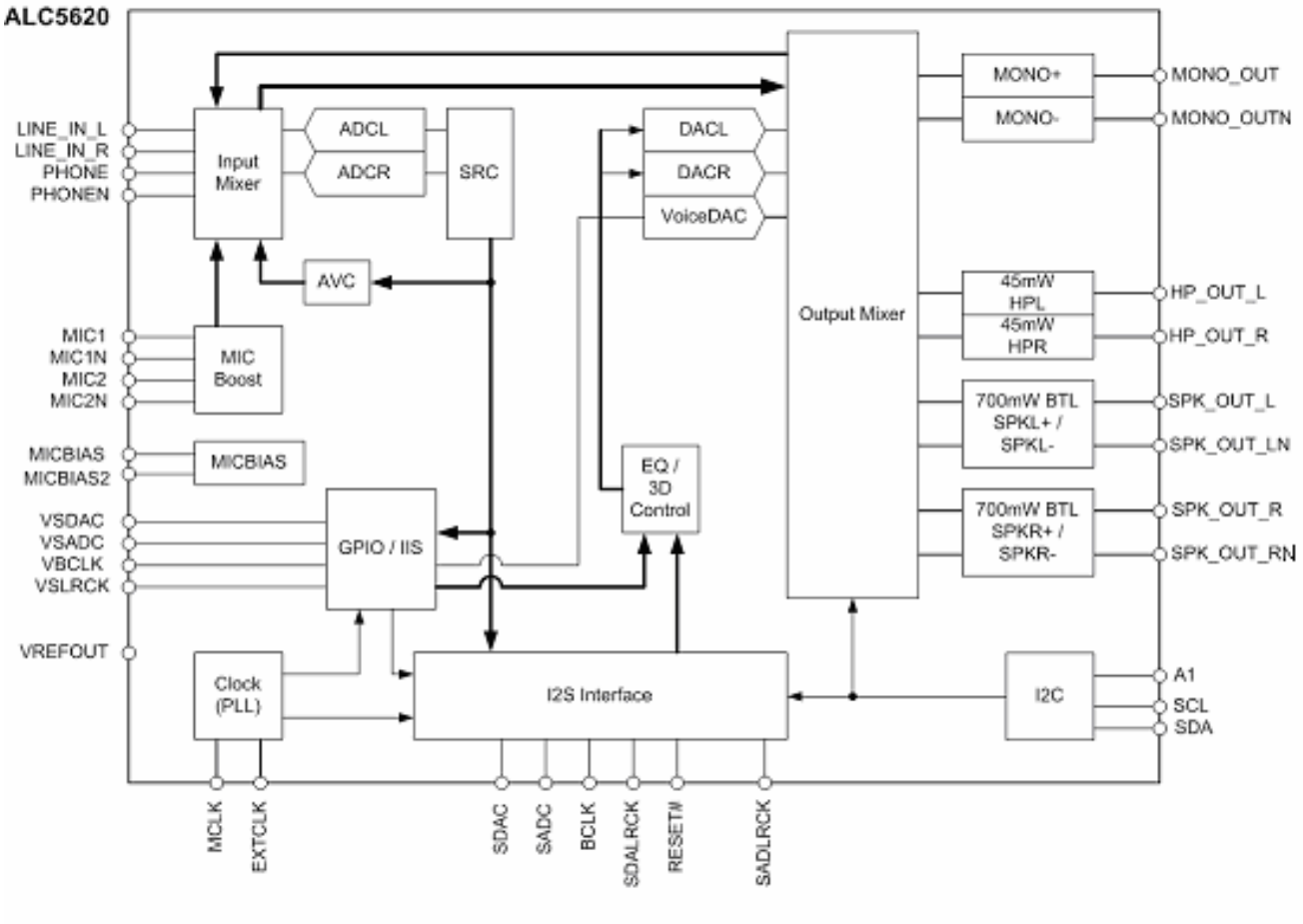


Figure 2.1-2. I²C Control Interface Function Block

2.2 Audio Mixer Path

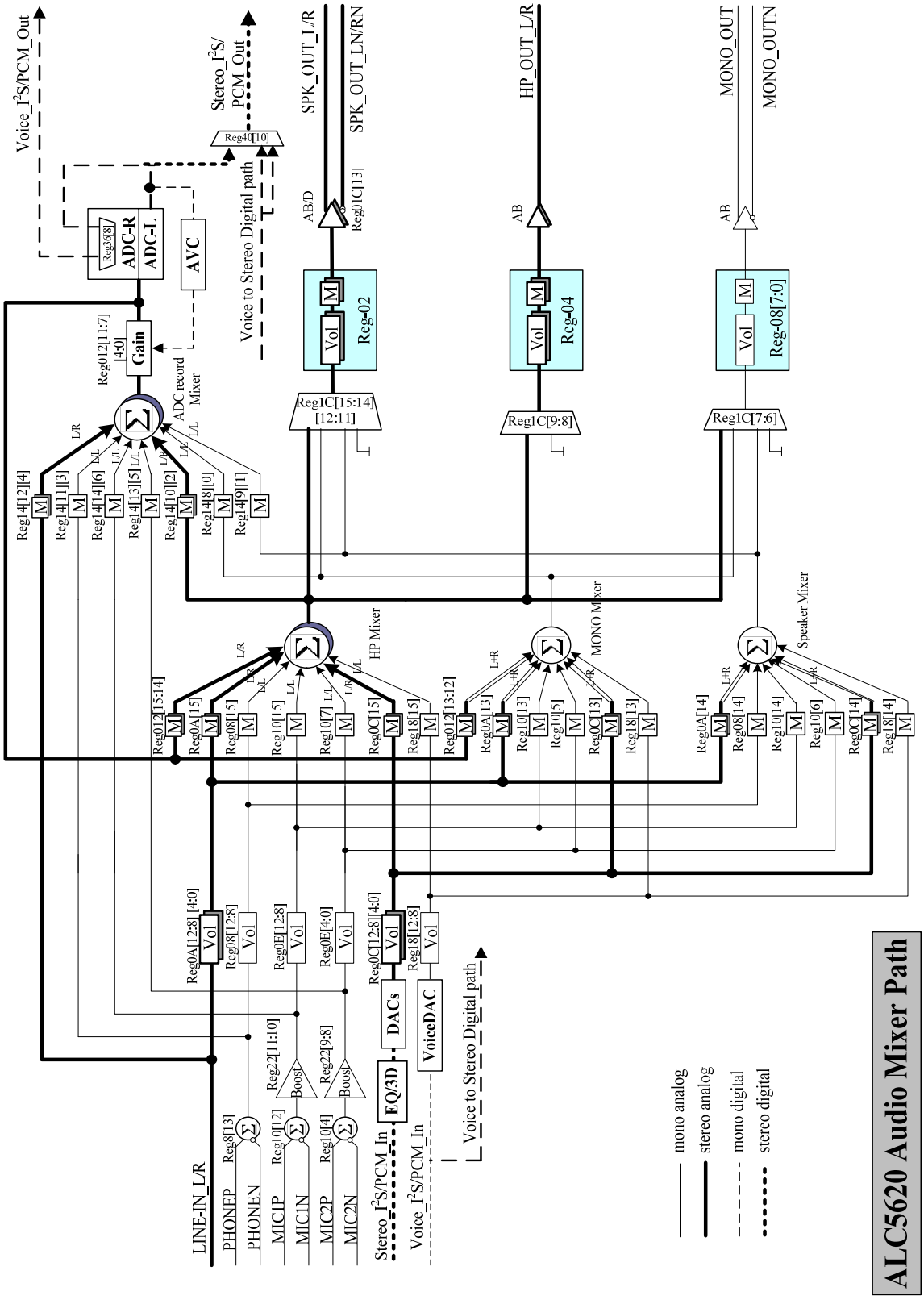


Figure 2.2-1. Analog Mixer Path

3. Pin Descriptions

3.1 Pin Assignment

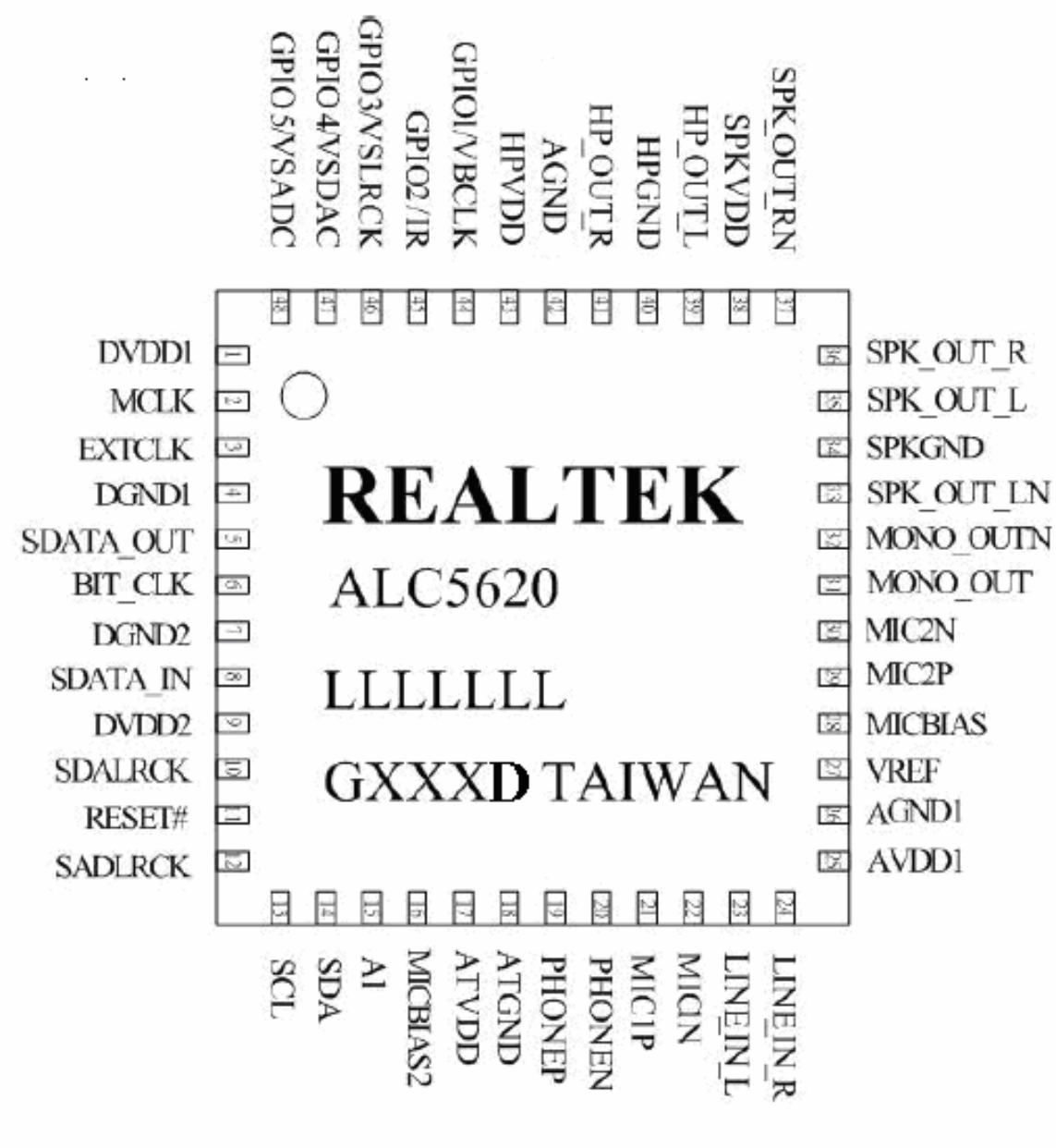


Figure 3.2.1-1. Pin Assignment

The ALC5620 series include the parts listed in section 7 Ordering Information, page 63.

Green package is indicated by a ‘G’ in the location marked “G” in Figure 3.2.1-1. The version number is shown in the location marked ‘D’.

3.2 Pin Descriptions

3.2.1 Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MCLK	I	2	Master Clock input	Schmitt trigger
EXTCLK	I/O	3	External reference clock input	Schmitt trigger
SDAC	I	5	Serial DAC data input	Schmitt trigger
BIT_CLK	I/O	6	Bit clock	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
SADC	O	8	Serial ADC data output	V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD
SDALRCK	I/O	10	DAC synchronous signal	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
RESET#	I	11	H/W reset input(Low Active)	Schmitt trigger
SADLRCK	I/O	12	ADC synchronous signal	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
SCL	I	13	I^2C Clock	Schmitt trigger
SDA	I/O	14	I^2C Data	Schmitt trigger
A1	I	15	I^2C address A1	A1: Input
GPIO1 / VBCLK	I/O	44	General Purpose Input and Output 1 / I^2S interface clock	GPIO: Input / Output VBCLK: Slave input / Master output
GPIO2 / IRQOUT/IR	I/O	45	General Purpose Input and Output 2 / Interrupt output/IR control signal output	GPIO: Input / Output IRQOUT: Output IR: IR control signal output
GPIO3 / VSLRCK	I/O	46	General Purpose Input and Output 3 / I^2S interface frame signal	GPIO: Input / Output VSLRCK: Slave input / Master output
GPIO4 / VSDAC	I/O	47	General Purpose Input and Output 4 / I^2S interface serial data input	GPIO: Input / Output SDAC: Schmitt trigger input
GPIO5 / VSADC	I/O	48	General Purpose Input and Output 5 / I^2S interface serial data output	GPIO: Input / Output SADC: Voice Data Output
				Total: 16 Pins

3.3.2 Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
PHONEP	I	19	Phone positive input	Analog input (1Vrms)
PHONEN	I	20	Phone negative input	Analog input (1Vrms)
MIC1P	I	21	First Mic positive input	Analog input (1Vrms)
MIC1N	I	22	First Mic negative input	Analog input (1Vrms)
MIC2P	I	29	Second Mic positive input	Analog input (1Vrms)
MIC2N	I	30	Second Mic negative input	Analog input (1Vrms)
LINE_IN_L	I	23	Line input Left channel	Analog input (1Vrms)
LINE_IN_R	I	24	Line input Right channel	Analog input (1Vrms)
MONO_OUT	O	31	Mono output	Analog output (1Vrms)
MONO_OUTN	O	32	Negative Mono output	Analog output (1Vrms)
HP_OUT_L	O	39	Headphone output Left channel	Analog output (1Vrms)
HP_OUT_R	O	41	Headphone output Right channel	Analog output (1Vrms)
SPK_OUT_L	O	35	Speaker output Left channel	Analog output (1.3Vrms, SPKVDD = 4.2V)
SPK_OUT_LN	O	33	Negative speaker output Left channel	Analog output (1.3Vrms, SPKVDD = 4.2V)
SPK_OUT_R	O	36	Speaker output Right channel	Analog output (1.3Vrms, SPKVDD = 4.2V)
SPK_OUT_RN	O	37	Negative speaker output Right channel	Analog output (1.3Vrms, SPKVDD = 4.2V)
				Total: 16 Pins

3.3.3 Reference Pins

Name	Type	Pin	Description	Characteristic Definition

MICBIAS	O	28	MIC BIAS Voltage output	Programmable Analog DC output with 3mA drive
MICBIAS2	O	16	MIC BIAS Voltage output 2	Programmable Analog DC output with 3mA drive
VREF	O	27	Internal Reference voltage	1uf capacitor to analog ground
				Total: 3 Pins

3.3.4 Power/Ground Pins

Name	Type	Pin	Description	Characteristic Definition
DVDD1	P	1	Digital VDD	1.8V~3.6V (IO)
DGND1	P	4	Digital GND	
DGND2	P	7	Digital GND	
DVDD2	P	9	Digital VDD	1.8V~3.6V (Core)
ATVDD	P	17	Analog VDD for test	2.3V~3.6V
ATGND	P	18	Analog GND for test	
AVDD1	P	25	Analog VDD	2.3V~3.6V
AGND1	P	26	Analog GND	
SPKGND	P	34	Analog GND for speaker amps	
SPKVDD	P	38	Analog VDD for speaker amps	3.0V~5V(for Ohm loading) 2.3V~5V(for KOhm loading)
HPGND	P	40	Analog GND for Headphone amps	
AGND2	P	42	Analog GND	
HPVDD	P	43	Analog VDD for Headphone amps	2.3V~3.6V
				Total: 13 Pins

Note: DVDD1 ≧ DVDD2, SPKVDD ≧ AVDD1, HPVDD ≧ AVDD1 ≧ DVDD2, ATVDD ≧ DVDD2

4. Electrical Characteristics

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings:

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO buffer	DVDD1	1.8	3.3	3.6	V
Digital core	DVDD2	1.8	3.3	3.6	V
Analog	AVDD	2.3	3.3	3.6	V
Analog Test	ATVDD	2.3	3.3	3.6	V
Headphone	HPVDD	2.3	3.3	3.6	V
Speaker	SPKVDD	2.3	3.3	5	V
Operating Ambient Temperature	Ta	-25	-	+85	^{o}C
Storage Temperature	Ts	-	-	+125	^{o}C
ESD Protection					
Human Body Model (HBM)		4000	5000	-	V

4.1.2 Static Characteristics:

DVDD= 3.3V, $T_{ambient}$=25^{0}C, with 50pF external load.

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{IN}	-0.30	-	DVDD+0.30	V
Low level input voltage	V_{IL}	-	-	0.35DVDD	V
High level input voltage	V_{IH}	0.65DVDD	-	-	V
High level output voltage	V_{OH}	0.9DVDD	-	-	V
Low level output voltage	V_{OL}	-	-	0.1DVDD	V
Input leakage current	-	-1	-	1	uA
Output leakage current (Hi-Z)	-	-1	-	1	uA
Output buffer high drive current	-	-	22	-	mA
Output buffer low drive current	-	-	10	-	mA
V_{MID} internal serial resistor	-	25	50	75	KΩ
V_{MID} internal serial resistor ratio	-	95	100	105	%

4.1.3 Analog Performance Characteristics:

Standard test conditions: $T_{ambient}$=25^{0}C, DVDD=AVDD=HPVDD=3.3V, SPKVDD = 4.2V
1KHz input sine wave; PCM Sampling frequency=48KHz; 0dB=1Vrms, Test bench Characterization BW: 10Hz~22KHz, 0dB attenuation; EQ and 3D disabled

Parameter	Min	Typ	Max	Units
Full scale input voltage				
Line inputs	-	1.0	-	Vrms
MIC inputs (Non-boost)	-	1.0	-	
MIC inputs (Boost 20dB)	-	0.1	-	
ADC		0.7		
Full scale output voltage				
MONO outputs	-	1.0	-	Vrms
Headphone amplifiers outputs	-	1.0	-	
Speaker amplifiers outputs	-	1.3	-	

S/N Ratio (A-weighted, HPL/R or MONO with 10KΩ/50pF load)				
STEREO DAC	-	90	-	dB
STEREO ADC	-	85	-	dB
Voice DAC	-	70	-	dB
Total Harmonic Distortion + Noise (A-weighted, HPL/R or MONO with 10KΩ/50pF load)				
STEREO DAC	-	-85	-	dB
STEREO ADC	-	-80	-	dB
Voice DAC	-	-60	-	dB
MIC Boost Amplifier				
Gain = 20dB	18	20	22	dB
Gain = 30dB		30		dB
Gain = 40dB		40		dB
Input impedance (gain = 0dB, ADC mixer = on/off)				
PHONEN (Differential mode)		16	-	KΩ
MIC1N, MIC2N (Differential mode)		16	-	KΩ
MIC1P, MIC2P,		16		KΩ
PHONEP		16		KΩ
Input impedance (gain = 0dB, ADC mixer = on)				
LINE_IN	12.8	16	19.2	KΩ
Input impedance (gain = 0dB, ADC mixer = off)				
LINE_IN	25.6	32	38.4	KΩ
Output Impedance				
MONO_OUT	-	2		Ω
HP_OUT	-	2		Ω
SPK_OUT (Class AB)	-	1		Ω
SPK_OUT (Class D)		0.3	0.4	Ω
MONO_OUT Amplifier Output Power (32Ω load)				
Single End Mode	25			mW
BTL Mode	75			mW
MONO_OUT Amplifier Quiescent Current (32Ω load)/CH	-	700		uA
MONO_OUT Amplifier Efficiency (f_{IN} = 1KHz, 32Ω load)				
Single End Mode (Output Power = 25 mW)	50	-	-	%
BTL Mode (Output Power = 75 mW)	50	-	-	%
MONO_OUT/AUXOUT_L/R Amplifier THD+N				
Single End Mode (10KΩ load)				
Output Power = 0.1 mW	-	0.01		%
BTL Mode (10KΩ load)				
Output Power = 0.1 mW	-	0.01		%
MONO_OUT Amplifier PSRR (217Hz)	-	50	-	dB
Headphone Amplifier Output Power (32Ω load)			31.25	mW
Headphone Amplifier Quiescent Current (32Ω load)/CH	-	700		uA

Headphone Amplifier Efficiency (f_{IN} = 1KHz, 32Ω load, Output Power = 25 mW)	50	-	-	%
Headphone Amplifier THD+N (32Ω load)				
Output Power = 20 mW	-	70		dB
Output Power = 25 mW	-	70		dB
Headphone Amplifier PSRR (217Hz)	-	50	-	dB
BTL Speaker Amplifier Output Power (SPKVDD=5V with 8Ω load)		1		W
BTL Speaker Amplifier Quiescent Current				
Class AB_Strong(8Ω load)			TBD	mA
Class AB_Weak(10KΩ load)	-	-	TBD	mA
Class D	-	-	4	mA
BTL Speaker Amplifier Efficiency (f_{IN} = 1KHz, 8Ω load, Output Power = 700 mW)				%
Class AB	50	-	-	
Class D		82	-	
BTL Speaker Amplifier THD+N (8Ω load)				
Class AB_Strong				
Output Power = 350 mW	-	70		dB
Output Power = 600 mW	-	70		dB
Class D				
Output Power = 350 mW	-	70		dB
Output Power = 600 mW	-	60		dB
BTL Speaker Amplifier THD+N				
Class AB_Weak(10KΩ/50pF load)		-85		dB
BTL Speaker Amplifier SNR				
Class AB_Weak(10KΩ/50pF load)		-90		dB
BTL Speaker Amplifier PSRR (217Hz)	-	50	-	dB
Power Supply Current				
I_{DDA} (Analog Block)	-	-	15	mA
I_{DDD} (Digital Block)	-	-	20	mA
Power Down Current				
I_{DDA} (Analog Block)	-	-	10	uA
I_{DDD} (Digital Block)	-	-	1	uA
MICBIAS1 output voltage				
0.75*Avdd Setting	-	2.475	-	V
0.9*Avdd Setting	-	2.97	-	V
MICBIAS1 and MICBIAS2 Drive Current		16		mA
MICBIAS2 output voltage				
0.75*Avdd Setting	-	2.475	-	V
0.9*Avdd Setting	-	2.97	-	V
Verf pull up Resistor		75		KΩ

4.2 Signal Timing

4.2.1 I²C Control Interface

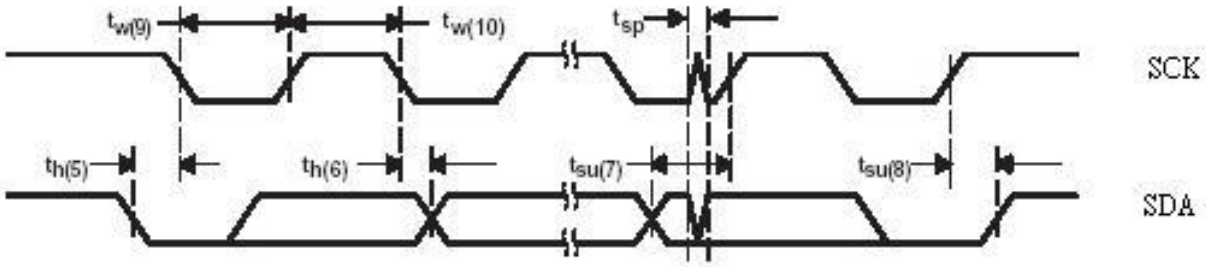


Figure 4.2.8-1. I²C Control Interface

Parameter	Symbol	Min	Typ	Max	Units
Clock pulse duration	Tw(9)	1.3	-	-	us
Clock pulse duration	Tw(10)	600	-	-	ns
Clock frequency	f	0	-	400K	Hz
Setup time	Tsu(6)	600	-	-	ns
Hold time	Th(5)	600	-	-	ns
Data Setup time	Tsu(7)	100	-	-	ns
Data Hold time	Th(6)	-	-	900	ns
Rising time	Tr	-	-	300	ns
Falling time	Tf	-	-	300	ns
Setup time	Tsu(8)	600	-	-	ns
Pulse width of spikes suppressed input filter	Tsp	0	50	-	ns

4.2.2 I²S Master Mode

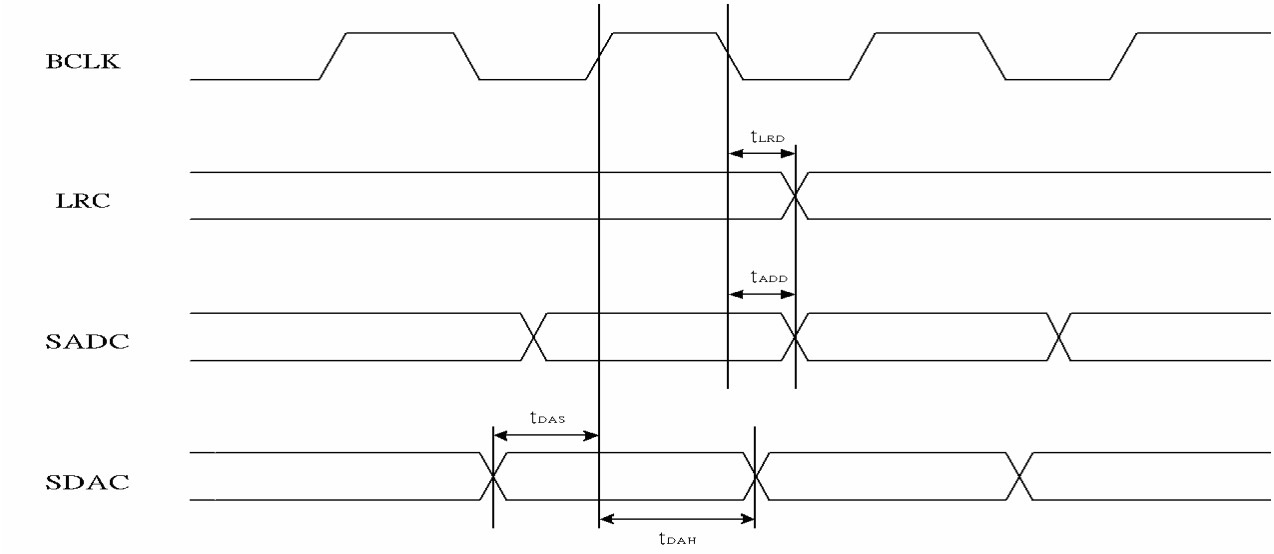


Figure 4.2.9-1. Timing of I²S Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRC output to BCLK delay	t_{LRD}	-	-	30	ns
Data output to BCLK delay	t_{ADD}	-	-	30	ns
Data input Setup time	t_{DAS}	10	-	-	ns
Data input Hold time	t_{DAH}	10	-	-	ns

4.2.3 I²S Slave Mode

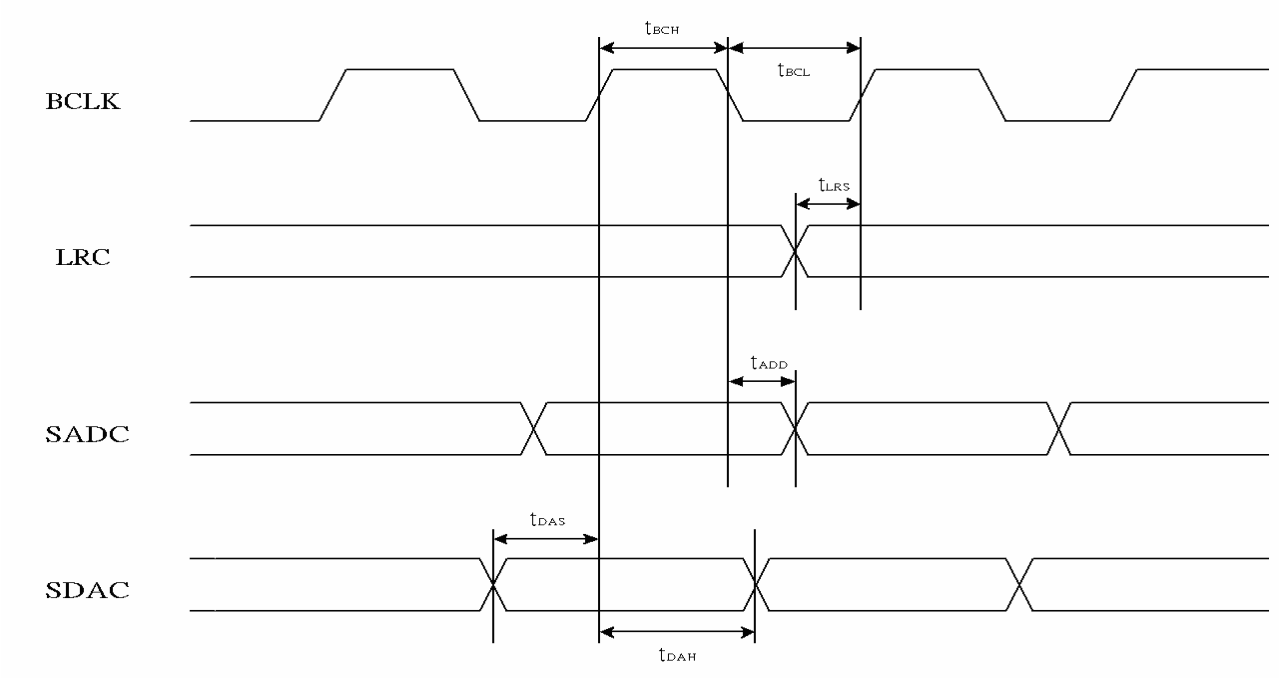


Figure 4.2.10-1. Timing of I²S Slaver Mode

Parameter	Symbol	Min	Typ	Max	Units
BCLK high pulse width	t_{BCH}	20	-	-	ns
BCLK low pulse width	t_{BCL}	20	-	-	ns
LRC input Setup time	t_{LRS}	-	-	30	ns
Data output to BCLK delay	t_{ADD}	-	-	30	ns
Data input Setup time	t_{DAS}	10	-	-	ns
Data input Hold time	t_{DAH}	10	-	-	ns

5. Function Description

5.1 Power

ALC5620 has many power blocks. SPKVDD operates between 2.3V and 5V. HPVDD and ATVDD and AVDD operate between 2.3V and 3.6V. DVDD1 and DVDD2 operate between 1.8V and 3.6V. The power supplier limit condition are DVDD1 ≧ DVDD2 and SPKVDD ≧ AVDD , HPVDD ≧ AVDD ≧ DVDD2, ATVDD ≧ DVDD2.Besides, **AVDD =ATVDD**

For the best performance, our design setting is show as below.

Power	DVDD1	DVDD2	HPVDD	ATVDD	AVDD	SPKVDD
Setting	3.3V	1.8V	3.3V	3.3V	3.3V	4.2V

5.2 Reset

There are 4 kinds of reset operation. ***POR, Cold*** and ***Register*** reset which listed below:

Reset Type	Trigger condition	CODEC response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Cold Reset	Assert RESET# for a specified period	Reset all hardware logic and all registers to default values except some specify control registers and logic.
Register Reset	Write Reg-00h (Word for AC-LINK and I^2C)	Reset all registers to default values except some specify control registers and logic.

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note:The V_{POR_OFF} must below V_{POR_ON}.

5.2.1. Power On Reset (POR)

When power on, DVDD2 pass through the V_{POR} band of ALC5620(V_{PORH} ~V_{PORL}), the Power On Reset (POR) will generate an internal reset signal (POR reset “LOW”) to reset whole chip.

5.3 Clocking

The Stereo_SYSCLK can be selected from MCLK or PLL. That means, MCLK is always provided externally. DRIVER has to arrange the clock of each block and setup each divider

The voice codec clock can be selected from MCLK (Master mode)., PLL (Master mode)., EXTCLK(Slave mode).or VBCLK(Slave mode). DRIVER has to arrange the clock of each block and setup each divider

In master mode of voice I2S/PCM, EXTCLK can be output by setting the **Extclk_dir=”1”** and output frequency will be determine by MCLK and setting of **Extclk_out_sel**.

The clock control diagram is shown as below.

5.3.1 PLL

PLL is used to provide flexible input clock from 2.048MHz to 40MHz. The source of PLL can be select to MCLK or BIT_CLK by setting **pll_sour_sel**.

DRIVER can set up PLL to output desire frequency as the SYSCLK.

The PLL transmit formula is

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

For I2C+I^{2}S clock setting table for 48K: (unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

For I^{2}C+I2S clock setting table for 44.1K: (unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

PLL related Register would not be reset to default value after soft-reset (write Reg00) but Cold Reset will. Besides, it is forbidden for FW to power down PLL while PLL output is used as Stereo_SYSCLK.

5.3.2 I^{2}C and Stereo I^{2}S Model

ALC5620 supports digital interface for Stereo Audio in I2C+I2S model.The stereo audio digital interface is used to input data to stereo DAC or output data from stereo ADC. The Stereo Audio Digital Interface can be configured as Master mode and Slave mode.For the Stereo I2S Interface, the source clock always input from MCLK.

In master mode, BCLK/SDALRCK/SADLRCK are configured as output. When PLL disabled and **sel_sysclk="0".** MCLK is used as Stereo SYSCLK. When PLL enable, MCLK is suggested to provide 13MHz and PLL can be configured to support 44.1K and 48K base sampling rate. DRIVER have to set each divider (Reg60 & Reg62) to arrange the clock distribution. Refer to **Appendix A** for detail. ALC5620 support different sample rate between SDALRCK and SADLRCK in Stereo_I2S/PCM.

In slave mode, BCLK/SDALRCK is configured as input, MCLK should be provide BCLK synchronized clock externally as Stereo_SYSCLK and DRIVER have to set each divider to arrange the clock distribution. Refer to **Appendix A** for detail. Besides, ALC5620 **did not** support different sample

rate between SDALRCK and SADLRCK. In Slave mode, Only SDALRCK is used.

- **Suggest setting:**

ADC	I2S DA clock @Stereo_SYSCLK=44100 Xx※		I2S DA clock @Stereo_SYSCLK=48000 Xx※	
Fs	**Stereo_ad _filter_sel=1**	**Stereo_ad _filter_sel=0**	**Stereo_ad _filter_sel=1**	**Stereo_ad _filter_sel=0**
48000	Not support	Not support	3072000	6144000
44100	2822400	5644800	Not support	Not support
32000	Not support	Not support	2048000	4096000
24000	Not support	Not support	1536000	3072000
22050	1411200	2822400	Not support	Not support
16000	Not support	Not support	1024000	2048000
11025	705600	1411200	Not support	Not support
8000	Not support	Not support	512000	1024000
8018.2	513163.64	1026327.27*	Not support	Not support

※ Xx mean 256x or 384x or 512x or 768x

5.3.3 Voice_I2S/PCM interface

ALC5620 supports independent digital interface for Voice Audio. The voice audio digital interface is used to input digital data to voice DAC or output digital data from voice ADC. The Voice Audio Digital Interface can be configured as Master mode and Slave mode. The Sample rate of Voice ADC and Voice DAC is the same by setting Reg64 & Reg 66 no matter in Master mode or Slave mode.

In Master mode, the main clock of Voice_I2S/PCM interface can be input selected from MCLK (with or without PLL) or EXTCLK. VBCLK and VSLRCK will be configured as output. DRIVER has to set each divider (Reg64 & Reg66) to arrange the clock distribution. Refer to **Appendix B** for detail.

In Slave mode, the main clock of Voice_I2S/PCM can be input from MCLK or EXTCLK by provide BCLK synchronized clock externally. VBCLK and VSLRCK will be configured as input DRIVER has to set each divider (Reg64 & Reg66) to arrange the clock distribution. Besides, If VBCLK can provide 64Fs,128Fs or 256Fs externally, ACL5620 can use VBCLK input as main clock of Voice_I2S/PCM. Refer to **Appendix B** for detail.

5.3.4 Voice ADC

ALC5620 support Voice ADC feature for transmiting the voice data to Blue Tooth device. The Voice ADC is implemented by input voice sample rate into Right channel of Stereo ADC and Left channel of stereo ADC still input stereo sample.

When **voice_adc_enable="0",** the L/R channel of stereo ADC sample rate is setting by Stereo sample rate and output to Stereo I2S interface. At the same time output Right channel to voice I2S/PCM interface.

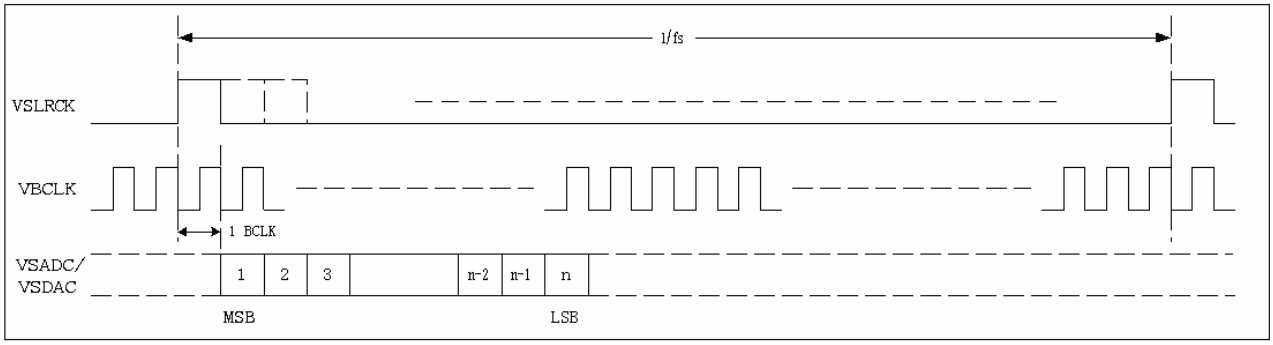
When **voice_adc_enable="1",** the sample rate of Left channel is setting by stereo sample rate but the sample rate of Right channel is setting by voice sample rate. The Left channel ADC is output to Left channel and duplicate to Right of Stereo I2S interface. The Right channel of Stereo ADC is now used as Voice ADC and output to voice_I2S/PCM.

5.4 Digital Data Interface

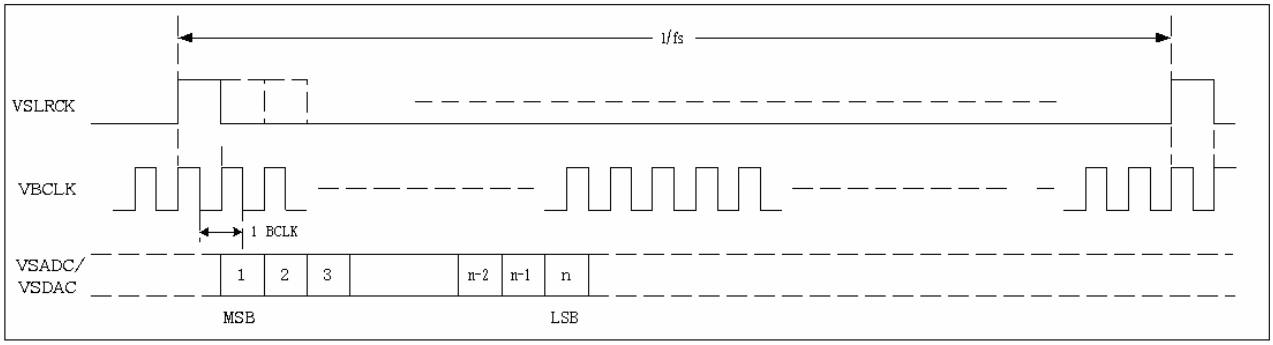
5.4.1 Main & Voice I2S/PCM Interface

Main & Voice I2S/PCM interface can be configured as Master mode, Slave mode and four different audio data formats are supported:

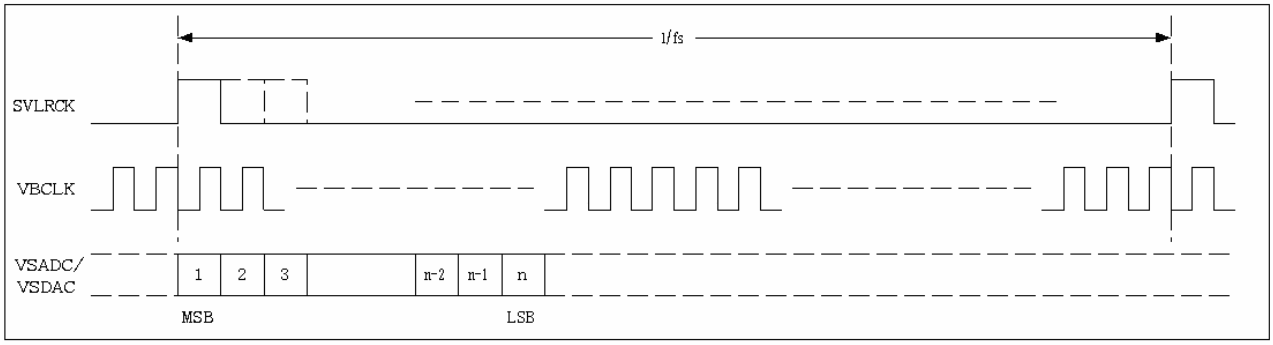
- PCM mode
- Left justified mode
- Right justified mode
- I2S mode



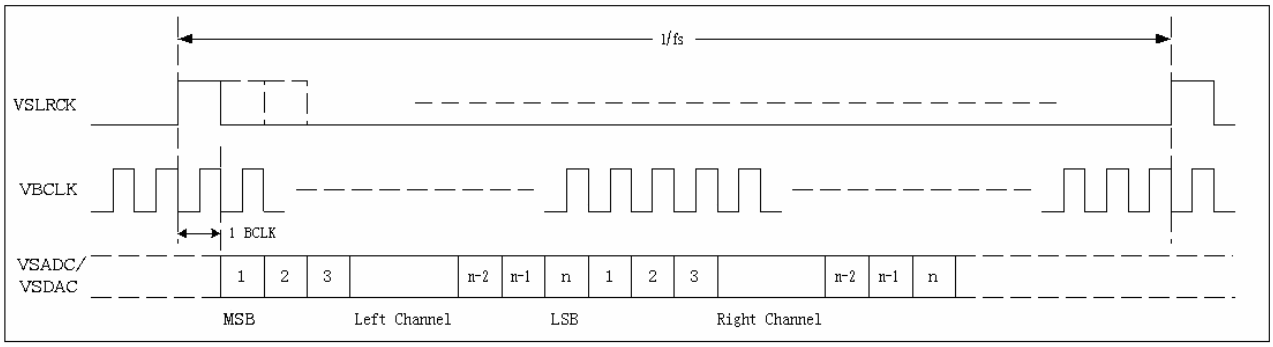
PCM Mono Data Mode A Format (bclk_polarity=0**)**



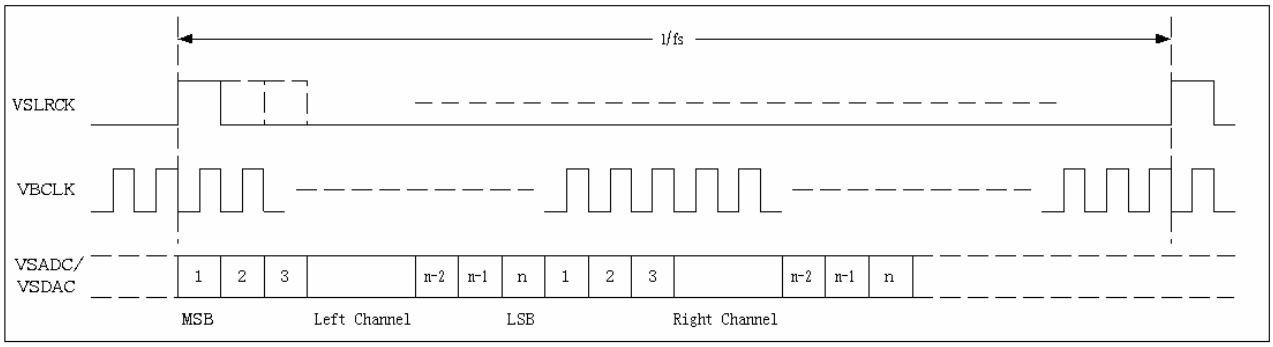
PCM Mono Data Mode A Format (bclk_polarity=1**)**



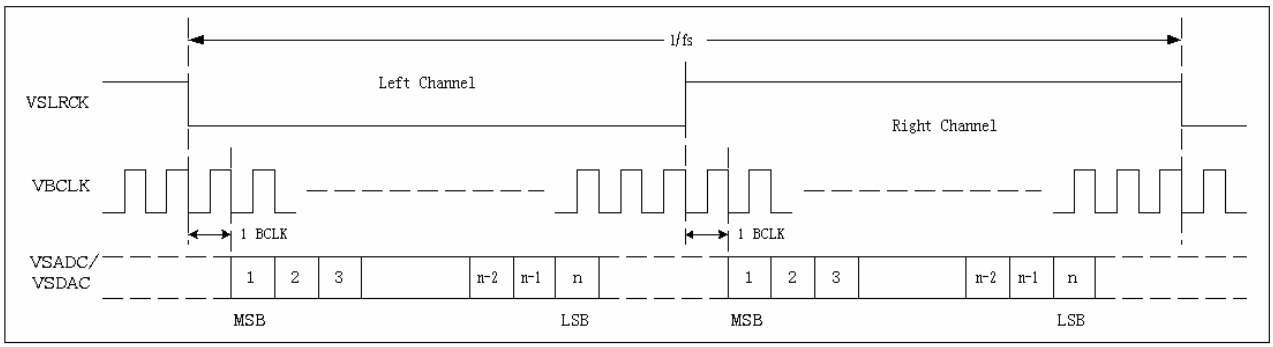
PCM Mono Data Mode B Format



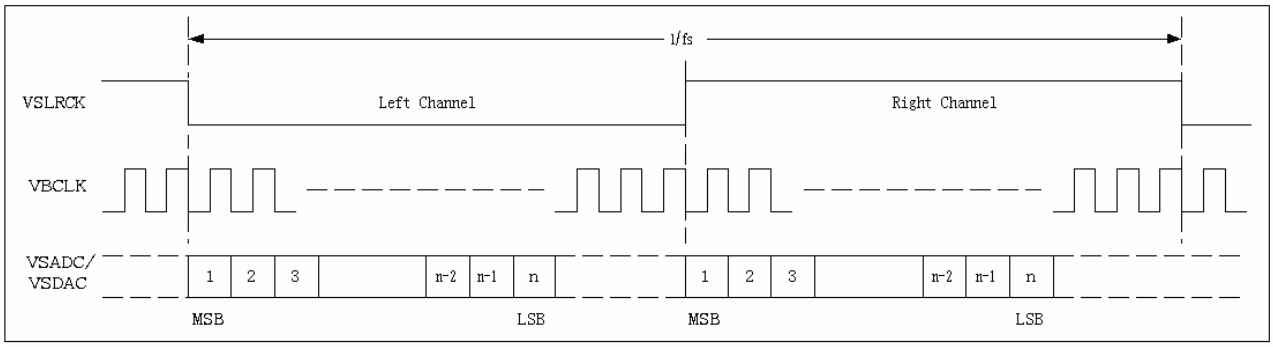
PCM Stereo Data Mode A Format



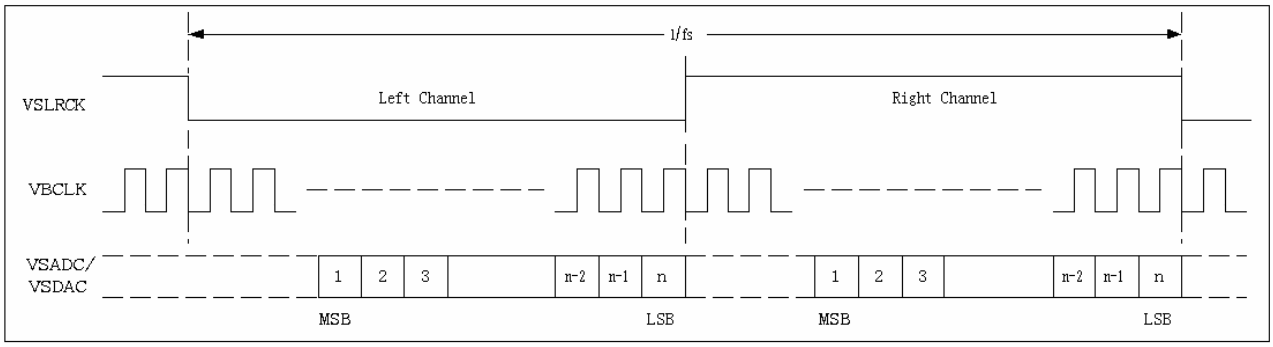
PCM Stereo Data Mode B Format



I²S Data Format



Left justified Data Format



Right justified Data Format

5.5 Audio Data Path

5.5.1. Stereo ADC & Voice ADC

Stereo ADC is used for recording stereo sound or can be configured to mono PCM ADC (Left channel of Stereo ADC) + voice ADC (Right channel of Stereo ADC) for the application of recording + blue-tooth by setting **voice_adc_enable.** (refer to 5.3.5 voice ADC)

The sample rate of stereo ADC is independent to Stereo DAC sample rate. When v**oice_adc_enabl ="1",** the sample rate of voice ADC is setting by Reg64/66 and sample rate of mono PCM ADC is setting by Reg60/62.

In order to save power, the left and right ADC can be power down separately by setting Reg3C [6], [7]). Besides, PR0="1" will disable both channel of ADC.

The volume control of Stereo ADC is by setting Reg12[11:7][4:0].

5.5.2. Stereo DAC

Stereo DAC can be configured to different sample rate by setting the stereo I2S clock divider (Reg60). In addition, Reg62[15:9] is used to control over sample rate clock divider of DA filter to 128Fs or 64Fs, and Reg62[8] have to be setting according to the over sample rate clock. The performance of 128Fs is better than 64Fs but with much more power consumption. Reg34[11] is used to control sigma delta clock source and Reg34[10:8] is used to set the divider of Stereo_DAC sigma delta clock in I2C+I2S model. The higher frequency will cause better performance. Besides, the frequency of Stereo DAC Sigma Delta clock must be equal or higher than DA filter over sampling rate for better performance.

Reg0C[12:8][4:0] can be used to control the volume of DAC output

5.5.2.1 Voice to Stereo Digital Path

ALC5620 supports voice to stereo digital path for Voice commander through blue-tooth by setting Reg42[15]="1". The Voice data will be transfer from Voice I2S/PCM to main I2S/I2C directly. This function only support when Voice & Stereo I2S/PCM are in Master Mode. Driver have to set the same sample rate between Voice DAC and stereo ADC sample rate.

When voice to stereo digital path is enabled, the signal from Voice_I2S/PCM is direct output to Left channel and duplicate to Right channel of Stereo I2S interface.

The function of Voice to Stereo Digital Path and Voice ADC can exist at the same time.

5.5.3. Voice DAC

Voice DAC is dedicated for playback received voice signal from voice_I2S/PCM interface. Typically, it is used in 8KHz sample rate.

In Voice I2S/PCM Master mode, sample rate is setting by VoDAC clock Divider (Reg64). In addition, Reg66[7:4][2:0] is used to control over sample rate clock divider of Voice ADC/DAC filter to 128Fs or 64Fs, and Reg66[13] have to be setting according to the over sample rate clock. the performance of 128Fs is better than 64Fs but with much more power consumption. Reg66[12] is used to control sigma delta clock source and Reg66[10:8] is used to set the divider of Voice DAC sigma delta clock. The higher frequency will cause better performance. Besides, the frequency of Voice DAC Sigma

Delta clock must be equal or higher than Voice DA filter over sampling rate for better performance.

The volume control of Voice DAC is by setting Reg18[12:8].

5.5.4. Mixer

ALC5620 support four mixers for all audio function requirements. Headphone mixer for 2 channels, one mono mixer, one Speaker mixer and one ADC record mixer.

5.5.4.1 Headphone Mixer

Headphone mixer is used to drive stereo output include HP_OUT_L/R, SPK_OUT_L/R (SPK_OUT_LN/RN) and MONO_OUT(MONO_OUTN).Besides, the output of Headphone mixer can be input to ADC record mixer.

The following signal can be mix into Headphone mixer:

- LINE-IN_L/R (controlled by Reg0A)
- PHONEP/N (controlled by Reg08)
- MIC1P/N and MIC2P/N (controlled by Reg22 & Reg10)
- Stereo DAC output (controlled by Reg0C)
- Voice DAC output (controlled by Reg18)
- Output of ADC record mixer (controlled by Reg12 & Reg14).

The headphone mixer can be power down by setting Reg3C[5][4].

5.5.4.2 Mono Mixer

Headphone mixer is used to drive MONO_OUT(MONO_OUTN) and SPK_OUT_L/R (SPK_OUT_LN/RN). The output of mono mixer can be input to ADC record mixer. The output of mono mixer is two channels with the same signal

The following signal can be mix into Mono mixer:

- LINE-IN_L/R (controlled by Reg0A)
- MIC1P/N and MIC2P/N (controlled by Reg22 & Reg10)
- Stereo DAC output (controlled by Reg0C)
- Voice DAC output (controlled by Reg18)
- Output of ADC record mixer (controlled by Reg12 & Reg14).

The mono mixer can be power down by setting Reg3C[2].

5.5.4.3 Speaker mixer

Speaker mixer is the same as mono mixer and used to drive MONO_OUT(MONO_OUTN) and SPK_OUT_L/R (SPK_OUT_LN/RN). Besides, the output of Speaker mixer can be input to ADC record mixer. The output of mono mixer is two channels with the same signal

The following signal can be mix into Speaker mixer:

- LINE-IN_L/R (controlled by Reg0A)

- PHONEP/N (controlled by Reg08)
- MIC1P/N and MIC2P/N (controlled by Reg22 & Reg10)
- Stereo DAC output (controlled by Reg0C)
- Voice DAC output (controlled by Reg18)

The Speaker mixer can be power down by setting Reg3C[3].

5.5.4.4 ADC record Mixer

ADC record mixer is used to mix the analog signal as input of Stereo ADC for recording. Besides, The output of ADC record mixer can be input to Headphone mixer, Mono mixer and Speaker mixer.

The following signal can be mix into ADC record mixer:

- LINE-IN_L/R (controlled by Reg0A)
- PHONEP/N (controlled by Reg08)
- MIC1P/N and MIC2P/N (controlled by Reg22 & Reg10)
- Output of Headphone mixer.
- Output of mono mixer.
- Output of Speaker mixer.

The headphone mixer can be power down by setting Reg3C[1][0].

5.5.5. Analog Audio Input Path

There are 4 sets Analog Audio Input path in ALC5620. Line_IN_L/R, AUXIN_L/R, MIC1 and MIC2.

5.5.5.1 Line Input

Line_In_L and Line_In_R provide 2 channels stereo single ended input which can be mix into one of analog output mixer and ADC record mixer.

The Line_In_L/R volume and mute are controlled by Reg0A. Besides, Reg3E[7:6] can be used to power down Line_In volume control

Line_In_L is pin share to GPIO2 and can be configure by Reg56[6:4], Line_In_R is pin share to GPIO3 and can be configure by Reg56[1:0].

5.5.5.2 Phone Input

PHONEP/N provides 1 channel mono differential input which can be mix into ADC record mixer.and any of analog output mixer except Mono Mixer.

The PHONEP/N volume and mute are controlled by Reg08. Besides, Reg3E[5:4] can be used to power down PHONEP/N volume control and admixer

5.5.5.3 Microphone Input

MIC1P/N and MIC2P/N provide 2 channels stereo differential or single ended input by Reg10[12],[4] which can be mix into any of analog output mixer and ADC record mixer.The boost of Microphone input of ALC5620 provide 20/30/40dB boost by select Reg22[11:10] (for MIC1) and Reg22[9:8](for MIC2).The MIC1/2 volume and mute are controlled by Reg0E.

For detail power management to MIC1/2, Reg3E[3][2] can be used to power down MIC1/2 volume control path. Reg3E[1][0] can be used to power down MIC1/2 admixer path.

5.5.6. Analog Audio Output Data Path

There are 3 sets Analog Audio Output path in ALC5620. SPK_OUT_L/R, HP_OUT_L/R and MONO_OUT.

5.5.6.1 Speaker Output

SPK_OUT_L/R provides 2 channels differential output.

The source of SPK_OUT_L can be select from Reg1C[15:14] as below.

- Vmid
- Headphone left mixer
- Speaker mixer
- Mono mixer

The source of SPK_OUT_R can be select from Reg1C[12:11] as below.

- Vmid
- Headphone right mixer
- Speaker mixer
- Mono mixer

The Speaker out of ALC5620 supports ClassAB and Class D type amplifier and can be select at Reg1C[13]:**spk_out_sel.** Owing to the power of voltage of SPKVDD is usually higher than AVDD, ALC5620 have to set Class AB Vmid ratio at Reg40[5:3] and Class D Vmid ratio at Reg40[7:6] in order to extend the output level.

The SPK_OUT_L/R volume and mute are controlled by Reg02. Besides, Reg3E[13]: **pow_spk_r** and Reg3E[12]**:pow_spk_rn** can be used to power down SPK output. Reg3C[14]: **pow_clsab** is used to power down Class AB and Index 46[15:12] is used to power down each output channel of Class D.

SPK_OUT_L/R supports zero corss detect function which can be enable at Reg02[6][14]

5.5.6.2 Headphone Output

HP_OUT_L/R provide 2 channel single ended output. And the source of HP_OUT_L/R can be select from Reg1C[9][8] as below.

- Vmid
- Headphone mixer

The HP_OUT_L/R volume and mute are controlled by Reg04. Besides, Reg3E[11]: **pow_hp_l_vol and** Reg3E[10]**: pow_hp_r_vol** can be used to power down the volume of HP output.

HP_OUT supports zero corss detect function which can be enable at Reg04[14][6]: **hp_l_dezero/ hp_r_dezero.**

5.5.6.3 Mono Output

MONO_OUT which provide 1 channel differential output.And the source of MONO_OUT can be select from Reg1C[7:6] as below.

- Vmid
- Headphone mixer (L+R)
- Speaker mixer
- Mono mixer

The MONO_OUT volume and mute are controlled by Reg08. Besides, Reg3E[14]: **pow_mono_out_vol** can be used to power down the volume of MONO_OUT.

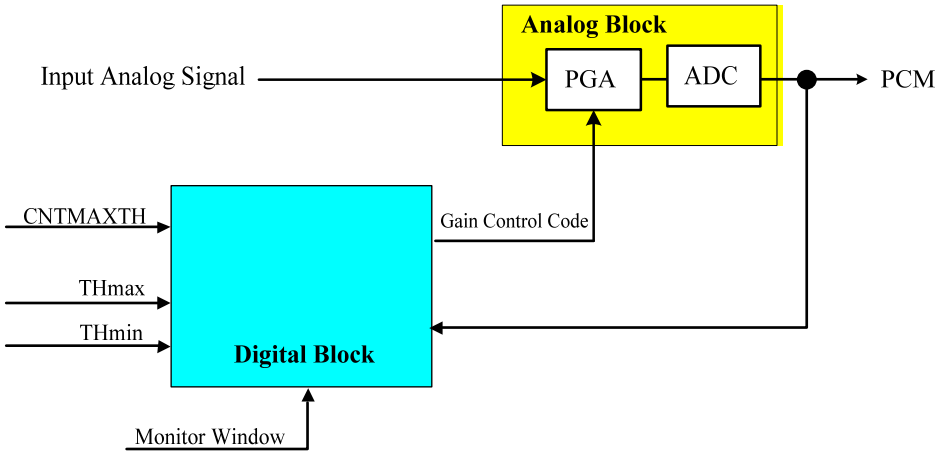
MONO_OUT supports zero corss detect function which can be enable at Reg08[6]:**mono_dezero.**

5.6 AVC Control

The Automatic Volume Control (AVC) function is dynamically adjust the input signal quantized by ADC to an expected sound level by setting THmax and THmin.
When the average level of input signal is higher than the THmax, AVC will decrease the selected analog gain to attenuate the quantized PCM has lower amplitude than THmax. When the average level of input signal is lower than the THmin, the AVC will increase the selected analog gain to amplify the input signal, then its quantized PCM by ADC will higher than THmin. The quantized PCM has average level between THmin and THmax.

AVC reference source channel and target channel can be individual setting by Index20[0] and Reg5E[13:12].

The Architecture of AVC is shown as below:



5.7 Hardware Sound Effect

The Sound Effect block is composted of Pseudo Stereo, Spatial 3D and Equalizer blocks. The Pseudo Stereo block is used to convert a mono source into virtualized stereo output. The Spatial 3D block is a surround sound generator which amplitude (Gain) and surround depth (Ratio) are adjustable. The Equalizer block can be used to compensate speaker response, or make environment sound effect like as 'Pub', 'Live' , 'Rock',… etc..

5.7.1 Equalizer Block

The Equalizer block cascades 5 bands of equalizer to compensate speaker response and emulate environment sound. One high pass filter cascaded in the front end is used to drop low frequency tone which has larger amplitude may damage the mini speaker, it can be also used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength, three bands bi-quad band pass filters are used to emulate environment sound.

To avoid PCM sample saturation, a digital volume control has 0%~100% attenuation in the front of equalizer is required. A 0~+12dB (1~4.0) digital gain control after equalizer is used to compensate PCM output to suitable level.

5.7.2 Pseudo Stereo and Spatial 3D Sound

There are two spatial effects in post-processing part, the Pseudo-Stereo Effect+ Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect is used to convert a mono signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhance the spatial effect. The Stereo Expansion Effect enhances the spatial effect when input signal is Stereo.

5.8 I²C Control Interface

I²C is a 2-wires half-duplex serial communication interface, supporting only slave mode. The host must support MCLK during register access.

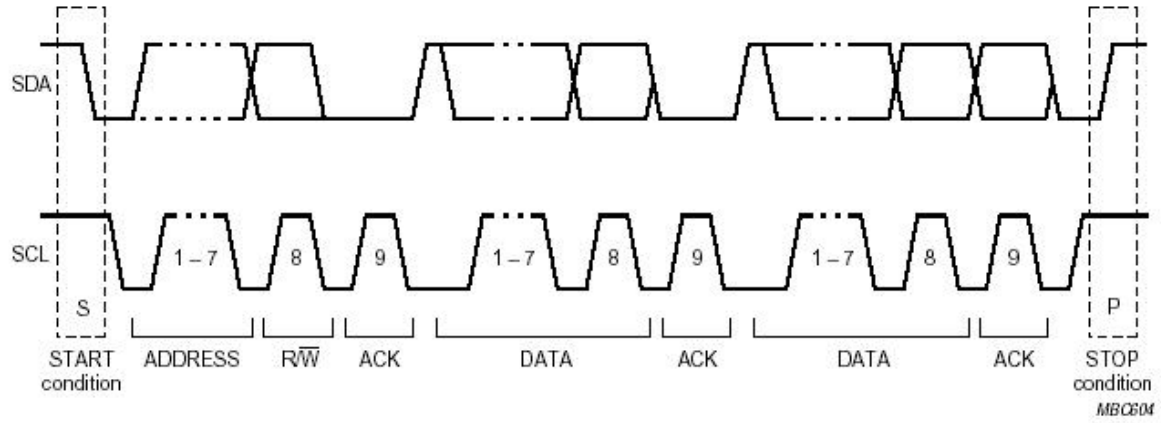
5.8.1 Addressing setting:

(MSB)			BIT				(LSB)
0	0	1	1	0	0	A1	R/W

Note: For A1: determined by external connect to VCC or GND

5.8.2 Complete Data Transfer

Data transfer over I2C control interface:



Write WORD Protocol:

1	7	1	1	8	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	Data Byte High	A	Data Byte Low	A	P

Read WORD Protocol:

1	7	1	1	8	1	7	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	S	Device Address	Rd	A	Data Byte High	A	Data Byte Low	NA	P

S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Mixer Address
A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
£ :Master-to-Slave
£ :Slave-to-Master

5.9 Odd Addressed Register Access

ALC5620 will return “0000h” when those odd-addressed registers and unimplemented registers are read.

5.10 Power Management

ALC5620 supports grouped power down control register (Reg26). Besides, ALC5620 supports more detail Power Management control register within Reg 3A, 3C & 3E. Each particular block will be active only when both Reg26 and Reg3A/3C/3E are set to enable.

5.11 GPIO and Interrupt

ALC5620 supports up to 5 GPIO. Each GPIO can be configured As Input/ Output by Reg4C. When GPIOs are configured as Input, The status will be indicated in Reg54. When GPIOs are configured as Output, Reg5C is used to Drive GPIOs to High (1b) or Low (0b), and the status can be read in Reg54 either.

GPIO input can be configured as sticky by setting Reg50, change polarity by setting Reg4E and wake-up by setting Reg52 in order to generate the interrupt (IRQ) and wake up signal. Wake up function can only be enabled when Wake up control (Reg5E[1])=”1”. Driver can write each bits of Reg54 =“1” to clear each status flag of IRQ.

In addition, when **VoPCM_En (Reg36[15])** =”1” The GPIO1,3,4 and 5 will be dedicated as VoDAC_I2S/PCM interface regardless the setting of GPIO Pin Sharing (Reg56) & GPIO Pin Configure (Reg4C).those pin can’t be use as GPIO in this case. In addition, GPIO pin2 can be configured and pin share to IRQ_Output or IR_Output function by setting Reg56.

Independent to GPIO, there are some Internal Event Signals (Over temperature and MICBIAS short detect) which the same as GPIO input and can be treat as Interrupts source. The application of Internal Event Signal is the same as GPIO and located in Reg4C, Reg4E, Reg50, Reg52 and Reg54.

Please refer to Page 50 for detail GPIO architecture.

6. Mixer Registers List

All mixer register access with odd-number will return with 0.

Note: The default of level shift of D-A/A-D interface should be All "0"

Reg-00h Reset **Default:59B4h**

Register:: (reg_00)			**0x00**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15	R	0'h	Reserved, read as 0
REG_MX00_b14_b10	14:10	R	16'h	SE[4:0]=10110b. (Support Realtek HW 3D)
REG_MX00_b9	9	R	0'h	Not support 20-bit ADC
REG_MX00_b8	8	R	1'h	Support 18-bit ADC
REG_MX00_b7	7	R	1'h	Support 20-bit DAC
REG_MX00_b6	6	R	0'h	Not support 18-bit DAC
REG_MX00_b5	5	R	1'h	Support for Loudness
REG_MX00_b4	4	R	1'h	Headphone output support
REG_MX00_b3	3	R	0'h	Not simulated stereo, for analog 3D block use
REG_MX00_b2	2	R	1'h	Support Bass & Treble Control
Reserved	1	R	0'h	Reserved, read as 0
Reserved	0	R	0'h	Reserved

Œ Write to this register will reset all register to their default value. The written data should be ignored.

Reg-02h Speaker Output Volume **Default:8080h**

Register:: (reg_02)			**0x02**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
sp_l_mute	15	R/W	1'h	Mute Left Control 0: On 1: Mute Left Channel (-∞ dB)
sp_l_dezero	14	R/W	0'h	Left zero cross detector control 0: Disable 1:Enable
Reserved	13	R	0'h	Reserved, read as 0
sp_l_vol	12:8	R/W	0'h	Speaker Output Left Volume (SPKL[4..0]) in 1.5 dB step
sp_r_mute	7	R/W	1'h	Mute Right Control 0: On 1: Mute Right Channel (-∞ dB)

sp_r_dezero	6	R/W	0'h	Right zero cross detector control 0: Disable 1:Enable
Reserved	5	R	0'h	Reserved, read as 0
sp_r_vol	4:0	R/W	0'h	Speaker Output Right Volume (SPKR[4..0]) in 1.5 dB step

Œ For SPKR/SPKL, 00h 0 dB attenuation
1Fh 46.5 dB attenuation

Reg-04h Headphone Output Volume **Default:8080h**

Register:: (reg_04)			**0x04**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
hp_l_mute	15	R/W	1'h	Mute Left Control 0: On 1: Mute Left Channel (-∞ dB)
hp_l_dezero	14	R/W	0'h	Left zero cross detector control 0: Disable 1:Enable
Reserved	13	R	0'h	Reserved, read as 0
hp_l_vol	12:8	R/W	0'h	Headphone Output Left Volume (HPL[4..0]) in 1.5 dB step
hp_r_mute	7	R/W	1'h	Mute Right Control 0: On 1: Mute Right Channel (-∞ dB)
hp_r_dezero	6	R/W	0'h	Right zero cross detector control 0: Disable 1:Enable
Reserved	5	R	0'h	Reserved, read as 0
hp_r_vol	4:0	R/W	0'h	Headphone Output Right Volume (HPR[4..0]) in 1.5 dB step

ŒFor HPR/HPL, 00h 0 dB attenuation
1Fh 46.5 dB attenuation

Reg-08h Phone Input / MONO Output Volume **Default:C880h**

Register:: (reg_08)			**0x08**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
phone2hp_mute	15	R/W	1'h	Mute Phone Input to headphone mixer Control 0: On 1: Mute (-∞ dB)
phone2spk_mute	14	R/W	1'h	Mute Phone Input to Speaker mixer Control 0: On 1: Mute (-∞ dB)
phone_diff_ctrl	13	R/W	0'h	Phone Differential Input Control 0: Disable 1: Enable
phone_vol	12:8	R/W	8'h	Phone Input Volume (PV[4:0]) in 1.5 dB step (not to ADC)
mono_mute	7	R/W	1'h	Mute MONO Output Control 0: On 1: Mute (-∞ dB)
mono_dezero	6	R/W	0'h	Zero cross detector control 0: Disable 1:Enable
mono_diff_	5	R/W	0'h	MONO Output Differential Control 0:

ctrl				Disable (SE) 1: Enable (BTL)
mono_vol	4:0	R/W	0'h	MONO Output Master Volume (MOV[4..0]) in 1.5 dB step

Œ For MOV, 00h 0 dB attenuation
1Fh 46.5 dB attenuation
• For PV, 00h +12 dB gain
08h 0 dB attenuation
1Fh 34.5 dB attenuation

Reg-0Ah LINE_IN Volume **Default:E808h**

Register:: (reg_0a)			**0x0a**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
li2hp_mute	15	R/W	1'h	Mute Volume Output to headphone mixer Control 0: On 1: Mute
li2spk_mute	14	R/W	1'h	Mute Volume Output to Speaker mixer Control 0: On 1: Mute
li2mono_mute	13	R/W	1'h	Mute Volume Output to mono mixer Control 0: On 1: Mute
li_l_vol	12:8	R/W	08'h	LINE_IN Left Volume (NLV[4..0]) in 1.5 dB step
Reserved	7:5	R	0'h	Reserved
li_r_vol	4:0	R/W	8'h	LINE_IN Right Volume (NRV[4..0]) in 1.5 dB step

Œ For NRV/NLV, 00h +12 dB gain
08h 0 dB attenuation
1Fh 34.5 dB attenuation

Reg-0Ch STEREO DAC Volume **Default:E808h**

Register:: (reg_0c)			**0x0c**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
dac2hp_mute	15	R/W	1'h	Mute Volume Output to headphone mixer Control 0: On 1: Mute (-∞ dB)
dac2spk_mute	14	R/W	1'h	Mute Volume Output to Speaker mixer Control 0: On 1: Mute (-∞ dB)
dac2mono_mute	13	R/W	1'h	Mute Volume Output to mono mixer Control 0: On 1: Mute (-∞ dB)
dac_l_vol	12:8	R/W	08'h	PCM Left DAC Volume (PLV[4..0]) in 1.5 dB step
Reserved	7:5	R	0'h	Reserved
dac_r_vol	4:0	R/W	8'h	PCM Right DAC Volume (PRV[4..0]) in 1.5 dB step

Œ For PRV/PLV, 00h +12 dB gain
08h 0 dB attenuation
1Fh 34.5 dB attenuation

Reg-0Eh MIC Volume **Default:0808h**

Register:: (reg_0e)			0x0e	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:13	R	0'h	Reserved
mic1_vol	12:8	R/W	08'h	MIC1 Volume (M1V[4..0]) in 1.5 dB step
Reserved	7:5	R	0'h	Reserved
mic2_vol	4:0	R/W	8'h	MIC2 Volume (M2V[4..0]) in 1.5 dB step

- For M2V/M1V, 00h +12 dB gain
  08h 0 dB attenuation
  1Fh 34.5 dB attenuation

Reg-10h MIC Routing Control **Default:E0E0h**

Register:: (reg_10)			0x10	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
mic12hp_ mute	15	R/W	1'h	Mute MIC1 Volume Output to headphone mixer 0: On 1: Mute
mic12spk_ mute	14	R/W	1'h	Mute MIC1 Volume Output to Speaker mixer 0: On 1: Mute
mic12mono _mute	13	R/W	1'h	Mute MIC1 Volume Output to mono mixer 0: On 1: Mute
mic1_diff_ ctrl	12	R/W	0'h	MIC1 Differential Input Control 0: Disable 1: Enable
Reserved	11:8	R	0'h	Reserved
mic22hp_ mute	7	R/W	1'h	Mute MIC2 Volume Output to headphone mixer 0: On 1: Mute
mic22spk_ mute	6	R/W	1'h	Mute MIC2 Volume Output to Speaker mixer 0: On 1: Mute
mic22mono _mute	5	R/W	1'h	Mute MIC2 Volume Output to mono mixer 0: On 1: Mute
mic2_diff_ ctrl	4	R/W	0'h	MIC2 Differential Input Control 0: Disable 1: Enable
Reserved	3:0	R	0'h	Reserved

Reg-12h ADC Record Gain **Default:F58Bh**

Register:: (reg_12)			0x12	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
adc2hp_l_ mute	15	R/W	1'h	Mute Left Gain Output to headphone mixer Control 0: On 1: Mute (-∞ dB)
adc2hp_r_ mute	14	R/W	1'h	Mute Right Gain Output to headphone mixer Control 0: On 1: Mute (-∞ dB)
adc2mono_	13	R/W	1'h	Mute Left Gain Output to mono mixer Control

l_mute				0: On 1: Mute (-∞ dB)
adc2mono_r_mute	12	R/W	1'h	Mute Right Gain Output to mono mixer Control 0: On 1: Mute (-∞ dB)
adc_l_vol	11:7	R/W	0B'h	ADC Record Gain Left Channel (LRG[4..0]) in 1.5 dB step 00h: -16.5 dB attenuation 0Bh:0 dB gain 1Fh: 30 dB gain
adc_l_dezero	6	R/W	0'h	ADC_L Zero cross detector Control 0: Disable 1: Enable
adc_r_dezero	5	R/W	0'h	ADC_R Zero cross detector Control 0: Disable 1: Enable
adc_r_vol	4:0	R/W	0B'h	ADC Record Gain Right Channel (RRG[4..0]) in 1.5 dB step 00h: -16.5 dB attenuation 0Bh:0 dB gain 1Fh: 30 dB gain

Reg-14h ADC record Mixer Control **Default:7F7Fh**

Register:: (reg_14)			**0x14**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15	R	0'h	Reserved
adcrec_l_mute	14:8	R/W	7F'h	Left Mixer Mute Control 0: On 1: Mute (-∞ dB) Bit 14: MIC1 Bit 13: MIC2 Bit 12: LINE_IN_L Bit 11: PHONE Bit 10: Headphone Mixer Left Channel Bit 9: Speaker mixer Bit 8: Mono Mixer
Reserved	7	R	0'h	Reserved
adcrec_r_mute	6:0	R/W	7F'h	Right Mixer Mute Control 0: On 1: Mute (-∞ dB) Bit 6: MIC1 Bit 5: MIC2 Bit 4: LINE_IN_R Bit 3: PHONE Bit 2: Headphone Mixer Right Channel Bit 1: Speaker mixer Bit 0: Mono Mixer

Reg-18h Voice DAC Output Volume **Default:E800h**

Register:: (reg_18)			**0x18**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**

voice2hp_mute	15	R/W	1'h	Mute DAC Output to headphone mixer Control 0: On 1: Mute (-∞ dB)
voice2spk_mute	14	R/W	1'h	Mute DAC Output to Speaker mixer Control 0: On 1: Mute (-∞ dB)
voice2mono_mute	13	R/W	1'h	Mute DAC Output to mono mixer Control 0: On 1: Mute (-∞ dB)
voice_vol	12:8	R/W	8'h	Voice Output Volume (VV[4..0]) in 1.5 dB step
Reserved	7:0	R	0'h	Reserved

Œ For NRV, 00h +12 dB gain
08h 0 dB attenuation
1Fh 34.5 dB attenuation

Reg-1Ch Output Mixer Control **Default:0000h**

Register:: (reg_1c)			**0x1c**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
spk_l_vol_in_sel	15:14	R/W	0'h	SPKL Volume Input Select 00: VMID (No input) 01: HP Left Mixer 10: Speaker mixer 11: MONO
spk_out_sel	13	R/W	0'h	SPKL and SPKR Output Select 0: Class AB 1: Class D
spk_r_vol_in_sel	12:11	R/W	0'h	SPKR Volume Input Select 00: VMID (No input) 01: HP Right Mixer 10: Speaker mixer 11: MONO
Reserved	10	R	0'h	Reserved
hp_l_in_sel	9	R/W	0'h	HPL Volume Input Select 0: VMID (No input) 1: HP Left Mixer
hp_r_in_sel	8	R/W	0'h	HPR Volume Input Select 0: VMID (No input) 1: HP Right Mixer
mono_in_sel	7:6	R/W	0'h	MONO Volume Input Select 00: VMID (No input) 01: HP Left + Right Mixer 10: Speaker mixer 11: MONO Mixer
Reserved	5	R	0'h	Reserved
clab_ampr_source_sel	4	R/W	0'h	At Class AB mode, SPK_OUT_R Output Amplifier Source Select 0: SPKR Volume Output 1: SPKL Volume Output

				Note: SPK_OUT_RN: SPKR Volume Negative Output,
Reserved	3:0	R	0'h	Reserved

Reg-20h Reserved **Default:0000h**

Register:: (reg_20)			**0x20**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:0	R/W	0'h	Reserved

Reg-22h Microphone Control **Default:0000h**

Register:: (reg_22)			**0x22**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	0'h	Reserved
mic1_boost_ctrl	11:10	R/W	0'h	MIC1 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: +40dB
mic2_boost_ctrl	9:8	R/W	0'h	MIC2 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: +40dB
Reserved	7:6	R	0'h	Reserved, Read as 0
mic1_bias_voltage_ctrl	5	R/W	0'h	MICBIAS1 Output Voltage Control 0: 0.9 * AVDD 1: 0.75 * AVDD
mic2_bias_voltage_ctrl	4	R/W	0'h	MICBIAS2 Output Voltage Control 0: 0.9 * AVDD 1: 0.75 * AVDD
Reserved	2:3	R	0'h	Reserved, Read as 0
mic_bias_threshold	1:0	R/W	0'h	MICBIAS1/2 Short Current Detector Threshold 00: 600uA 01: 1200uA 1x: 1800uA

Reg-26h Power down Control/Status **Default:EF00h**

Register:: (reg_26)			**0x26**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
ac_pr7	15	R/W	1'h	PR7 0: Normal 1: Power down Speaker Amplifier

ac_pr6	14	R/W	1'h	PR6 0: Normal 1: Power down Headphone Out and MONO Out
ac_pr5	13	R/W	1'h	PR5 0: Normal 1: Disable internal clock
Reserved	12	R/W	0'h	Reserved
ac_pr3	11	R/W	1'h	PR3 0: Normal 1: Power down Mixer (Vref /Vrefout off)
ac_pr2	10	R/W	1'h	PR2 0: Normal 1: Power down Mixer (Vref /Vrefout are still on)
ac_pr1	9	R/W	1'h	PR1 0: Normal 1: Power down STEREO DAC
ac_pr0	8	R/W	1'h	PR0 0: Normal 1: Power down STEREO ADC, and input MUX
Reserved	7:4	R	0'h	Reserved, Read as 0
vref_status	3	R	0'h	Vref status 1: Vref is up to normal level 0: Not yet
analog_mixer_status	2	R	0'h	Analog Mixer status 1: Ready 0: Not yet
dac_status	1	R	0'h	DAC status 1: Ready 0: Not yet (Inverse of PR1)
adc_status	0	R	0'h	ADC status 1: Ready 0: Not yet (Inverse of PR0)

True table for power down mode: (PD= Power down)

	ADC	DAC	Mixer	Verf	Int CLK	HP-OUT	Mono-OUT	SPK-OUT
PR0=1	PD							
PR1=1		PD						
PR2=1			PD			PD		
PR3=1	PD	PD	PD	PD		PD		
PR5=1	PD	PD			PD			
PR6=1						PD	PD	
PR7=1								PD

Reg-34h Main Serial Data Port Control (Stereo I2S) **Default:0000h**

Register:: (reg_34)			**0x34**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
stereo_i2s_mode_sel	15	R/W	0'h	Main Serial Data Port Mode Selection 0: Master 1: Slave
stereo_i2s_sadlrck_ctrl_en	14	R/W	0'h	SADLRCK Control: Set to "1" when ADC and DAC are different sampling rate 0: Disable, ADC and DAC use the same Fs 1: Enable Note: frame clock have to input from SDALRCK

				when this bit set to"0"
Reserved	13	R	0'h	Reserved
stereo_i2s_bclk_polarity_ctrl	12	R/W	0'h	Stereo I2S BCLK Polarity Control 0: Normal 1: Invert
i2s_da_sigma_delta_clock_sel	11	R/W	0'h	I2S_DA_Sigma_Delta_clock source select 0b:from DA Filter 1b:from DA Sigma Delta Clock Divider
i2s_da_sigma_delta_clock_div	10:8	R/W	0'h	I2S DA Sigma Delta clock divider 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 101b: ÷ 64 Others: Reserved
da_li_filter_en	7	R/W	0'h	Stereo DAC linear interpolation filter enable 0b: Disable 1b: Enable Note: just for performance verification
stereo_i2s_pcm_mode_sel	6	R/W	0'h	PCM Mode Select 0: Mode A 1: Mode B Non PCM Mode Control 0: Normal SADLRCK / SDALRCK 1: Invert SADLRCK / SDALRCK Note: only support when stereo_i2s_sadlrck_ctrl_en ="0"
Reserved	5:4	R	0'h	Reserved
stereo_i2s_data_len_sel	3:2	R/W	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits
stereo_i2s_data_format_sel	1:0	R/W	0'h	Stereo PCM Data Format Selection 00: I^2S format 01: Right justified 10: Left justified 11: PCM format

Note: Main DAC 32*Fs BITCLK INV not support to Left justified format.

Reg-36h Extend Serial Data Port Control (VoDAC_I2S/PCM) **Default:0000h**

Register:: (reg_36)			**0x36**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**

VoPCM_En	15	R/W	0'b	Enable PCM interface on GPIO1,3,4,5. Œ 0: GPIO function 1: VoPCM interface
voice_port_sel	14	R/W	0'h	Extend Serial Data Port Mode Selection 0: Master 1: Slave
Reserved	13:9	R	00'h	Reserved
voice_adc_enable	8	R/W	0'b	Voice ADC Enable 0b:Disable (ADC_L=ADC_R=Stereo) 1b:Enable (ADC_L=Stereo, ADC_R=Voice)
voice_vbclk_polarity_ctrl	7	R/W	0'h	Voice I2S VBCLK Polarity Control 0: Normal 1: Invert
voice_pcm_mode_sel	6	R/W	0'h	PCM Mode Select 0: Mode A 1: Mode B Non PCM Mode Control 0: Normal VSLRCK 1: Invert VSLRCK
Reserved	5:4	R	0'h	Reserved
voice_data_len_sel	3:2	R/W	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits
voice_data_format_sel	1:0	R/W	0'h	Voice Data Format Selection 00: I^2S format 01: Right justified 10: Left justified 11: PCM format

Reg-3Ah Power management addition 1 **Default:0000h**

Register:: (reg_3A)			**0x3A**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Depop_monooutb	15	R/W	0'h	Depop of Mono Out 0:Enable (De-pop Enable) 1:Disable (De-pop Disable)
Depop_hp_outb	14	R/W	0'h	Depop of HP Out 0:Enable (De-pop Enable) 1:Disable (De-pop Disable)
pow_zcd	13	R/W	0'h	All Zero Cross Detect Power down (include digital) 0:Disable 1:Enable
ip_en	12	R/W	0'h	Pressure measurement source current enable 0:Disable

				1:Enable
Main_i2s_en	11	R/W	0'h	Main I2S Digital interface enable 0:Disable 1:Enable
Reserved	10:6	R/W	0'h	Reserved
pow_mic1_bias_det_ctrl	5	R/W	0'h	MICBIAS1 Short Current Detector Control 0: Disable 1: Enable
pow_mic2_bias_det_ctrl	4	R/W	0'h	MICBIAS2 Short Current Detector Control 0: Disable 1: Enable
pow_mic1_bias	3	R/W	0'h	0: Disable 1: Enable microphone1 bias
pow_mic2_bias	2	R/W	0'h	0: Disable 1: Enable microphone2 bias
pow_main_bias	1	R/W	0'h	0:Disable……1:Enable Main bias of ALC5620
pow_dac_ref	0	R/W	0'h	0:Disable……1:Enable dac reference of ALC5620

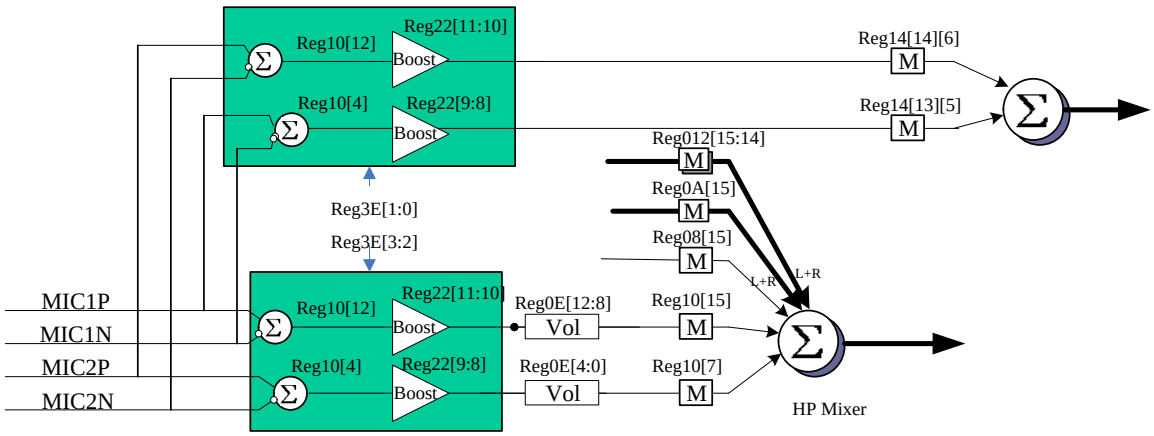
Reg-3Ch Power management addition 2 **Default:0000h**

Register:: (reg_3C)			**0x3C**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
pow_thermal	15	R/W	0'h	0: Disable 1: Enable thermal detect (temp sensor)
pow_clsab	14	R/W	0'h	0: Disable 1: Enable ALL Class_AB Power
pow_vref	13	R/W	0'h	0: Disable 1: Enable VREF of All Analog Circuit (Vref pin)
pow_pll	12	R/W	0'h	0: Disable 1: Enable PLL
Reserved	11	R/W	0'h	Reserved
pow_voice_dac	10	R/W	0'h	0: Disable 1: Enable Voice DAC/ADC VoDAC clock will be disable while Disable (Include Voice_I2S interface)
pow_dac_l	9	R/W	0'h	0: Disable 1: Enable left STEREO DAC filter clock
pow_dac_r	8	R/W	0'h	0: Disable 1: Enable right STEREO DAC filter clock
pow_adc_l	7	R/W	0'h	0: Disable 1: Enable left STEREO ADC filter clock and input gain
pow_adc_r	6	R/W	0'h	0: Disable 1: Enable right STEREO ADC filter clock and input gain
pow_hp_l_mix	5	R/W	0'h	0: Disable 1: Enable left headphone mixer
pow_hp_r_	4	R/W	0'h	0: Disable 1: Enable right headphone mixer

mix				
pow_spk_mix	3	R/W	0'h	0: Disable 1: Enable Speaker mixer
pow_mono_mix	2	R/W	0'h	0: Disable 1: Enable MONO mixer
pow_adc_rec_l	1	R/W	0'h	0: Disable 1: Enable left ADC record mixer
pow_adc_rec_r	0	R/W	0'h	0: Disable 1: Enable right ADC record mixer

Reg-3Eh Power management addition 3 **Default:0000h**

Register:: (reg_3E)			**0x3E**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15	R	0'h	Reserved
pow_mono_out_vol	14	R/W	0'h	0: Disable 1: Enable MONO_OUT Volume control (Amp)
pow_spk_outln	13	R/W	0'h	0: Disable 1: Enable SPK_OUTLN Output (enable Class AB & Class D)
pow_spk_outrn	12	R/W	0'h	0: Disable 1: Enable SPK_OUTRN Output (enable Class AB & Class D)
pow_hp_l_vol	11	R/W	0'h	0: Disable 1: Enable HP_OUT_L Volume control (Amp)
pow_hp_r_vol	10	R/W	0'h	0: Disable 1: Enable HP_OUT_R Volume control (Amp)
pow_spk_l	9	R/W	0'h	0: Disable 1: Enable SPK_OUT_L Output (enable Class AB & Class D)
pow_spk_r	8	R/W	0'h	0: Disable 1: Enable SPK_OUT_R Output (enable Class AB & Class D)
pow_li_l_vol	7	R/W	0'h	0: Disable 1: Enable LINE_IN Left Volume control
pow_li_r_vol	6	R/W	0'h	0: Disable 1: Enable LINE_IN Right Volume control
pow_phone_vol	5	R/W	0'h	0: Disable 1: Enable PHONE Volume control
pow_phone_admixer	4	R/W	0'h	0: Disable 1: Enable PHONE ADmixder
pow_mic1_vol	3	R/W	0'h	0: Disable 1: Enable MIC1 Volume control
pow_mic2_vol	2	R/W	0'h	0: Disable 1: Enable MIC2 Volume control
pow_mic1_admixer	1	R/W	0'h	0: Disable 1: Enable MIC1 Admixer and Boost
pow_mic2_admixer	0	R/W	0'h	0: Disable 1: Enable MIC2 Admixer and Boost



Reg-40h General Purpose Control Register 1 **Default:0428h**

Register:: (reg_40)			**0x40**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
sel_sysclk	15	R/W	0'h	Stereo SYSCLK Source Select 0: MCLK 1: PLL Output
Extclk_dir	14	R/W	0'h	EXTCLK Direction Control 0: Input 1: Output
Reserved	13:10	R/W	1'h	Reserved
hp_amp_ctrl	9:8	R/W	0'h	Headphone amplifier V_{MID} ratio control (output gain control) 00: 1 01: 1.25 1x: 1.5
spk_ampD_ctrl	7:6	R/W	0'h	Speaker Class D amplifier V_{MID} ratio control (output gain control) 00: 1.75 Vdd 01: 1.5 Vdd 10: 1.25 Vdd 11: 1.0 Vdd
spk_ampAB_ctrl	5:3	R/W	5'h	Speaker Class AB amplifier V_{MID} ratio control (output gain control) 000: 2.25 Vdd 001: 2.00 Vdd 010: 1.75 Vdd 011: 1.5 Vdd 100: 1.25 Vdd 101: 1 Vdd Others: not allowed

Reserved	2	R/W	0'h	**Reserved**
a1_status	1	R	0'h	A1 pin status for I^2C 0: 0 1: 1
ir_out_en	0	R/W	0'h	IR data output control 0: Disable 1: Enable

Reg-42h General Purpose Control Register 2 **Default:0000h**

Register:: (reg_42)			**0x42**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
voice_stereo_digitalpath_en	**15**	**R/W**	**0'b**	**Voice to Stereo digital path Enable** **0b:Disable** **1b:Enable**
pll_sour_sel	14	R/W	0'h	pll_source_select 0: from MCLK 1: from BIT_CLK
se_btl_clsab	13	R/W	0'b	Single End & BTL of Class AB selection: 0: Differential Mode 1: Single-End Mode
Reserved	12:6	R/W	0'h	Reserved
ir_div	5:4	R/W	00'b	IR_divider 00: ÷ 1 01: ÷ 2 10: ÷ 4 11: Reserved
Reserved	3:1	R/W	0'h	Reserved
PLL_pre_div	0	R/W	0'b	Pll_pre_divider 0b: ÷ 1 1b: ÷ 2

Reg-44h PLL Control **Default:0000h**

Register:: (reg_44)			**0x44**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
pll_n_code	15:8	R/W	00'h	N[7:0] code for analog PLL 00000000: Div 2 00000001: Div 3 …….. 11111111: Div 257
pll_m_bypass	7	R/W	0'h	Bypass PLL M 0b:no bypass 1b:Bypass
pll_k_code	6:4	R/W	0'h	K[2:0] code for analog PLL

				000: Div 2 001: Div 3 …….. 111: Div 9
pll_m_code	3:0	R/W	0'h	M[3:0] code for analog PLL 0000: Div 2 0001: Div 3 …….. 1111: Div 17

The PLL1 transmit formula is

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

For I2C+I^{2}S clock setting table for 48K: (unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

For I^{2}C+I2S clock setting table for 44.1K: (unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

Reg-4Ch GPIO Pin Configuration **Default:2E3Eh**

Register:: (reg_4c)			**0x4c**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	00'b	Reserved
over_temp _conf	11	R/W	1'h	Over temperature status source configure 0: bypass 1: Normal
mic1_short	10	R/W	1'h	MICBIAS1 short current status source configure

_det_conf				0: bypass 1: Normal
mic2_short _det_conf	9	R/W	1'h	MICBIAS2 short current status source configure 0: bypass 1: Normal
Reserved	8:6	R	0'h	Reserved
gpio5_conf	5	R/W	1'h	GPIO5 Pin Configuration 0: Output 1: Input
gpio4_conf	4	R/W	1'h	GPIO4 Pin Configuration 0: Output 1: Input
gpio3_conf	3	R/W	1'h	GPIO3 Pin Configuration 0: Output 1: Input
gpio2_conf	2	R/W	1'h	GPIO2 Pin Configuration 0: Output 1: Input
gpio1_conf	1	R/W	1'h	GPIO1 Pin Configuration 0: Output 1: Input
Reserved	0	R	0'h	Reserved, Read as 0

Reg-4Eh GPIO Pin Polarity **Default:2E3Eh**

Register:: (reg_4e)			**0x4e**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	00'b	Reserved
over_temp _polarity	11	R/W	1'h	Over temperature Polarity 0: Low Active 1: High Active
mic1_short _det_polarity	10	R/W	1'h	MICBIAS1 short current detect Polarity 0: Low Active 1: High Active
mic2_short _det_polarity	9	R/W	1'h	MICBIAS2 short current detect Polarity 0: Low Active 1: High Active
Reserved	8:6	R	0'h	Reserved, Read as 0
gpio5_polarity	5	R/W	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio4_polarity	4	R/W	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio3_polarity	3	R/W	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio2_polarity	2	R/W	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio1_polarity	1	R/W	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
Reserved	0	R	0'h	Reserved, Read as 0

Reg-50h GPIO Pin Sticky **Default:0000h**

Register:: (reg_50)			0x50	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	00'b	Reserved
over_temp_sticky_En	11	R/W	0'h	Over temperature Sticky Enable 0: Not sticky 1: Sticky
mic1_short_det_sticky_En	10	R/W	0'h	MICBIAS1 short current detect Sticky Enable 0: Not sticky 1: Sticky
mic2_short_det_sticky_En	9	R/W	0'h	MICBIAS2 short current detect Sticky Enable 0: Not sticky 1: Sticky
Reserved	8:6	R	0'h	Reserved, Read as 0
gpio5_sticky_En	5	R/W	0'h	GPIO5 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio4_sticky_En	4	R/W	0'h	GPIO4 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio3_sticky_En	3	R/W	0'h	GPIO3 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio2_sticky_En	2	R/W	0'h	GPIO2 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio1_sticky_En	1	R/W	0'h	GPIO1 Pin Sticky Enable 0: Not sticky 1: Sticky
Reserved	0	R	0'h	Reserved, Read as 0

Reg-52h GPIO Pin Wake-up **Default:0000h**

Register:: (reg_52)			0x52	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	00'b	Reserved
over_temp_wakeup_en	11	R/W	0'h	Over temperature Wake-up Enable 0: No wake-up 1: Wake Up
mic1_short_det_wakeup_en	10	R/W	0'h	MICBIAS1 short current detect Wake-up Enable 0: No wake-up 1: Wake Up
mic2_short_det_wakeup_en	9	R/W	0'h	MICBIAS2 short current detect Wake-up Enable 0: No wake-up 1: Wake Up
Reserved	8:6	R	0'h	Reserved, Read as 0
gpio5_wakeup_en	5	R/W	0'h	GPIO5 Pin Wake-up Enable 0: No wake-up 1: Wake Up

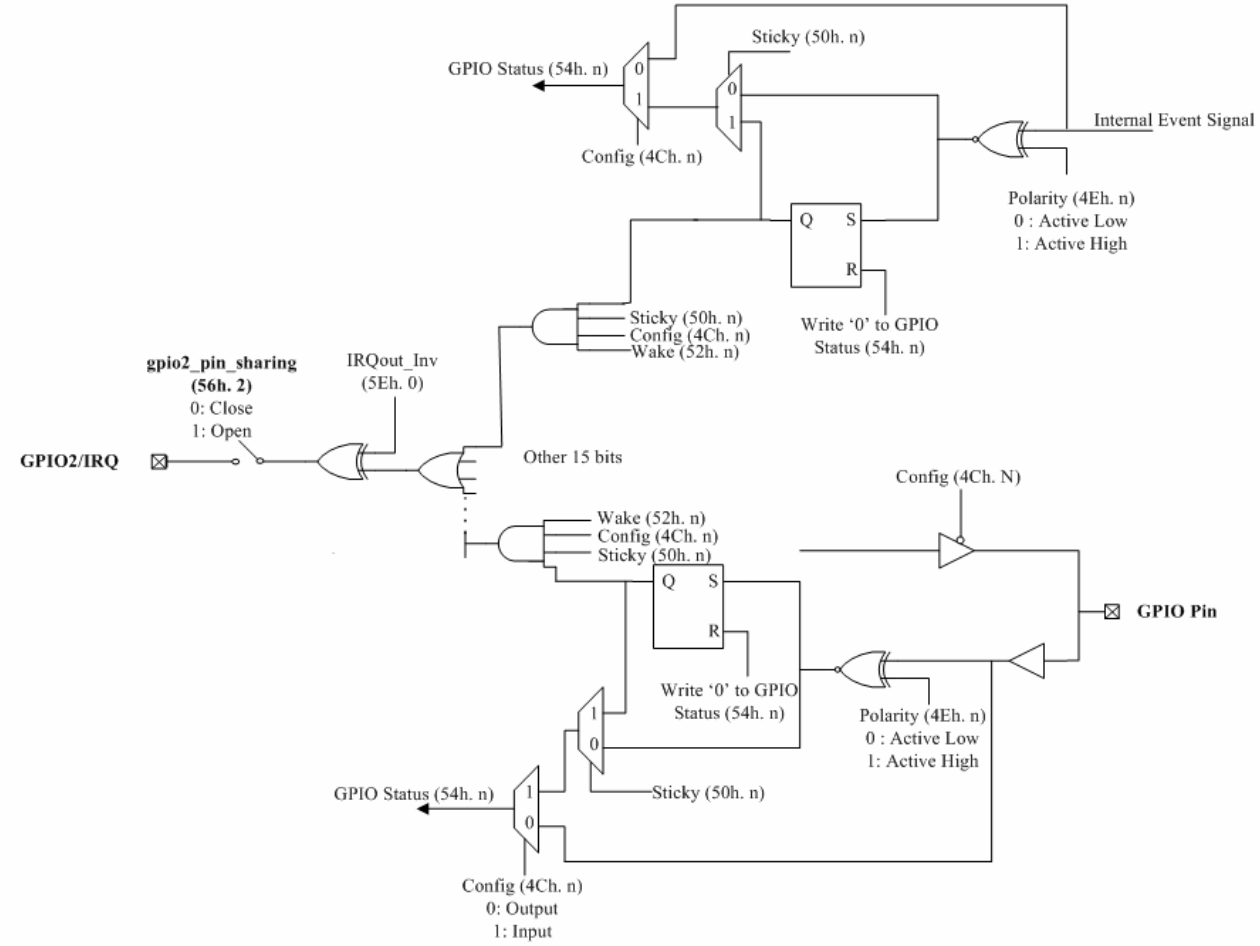
gpio4_wakeup_en	4	R/W	0'h	GPIO4 Pin Wake-up Enable 0: No wake-up 1: Wake Up
gpio3_wakeup_en	3	R/W	0'h	GPIO3 Pin Wake-up Enable 0: No wake-up 1: Wake Up
gpio2_wakeup_en	2	R/W	0'h	GPIO2 Pin Wake-up Enable 0: No wake-up 1: Wake Up
gpio1_wakeup_en	1	R/W	0'h	GPIO1 Pin Wake-up Enable 0: No wake-up 1: Wake Up
Reserved	0	R	0'h	Reserved, Read as 0

Reg-54h GPIO Pin Status **Default:003Ah**

Register:: (reg_54)			**0x54**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	00'b	Reserved
over_temp_status	11	R	0'h	Over temperature Status Read: Return status Write: Writing '0' clears sticky bit
mic1_short_det_status	10	R	0'h	MICBIAS1 short current detect Status Read: Return status Write: Writing '0' clears sticky bit
mic2_short_det_status	9	R	0'h	MICBIAS2 short current detect Status Read: Return status Write: Writing '0' clears sticky bit
Reserved	8:6	R	0'h	Reserved, Read as 0
gpio5_status	5	R	1'h	GPIO5 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears sticky bit
gpio4_status	4	R	1'h	GPIO4 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears sticky bit
gpio3_status	3	R	1'h	GPIO3 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears sticky bit
gpio2_status	2	R	1'h	GPIO2 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears sticky bit
gpio1_status	1	R	1'h	GPIO1 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears sticky bit
Reserved	0	R	0'h	Reserved, Read as 0

Reg-56h Pin Sharing **Default:0000h**

Register:: (reg_56)			0x56	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:7	R	0'h	Reserved
MX56_6	6	R/W	0'b	Reserved
MX56_5	5	R/W	0'b	Reserved
Reserved	4	R	0'h	Reserved
gpio2_pin_ sharing	3:2	R/W	0'h	GPIO2 Pin Sharing 00: IRQ_Out 01: GPIO enable 10: IR Out Others: Reserved
Reserved	1:0	R	0'h	Reserved



GPIO BIT Reg54[15:1]	SLOT 12 BIT	SOURCE	DESCRIPTION
1	5	GPIO Pin	GPIO1 input status

2	6	GPIO Pin	GPIO2 input status
3	7	GPIO Pin	GPIO3 input status
4	8	GPIO Pin	GPIO4 input status
5	9	GPIO Pin	GPIO5 input status
6	10	-	Unused
7	11	-	Unused
8	12	-	Unused
9	13	VGPIO	MICBIAS2 short current detect
10	14	VGPIO	MICBIAS1 short current detect
11	15	VGPIO	Over temperature
12	16	-	Unused
13	17	-	Unused
14	18	-	Unused
15	19	-	Unused

Reg-58h OverTemp/Cuttent status **Default:0CFFh**

Register:: (reg_58)			**0x58**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:12	R	0000'h	Reserved
ovt_hp_status	11	R	1'h	Headphone Amp over temperature 0:normal 1:over temperature
ovt_mono_status	10	R	1'h	MONO Amp over temperature 0:normal 1: Over temperature
ovc_micbias1_status	9	R	0'h	MICBIAS1 Over current 0:normal 1: Over current
ovc_micbias2_status	8	R	0'h	MICBIAS2 Over current 0:normal 1: Over current
rp_depup_status	7	R	1'h	RP channel depop status 0:depop ready , 1:depop finish
rn_depup_status	6	R	1'h	RN channel depop status 0:depop ready , 1:depop finish
lp_depup_status	5	R	1'h	LP channel depop status 0:depop ready , 1:depop finish
ln_depup_status	4	R	1'h	LN channel depop status 0:depop ready , 1:depop finish
ovt_rp_status	3	R	1'h	RP channel Temp. Sensor status 0:normal , 1:over-temp
ovt_rn_status	2	R	1'h	RN channel Temp. Sensor status 0:normal , 1:over-temp
ovt_lp_status	1	R	1'h	LP channel Temp. Sensor status 0:normal , 1:over-temp
ovt_ln_stat	0	R	1'h	LN channel Temp. Sensor status 0:normal ,

us				1:over-temp

Reg-5Ch GPIO_Output Pin Control **Default:0000h**

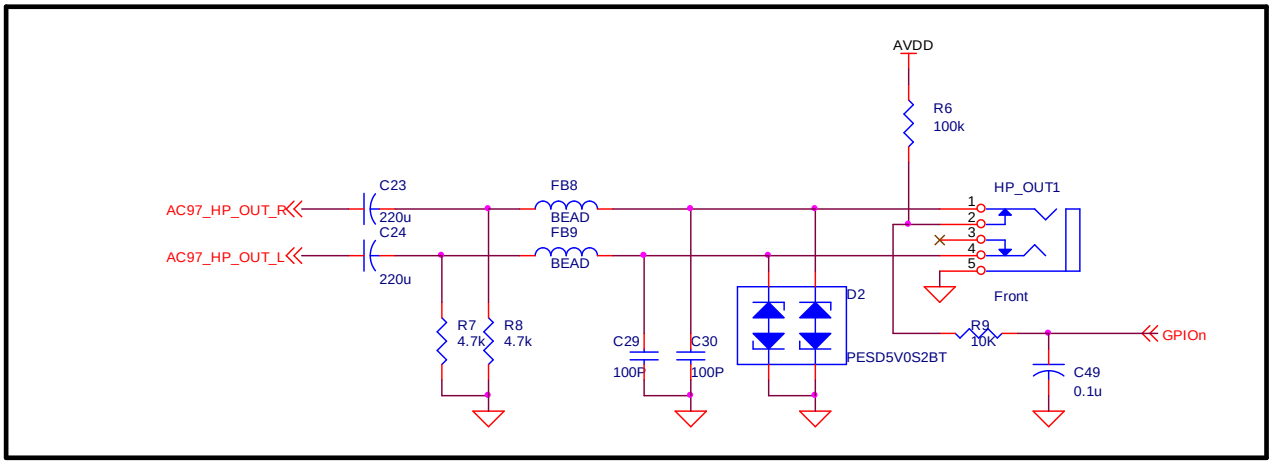
Register:: (reg_5C)			**0x5C**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Reserved	15:6	R	0000'h	Reserved
gpio5_out_status	5	R/W	0'h	GPIO5 Output Pin Control 0b: Drive Low 1b: Drive High
gpio4_out_status	4	R/W	0'h	GPIO4 Output Pin Control 0b: Drive Low 1b: Drive High
gpio3_out_status	3	R/W	0'h	GPIO3 Output Pin Control 0b: Drive Low 1b: Drive High
gpio2_out_status	2	R/W	0'h	GPIO2 Output Pin Control 0b: Drive Low 1b: Drive High
gpio1_out_status	1	R/W	0'h	GPIO1 Output Pin Control 0b: Drive Low 1b: Drive High
REG_MX52_b0	0	R	0'h	Reserved, Read as 0

Reg-5Eh MISC Control **Default:0000h**

Register:: (reg_5E)			**0x5E**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
en_vref_fast	15	R/W	0'b	Enable fast Vreg (This bit have to be disable before play back & record) Ž 0: Enable fast Vref 1: Disable fast Vref
clsab_amp_sel	14	R/W	0'b	Class AB Output Amplifier Select • 0: Strong Amp 1: Weak Amp
AVC_target_sel	13:12	R/W	0'b	AVC target sel 00: Reserved (No AVC) 01: R Channel 10: L Channel 11: Both channel
thermal_shutdown_en	11	R/W	0'b	Thermal Shut Down Enable 0: Disable 1: Enable
REG_MX5A_b9_b8	10:7	R/W	0'h	Reserved

main_dac_l_mute	6	R/W	0'h	Mute Main DAC Left Input 0: On 1: Mute (-∞ dB)
main_dac_r_mute	5	R/W	0'h	Mute Main DAC Right Input 0: On 1: Mute (-∞ dB)
voice_dac_mute	4	R/W	0'h	Mute Voice DAC Input 0: On 1: Mute (-∞ dB)
REG_MX5A_b3_b2	3:1	R/W	0'h	Reserved
irqout_inv_ctrl	0	R/W	0'h	IRQOUT Inverter Control 0: Normal 1: Invert

Œ Jack insert detect pull up resister is implemented by external circuit



- Strong Amp **è** SPKVDD: 3.0V~5V and Set index44[8:6]=100'b
  Weak Amp **è** SPKVDD: 2.3V~5V and Set index44[8:6]=000'b

Ž en_vref_fast have to be disable before playback/Record to improve RSRR.

Reg-60h Stereo DAC Clock Control_1 **Default:3075h**

Register:: (reg_60)			**0x60**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
stereo_i2s_sclk_div1	15:12	R/W	3'h	Stereo_I2S_SCLK_Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 …….. 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
Reserved	11	R/W	0'h	Reserved
stereo_i2s_sclk_div2	10:8	R/W	0'h	Stereo_I2S_SCLK_Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8

				011b: ÷ 16 100b: ÷ 32 Others: Reserved
Stereo_i2s_ad_wclk_div1	7:4	R/W	7'h	Stereo_I2S_AD_WCLK_Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 …….. 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
Stereo_i2s_ad_wclk_div2	3:1	R/W	010'b	Stereo_I2S_AD_WCLK_Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
Stereo_i2s_da_wclk_div	0	R/W	1'h	Stereo_I2S_DA_WCLK_Div 0b:32 1b:64

Reg-62h Stereo DAC Clock Control_2 **Default:1010h**

Register:: (reg_62)			**0x62**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Stereo_i2s_da_filter_div1	15:12	R/W	1'h	Stereo_I2S_DA_Filter_Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 ……. 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
Stereo_i2s_da_filter_div2	11:9	R/W	0'h	Stereo_I2S_DA_Filter_Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
Stereo_da_64osr	8	R/W	0'h	Stereo DA filter Select 0b:128x 1b:64x

Stereo_i2s_ad_filter_div1	7:4	R/W	1'h	Stereo_I2S_AD_Filter_Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 …… 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
Stereo_i2s_ad_filter_div2	3:1	R/W	0'h	Stereo_I2S_AD_Filter_Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
Stereo_ad_64osr	0	R/W	0'h	Stereo AD filter Select 0b:128x 1b:64x

Reg-64h VoDAC_PCM Clock Control_1 **Default:2130h**

Register:: (reg_64)			**0x64**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Voice_mclk_sel	15	R/W	0'h	VCLK_selection 0b:MCLK input 1b:PLL output
Voice_sysclk_sel	14	R/W	0'h	Voice_sysclk_selection 0b:VCLK 1b:EXTCLK
I2s_wclk voice_master_sel	13	R/W	1'h	I2s_wclk voice_master_sel 0b: ÷32 1b: ÷64
Reserved	12:11	R	0'b	Reserved
Extclk_out_sel	10:8	R/W	1'h	Extclk_out_sel 000b: ÷ 1 001b: ÷ 2 010b: ÷ 4 011b: ÷ 8 100b: ÷ 16 Others: Reserved
I2s_sclk_voice_master_sel_1	7:4	R/W	3'h	I2s_sclk_voice_master_sel_1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 ……

				1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
Reserved	3	R	0'b	Reserved
I2s_sclk_voice_master_sel_2	2:0	R/W	0'h	I2s_sclk_voice_master_sel_2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved

Reg-66h VoDAC_PCM Clock Control_2 **Default:0010h**

Register:: (reg_66)			**0x66**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
Sel_clk_filter_slave	15	R/W	0'h	Sel_clk_filter_slave 0b: ÷ 1 1b: ÷ 2
Sel_clk_filter	14	R/W	0'h	Select Voice filter Clock source 0b: from MCLK/EXTCLK 1b: from VBCLK
Voice_64osr	13	R/W	0'h	Voice DA/AD filter select 0b:128x 1b:64x
voice_sigma_delta_clock_sel	12	R/W	0'h	Voice_DA/AD_Sigma_Delta_clock source select 0b:from DA Filter 1b:from DA Sigma Delta Clock Divider
Reserved	11	R	0'h	Reserved
voice_sigma_delta_clock_div	10:8	R/W	0'h	Voice DA/AD Sigma Delta clock divider 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 101b: ÷ 64
clk_filter_master_sel_1	7:4	R/W	1'h	clk_filter_master_sel_2 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 ……. 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16

Reserved	3	R	0'h	Reserved
clk_filter_master_sel_2	2:0	R/W	0'h	clk_filter_master_sel_1 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved

Reg-68h Psedueo Stereo & Spatial Effect Block Control **Default:0053h**

Register:: (reg_68)			**0x68**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
spatial_ctrl_enable	15	R/W	0'b	Spatial Enable 0b:Disable(clear internal state) 1b:Enable
apf_en	14	R/W	0'h	Enable All Pass Filter APF(z), EN-APF 0: Disabled (bypass) and reset. 1: Enable all pass filter, the coefficient a1 is loaded from REG_MX64.[7:0]
pseudo_stereo_en	13	R/W	0'h	Enable Pseudo Stereo Block, EN-PSB 0: Disabled 1: Enabled
en_3d	12	R/W	0'h	Enable Stereo Expension Block , EN-SEB 0: Disable 1:Enabled, load 3D Ratio from ratio_parm_3d and 3D Gain from gain_parm_3d
Reserved	11:8		0'h	Reserved
gain_parm_3d	7:6	R/W	1'h	3D Gain Parameter (SEGn) 00: Gain=1.0 01: Gain=1.5 10:Gain=2.0 11:Reserved
ratio_parm_3d	5:4	R/W	1'h	3D Ratio Parameter (DPn) 00: Ratio=0.0 01: Ratio=0.66 10:Ratio=1.0 11:Reserved
Reserved	3:2		0'h	Reserved
apf_parm_a1	1:0	R/W	3'h	All Pass Filter parameter a1 in 2's complement 1.7 format. (-1.0~0.99) 00: a1=0. 01: a1=-0.25 (for 32kHz sample rate or lower) 10: a1=-0.52 (for 44.1kHz sample rate) 11: a1=-0.55 (for 48kHz sample rate)

Note:Write to **SEGn** and **DPn** will be ignored when Spatial effect control bit is enabled, it means modify individual Spatial coefficients is forbidden when Spatial is working.

Reg-6Ah Index Address **Default:0000h**

Register:: (reg_6a)	**0x6a**

Name	Bits	Read/Write	Reset State	Function Description
REG_MX6A_b15_b6	15:7	R	0'h	Reserved
ex_analog_ctrl_register_index	6:0	R/W	0'h	**Index Address**

Reg-6Ch Index Data **Default:0000h**

Register:: (reg_6c)			**0x6c**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
REG_MX6C	15:0	R/W	0'h	**Index Data**

Note: It is strong suggest not writting to un-available Hiden Register.
Note: If un-available Hiden Register is written, the value of index 00 will be reported.

Reg-6Eh EQ status **Default:0000h**

Register:: (reg_6e)			**0x6e**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
REG_MX6C_b15_b5	15:5	R	0'h	Reserved
eq_hpf_status	4	R	0'h	EQ High Pass Filter (HPF) Status. 0: Normal 1: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Eq_bpf3_status	3	R	0'h	EQ Band-3 (BP3) Status. 0: Normal 1: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Eq_bpf2_status	2	R	0'h	EQ Band-2 (BP2) Status. 0: Normal 1: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Eq_bpf1_status	1	R	0'h	EQ Band-1 (BP1) Status. 0: Normal 1: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Eq_lpf_status	0	R	0'h	EQ Low Pass Filter (LPF) Status. 0: Normal 1: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

Index::	**EQ Band-0 Coefficient (LP0: a1)**	**0x00**	**Default:0000h**
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)	

Index::	EQ Band-0 Gain (LP0: Ho)	0x01	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)	

Index::	EQ Band-1 Coefficient (BP1: a1)	0x02	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)	

Index::	EQ Band-1 Coefficient (BP1: a2)	0x03	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)	

Index::	EQ Band-1 Gain (BP1: Ho)	0x04	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)	

Index::	EQ Band-2 Coefficient (BP2: a1)	0x05	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)	

Index::	EQ Band-2 Coefficient (BP2: a2)	0x06	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)	

Index::	EQ Band-2 Gain (BP2: Ho)	0x07	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)	

Index::	EQ Band-3 Coefficient (BP3: a1)	0x08	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)	

Index::	EQ Band-3 Coefficient (BP3: a2)	0x09	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)	

Index::	EQ Band-3 Gain (BP3: Ho)	0x0A	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)	

Index::	EQ Band-4 Coefficient (HPF: a1)	0x0B	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)	

Index::	EQ Band-4 Gain (HPF: Ho)	0x0C	Default:0000h
Bit	**Type**	Function	
15:0	R/W	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -4 ~ 3.99)	

Index::	EQ Control & Status Register	0x10	Default:0000h
Bit	**Type**	Function	
15	R/W	**EQ block Control** 0b:Disable 1b:Enable	
14:5		Reserved	
4	R/W	**EQ High Pass Filter (HPF) Control.** 0: Disabled (bypass) and reset 1: Enabled	
3	R/W	**EQ Band-3 (BP3) Control.** 0: Disabled and reset	1: Enabled.
2	R/W	**EQ Band-2 (BP2) Control.** 0: Disabled and reset	1: Enabled.
1	R/W	**EQ Band-1 (BP1) Control.** 0: Disabled and reset	1: Enabled.
0	R/W	**EQ Low Pass Filter (LPF) Control.** 0: Disabled and reset	1: Enabled.

Note:update individual EQ coefficients is forbidden when EQ is working.

Index::	EQ Input Volume Control	0x11	Default:0000h
Bit	**Type**	Function	
15:2		Reserved	
1:0	R/W	**7-bit Volume EQIn-VOL-LR** 00b:0dB 01b:-6dB 10b:-12dB 11b:-18dB	

Index::	EQ Output Volume Control	0x12	Default:0001h
Bit	**Type**	Function	
15:3		Reserved	
2:0	R/W	**7-bit Volume EQOut-VOL-LR** 000b:-3dB 001b: 0dB	

		010b:3dB 011b:6dB 100b:9dB 101b:12dB 110b:15dB 111b:18dB

The AVC registers:

Index::	**Auto Volume Control Register 0**	**0x20**	**Default:0050h**
Bit	**Type**	**Function**	
15	R/W	**Select the controlled Gain block for AVC (default:00b)** 0: Disable AVC 1: Enable AVC to control ADC gain	
14:8		Reserved	
7:3	R/W	**Monitor Window Control (Unit: 2^(n+1) samples) (default:01010b)** 00000b: 2^(1) sample 00001b: 2^(2) samples 00010b: 2^(3) samples, … 10000b: 2^(17) samples,……Others: Reserved. The maximum n=16 **Note:Monitor Window can only be changed after soft-reset once AVC enabled**	
2:1		Reserved	
0	R/W	**AVC Reference Channel Selection (default:0b)** 0: Left Channel 1: Right Channel	

Index::	**Auto Volume Control Register 1**	**0x21**	**Default:2710h**
Bit	**Type**	**Function**	
15	-	Reserved	
14:0	R/W	**The Maximum PCM absolute level after AVC, Thmax (=0 ~ 2^15-1)**	

Index::	**Auto Volume Control Register 2**	**0x22**	**Default:0BB8h**
Bit	**Type**	**Function**	
15	-	Reserved	
14:0	R/W	**The Mimimum PCM absolute level after AVC, Thmin (=0 ~ 2^15-1)**	

Index::	**Auto Volume Control Register 3**	**0x23**	**Default:01F4h**
Bit	**Type**	**Function**	
15	-	Reserved	
14:0	R/W	**The Non-active PCM absolute level AVC will keep analog unit gain, Thnonact (=0 ~ 2^15-1)**	

Note: Initial of Index23=0001'h

Index::	**Auto Volume Control Register 4**	**0x24**	**Default:0190h**
Bit	**Type**	**Function**	
15:0	R/W	**The CNTMAXTH1 to control the sensitivity to increase Gain (unit:2^1)** This value shoule be less than **CNTMAXTH2**. (Max:2^17)	

Index::	**Auto Volume Control Register 5**	**0x25**	**Default:0200h**

Bit	Type	Function
15:0	R/W	**The CNTMAXTH2 to control the sensitivity to decrease Gain (unit:2^1)** This value shoule be less than Monitor Window. (Optimalized: 1/2 Monitor Window) (Max:2^17)

Note: **CNTMAXTH1 < CNTMAXTH2,**

Index:: Digital Internal Register		**0x39 Default:9000h**
Bit	**Type**	Function
15	R/W	**Pad drive capability** 0b:Weak drive 1b:Strong drive
14:13	R/W	Reserved
12	R/W	**Voice DAC high pass filter for DC level testing** 0: OFF 1: ON
11:0	R/W	Reserved

Index:: Class AB internal Register1		**0x44 Default:F920h**
Bit	**Type**	Function
15	R/W	**POW_CLSAB LP: Class_AB Left Positive channel** 0: Power Down 1: Power ON
14	R/W	**POW_CLSAB LN: Class_AB Left Negative channel** 0: Power Down 1: Power ON
13	R/W	**POW_CLSAB RP: Class_AB Right Positive channel** 0: Power Down 1: Power ON
12	R/W	**POW_CLSAB RN: Class_AB Right Negative channel** 0: Power Down 1: Power ON
11:0	R/W	Reserved

Index:: Class D Temp. Sensor		**0x4A Default:4444h**
Bit	**Type**	Function
15	R/W	Reserved
14:12	R/W	**RP channel Temp. Sensor Threshold Setting** 000:25oC 001:35oC 010:45oC 011:65oC 100:80oC 101:95oC 110:125oC 111:125oC Note: Tolerance: +/- 15oC
11	R/W	Reserved
10:8	R/W	**RN channel Temp. Sensor Threshold Setting** 000:25oC 001:35oC 010:45oC 011:65oC 100:80oC 101:95oC 110:125oC 111:125oC Note: Tolerance: +/- 15oC
7	R/W	Reserved
6:4	R/W	**LP channel Temp. Sensor Threshold Setting** 000:25oC 001:35oC 010:45oC 011:65oC 100:80oC 101:95oC 110:125oC 111:125oC Note: Tolerance: +/- 15oC

3	R/W	Reserved
2:0	R/W	**LN channel Temp. Sensor Threshold Setting** 000:25oC 001:35oC 010:45oC 011:65oC 100:80oC 101:95oC 110:125oC 111:125oC Note: Tolerance: +/- 15oC

Index:: AD_DA_Mixer_internal Register5 0x54 Default: 8184h		
Bit	**Type**	Function
15	R/W	Reserved
14:13	R/W	**DAC Reference Source** 01: Internal DAC reference 11: External DAC reference Others:Reserved
12:3	R/W	Reserved
2:0	R/W	**Temp. sensor threshold setting** 000:25oC 001:35oC 010:45oC 011:65oC 100:80oC 101:95oC 110:110oC 111:125oC Note: Tolerance: +/- 15oC

Note: for saving DAC power consumption, It is strong suggest to initial Index54=E184'h .

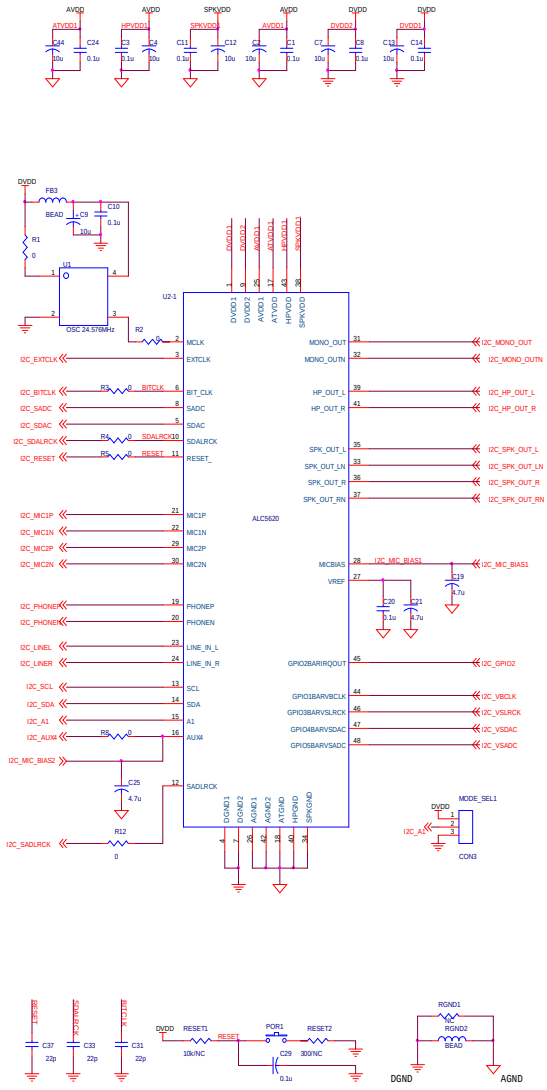
Reg-7Ch VENDOR ID1 **Default:10ECh**

Register:: (reg_7c)			**0x7c**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
vender_id1	15:0	R	10EC'h	**Vendor ID "10EC"**

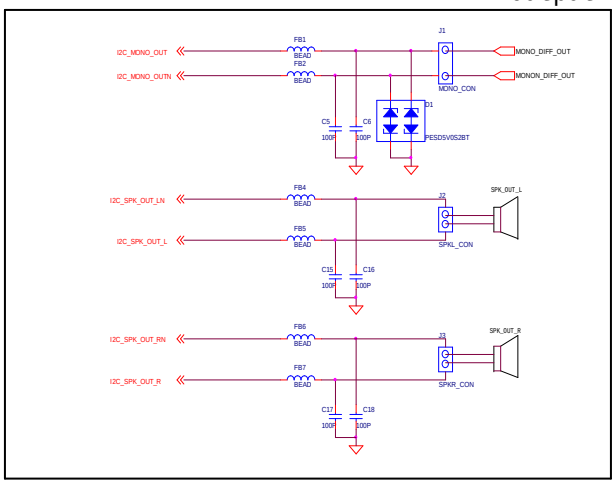
Reg-7Eh VENDOR ID2 **Default:2003h**

Register:: (reg_7e)			**0x7e**	
Name	**Bits**	**Read/Write**	**Reset State**	**Function Description**
vender_id	15:8	R	20'h	**Device ID - "20"**
device_id2	7:0	R	03'h	**Version ID –"03"**

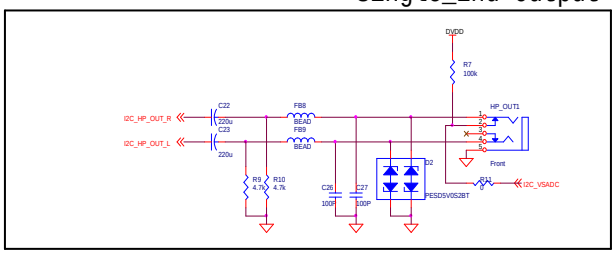
7. Application Circuit



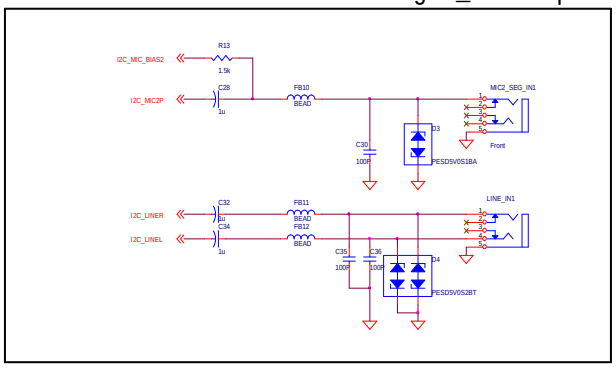
BTL Output



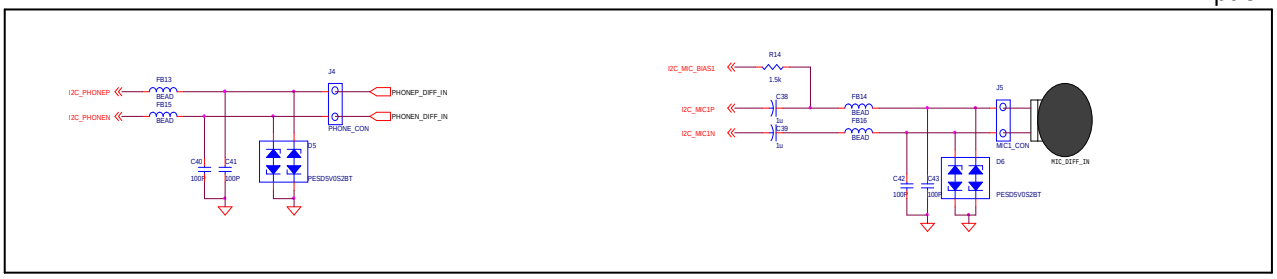
Single_End Output



Single_End Input



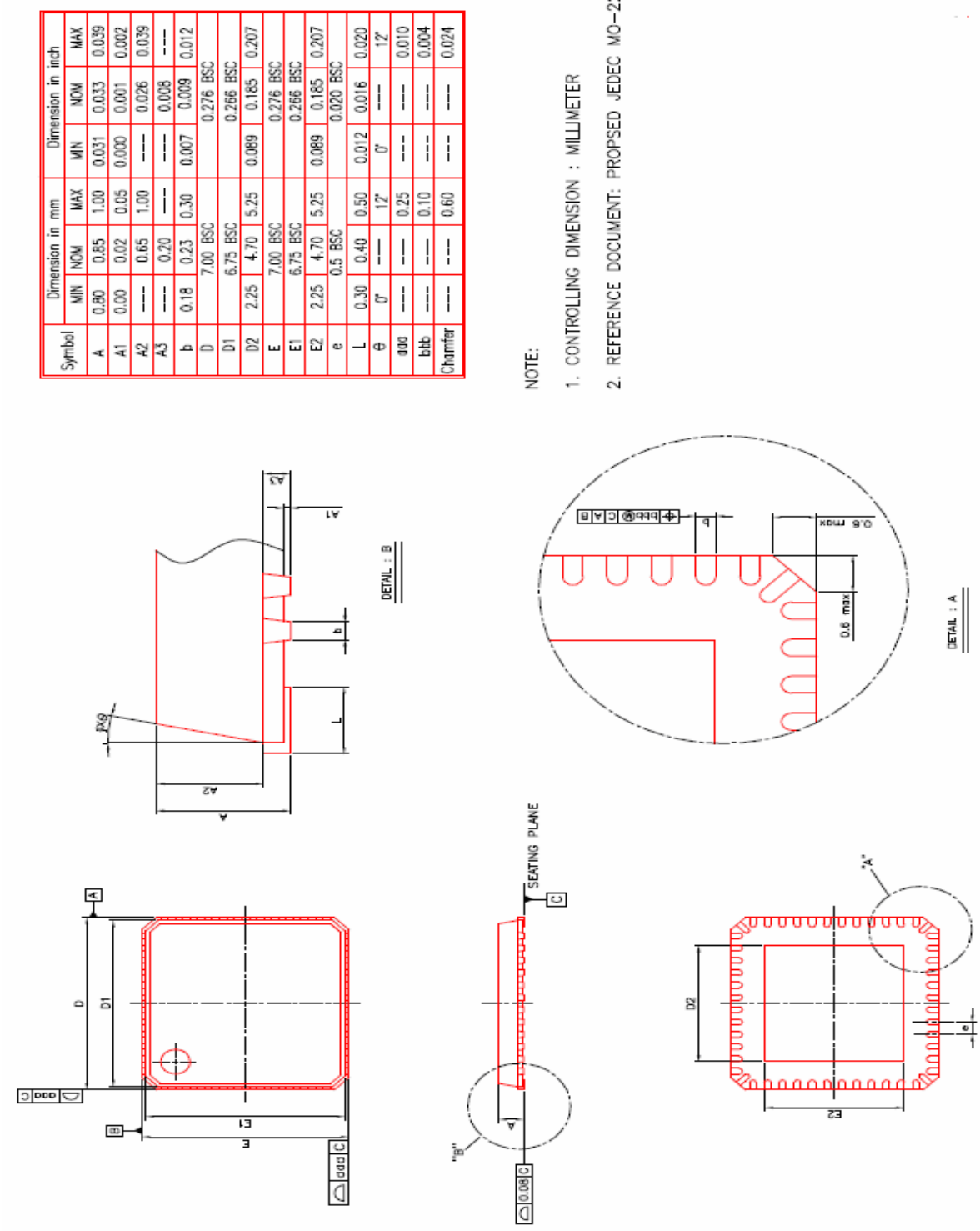
BTL Input



8. Mechanical Dimension

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	---	0.20	---	---	0.008	---
b	0.18	0.23	0.30	0.007	0.009	0.012
D		7.00 BSC			0.276 BSC	
D1		6.75 BSC			0.266 BSC	
D2	2.25	4.70	5.25	0.089	0.185	0.207
E		7.00 BSC			0.276 BSC	
E1		6.75 BSC			0.266 BSC	
E2	2.25	4.70	5.25	0.089	0.185	0.207
e		0.5 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
Chamfer	---	---	0.60	---	---	0.024

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.



9. Ordering Information

Part Number	Package	Status
ALC5620D-GR	QFN-48 & 'Green' package	Sample

☞ See page 6 for Green package and version identification

Appendix A: Main I2S Clock Table

- Master/Slave Mode:

MCLK	PLL Output	DAC Sample Rate	Sel_sysclk	Stereo_i2s_da_filter_div	Stereo_i2s_sclk_div	Stereo_i2s_da_wclk_div	ADC Sample rate	Stereo_i2s_ad_filter_div	Stereo_i2s_ad_wclk_div
		SDALRCK	Reg40[15]	Reg62[15:12] * Reg62[11:9]	Reg60[15:12] * Reg60[10:8]	Reg60[0]	**SADLRCK**	Reg62[7:4] * Reg62[3:1]	Reg60[7:4] * Reg60[3:1]
24576000	X/24576000	8000	0'b/1'b	48/24	48/96	1'b/0'b	8000	48/24	64/32
24576000	X/24576000	16000	0'b/1'b	12/24	24/48	1'b/0'b	16000	12/24	64/32
24576000	X/24576000	16000	0'b/1'b	12/24	24/48	1'b/0'b	8000	48/24	128/64
24576000	X/24576000	48000	0'b/1'b	8/4	8/16	1'b/0'b	48000	8/4	64/32
24576000	X/24576000	48000	0'b/1'b	8/4	8/16	1'b/0'b	32000	12/6	96/48
24576000	X/24576000	48000	0'b/1'b	8/4	8/16	1'b/0'b	16000	12/24	192/96
24576000	X/24576000	48000	0'b/1'b	8/4	8/16	1'b/0'b	8000	48/24	384/192
22579200	X/22579200	11025	0'b/1'b	32/16	32/64	1'b/0'b	11025	32/16	64/32
22579200	X/22579200	11025	0'b/1'b	32/16	32/64	1'b/0'b	8000	44/22	88/44
22579200	X/22579200	22050	0'b/1'b	8/16	16/32	1'b/0'b	22050	8/16	64/32
22579200	X/22579200	22050	0'b/1'b	8/16	16/32	1'b/0'b	11025	32/16	128/64
22579200	X/22579200	22050	0'b/1'b	8/16	16/32	1'b/0'b	8000	44/22	176/88
22579200	X/22579200	44100	0'b/1'b	8/4	8/16	1'b/0'b	44100	8/4	64/32
22579200	X/22579200	44100	0'b/1'b	8/4	8/16	1'b/0'b	22050	8/16	128/64
22579200	X/22579200	44100	0'b/1'b	8/4	8/16	1'b/0'b	11025	32/16	256/128
22579200	X/22579200	44100	0'b/1'b	8/4	8/16	1'b/0'b	8000	44/22	352/176

- PLL output as System Clock only support Master Mode
- **SDALRCL & SADLRCK are Output in Master Mode, SDALRCL & SADLRCK are Input in Slave Mode.**

Appendix B :Voice PCM Interface Clock Table

- Master Mode: (**voice_port_sel="0"**)

MCLK	EXTCLK	PLL	VoDAC Sample Rate	Voice_mclk_sel	Voice_sysclk_sel	Clk_filter_master_div	I2S_sclk_voice_master_div	I2S_wclk_voice_master sel	Extclk_out_sel	Voice_64osr	Extclk_dir	VBCLK (Output)
				Reg64[15]	Reg64[14]	Reg66[7:4]* Reg66[2:0]	Reg64[7:4]* Reg64[2:0]	Reg64[13]	Reg64[10:8]	Reg66[13]	Reg40[14]	
24576000	X	X	8000	0'b	0'b	24/48	48	1'b	X	0'b/1'b	X	512000
24576000	X	X	8000	0'b	0'b	24/48	96	0'b	X	0'b/1'b	X	256000
24576000	2048000	X	8000	0'b	1'b	24/48	48	1'b	12	0'b/1'b	1'b	512000
24576000	X	X	16000	0'b	0'b	12/24	24	1'b	X	0'b/1'b	X	1024000
24576000	X	X	16000	0'b	0'b	12/24	48	0'b	X	0'b/1'b	X	512000
24576000	4096000	X	16000	0'b	1'b	12/24	24	1'b	6	0'b/1'b	1'b	1024000
24576000	X	X	24000	0'b	0'b	8/16	16	1'b	X	0'b/1'b	X	1536000
24576000	X	X	24000	0'b	0'b	8/16	32	0'b	X	0'b/1'b	X	768000
24576000	6144000	X	24000	0'b	1'b	8/16	16	1'b	4	0'b/1'b	1'b	1536000
24576000	X	X	32000	0'b	0'b	6/12	12	1'b	X	0'b/1'b	X	2048000
24576000	X	X	32000	0'b	0'b	6/12	24	0'b	X	0'b/1'b	X	1024000
24576000	8192000	X	32000	0'b	1'b	6/12	12	1'b	3	0'b/1'b	1'b	2048000
24576000	X	X	48000	0'b	0'b	4/8	8	1'b	X	0'b/1'b	X	3072000
24576000	X	X	48000	0'b	0'b	4/8	16	0'b	X	0'b/1'b	X	1536000
24576000	12288000	X	48000	0'b	1'b	4/8	8	1'b	2	0'b/1'b	1'b	3072000
22579200	X	X	8018	0'b	0'b	22/44	44	1'b	X	0'b/1'b	X	513163
22579200	X	X	8018	0'b	0'b	22/44	88	0'b	X	0'b/1'b	X	256582
22579200	X	X	11025	0'b	0'b	16/32	32	1'b	X	0'b/1'b	X	705600
22579200	X	X	11025	0'b	0'b	16/32	64	0'b	X	0'b/1'b	X	352800
22579200	2822400	X	11025	0'b	1'b	16/32	32	1'b	8	0'b/1'b	1'b	705600
22579200	X	X	22050	0'b	0'b	8/16	16	1'b	X	0'b/1'b	X	1411200
22579200	X	X	22050	0'b	0'b	8/16	32	0'b	X	0'b/1'b	X	705600
22579200	5644800	X	22050	0'b	1'b	8/16	16	1'b	4	0'b/1'b	1'b	1411200
22579200	X	X	44100	0'b	0'b	4/8	8	1'b	X	0'b/1'b	X	2822400
22579200	X	X	44100	0'b	0'b	4/8	16	0'b	X	0'b/1'b	X	1411200
22579200	11289600	X	44100	0'b	1'b	4/8	8	1'b	2	0'b/1'b	1'b	2822400
13000000	X	24576000	8000	1'b	0'b	24/48	96	0'b	X	0'b/1'b	X	256000
13000000	X	24576000	8000	1'b	0'b	24/48	48	1'b	X	0'b/1'b	X	512000
13000000	X	22579200	11025	1'b	0'b	16/32	32	1'b	X	0'b/1'b	X	705600
13000000	X	22579200	11025	1'b	0'b	16/32	64	0'b	X	0'b/1'b	X	352800
13000000	X	24576000	16000	1'b	0'b	12/24	24	1'b	X	0'b/1'b	X	1024000
13000000	X	24576000	16000	1'b	0'b	12/24	48	0'b	X	0'b/1'b	X	512000
13000000	X	22579200	22050	1'b	0'b	8/16	16	1'b	X	0'b/1'b	X	1411200
13000000	X	22579200	22050	1'b	0'b	8/16	32	0'b	X	0'b/1'b	X	705600
13000000	X	24576000	24000	1'b	0'b	8/16	16	1'b	X	0'b/1'b	X	1536000
13000000	X	24576000	24000	1'b	0'b	8/16	32	0'b	X	0'b/1'b	X	768000
13000000	X	24576000	32000	1'b	0'b	6/12	24	0'b	X	0'b/1'b	X	1024000
13000000	X	24576000	32000	1'b	0'b	6/12	12	1'b	3	0'b/1'b	X	2048000
13000000	X	22579200	44100	1'b	0'b	4/8	8	1'b	X	0'b/1'b	X	2822400
13000000	X	22579200	44100	1'b	0'b	4/8	16	0'b	X	0'b/1'b	X	1411200
13000000	X	24576000	48000	1'b	0'b	4/8	8	1'b	X	0'b/1'b	X	3072000
13000000	X	24576000	48000	1'b	0'b	4/8	16	0'b	X	0'b/1'b	X	1536000

X ==> Don't Care
– ==> forbidden

- Slave Mode: (**voice_port_sel="1"**)

MCLK	EXTCLK	PLL	VDAC	VBCLK (Input)	Voice_mclk_sel Reg64[15]	Voice_sysclk_sel Reg64[14]	Sel_clk_filter Reg66[14]	Clk_filter_master_div Reg66[7:4]* Reg66[2:0]	I2S_sclk_voice_master_div Reg64[7:4]* Reg64[2:0]	I2S_wclk_voice_master_sel Reg64[13]	Sel_clk_filter_slave Reg66[15]	Extclk_out_sel Reg64[10:8]	Voice_64osr Reg66[13]
X	1024000	X	8000	X	0	1	0	-/2	X	X	X	X	-/1
X	2048000	X	8000	X	0	1	0	2/4	X	X	X	X	0/1
X	3072000	X	8000	X	0	1	0	3/6	X	X	X	X	0/1
X	4096000	X	8000	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	8000	1024000 /512000	0	X	1	X	X	X	1	X	0/1
X	1411200	X	11025	X	0	1	0	-/2	X	X	X	X	-/1
X	2822400	X	11025	X	0	1	0	2/4	X	X	X	X	0/1
X	4233600	X	11025	X	0	1	0	3/6	X	X	X	X	0/1
X	5644800	X	11025	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	11025	1411200 /705600	0	X	1	X	X	X	1	X	0/1
X	2048000	X	16000	X	0	1	0	-/2	X	X	X	X	-/1
X	4096000	X	16000	X	0	1	0	2/4	X	X	X	X	0/1
X	6144000	X	16000	X	0	1	0	3/6	X	X	X	X	0/1
X	8192000	X	16000	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	16000	2048000 /1024000	0	X	1	X	X	X	1	X	0/1
X	2822400	X	22050	X	0	1	0	-/2	X	X	X	X	-/1
X	5644800	X	22050	X	0	1	0	2/4	X	X	X	X	0/1
X	8467200	X	22050	X	0	1	0	3/6	X	X	X	X	0/1
X	11289600	X	22050	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	22050	2822400 /1411200	0	X	1	X	X	X	1	X	0/1
X	3072000	X	24000	X	0	1	0	-/2	X	X	X	X	-/1
X	6144000	X	24000	X	0	1	0	2/4	X	X	X	X	0/1
X	9216000	X	24000	X	0	1	0	3/6	X	X	X	X	0/1
X	12288000	X	24000	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	24000	3072000 /1536000	0	X	1	X	X	X	1	X	0/1
X	4096000	X	32000	X	0	1	0	-/2	X	X	X	X	-/1
X	8192000	X	0.32	X	0	1	0	2/4	X	X	X	X	0/1
X	12288000	X	32000	X	0	1	0	3/6	X	X	X	X	0/1
X	16384000	X	32000	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	32000		0	X	1	X	X	X	1	X	0/1
X	5644800	X	44100	X	0	1	0	-/2	X	X	X	X	-/1
X	11289600	X	44100	X	0	1	0	2/4	X	X	X	X	0/1
X	16934400	X	44100	X	0	1	0	3/6	X	X	X	X	0/1
X	22579200	X	44100	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	44100	5644800 /2822400	0	X	1	X	X	X	1	X	0/1
X	6144000	X	48000	X	0	1	0	-/2	X	X	X	X	-/1
X	12288000	X	48000	X	0	1	0	2/4	X	X	X	X	0/1
X	18432000	X	48000	X	0	1	0	3/6	X	X	X	X	0/1
X	24576000	X	48000	X	0	1	0	4/8	X	X	X	X	0/1
X	X	X	48000	6144000 /3072000	0	X	1	X	X	X	1	X	0/1

X ==> Don't Care
- ==> forbidden

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