ALC5624

HAND-HELD MULTIMEDIA I²S AUDIO CODEC

DATASHEET

Rev. 1.3
07 August 2009
Track ID: JATR-1076-21

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC5624 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/08/24	First release
1.1	2008/01/11	Revised section 1 General Description, page 1. Revised Figure 1, page 4. Added note in Table 4, page 8. Revised Figure 4 to Figure 11, page 12to 14. Revised section 7.8.1 Speaker Output, page 18. Revised Table 29, page 34. Revised section 10 Application Circuits, page 66. Revised section 12 Appendix A: Stereo I^2S Clock Table, page 69. Revised section 13 Ordering Information, page 70.
1.2	2008/07/23	Revised section 13 Ordering Information, page 70.
1.3	2009/08/07	Revised Figure 1 Block Diagram, page 4. Revised Table 3 Filter/Reference, page 8. Revised Table 4 Power/Ground, page 8. Revised Table 81 Analog Performance Characteristics, page 60. Added section 9.3 Signal Timing, page 63. Revised section 11 Mechanical Dimensions, page 67. Revised Table 85 Ordering Information, page 70.

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1. General Description

The ALC5624 is a highly-integrated I²S/PCM interface audio codec with multiple input/output ports and is designed for mobile computing and communications. It provides a stereo DAC for playback, and a stereo ADC for recording via the I²S/PCM interface.

Stereo audio functions are supported via the I²S/PCM configurable interface. To reduce component count, the device can connect directly to:

- MONO or stereo differential analog inputs
- Stereo headphone
- Single-ended or BTL MONO output
- MONO or Stereo Bridge-Tied Load (BTL) speaker

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality. Class-AB or Class-D amplifiers are easily swapped via simple register configuration, and the 1.7 Watt speaker removes the need for an additional amplifier, further cutting both cost and required board area. Additionally, a flexible hardware 5-band equalizer with configurable gain, bandwidth, and center frequency, and enriches the sound experience.

ALC5624 Digital power operates at supply voltages from 1.8V to 3.6V. Analog power operates from 2.3V to 3.6V, and Speaker power operates from 2.3V to 5V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10μA.

The ALC5624 is available in a 7x7mm 'Green' QFN package, making it ideal for use in handheld portable systems.

2. Features

- High Performance I^2S Codec
  - 16-bit stereo DAC SNR 90dB, THD+N -85dB
  - 16-bit stereo ADC SNR 85dB, THD+N -80dB
- One analog stereo input (LINE-IN)
- One analog MONO single-ended or differential input (PHONE and PHONEN input)
- Stereo, single-ended MONO, or differential analog microphone inputs, with boost pre-amplifiers (+20/+30/+40dB)
- BTL (Bridge-Tied Load) Max. output with on-chip 1.7W speaker driver (SPKVDD=5V, 8Ω load, 10% THD+N)
- Stereo headphone output with on-chip 45mW headphone driver (HPVDD=3.3V, 16Ω load)
- 25mW SE or 75mW BTL MONO output support (AVDD=3.3V, 32Ω load)
- Microphone switch detection
- Power management and enhanced power saving
- Supports digital 5-band equalizer (EQ)
- Supports digital spatial sound and pseudo stereo effect
- Supports pop noise suppression
- Internal PLL can receive wide range of clock input (Digital IO power > 1.8V)
- Digital power supplies from 1.8V to 3.6V, speaker amplifier power supplies from 2.3V to 5V
- Analog power and headphone power supplies from 2.3V to 3.6V
- 7x7mm 48-pin QFN package

3. System Applications

- Tablet PC system/Ultra-Mobile PC (UMPC)
- GPS/Personal Navigation Device (PND) or Multi-Media phone
- PDA Phone/Smartphone
- Personal Media Player (PMP)

4. Function Block Diagram

4.1. Function Block

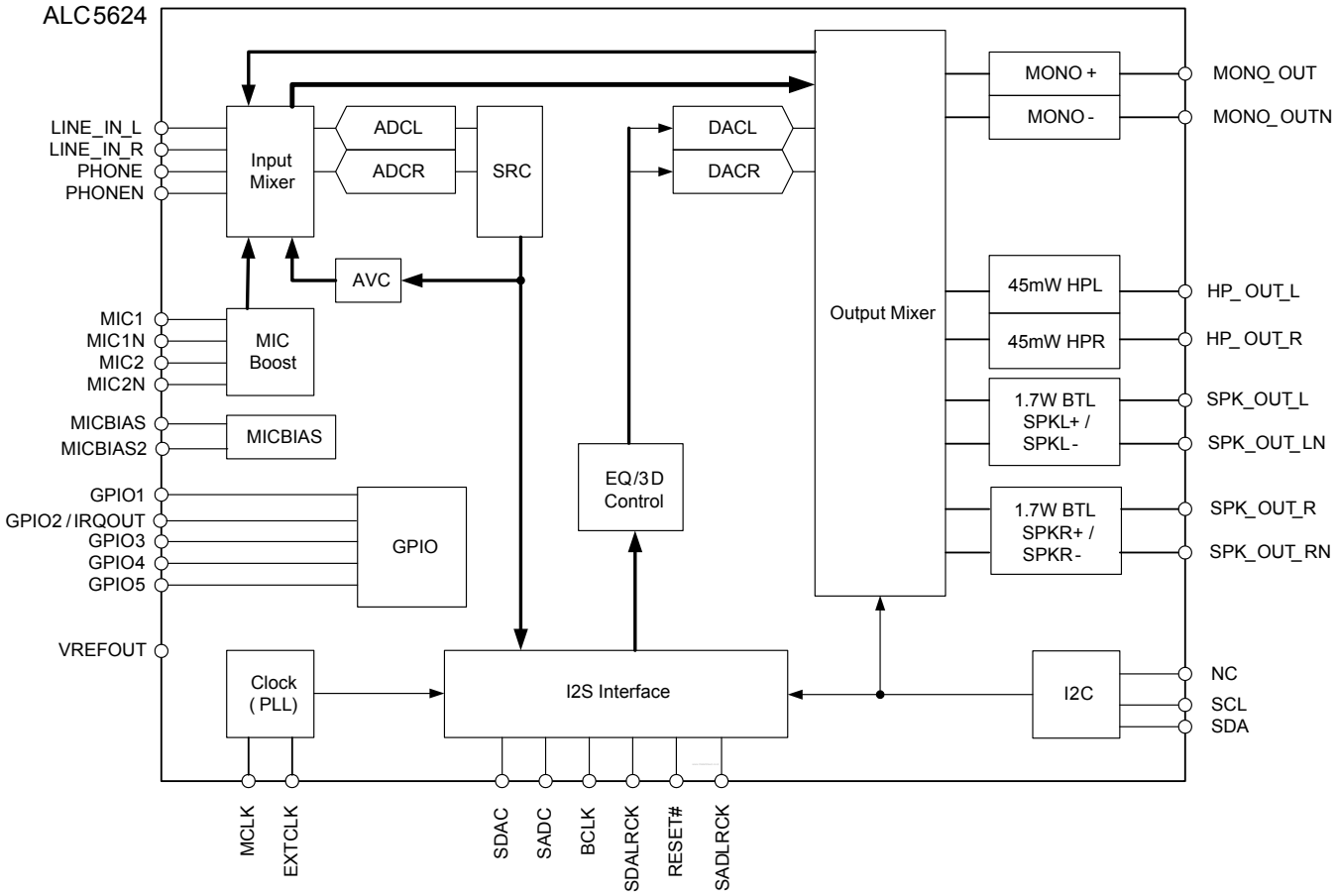


Figure 1. Block Diagram

4.2. Audio Mixer Path

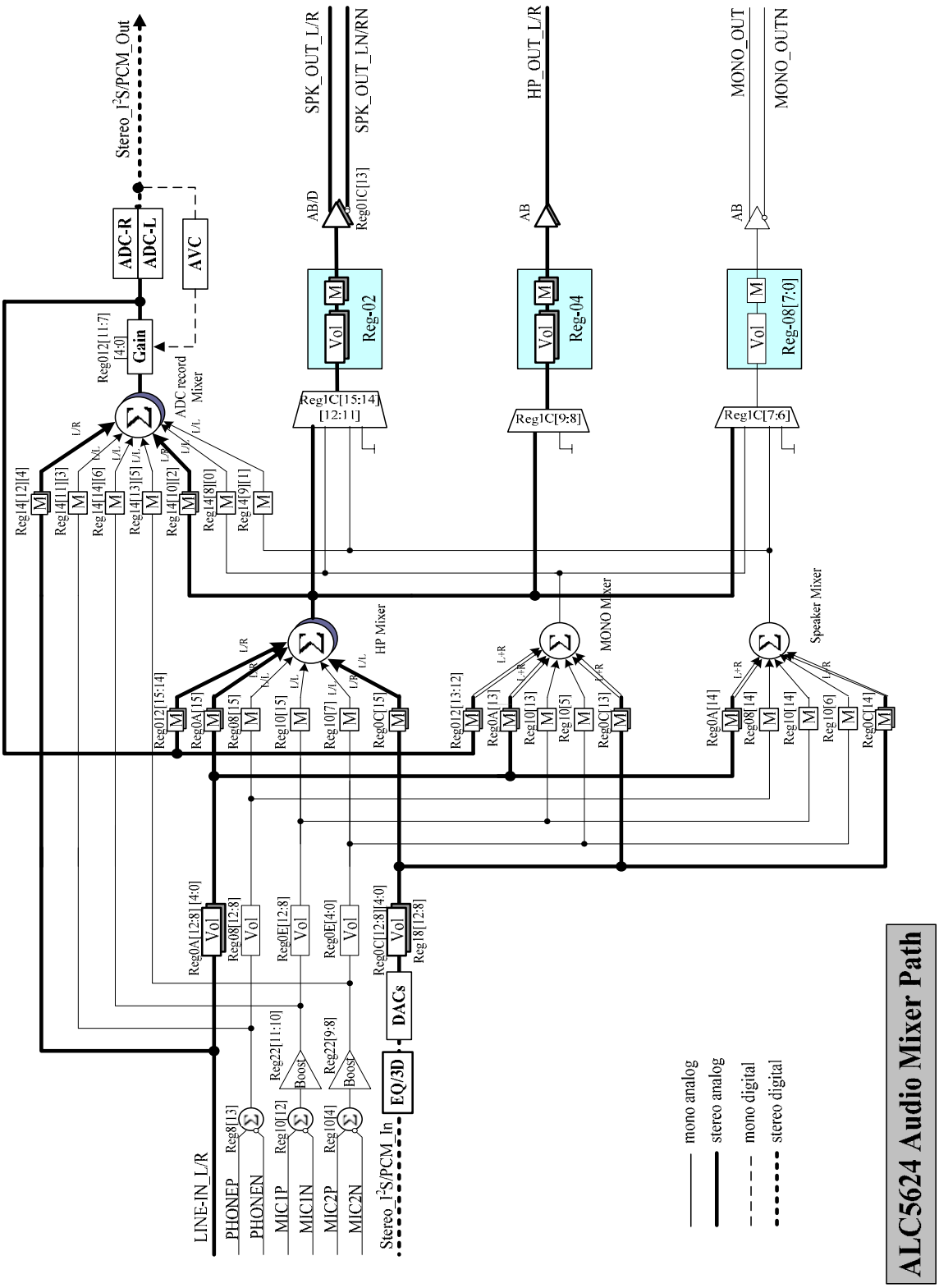


Figure 2. Audio Mixer Path

5. Pin Assignments

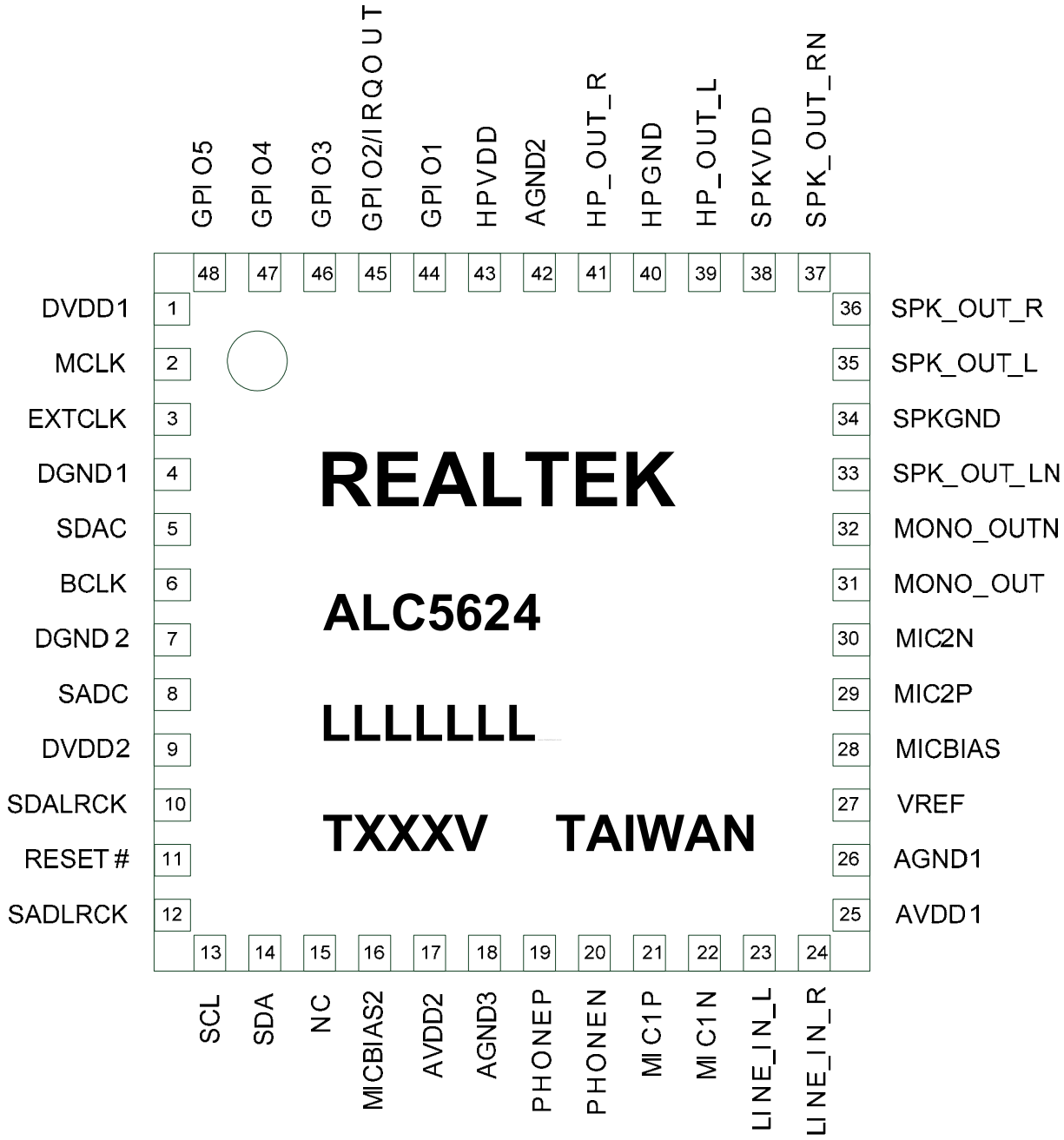


Figure 3. Pin Assignments

5.1. Package and Version Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 3.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MCLK	I	2	Master Clock Input	Schmitt trigger
EXTCLK	O	3	External Reference Clock Output	Schmitt trigger
SDAC	I	5	Stereo I^2S/PCM DAC Data Input	Schmitt trigger
BCLK	IO	6	Stereo I^2S/PCM Bit Clock	Master: V_{OL}=0.1*DVDD, V_{OH}=0.9*DVDD Slave: Schmitt trigger
SADC	O	8	Stereo I^2S/PCM ADC Data Output	V_{OL}=0.1*DVDD, V_{OH} =0.9*DVDD
SDALRCK	IO	10	Stereo I^2S/PCM DAC Synchronous Signal	Master: V_{OL}=0.1*DVDD, V_{OH}=0.9*DVDD Slave: Schmitt trigger
RESET#	I	11	H/W Reset Input (Low Active)	Schmitt trigger
SADLRCK	IO	12	Stereo I^2S/PCM ADC Synchronous Signal	Master: V_{OL}=0.1*DVDD, V_{OH}=0.9*DVDD Slave: Schmitt trigger
SCL	I	13	I^2C Clock	Schmitt trigger
SDA	IO	14	I^2C Data	Schmitt trigger
NC	-	15	Not Connected	Not Connected
GPIO1	IO	44	General Purpose Input and Output 1	GPIO: Input / Output
GPIO2/ IRQOUT	IO	45	General Purpose Input and Output 2/ Interrupt Output	GPIO: Input/Output IRQOUT: Output
GPIO3	IO	46	General Purpose Input and Output 3	GPIO: Input/Output
GPIO4	IO	47	General Purpose Input and Output 4	GPIO: Input/Output
GPIO5	IO	48	General Purpose Input and Output 5	GPIO: Input/Output
				Total: 16 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
PHONEP	I	19	Phone Positive Input	Analog Input (1Vrms)
PHONEN	I	20	Phone Negative Input	Analog Input (1Vrms)
MIC1P	I	21	First Mic Positive Input	Analog Input (1Vrms)
MIC1N	I	22	First Mic Negative Input	Analog Input (1Vrms)
MIC2P	I	29	Second Mic Positive Input	Analog Input (1Vrms)
MIC2N	I	30	Second Mic Negative Input	Analog Input (1Vrms)
LINE_IN_L	I	23	Line Input Left Channel	Analog Input (1Vrms)
LINE_IN_R	I	24	Line Input Right Channel	Analog Input (1Vrms)
MONO_OUT	O	31	Positive MONO Output	Analog Output (1Vrms)
MONO_OUTN	O	32	Negative MONO Output	Analog Output (1Vrms)
HP_OUT_L	O	39	Headphone Output Left Channel	Analog Output (1Vrms)

Name	Type	Pin	Description	Characteristic Definition
HP_OUT_R	O	41	Headphone Output Right Channel	Analog Output (1Vrms)
SPK_OUT_L	O	35	Speaker Output Left Channel	Analog Output (1.3Vrms, SPKVDD = 4.2V)
SPK_OUT_LN	O	33	Negative Speaker Output Left Channel	Analog Output (1.3Vrms, SPKVDD = 4.2V)
SPK_OUT_R	O	36	Speaker Output Right Channel	Analog Output (1.3Vrms, SPKVDD = 4.2V)
SPK_OUT_RN	O	37	Negative Speaker Output Right Channel	Analog Output (1.3Vrms, SPKVDD = 4.2V)
				Total: 16 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
MICBIAS2	O	16	MIC BIAS Voltage Output 2	Programmable Analog DC Output with 3mA drive
MICBIAS	O	28	MIC BIAS Voltage Output	Programmable Analog DC Output with 3mA drive
VREF	O	27	Internal Reference Voltage	4.7µF capacitor to analog ground
				Total: 3 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
DVDD1	P	1	Digital VDD	1.8V~3.6V (IO)
DGND1	P	4	Digital GND	-
DGND2	P	7	Digital GND	-
DVDD2	P	9	Digital VDD	1.8V~3.6V (Core)
AVDD2	P	17	Analog VDD	2.3V~3.6V
AGND3	P	18	Analog GND	-
AVDD1	P	25	Analog VDD	2.3V~3.6V
AGND1	P	26	Analog GND	-
SPKGND	P	34	Analog GND for Speaker Amps	-
SPKVDD	P	38	Analog VDD for Speaker Amps	3.0V~5V (for ohm loading) 2.3V~5V (for ohm loading)
HPGND	P	40	Analog GND for Headphone Amps	-
AGND2	P	42	Analog GND	-
HPVDD	P	43	Analog VDD for Headphone Amps	2.3V~3.6V
Exposed_GND	P	49	Thermal Pad Must be Connected to System GND	-
				Total: 14 Pins

Note1: DVDD1 ≧ DVDD2, SPKVDD ≧ AVDD1 = AVDD2, HPVDD ≧ AVDD1 = AVDD2 ≧ DVDD2.
Note2: SPDVDD connect 10µF Capacitor to SPKGND is required.
Note3: The Thermal pad must be connected to system ground.

7. Functional Description

7.1. Power

The ALC5624 has many power blocks. SPKVDD operates between 2.3V and 5V. HPVDD, AVDD2, and AVDD1 operate between 2.3V and 3.6V. DVDD1 and DVDD2 operate between 1.8V and 3.6V. The power supply limit condition are DVDD1≥DVDD2, SPKVDD≥AVDD1=AVDD2, HPVDD≥AVDD1=AVDD2≥DVDD2.

Table 5. Power Setting for Best Performance

Power	DVDD1	DVDD2	HPVDD	AVDD2	AVDD1	SPKVDD
Setting	3.3V	1.8V	3.3V	3.3V	3.3V	4.2V

7.2. Reset

There are 3 types of reset operation: Power-On Reset (POR), Cold, and Register reset.

Table 6. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Cold Reset	Assert RESET# for a specified period	Reset all hardware logic and all registers to default values except some specify control registers and logic.
Register Reset	Write Reg-00h	Reset all registers to default values except some specify control registers and logic.

7.2.1. Power-On Reset (POR)

When powered on, DVDD2 passes through the V_{POR} band of the ALC5624 (V_{POR_ON} ~V_{POR_OFF}). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 7. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: V_{POR_OFF} must be below V_{POR_ON}.

7.3. Clocking

The Stereo_SYSCLK can be selected from MCLK or PLL. This means MCLK is always provided externally, and the driver should arrange the clock of each block and setup each divider.

EXTCLK can be output by setting Extclk_out_en =1 & pow_extclk=1. The output frequency is determined by MCLK and the setting of Extclk_out_sel.

7.3.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. The source of the PLL can be set to MCLK or BCLK by setting pll_sour_sel.

The driver can set up the PLL to output a frequency close to the SYSCLK.

The PLL transmit formula is:

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 8. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

Table 9. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

After a Cold Reset, PLL related Registers are reset to default values, however, they are not reset to default values after a soft-reset (write Reg00). Firmware should not power down the PLL when the PLL output is used as Stereo_SYSCLK.

7.3.2. I²C and Stereo I²S

The ALC5624 supports I²C for the digital control interface, and I²S/PCM for the digital data interface. The I²S/PCM audio digital interface is used to input data to a stereo DAC or output data from a stereo ADC. The I²S/PCM Audio Digital Interface can be configured to Master mode or Slave mode. For the Stereo I²S Interface, the source clock is always input from MCLK.

Master Mode

In master mode BCLK/SDALRCK/SADLRCK are configured as output. When PLL is disabled and sel_sysclk=0, MCLK is used as Stereo SYSCLK. When PLL is enabled, MCLK is suggested to provide 13MHz, and PLL should be configured to support 44.1K and 48K base sampling rates. The driver should set each divider (Reg60 & Reg62) to arrange the clock distribution. Refer to section 12 Appendix A: Stereo I²S Clock Table, page 69 for details.

Note: The ALC5624 supports different sample rates between SDALRCK and SADLRCK in Master mode.

Slave Mode

In slave mode BCLK/SDALRCK are configured as input. MCLK should provide the BCLK synchronized clock externally. Stereo_SYSCLK and the driver should set each divider to arrange the clock distribution. Refer to section 12 Appendix A: Stereo I²S Clock Table, page 69, for details.

Note: In Slave mode, the ALC5624 does NOT support different sample rates between SDALRCK and SADLRCK. Only SDALRCK is used in slave mode.

7.4. Digital Data Interface

7.4.1. Stereo I²S/PCM Interface

The stereo I²S/PCM interface can be configured as Master mode or Slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- Right justified mode
- I²S mode

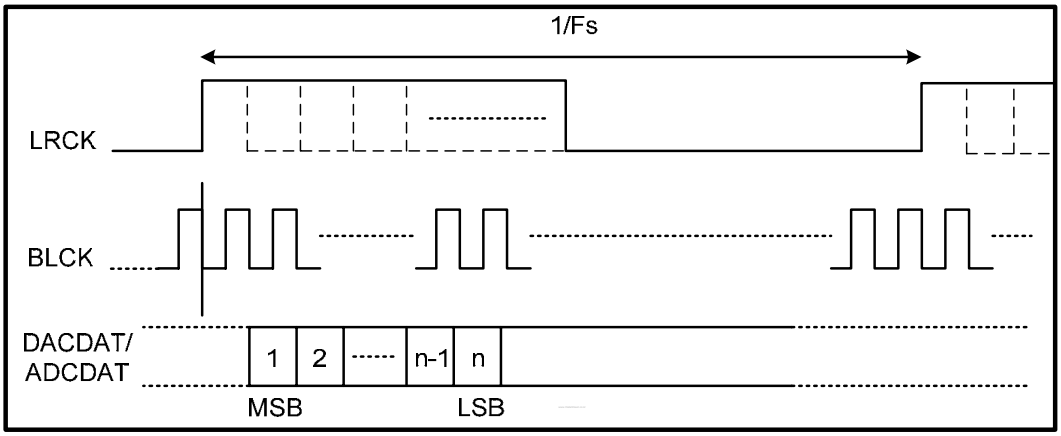


Figure 4. PCM MONO Data Mode A Format (bclk_polarity=0)

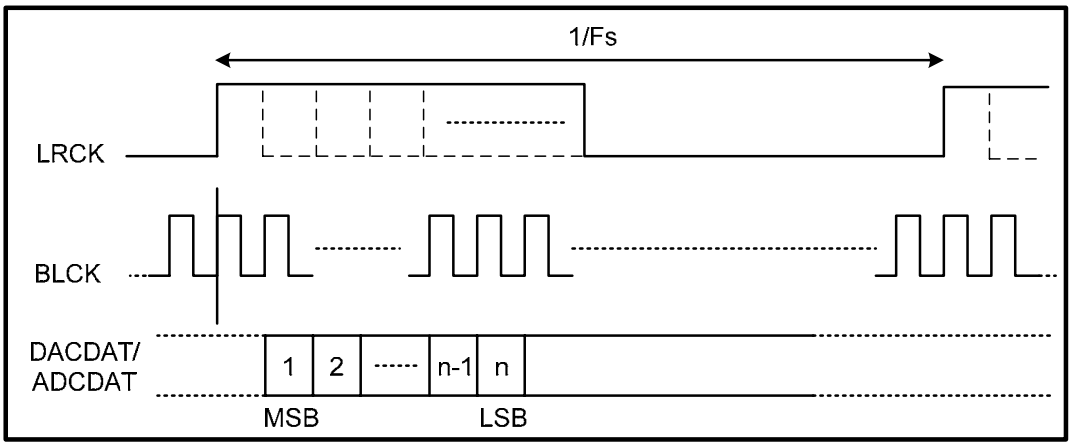


Figure 5. PCM MONO Data Mode A Format (bclk_polarity=1)

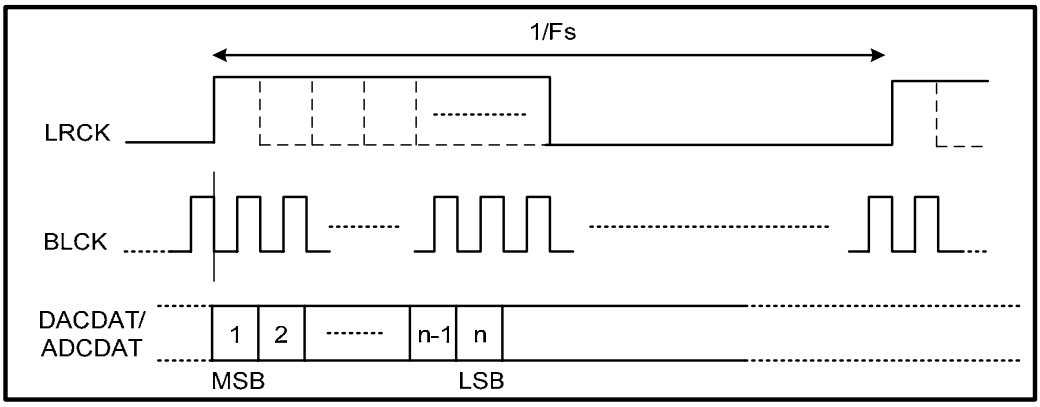


Figure 6. PCM MONO Data Mode B Format (bclk_polarity=0)

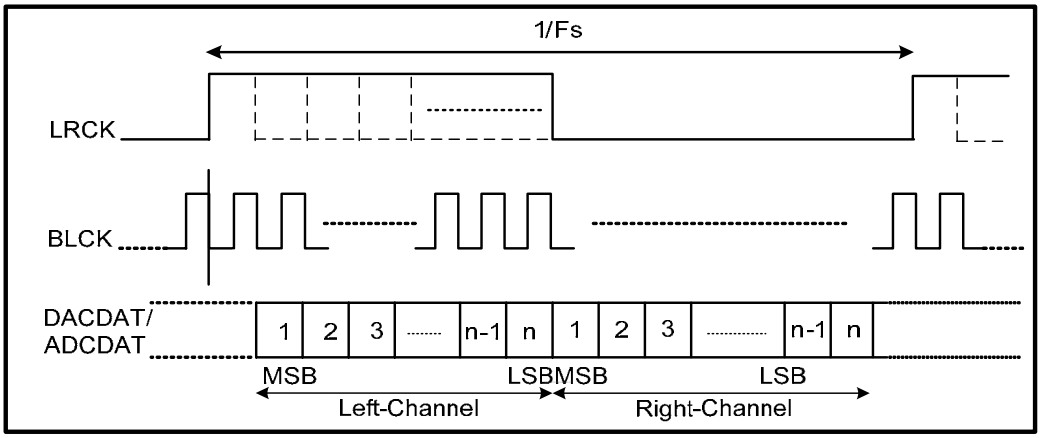


Figure 7. PCM Stereo Data Mode A Format (bclk_polarity=0)

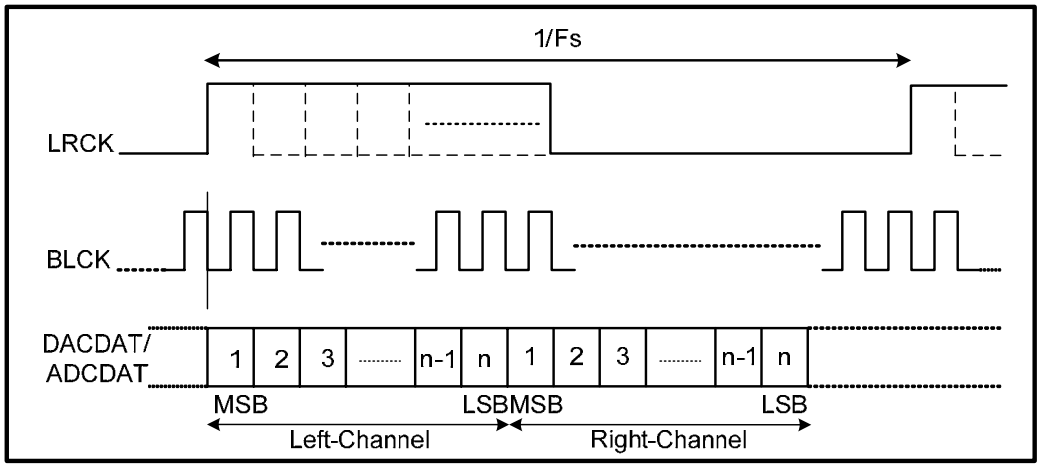


Figure 8. PCM Stereo Data Mode B Format (bclk_polarity=0)

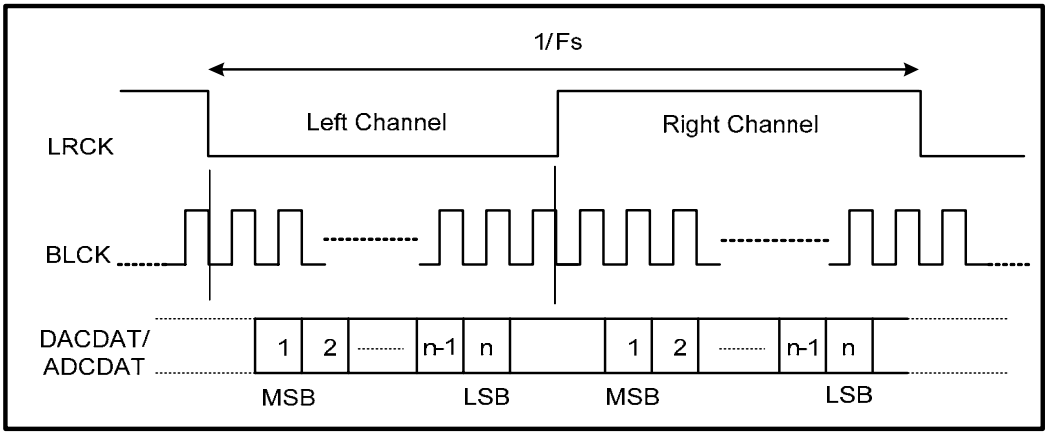


Figure 9. I²S Data Format (bclk_polarity=0)

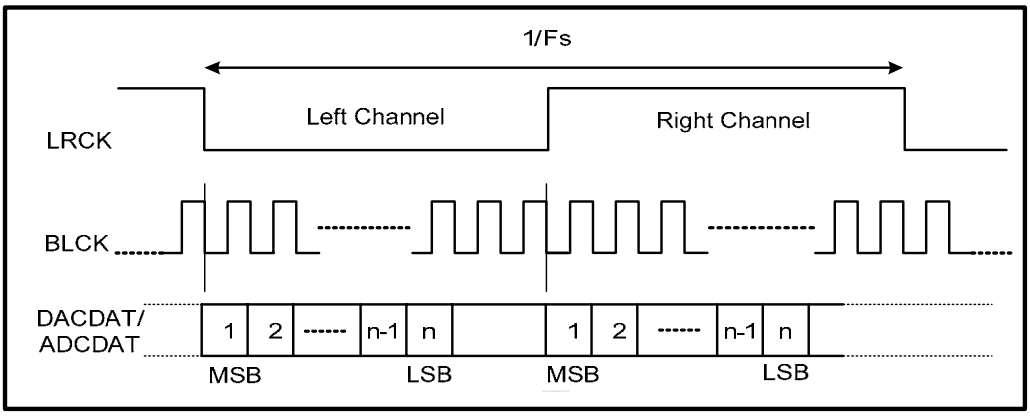


Figure 10. Left-Justified Data Format (bclk_polarity=0)

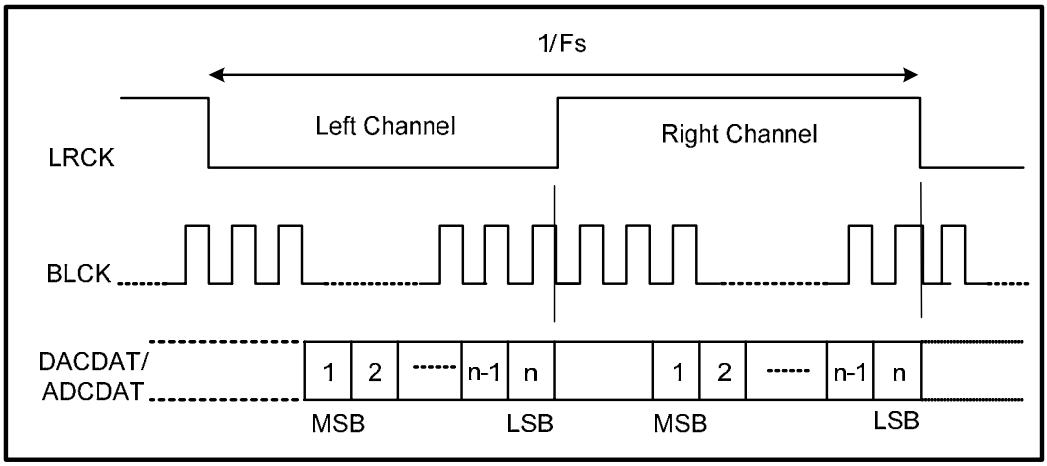


Figure 11. Right-Justified Data Format (bclk_polarity=0)

7.5. Audio Data Path

7.5.1. Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC is independent of the stereo DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting Reg3C [6], [7].

The volume control of the stereo ADC is set via Reg12[11:7][4:0].

7.5.2. Stereo DAC

The stereo DAC can be configured to different sample rate by setting the stereo I^2S clock divider (Reg60).

Reg0C[12:8][4:0] can be used to control the volume of DAC output.

7.6. Mixers

The ALC5624 supports four mixers for all audio function requirements:

- Headphone mixer for 2 channels
- MONO mixer
- Speaker mixer
- ADC record mixer

7.6.1. Headphone Mixer

The headphone mixer is used to drive stereo output, including HP_OUT_L/R, SPK_OUT_L/R (SPK_OUT_LN/RN) and MONO_OUT (MONO_OUTN). The output of the headphone mixer can be input to the ADC record mixer.

The following signals can be mixed into the headphone mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

Note: The headphone mixer can be powered down by setting Reg3C[5][4].

7.6.2. MONO Mixer

The MONO mixer is used to drive MONO_OUT (MONO_OUTN) and SPK_OUT_L/R (SPK_OUT_LN/RN). The output of the MONO mixer can be input to the ADC record mixer. The output of the MONO mixer is two channels with the same signal.

The following signals can be mixed into the MONO mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

Note: The MONO mixer can be powered down by setting Reg3C[2].

7.6.3. Speaker Mixer

The speaker mixer is the same as the MONO mixer and is used to drive MONO_OUT (MONO_OUTN) and SPK_OUT_L/R (SPK_OUT_LN/RN). The output of the speaker mixer can be input to the ADC record mixer. The output of the speaker mixer is two channels with the same signal.

The following signals can be mixed into the speaker mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)

Note: The speaker mixer can be powered down by setting Reg3C[3].

7.6.4. ADC Record Mixer

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. Output of the ADC record mixer can be input to the headphone mixer, MONO mixer, and speaker mixer.

The following signals can be mixed into the ADC record mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Headphone mixer output
- MONO mixer output
- Speaker mixer output

Note: The ADC record mixer can be powered down by setting Reg3C[1][0].

7.7. Analog Audio Input Path

The ALC5624 supports four Analog Audio Input paths:

- Line_IN_L/R
- PHONEP/N
- MIC1
- MIC2

7.7.1. Line Input

Line_In_L and Line_In_R provide 2-channel stereo single-ended input that can be mixed into the MONO mixer, Headphone mixer, Speaker mixer, or the ADC record mixer.

The Line_In_L/R volume and mute are controlled by Reg0A. Reg3E[7:6] can be used to power down the Line_In volume control.

7.7.2. Phone Input

PHONEP/N provides one-channel MONO differential or single-ended input configured by Reg08[13] that can be mixed into the ADC record mixer, or any analog output mixer except for the MONO mixer. PHONEP is main input when differential mode is disabled.

The PHONEP/N volume and mute are controlled by Reg08.

Reg3E[5:4] can be used to power down PHONEP/N volume control and mixer.

7.7.3. Microphone Input

MIC1P/N and MIC2P/N provide two-channel stereo differential or single-ended input via Reg10[12], [4], that can be mixed into the ADC record mixer, or any analog output mixer. MIC1P and MIC2P are main inputs when differential mode is disabled.

The ALC5624 Microphone input boost provides 20/30/40dB boost, set by Reg22[11:10] (for MIC1), and by Reg22[9:8] (for MIC2). The MIC1/2 volume and mute are controlled by Reg0E.

For detailed power management of MIC1/2, Reg3E[3][2] can be used to power down the MIC1/2 volume control. Reg3E[1][0] can be used to power down MIC1/2 boost.

7.8. Analog Audio Output Data Path

The ALC5624 supports three Analog Audio output paths:

- SPK_OUT_L/R
- HP_OUT_L/R
- MONO_OUT

7.8.1. Speaker Output

SPK_OUT_L/R provides two-channel differential output.

The SPK_OUT_L source is set in Reg1C[15:14]. Sources are shown below:

- Vmid
- Headphone left mixer
- Speaker mixer
- MONO mixer

The SPK_OUT_R source is set in Reg1C[12:11]. Sources are shown below:

- Vmid
- Headphone right mixer
- Speaker mixer
- MONO mixer

The ALC5624 speaker supports Class-AB and Class-D type amplifiers (set in Reg1C[13]:spk_out_sel). As the voltage of SPKVDD is usually higher than AVDD, the driver should set the Class-AB Vmid ratio in Reg40[5:3], and the Class-D Vmid ratio in Reg40[7:6] in order to extend the output level.

In Class-AB mode, for L+R MONO speaker solutions, SPK_OUT_R can select a different signal source (SPKR Volume output or SPKL Volume output by Reg1C[14]) but SPK_OUT_RN only outputs SPKR Volume Negative Output.

The SPK_OUT_L/R volume and mute are controlled by Reg02. Reg3E[13:12] and Reg3E[9:8] can be used to power down SPK output. Reg3C[14]: pow_clsab is used to power down Class-AB output.

SPK_OUT_L/R supports the zero-cross detect function (enabled at Reg02[6][14]: sp_l_dezero/ sp_r_dezero).

7.8.2. Headphone Output

HP_OUT_L/R provides two-channel single-ended output. The HP_OUT_L/R source is set in Reg1C[9][8]. Sources are shown below:

- Vmid
- Headphone mixer

The HP_OUT_L/R volume and mute are controlled by Reg04.

Reg3E[11]: pow_hp_l_vol and Reg3E[10]: pow_hp_r_vol can be used to power down the volume of HP output.

HP_OUT supports the zero-cross detect function (enabled at Reg04[14][6]:hp_l_dezero/ hp_r_dezero).

7.8.3. MONO Output

MONO_OUT provide one-channel differential or single-ended output configured by Reg08[15]. The MONO_OUT source is set in Reg1C[7:6]. Sources are shown below:

- Vmid
- Headphone mixer (L+R)
- Speaker mixer
- MONO mixer

The MONO_OUT volume and mute are controlled by Reg08.

Reg3E[14]: pow_MONO_out_vol can be used to power down the volume of MONO_OUT.

MONO_OUT supports the zero-cross detect function (enabled at Reg08[6]:MONO_dezero).

7.9. AVC Control

The Automatic Volume Control (AVC) function dynamically adjusts the input signal quantized by the ADC to an expected sound level by setting THmax and THmin.

When the average level of input signal is higher than THmax, the AVC will decrease the selected analog gain to attenuate the quantized Pulse Code Modulation (PCM) signal to a lower amplitude than THmax.

When the average level of input signal is lower than THmin, the AVC will increase the selected analog gain to amplify the input signal. The quantized Pulse Code Modulation (PCM) signal is then set higher than THmin. The quantized PCM has an average level between THmin and THmax.

The AVC reference source channel and target channel can be individually set by Index20[0] and Reg5E[13:12].

The AVC architecture is shown in Figure 12 below:

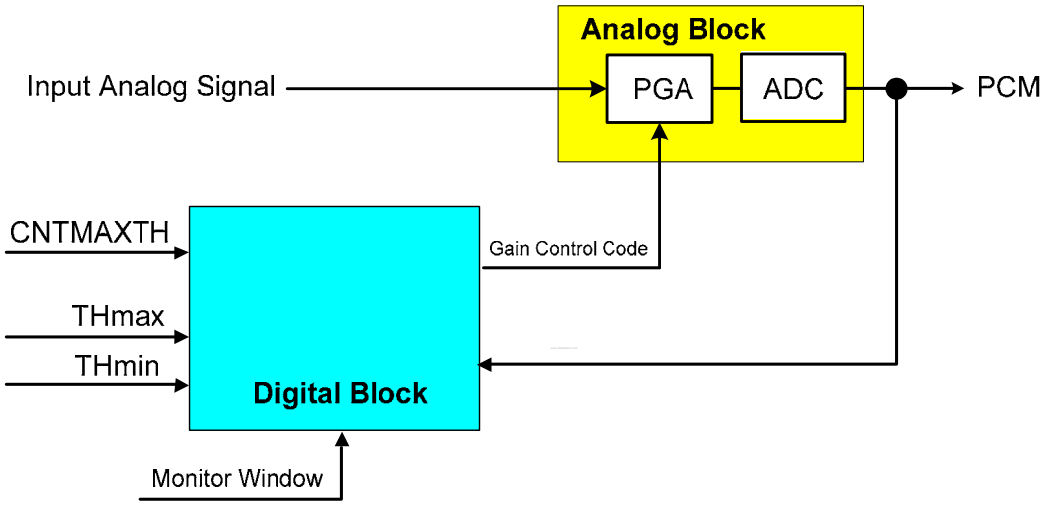


Figure 12. Auto Volume Control Block Diagram

7.10. Hardware Sound Effects

The Sound Effect block is composed of Pseudo Stereo, Spatial 3D, and Equalizer blocks. The Pseudo Stereo block is used to convert a MONO source into virtualized stereo output. The Spatial 3D block is a surround sound generator with adjustable amplitude (Gain) and surround depth (Ratio). The Equalizer block can be used to compensate for speaker response, or to make environment sound effects, e.g., 'Pub', 'Live', 'Rock',… etc..

7.10.1. Equalizer Block

The Equalizer block cascades 5 bands of equalizer to compensate for speaker response and to emulate environment sound. One high-pass filter cascaded in the front end is used to drop low frequency tone, which has a larger amplitude and may damage a mini speaker.

The high-pass filter can also be used to adjust Treble strength with gain control. A low-pass filter with gain control can adjust the Bass strength. Three bands of bi-quad bandpass filters are used to emulate environment sounds.

To avoid PCM sample saturation, the digital volume control has up to 18dB of attenuation before the equalizer. A 0~+18dB digital gain after the equalizer is used to correct PCM output to a suitable level.

7.10.2. Pseudo Stereo and Spatial 3D Sound

There are two spatial effects in post-processing; the Pseudo-Stereo Effect + Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect converts a MONO signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhancing the spatial effect. The Stereo Expansion Effect enhances the spatial effect when the input signal is Stereo.

7.11. I²C Control Interface

I²C is a 2-wire half-duplex serial communication interface, supporting only slave mode. The host must support MCLK during register access.

7.11.1. Addressing Setting

Table 10. Addressing Setting

(MSB)			BIT				(LSB)
0	0	1	1	0	0	0	R/W

7.11.2. Complete Data Transfer

Data Transfer over I²C Control Interface

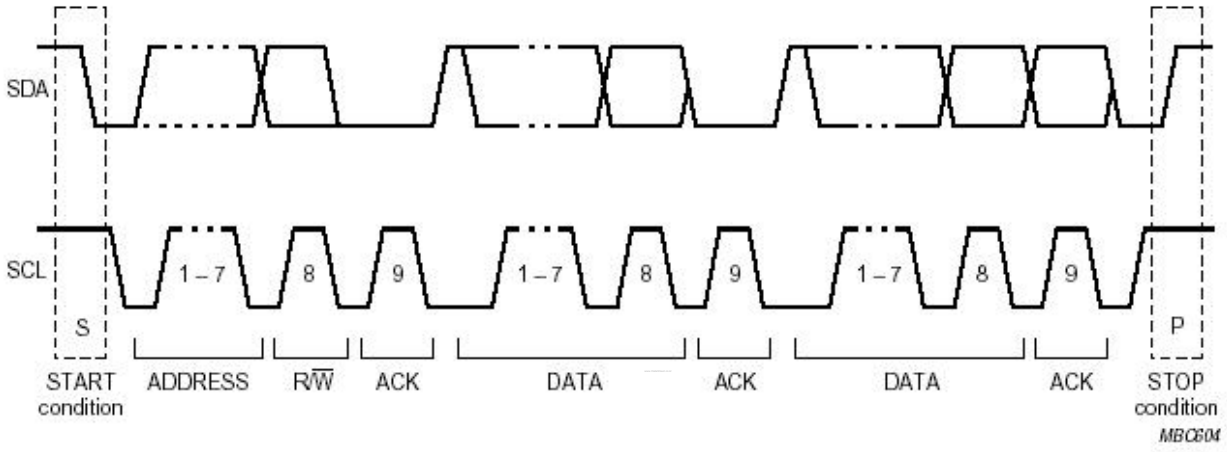
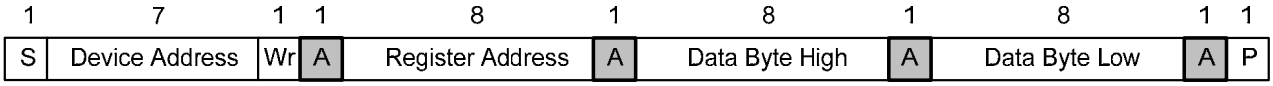


Figure 13. Data Transfer Over I²C Control Interface

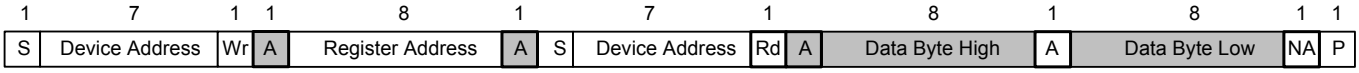
Write WORD Protocol

Table 11. Write WORD Protocol



Read WORD Protocol

Table 12. Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

7.12. Odd-Addressed Register Access

The ALC5624 will return '0000h' when odd-addressed and unimplemented registers are read.

7.13. Power Management

The ALC5624 supports a grouped power down control register (Reg26). More detailed Power Management control is supported in Reg 3A, 3C, and 3E. Each particular block will only be active when both Reg26 and Reg3A/3C/3E are set to 'Enable'.

7.14. GPIO and Interrupt

The ALC5624 supports up to five GPIOs. Each GPIO can be configured as Input/Output by Reg4C. When GPIOs are configured as Input, the status will be indicated in Reg54. When GPIOs are configured as Output, Reg5C is used to drive GPIOs to High (1b) or Low (0b). The status can be read in Reg54.

Interrupt request (IRQ) can be configured as:

- Sticky by setting Reg50
- Changed polarity by setting Reg4E
- Wake-up by setting Reg52

The driver can write each bit of Reg54=1 to clear each IRQ status flag.

GPIO pin2 can be configured and pin-shared with IRQ_Output by setting Reg56.

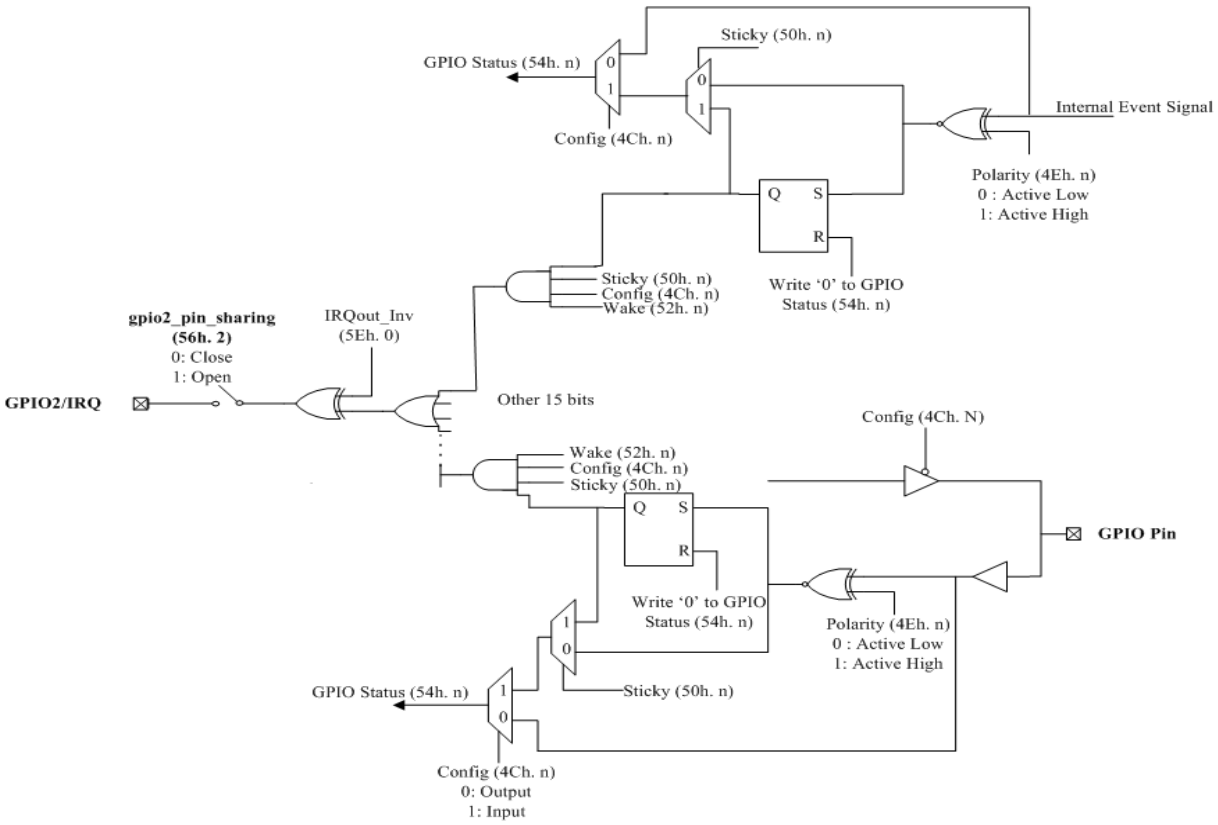


Figure 14. GPIO Implementation

There are some internal events (over-temperature, MICBIAS short detect) where GPIOs can be an interrupt source. GPIO Internal event application is located in Reg4C, Reg4E, Reg50, Reg52, and Reg54.

8. Mixer Registers List

Accessing odd numbered registers, or reading unimplemented registers, will return a 0.

8.1. Reg-00h: Reset

Default: 59B4h

Table 13. Reg-00h: Reset

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved. Read as 0
REG-00_b14_b10	14:10	R	16'h	SE[4:0]=10110b
REG-00_b9	9	R	0'h	No Support for 20-Bit ADC
REG-00_b8	8	R	1'h	Supports 16-Bit ADC
REG-00_b7	7	R	1'h	Supports 16-Bit DAC
REG-00_b6	6	R	0'h	No Support for 18-Bit DAC
REG-00_b5	5	R	1'h	Support for Loudness
REG-00_b4	4	R	1'h	Headphone Output Support
Reserved	3	R	0'h	Reserved
REG-00_b2	2	R	1'h	Supports EQ Control
Reserved	1	R	0'h	Reserved. Read as 0
REG-00_b0	0	R	0'h	Dedicated MIC PCM Input is Not Supported.

Note: Writes to this register will reset all registers to their default values except PLL related Register. The written data will be ignored.

8.2. Reg-02h: Speaker Output Volume

Default: 8080h

Table 14. Reg-02h: Speaker Output Volume

Name	Bits	Read/Write	Reset State	Description
sp_l_mute	15	RW	1'h	Mute Left Control 0: On 1: Mute Left Channel (-∞dB)
sp_l_dezero	14	RW	0'h	Left Zero-Cross Detector Control 0: Disable 1: Enable
Reserved	13	R	0'h	Reserved. Read as 0
sp_l_vol	12:8	RW	0'h	Speaker Output Left Volume (SPKL[4:0]) in 1.5dB Steps
sp_r_mute	7	RW	1'h	Mute Right Control 0: On 1: Mute Right Channel (-∞dB)
sp_r_dezero	6	RW	0'h	Right Zero-Cross Detector Control 0: Disable 1: Enable
Reserved	5	R	0'h	Reserved. Read as 0
sp_r_vol	4:0	RW	0'h	Speaker Output Right Volume (SPKR[4:0]) in 1.5dB Steps

Note: For SPKR/SPKL, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.3. Reg-04h: Headphone Output Volume

Default: 8080h

Table 15. Reg-04h: Headphone Output Volume

Name	Bits	Read/Write	Reset State	Description
hp_l_mute	15	RW	1'h	Mute Left Control 0: On 1: Mute Left Channel (-∞dB)
hp_l_dezero	14	RW	0'h	Left Zero-Cross Detector Control 0: Disable 1: Enable
Reserved	13	R	0'h	Reserved. Read as 0
hp_l_vol	12:8	RW	0'h	Headphone Output Left Volume (HPL[4:0]) in 1.5dB Steps
hp_r_mute	7	RW	1'h	Mute Right Control 0: On 1: Mute Right Channel (-∞dB)
hp_r_dezero	6	RW	0'h	Right Zero-Cross Detector Control 0: Disable 1: Enable
Reserved	5	R	0'h	Reserved. Read as 0
hp_r_vol	4:0	RW	0'h	Headphone Output Right Volume (HPR[4:0]) in 1.5dB Steps

Note: For HPR/HPL, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.4. Reg-08h: Phone Input/MONO Output Volume

Default: C880h

Table 16. Reg-08h: Phone Input / MONO Output Volume

Name	Bits	Read/Write	Reset State	Description
phone2hp_mute	15	RW	1'h	Mute Phone Input to Headphone Mixer Control 0: On 1: Mute (-∞dB)
phone2spk_mute	14	RW	1'h	Mute Phone Input to Speaker Mixer Control 0: On 1: Mute (-∞dB)
phone_diff_ctrl	13	RW	0'h	Phone Differential Input Control 0: Disable 1: Enable
phone_vol	12:8	RW	8'h	Phone Input Volume (PV[4:0]) in 1.5dB Steps (Not to ADC)
MONO_mute	7	RW	1'h	Mute MONO Output Control 0: On 1: Mute (-∞dB)
MONO_dezero	6	RW	0'h	Zero-Cross Detector Control 0: Disable 1: Enable
MONO_diff_ctrl	5	RW	0'h	MONO Output Differential Control 0: Disable (SE) 1: Enable (BTL)
MONO_vol	4:0	RW	0'h	MONO Output Master Volume (MOV[4:0]) in 1.5dB Steps

Note: For MOV, 00h: 0dB attenuation 1Fh: 46.5dB attenuation
For PV, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.5. Reg-0Ah: LINE_IN Volume

Default: E808h

Table 17. Reg-0Ah: LINE_IN Volume

Name	Bits	Read/Write	Reset State	Description
li2hp_mute	15	RW	1'h	Mute Volume Output to Headphone Mixer Control 0: On 1: Mute
li2spk_mute	14	RW	1'h	Mute Volume Output to Speaker Mixer Control 0: On 1: Mute
li2MONO_mute	13	RW	1'h	Mute Volume Output to MONO Mixer Control 0: On 1: Mute
li_l_vol	12:8	RW	08'h	LINE_IN Left Volume (NLV[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
li_r_vol	4:0	RW	8'h	LINE_IN Right Volume (NRV[4:0]) in 1.5dB Steps

Note: For NRV/NLV, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.6. Reg-0Ch: STEREO DAC Volume

Default: E808h

Table 18. Reg-0Ch: STEREO DAC Volume

Name	Bits	Read/Write	Reset State	Description
dac2hp_mute	15	RW	1'h	Mute Volume Output to Headphone Mixer Control 0: On 1: Mute (-∞dB)
dac2spk_mute	14	RW	1'h	Mute Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞dB)
dac2MONO_mute	13	RW	1'h	Mute Volume Output to MONO Mixer Control 0: On 1: Mute (-∞dB)
dac_l_vol	12:8	RW	08'h	PCM Left DAC Volume (PLV[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
dac_r_vol	4:0	RW	8'h	PCM Right DAC Volume (PRV[4:0]) in 1.5dB Steps

Note: For PRV/PLV, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.7. Reg-0Eh: MIC Volume

Default: 0808h

Table 19. Reg-0Eh: MIC Volume

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0'h	Reserved
mic1_vol	12:8	RW	08'h	MIC1 Volume (M1V[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
mic2_vol	4:0	RW	8'h	MIC2 Volume (M2V[4:0]) in 1.5dB Steps

Note: For M2V/M1V, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.8. Reg-10h: MIC Routing Control

Default: E0E0h

Table 20. Reg-10h: MIC Routing Control

Name	Bits	Read/Write	Reset State	Description
mic12hp_mute	15	RW	1'h	Mute MIC1 Volume Output to Headphone Mixer 0: On 1: Mute
mic12spk_mute	14	RW	1'h	Mute MIC1 Volume Output to Speaker Mixer 0: On 1: Mute
mic12MONO_mute	13	RW	1'h	Mute MIC1 Volume Output to MONO Mixer 0: On 1: Mute
mic1_diff_ctrl	12	RW	0'h	MIC1 Differential Input Control 0: Disable 1: Enable
Reserved	11:8	R	0'h	Reserved
mic22hp_mute	7	RW	1'h	Mute MIC2 Volume Output to Headphone Mixer 0: On 1: Mute
mic22spk_mute	6	RW	1'h	Mute MIC2 Volume Output to Speaker Mixer 0: On 1: Mute
mic22MONO_mute	5	RW	1'h	Mute MIC2 Volume Output to MONO Mixer 0: On 1: Mute
mic2_diff_ctrl	4	RW	0'h	MIC2 Differential Input Control 0: Disable 1: Enable
Reserved	3:0	R	0'h	Reserved

8.9. Reg-12h: ADC Record Gain

Default: F58Bh

Table 21. Reg-12h: ADC Record Gain

Name	Bits	Read/Write	Reset State	Description
adc2hp_l_mute	15	RW	1'h	Mute Left Gain Output to Headphone Mixer Control 0: On 1: Mute (-∞dB)
adc2hp_r_mute	14	RW	1'h	Mute Right Gain Output to Headphone Mixer Control 0: On 1: Mute (-∞dB)
adc2MONO_l_mute	13	RW	1'h	Mute Left Gain Output to MONO Mixer Control 0: On 1: Mute (-∞dB)
adc2MONO_r_mute	12	RW	1'h	Mute Right Gain Output to MONO Mixer Control 0: On 1: Mute (-∞dB)
adc_l_vol	11:7	RW	0B'h	ADC Record Gain Left Channel (LRG[4:0]) in 1.5dB Steps 00h: -16.5dB attenuation 0Bh: 0dB gain 1Fh: 30dB gain
adc_l_dezero	6	RW	0'h	ADC_L Zero-Cross Detector Control 0: Disable 1: Enable
adc_r_dezero	5	RW	0'h	ADC_R Zero-Cross Detector Control 0: Disable 1: Enable
adc_r_vol	4:0	RW	0B'h	ADC Record Gain Right Channel (RRG[4:0]) in 1.5dB Steps 00h: -16.5dB attenuation 0Bh: 0dB gain 1Fh: 30dB gain

8.10. Reg-14h: ADC Record Mixer Control

Default: 7F7Fh

Table 22. Reg-14h: ADC Record Mixer Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
adcrec_l_mute	14:8	RW	7F'h	Left Mixer Mute Control 0: On 1: Mute (-∞dB) Bit 14: MIC1 Bit 13: MIC2 Bit 12: LINE_IN_L Bit 11: PHONE Bit 10: Headphone Mixer Left Channel Bit 9: Speaker Mixer Bit 8: MONO Mixer
Reserved	7	R	0'h	Reserved
adcrec_r_mute	6:0	RW	7F'h	Right Mixer Mute Control 0: On 1: Mute (-∞dB) Bit 6: MIC1 Bit 5: MIC2 Bit 4: LINE_IN_R Bit 3: PHONE Bit 2: Headphone Mixer Right Channel Bit 1: Speaker Mixer Bit 0: MONO Mixer

8.11. Reg-1Ch: Output Mixer Control

Default: 0000h

Table 23. Reg-1Ch: Output Mixer Control

Name	Bits	Read/Write	Reset State	Description
spk_l_vol_in_sel	15:14	RW	0'h	SPKL Volume Input Select 00: VMID (No input) 01: HP Left Mixer 10: Speaker Mixer 11: MONO
spk_l_out_sel	13	RW	0'h	SPKL and SPKR Output Select 0: Class-AB 1: Class-D
spk_r_vol_in_sel	12:11	RW	0'h	SPKR Volume Input Select 00: VMID (No input) 01: HP Right Mixer 10: Speaker Mixer 11: MONO
Reserved	10	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
hp_l_in_sel	9	RW	0'h	HPL Volume Input Select 0: VMID (No input) 1: HP Left Mixer
hp_r_in_sel	8	RW	0'h	HPR Volume Input Select 0: VMID (No input) 1: HP Right Mixer
MONO_in_sel	7:6	RW	0'h	MONO Volume Input Select 00: VMID (No input) 01: HP Left + Right Mixer 10: Speaker Mixer 11: MONO Mixer
Reserved	5	R	0'h	Reserved
clab_amp_source_sel	4	RW	0'h	In Class-AB Mode SPK_OUT_R Output Amplifier Source Select 0: SPKR Volume Output 1: SPKL Volume Output *Note: SPK_OUT_RN: SPKR Volume Negative Output.*
Reserved	3:0	R	0'h	Reserved

8.12. Reg-22h: Microphone Control

Default: 0000h

Table 24. Reg-22h: Microphone Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0'h	Reserved
mic1_boost_ctrl	11:10	RW	0'h	MIC1 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: +40dB
mic2_boost_ctrl	9:8	RW	0'h	MIC2 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: +40dB
Reserved	7:6	R	0'h	Reserved. Read as 0
mic1_bias_voltage_ctrl	5	RW	0'h	MICBIAS1 Output Voltage Control 0: 0.9*AVDD 1: 0.75*AVDD
mic2_bias_voltage_ctrl	4	RW	0'h	MICBIAS2 Output Voltage Control 0: 0.9*AVDD 1: 0.75*AVDD
Reserved	2:3	R	0'h	Reserved. Read as 0
mic_bias_threshold	1:0	RW	0'h	MICBIAS1/2 Short Current Detector Threshold 00: 600µA 01: 1200µA 1x: 1800µA

8.13. Reg-26h: Power Down Control/Status

Default: EF00h

Table 25. Reg-26h: Power Down Control/Status

Name	Bits	Read/Write	Reset State	Description
ac_pr7	15	RW	1'h	PR7 0: Normal 1: Power down Speaker Amplifier
ac_pr6	14	RW	1'h	PR6 0: Normal 1: Power down Headphone Out and MONO Out
ac_pr5	13	RW	1'h	PR5 0: Normal 1: Disable internal clock
Reserved	12	RW	0'h	Reserved
ac_pr3	11	RW	1'h	PR3 0: Normal 1: Power down Mixer (Vref/Vrefout off)
ac_pr2	10	RW	1'h	PR2 0: Normal 1: Power down Mixer (Vref/Vrefout are still on)
ac_pr1	9	RW	1'h	PR1 0: Normal 1: Power down STEREO DAC
ac_pr0	8	RW	1'h	PR0 0: Normal 1: Power down STEREO ADC, and input MUX
Reserved	7:4	R	0'h	Reserved. Read as 0
vref_status	3	R	0'h	Vref Status 1: Vref is up to normal level 0: Not yet up to normal level
analog_mixer_status	2	R	0'h	Analog Mixer Status 1: Ready 0: Not yet ready
dac_status	1	R	0'h	DAC Status 1: Ready 0: Not yet ready
adc_status	0	R	0'h	ADC Status 1: Ready 0: Not yet ready

Table 26. Truth Table for Power Down Mode (PD=Power Down)

	ADC	DAC	Mixer	Vref	Int CLK	HP-OUT	MONO-OUT	SPK-OUT
PR0=1	PD	-	-	-	-	-	-	-
PR1=1	-	PD	-	-	-	-	-	-
PR2=1	-	-	PD	-	-	PD	-	-
PR3=1	PD	PD	PD	PD	-	PD	-	-
PR5=1	PD	PD	-	-	PD	-	-	-
PR6=1	-	-	-	-	-	PD	PD	-
PR7=1	-	-	-	-	-	-	-	PD

8.14. Reg-34h: Main Serial Data Port Control (Stereo I²S)

Default: 0000h

Table 27. Reg-34h: Main Serial Data Port Control (Stereo I²S)

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_mode_sel	15	RW	0'h	Main Serial Data Port Mode Selection 0: Master 1: Slave
stereo_i2s_sadlrck_ctrl_en	14	RW	0'h	SADLRCK Control: Set to '1' when ADC and DAC are different sampling rate 0: Disable, ADC and DAC use the same Fs 1: Enable *Note: Frame clock have to input from SDALRCK when this bit set to '0'.*
Reserved	13	R	0'h	Reserved
stereo_i2s_bclk_polarity_ctrl	12	RW	0'h	Stereo I²S BCLK Polarity Control 0: Normal 1: Invert
i2s_da_sigma_delta_clock_sel	11	RW	0'h	I²S_DA Sigma Delta Clock Source Select 0b: From DA Filter 1b: From DA Sigma Delta Clock Divider
i2s_da_sigma_delta_clock_div	10:8	RW	0'h	I²S DA Sigma Delta Clock Divider 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 101b: ÷ 64 Others: Reserved
Reserved	7	RW	0'h	Reserved
stereo_i2s_pcm_mode_sel	6	RW	0'h	PCM Mode Select 0: Mode A 1: Mode B Non PCM Mode Control 0: Normal SADLRCK / SDALRCK 1: Invert SADLRCK / SDALRCK *Note: Only support when stereo_i2s_sadlrck_ctrl_en='0'.*
Reserved	5:4	R	0'h	Reserved
stereo_i2s_data_len_sel	3:2	RW	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits
stereo_i2s_data_format_sel	1:0	RW	0'h	Stereo PCM Data Format Selection 00: I²S format 01: Right justified 10: Left justified 11: PCM format

8.15. Reg-3Ah: Power Management Addition 1

Default: 0000h

Table 28. Reg-3Ah: Power Management Addition 1

Name	Bits	Read/Write	Reset State	Description
depop_MONOoutb	15	RW	0'h	Depop of MONO Out 0: Enable (De-pop Enable) 1: Disable (De-pop Disable)
depop_hp_outb	14	RW	0'h	Depop of HP Out 0: Enable (De-pop Enable) 1: Disable (De-pop Disable)
pow_zcd	13	RW	0'h	All Zero-Cross Detect Power Down 0: Disable 1: Enable
Reserved	12	RW	0'h	Reserved
main_i2s_en	11	RW	0'h	Main I^2S Digital Interface Enable 0: Disable 1: Enable
Reserved	10:6	RW	0'h	Reserved
pow_mic1_bias_det_ctrl	5	RW	0'h	MICBIAS1 Short Current Detector Control 0: Disable 1: Enable
pow_mic2_bias_det_ctrl	4	RW	0'h	MICBIAS2 Short Current Detector Control 0: Disable 1: Enable
pow_mic1_bias	3	RW	0'h	0: Disable 1: Enable microphone1 bias
pow_mic2_bias	2	RW	0'h	0: Disable 1: Enable microphone2 bias
pow_main_bias	1	RW	0'h	0: Disable 1: Enable Main bias of the ALC5624
pow_dac_ref	0	RW	0'h	0: Disable 1: Enable ALL DAC reference of the ALC5624

8.16. Reg-3Ch: Power Management Addition 2

Default: 0000h

Table 29. Reg-3Ch: Power Management Addition 2

Name	Bits	Read/Write	Reset State	Description
pow_thermal	15	RW	0'h	Thermal Detect (Temp Sensor) 0: Disable 1: Enable
pow_clsab	14	RW	0'h	Class_AB Power (All) 0: Disable 1: Enable
pow_vref	13	RW	0'h	VREF of All Analog Circuits 0: Disable 1: Enable
pow_pll	12	RW	0'h	PLL 0: Disable 1: Enable PLL
Reserved	11	RW	0'h	Reserved
pow_extclk	10	RW	0'h	Extclk output 0: Disable 1: Enable
pow_dac_l	9	RW	0'h	Left Stereo DAC Filter Clock 0: Disable 1: Enable
pow_dac_r	8	RW	0'h	Right Stereo DAC Filter Clock 0: Disable 1: Enable
pow_adc_l	7	RW	0'h	Left Stereo ADC Filter Clock and Input Gain 0: Disable 1: Enable
pow_adc_r	6	RW	0'h	Right Stereo ADC Filter Clock and Input Gain 0: Disable 1: Enable
pow_hp_l	5	RW	0'h	Left Headphone Mixer 0: Disable 1: Enable
pow_hp_r	4	RW	0'h	Right Headphone Mixer 0: Disable 1: Enable
pow_spk_mixer	3	RW	0'h	Speaker Mixer 0: Disable 1: Enable
pow_MONO_mixer	2	RW	0'h	MONO Mixer 0: Disable 1: Enable
pow_adc_rec_l_mixer	1	RW	0'h	Left ADC Record Mixer 0: Disable 1: Enable
pow_adc_rec_r_mixer	0	RW	0'h	Right ADC Record Mixer 0: Disable 1: Enable

8.17. Reg-3Eh: Power Management Addition 3

Default: 0000h

Table 30. Reg-3Eh: Power Management Addition 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
pow_MONO_out_vol	14	RW	0'h	MONO_OUT Volume Control (Amp) 0: Disable 1: Enable
pow_spk_outln	13	RW	0'h	SPK_OUTLN Output (Enable Class-AB & Class-D) 0: Disable 1: Enable
pow_spk_outrn	12	RW	0'h	SPK_OUTRN Output (Enable Class-AB & Class-D) 0: Disable 1: Enable
pow_hp_l_vol	11	RW	0'h	HP_OUT_L Volume Control (Amp) 0: Disable 1: Enable
pow_hp_r_vol	10	RW	0'h	HP_OUT_R Volume Control (Amp) 0: Disable 1: Enable
pow_spk_l	9	RW	0'h	SPK_OUT_L Output (Enable Class-AB & Class-D) 0: Disable 1: Enable
pow_spk_r	8	RW	0'h	SPK_OUT_R Output (Enable Class-AB & Class-D) 0: Disable 1: Enable
pow_li_l_vol	7	RW	0'h	LINE_IN Left Volume Control 0: Disable 1: Enable
pow_li_r_vol	6	RW	0'h	LINE_IN Right Volume Control 0: Disable 1: Enable
pow_phone_vol	5	RW	0'h	PHONE Volume Control 0: Disable 1: Enable
pow_phone_admixer	4	RW	0'h	PHONE AD Mixer 0: Disable 1: Enable
pow_mic1_vol	3	RW	0'h	MIC1 Volume Control 0: Disable 1: Enable
pow_mic2_vol	2	RW	0'h	MIC2 Volume Control 0: Disable 1: Enable
pow_mic1_admixer	1	RW	0'h	MIC1 AD Mixer and Boost 0: Disable 1: Enable
pow_mic2_admixer	0	RW	0'h	MIC2 AD Mixer and Boost 0: Disable 1: Enable

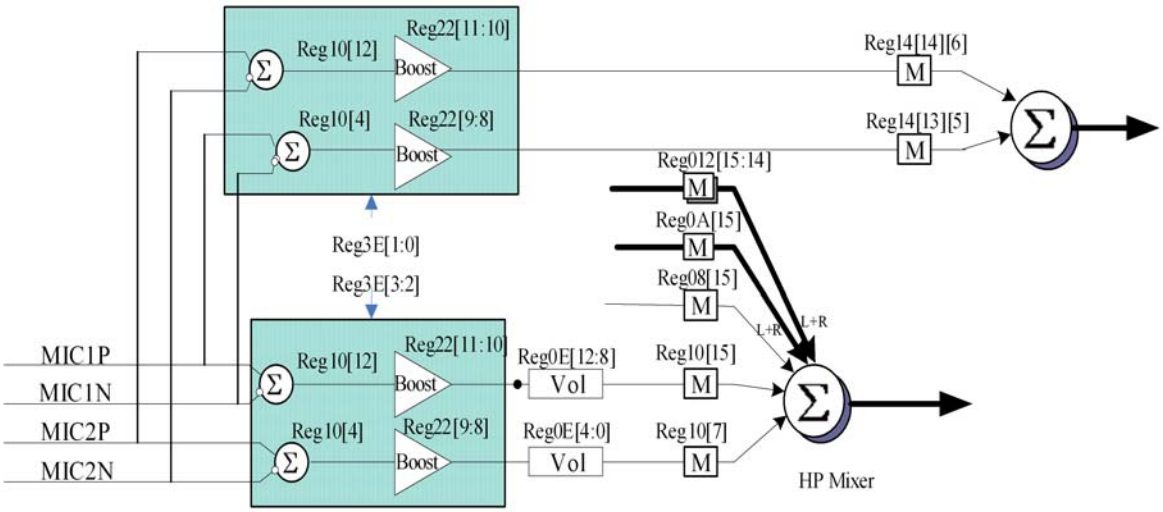


Figure 15. Power Control to MIC Input

8.18. Reg-40h: General Purpose Control Register 1

Default: 0428h

Table 31. Reg-40h: General Purpose Control Register 1

Name	Bits	Read/Write	Reset State	Description
sel_sysclk	15	RW	0'h	Stereo SYSCLK Source Select 0: MCLK 1: PLL Output
extclk_out_en	14	RW	0'h	EXTCLK Output Control 0: Disable 1: Enable
Reserved	13:10	RW	1'h	Reserved
hp_amp_ctrl	9:8	RW	0'h	Headphone Amplifier V_{MID} Ratio Control (Output Gain Control) 00: 1 01: 1.25 1x: 1.5
spk_ampD_ctrl	7:6	RW	0'h	Speaker Class-D Amplifier V_{MID} Ratio Control (Output Gain Control) 00: 1.75 Vdd 01: 1.5 Vdd 10: 1.25 Vdd 11: 1.0 Vdd
spk_ampAB_ctrl	5:3	RW	5'h	Speaker Class-AB Amplifier V_{MID} Ratio Control (Output Gain Control) 000: 2.25 Vdd 001: 2.00 Vdd 010: 1.75 Vdd 011: 1.5 Vdd 100: 1.25 Vdd 101: 1 Vdd Others: Not allowed
Reserved	2:0	RW	0'h	Reserved

8.19. Reg-42h: General Purpose Control Register 2

Default: 0000h

Table 32. Reg-42h: General Purpose Control Register 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	RW	0'h	Reserved
se_btl_clsab	13	RW	0'b	Single-Ended & BTL of SPK_Class-AB Selection 0: Differential Mode 1: Single-ended Mode
Reserved	12:1	RW	0'h	Reserved
pll_pre_div	0	RW	0'b	PLL Pre-Divider 0b: ÷1 1b: ÷2

8.20. Reg-44h: PLL Control

Default: 0000h

Table 33. Reg-44h: PLL Control

Name	Bits	Read/Write	Reset State	Description
pll_n_code	15:8	RW	00'h	N[7:0] Code for Analog PLL 00000000: Div 2 00000001: Div 3 …….. 11111111: Div 257
pll_m_bypass	7	RW	0'h	Bypass PLL M 0b: No bypass 1b: Bypass
pll_k_code	6:4	RW	0'h	K[2:0] Code for Analog PLL 000: Div 2 001: Div 3 …… 111: Div 9
pll_m_code	3:0	RW	0'h	M[3:0] Code for Analog PLL 0000: Div 2 0001: Div 3 …… 1111: Div 17

*Note: The PLL transmit formula is FOUT = (MCLK * (N+2))/((M+2) * (K+2)) {Typical K=2}.*

8.20.1. PLL Clock Setting Table for 48K: (Unit: MHz)

Table 34. PLL Clock Setting Table for 48K: (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

8.20.2. PLL Clock Setting Table for 44.1K: (Unit: MHz)

Table 35. PLL Clock Setting Table for 44.1K: (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

8.21. Reg-4Ch: GPIO Pin Configuration

Default: 2E3Eh

Table 36. Reg-4Ch: GPIO Pin Configuration

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	00'h	Reserved
over_temp_conf	11	RW	1'h	Over-Temperature Status Source Configuration 0: Bypass 1: Normal
mic1_short_det_conf	10	RW	1'h	MICBIAS1 Short Current Status Source Configuration 0: Bypass 1: Normal
mic2_short_det_conf	9	RW	1'h	MICBIAS2 Short Current Status Source Configuration 0: Bypass 1: Normal
Reserved	8:6	R	0'h	Reserved
gpio5_conf	5	RW	1'h	GPIO5 Pin Configuration 0: Output 1: Input
gpio4_conf	4	RW	1'h	GPIO4 Pin Configuration 0: Output 1: Input
gpio3_conf	3	RW	1'h	GPIO3 Pin Configuration 0: Output 1: Input
gpio2_conf	2	RW	1'h	GPIO2 Pin Configuration 0: Output 1: Input
gpio1_conf	1	RW	1'h	GPIO1 Pin Configuration 0: Output 1: Input
Reserved	0	R	0'h	Reserved. Read as 0

8.22. Reg-4Eh: GPIO Pin Polarity

Default: 2E3Eh

Table 37. Reg-4Eh: GPIO Pin Polarity

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	00'h	Reserved
over_temp_polarity	11	RW	1'h	Over-Temperature Polarity 0: Low Active 1: High Active
mic1_short_det_polarity	10	RW	1'h	MICBIAS1 Short Current Detect Polarity 0: Low Active 1: High Active
mic2_short_det_polarity	9	RW	1'h	MICBIAS2 Short Current Detect Polarity 0: Low Active 1: High Active
Reserved	8:6	R	0'h	Reserved. Read as 0
gpio5_polarity	5	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio4_polarity	4	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio3_polarity	3	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio2_polarity	2	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio1_polarity	1	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
Reserved	0	R	0'h	Reserved. Read as 0

8.23. Reg-50h: GPIO Pin Sticky

Default: 0000h

Table 38. Reg-50h: GPIO Pin Sticky

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	00’b	Reserved
over_temp_sticky_En	11	RW	0’h	Over-Temperature Sticky Enable 0: Not sticky 1: Sticky
mic1_short_det_sticky_En	10	RW	0’h	MICBIAS1 Short Current Detect Sticky Enable 0: Not sticky 1: Sticky
mic2_short_det_sticky_En	9	RW	0’h	MICBIAS2 Short Current Detect Sticky Enable 0: Not sticky 1: Sticky
Reserved	8:6	R	0’h	Reserved. Read as 0
gpio5_sticky_En	5	RW	0’h	GPIO5 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio4_sticky_En	4	RW	0’h	GPIO4 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio3_sticky_En	3	RW	0’h	GPIO3 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio2_sticky_En	2	RW	0’h	GPIO2 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio1_sticky_En	1	RW	0’h	GPIO1 Pin Sticky Enable 0: Not sticky 1: Sticky
Reserved	0	R	0’h	Reserved. Read as 0

8.24. Reg-52h: GPIO Pin Wake-Up

Default: 0000h

Table 39. Reg-52h: GPIO Pin Wake-Up

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	00’b	Reserved
over_temp_wakeup_en	11	RW	0’h	Over-Temperature Wake-Up Enable 0: No wake-up 1: Wake up
mic1_short_det_wakeup_en	10	RW	0’h	MICBIAS1 Short Current Detect Wake-Up Enable 0: No wake-up 1: Wake up
mic2_short_det_wakeup_en	9	RW	0’h	MICBIAS2 Short Current Detect Wake-Up Enable 0: No wake-up 1: Wake up
Reserved	8:6	R	0’h	Reserved. Read as 0
gpio5_wakeup_en	5	RW	0’h	GPIO5 Pin Wake-Up Enable 0: No wake-up 1: Wake up
gpio4_wakeup_en	4	RW	0’h	GPIO4 Pin Wake-Up Enable 0: No wake-up 1: Wake up
gpio3_wakeup_en	3	RW	0’h	GPIO3 Pin Wake-Up Enable 0: No wake-up 1: Wake up
gpio2_wakeup_en	2	RW	0’h	GPIO2 Pin Wake-Up Enable 0: No wake-up 1: Wake up
gpio1_wakeup_en	1	RW	0’h	GPIO1 Pin Wake-Up Enable 0: No wake-up 1: Wake up
Reserved	0	R	0’h	Reserved. Read as 0

8.25. Reg-54h: GPIO Pin Status

Default: 003Ah

Table 40. Reg-54h: GPIO Pin Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	00’b	Reserved
over_temp_status	11	R	0’h	Over-Temperature Status Read: Return status Write: Writing ‘0’ clears the sticky bit
mic1_short_det_status	10	R	0’h	MICBIAS1 Short Current Detect Status Read: Return status Write: Writing ‘0’ clears the sticky bit
mic2_short_det_status	9	R	0’h	MICBIAS2 Short Current Detect Status Read: Return status Write: Writing ‘0’ clears the sticky bit
Reserved	8:6	R	0’h	Reserved. Read as 0
gpio5_status	5	R	1’h	GPIO5 Pin Status Read: Return status of each GPIO pin Write: Writing ‘0’ clears the sticky bit
gpio4_status	4	R	1’h	GPIO4 Pin Status Read: Return status of each GPIO pin Write: Writing ‘0’ clears the sticky bit
gpio3_status	3	R	1’h	GPIO3 Pin Status Read: Return status of each GPIO pin Write: Writing ‘0’ clears the sticky bit
gpio2_status	2	R	1’h	GPIO2 Pin Status Read: Return status of each GPIO pin Write: Writing ‘0’ clears the sticky bit
gpio1_status	1	R	1’h	GPIO1 Pin Status Read: Return status of each GPIO pin Write: Writing ‘0’ clears the sticky bit
Reserved	0	R	0’h	Reserved. Read as 0

8.26. Reg-56h: Pin Sharing

Default: 0000h

Table 41. Reg-56h: Pin Sharing

Name	Bits	Read/Write	Reset State	Description
Reserved	15:3	R	0'h	Reserved
gpio2_pin_sharing	2	RW	0'h	GPIO2 Pin Sharing 0: IRQ_Out 1: GPIO enable
Reserved	1:0	R	0'h	Reserved

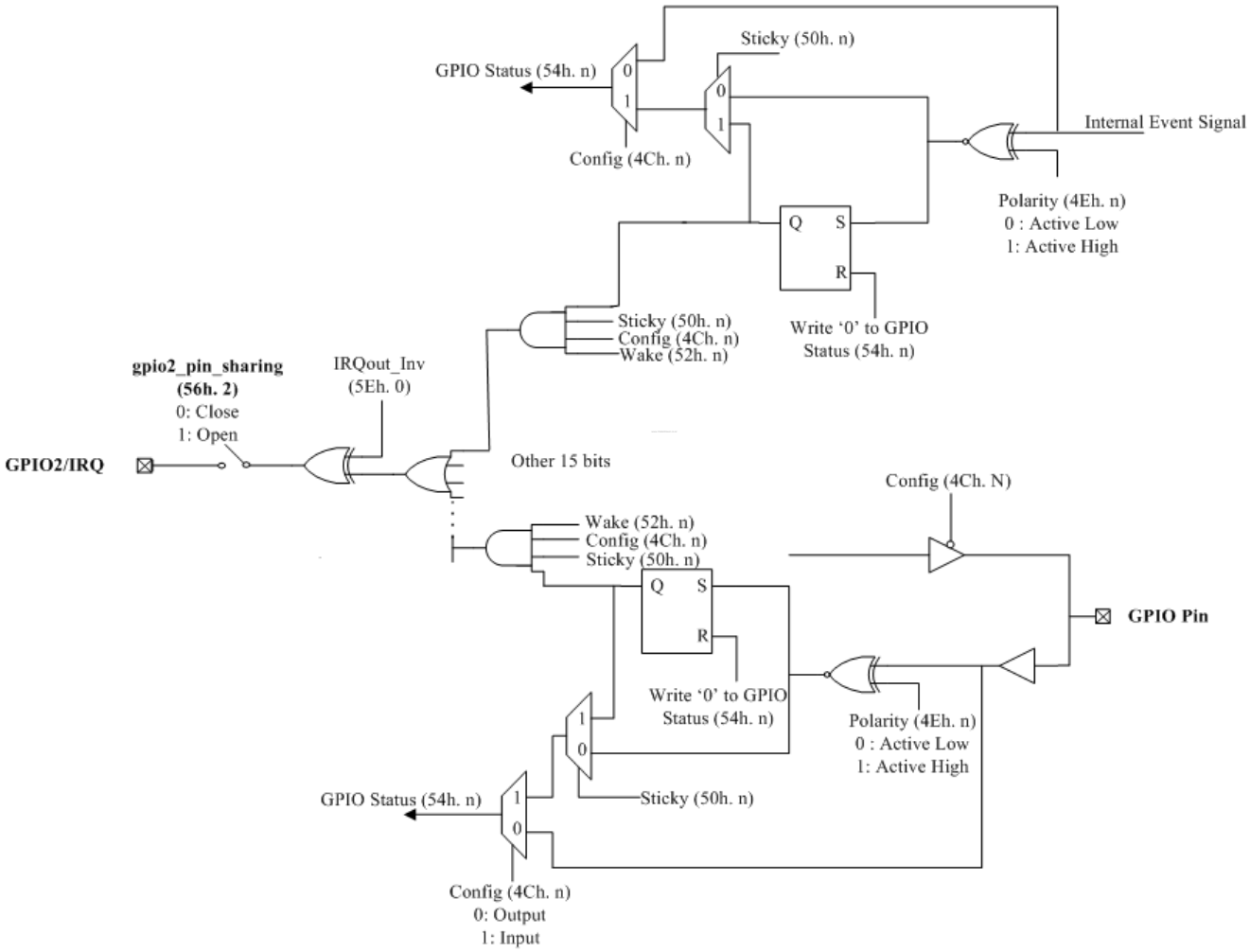


Figure 16. GPIO and IRQ Logic

8.27. Reg-58h: Over-Temp/Current Status

Default: 0CFFh

Table 42. Reg-58h: Over-Temp/Current Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0000'h	Reserved
ovt_hp_status	11	R	1'h	Headphone Amp Over-Temperature 0: Normal 1: Over-temperature
ovt_MONO_status	10	R	1'h	MONO Amp Over-Temperature 0: Normal 1: Over-temperature
ovc_micbias1_status	9	R	0'h	MICBIAS1 Over-Current 0: Normal 1: Over-current
ovc_micbias2_status	8	R	0'h	MICBIAS2 Over-Current 0: Normal 1: Over-current
rp_depop_status	7	R	1'h	RP Channel Depop Status 0: Depop ready 1: Depop finished
rn_depop_status	6	R	1'h	RN Channel Depop Status 0: Depop ready 1: Depop finished
lp_depop_status	5	R	1'h	LP Channel Depop Status 0: Depop ready 1: Depop finished
ln_depop_status	4	R	1'h	LN Channel Depop Status 0: Depop ready 1: Depop finished
ovt_rp_status	3	R	1'h	RP Channel Temperature Sensor Status 0: Normal 1: Over-temperature
ovt_rn_status	2	R	1'h	RN Channel Temperature Sensor Status 0: Normal 1: Over-temperature
ovt_lp_status	1	R	1'h	LP Channel Temperature Sensor Status 0: Normal 1: Over-temperature
ovt_ln_status	0	R	1'h	LN Channel Temperature Sensor Status 0: Normal 1: Over-temperature

8.28. Reg-5Ch: GPIO_Output Pin Control

Default: 0000h

Table 43. Reg-5Ch: GPIO_Output Pin Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	0000'h	Reserved
gpio5_out_status	5	RW	0'h	GPIO5 Output Pin Control 0b: Drive Low 1b: Drive High
gpio4_out_status	4	RW	0'h	GPIO4 Output Pin Control 0b: Drive Low 1b: Drive High
gpio3_out_status	3	RW	0'h	GPIO3 Output Pin Control 0b: Drive Low 1b: Drive High
gpio2_out_status	2	RW	0'h	GPIO2 Output Pin Control 0b: Drive Low 1b: Drive High
gpio1_out_status	1	RW	0'h	GPIO1 Output Pin Control 0b: Drive Low 1b: Drive High
Reserved	0	R	0'h	Reserved. Read as 0

8.29. Reg-5Eh: MISC Control

Default: 0000h

Table 44. Reg-5Eh: MISC Control

Name	Bits	Read/ Write	Reset State	Description
en_vref_fast	15	RW	0'b	Enable Fast Vref 0: Enable fast Vref 1: Disable fast Vref *Note: To improve PSRR, en_vref_fast should be disabled before playback/record.*
clsab_amp_sel	14	RW	0'b	Class-AB Output Amplifier Select 0: Strong Amp 1: Weak Amp *Note: Strong Amp, SPKVDD: 3.0V~5V and Set index44[8:6]=100'b. Weak Amp, SPKVDD: 2.3V~5V and set index44[8:6]=000'b.*
AVC_target_sel	13:12	RW	0'b	AVC Target Select 00: Reserved (No AVC) 01: R Channel 10: L Channel 11: Both channels
thermal_shutdown_en	11	RW	0'b	Thermal Shutdown Enable 0: Disable 1: Enable
Reserved	10:7	RW	0'h	Reserved
main_dac_l_mute	6	RW	0'h	Mute Main DAC Left Input 0: On 1: Mute (-∞dB)
main_dac_r_mute	5	RW	0'h	Mute Main DAC Right Input 0: On 1: Mute (-∞dB)
Reserved	4:1	RW	0'h	Reserved
irqout_inv_ctrl	0	RW	0'h	IRQOUT Inverter Control 0: Normal 1: Invert

The Jack-insert-detect pull up resistor is implemented via an external circuit (see Figure 17 below).

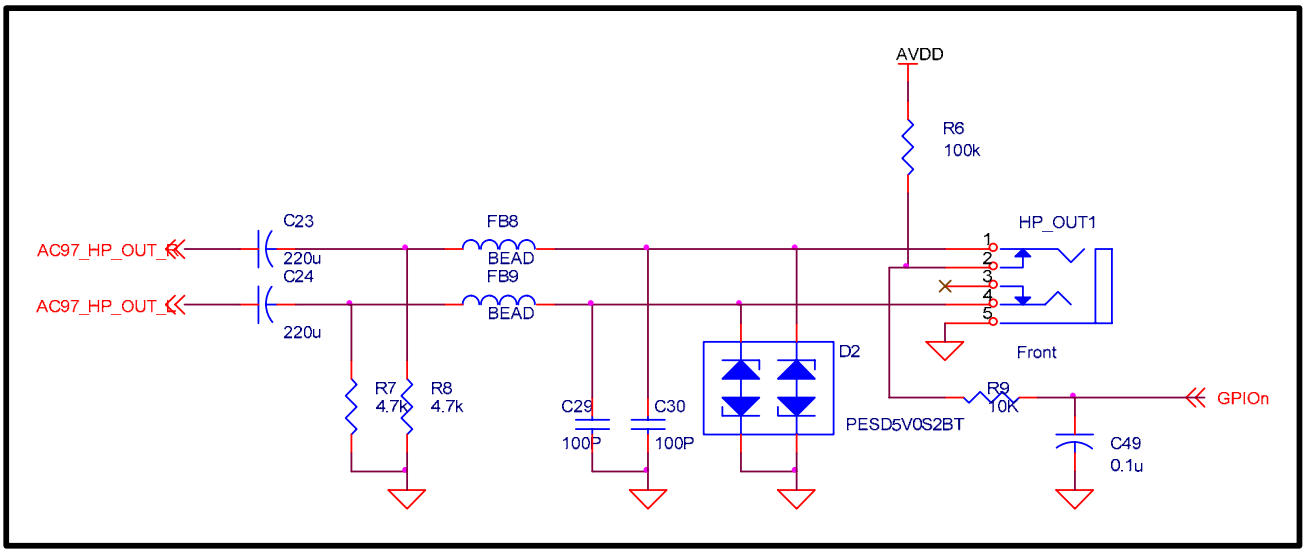


Figure 17. Jack-Insert-Detect Pull Up Resistor Implemented via an External Circuit

8.30. Reg-60h: Stereo DAC Clock Control_1

Default: 3075h

Table 45. Reg-60h: Stereo DAC Clock Control_1

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_sclk_div1	15:12	RW	3'h	Stereo I²S SCLK Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 ……. 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
Reserved	11	RW	0'h	Reserved
stereo_i2s_sclk_div2	10:8	RW	0'h	Stereo I²S SCLK Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
stereo_i2s_ad_wclk_div1	7:4	RW	7'h	Stereo I²S AD WCLK Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 ……. 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
stereo_i2s_ad_wclk_div2	3:1	RW	010'b	Stereo I²S AD WCLK Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
stereo_i2s_da_wclk_div	0	RW	1'h	Stereo I²S DA WCLK Div 0b: 32 1b: 64

8.31. Reg-62h: Stereo DAC Clock Control_2

Default: 1010h

Table 46. Reg-62h: Stereo DAC Clock Control_2

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_da_filter_div1	15:12	RW	1'h	Stereo I²S DA Filter Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 …… 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
stereo_i2s_da_filter_div2	11:9	RW	0'h	Stereo I²S DA Filter Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
Reserved	8	RW	0'h	Reserved
stereo_i2s_ad_filter_div1	7:4	RW	1'h	Stereo I²S AD Filter Div1 0000b: ÷ 1 0001b: ÷ 2 0010b: ÷ 3 …… 1101b: ÷ 14 1110b: ÷ 15 1111b: ÷ 16
stereo_i2s_ad_filter_div2	3:1	RW	0'h	Stereo I²S AD Filter Div2 000b: ÷ 2 001b: ÷ 4 010b: ÷ 8 011b: ÷ 16 100b: ÷ 32 Others: Reserved
Reserved	0	RW	0'h	Reserved

8.32. Reg-68h: Pseudo Stereo and Spatial Effect Block Control

Default: 0053h

Table 47. Reg-68h: Pseudo Stereo and Spatial Effect Block Control

Name	Bits	Read/Write	Reset State	Description
spatial_ctrl_enable	15	RW	0'b	Spatial Enable 0b: Disable (Clear internal state) 1b: Enable
apf_en	14	RW	0'h	Enable All Pass Filter APF(z) (EN-APF) 0: Disable (Bypass) and reset. 1: Enable all pass filters. The coefficient a1 is loaded from apf_parm_a1[7:0]
pseudo_stereo_en	13	RW	0'h	Enable Pseudo Stereo Block (EN-PSB) 0: Disabled 1: Enabled
en_3d	12	RW	0'h	Enable Stereo Expansion Block (EN-SEB) 0: Disable 1: Enabled. Load 3D Ratio from ratio_parm_3d and 3D Gain from gain_parm_3d
Reserved	11:8	-	0'h	Reserved
gain_parm_3d	7:6	RW	1'h	3D Gain Parameter (SEGn) 00: Gain=1.0 01: Gain=1.5 10: Gain=2.0 11: Reserved
ratio_parm_3d	5:4	RW	1'h	3D Ratio Parameter (DPn) 00: Ratio=0.0 01: Ratio=0.66 10: Ratio=1.0 11: Reserved
Reserved	3:2	-	0'h	Reserved
apf_parm_a1	1:0	RW	3'h	All Pass Filter parameter 00: Disable 01: Enable for 32kHz sample rate or lower 10: Enable for 44.1kHz sample rate 11: Enable for 48kHz sample rate

Note: Writes to SEGn and DPn will be ignored when the Spatial effect control bit is enabled. This means individual Spatial coefficients cannot be modified when Spatial is enabled.

8.33. Reg-6Ah: Index Address

Default: 0000h

Table 48. Reg-6Ah: Index Address

Name	Bits	Read/Write	Reset State	Description
Reserved	15:7	R	0'h	Reserved
index_addr	6:0	RW	0'h	Index Address

8.34. Reg-6Ch: Index Data

Default: 0000h

Table 49. Reg-6Ch: Index Data

Name	Bits	Read/Write	Reset State	Description
index_data	15:0	RW	0'h	Index Data

8.35. Reg-6Eh: EQ Status

Default: 0000h

Table 50. Reg-6Eh: EQ Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15:5	R	0'h	Reserved
eq_hpf_status	4	R	0'h	EQ High-Pass Filter (HPF) Status 0: Normal 1: Overflow. This bit is set if overflow has occurred. Write 1 to clear.
eq_bpf3_status	3	R	0'h	EQ Band-3 (BP3) Status 0: Normal 1: Overflow. This bit is set if overflow has occurred. Write 1 to clear.
eq_bpf2_status	2	R	0'h	EQ Band-2 (BP2) Status 0: Normal 1: Overflow. This bit is set if overflow has occurred. Write 1 to clear.
eq_bpf1_status	1	R	0'h	EQ Band-1 (BP1) Status 0: Normal 1: Overflow. This bit is set if overflow has occurred. Write 1 to clear.
eq_lpf_status	0	R	0'h	EQ Low-Pass Filter (LPF) Status 0: Normal 1: Overflow. This bit is set if overflow has occurred. Write 1 to clear.

8.36. Index-00h: EQ Band-0 Coefficient (LP0: a1)

Default: 0000h

Table 51. Index-00h: EQ Band-0 Coefficient (LP0: a1)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Formats (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

Note: For low pass filter for Bass control – LP0 has filter coefficient a1 and gain Ho must be set (see Table 52).

8.37. Index-01h: EQ Band-0 Gain (LP0: Ho)

Default: 0000h

Table 52. Index-01h: EQ Band-0 Gain (LP0: Ho)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.38. Index-02h: EQ Band-1 Coefficient (BP1: a1)

Default: 0000h

Table 53. Index-02h: EQ Band-1 Coefficient (BP1: a1)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.39. Index-03h: EQ Band-1 Coefficient (BP1: a2)

Default: 0000h

Table 54. Index-03h: EQ Band-1 Coefficient (BP1: a2)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.40. Index-04h: EQ Band-1 Gain (BP1: Ho)

Default: 0000h

Table 55. Index-04h: EQ Band-1 Gain (BP1: Ho)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.41. Index-05h: EQ Band-2 Coefficient (BP2: a1)

Default: 0000h

Table 56. Index-05h: EQ Band-2 Coefficient (BP2: a1)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.42. Index-06h: EQ Band-2 Coefficient (BP2: a2)

Default: 0000h

Table 57. Index-06h: EQ Band-2 Coefficient (BP2: a2)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.43. Index-07h: EQ Band-2 Gain (BP2: Ho)

Default: 0000h

Table 58. Index-07h: EQ Band-2 Gain (BP2: Ho)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.44. Index-08h: EQ Band-3 Coefficient (BP3: a1)

Default: 0000h

Table 59. Index-08h: EQ Band-3 Coefficient (BP3: a1)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.45. Index-09h: EQ Band-3 Coefficient (BP3: a2)

Default: 0000h

Table 60. Index-09h: EQ Band-3 Coefficient (BP3: a2)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.46. Index-0Ah: EQ Band-3 Gain (BP3: Ho)

Default: 0000h

Table 61. Index-0Ah: EQ Band-3 Gain (BP3: Ho)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.47. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)

Default: 0000h

Table 62. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.48. Index-0Ch: EQ Band-4 Gain (HPF: Ho)

Default: 0000h

Table 63. Index-0Ch: EQ Band-4 Gain (HPF: Ho)

Bit	Type	Function
15:0	RW	2's Complement in 3.13 Format (The range is from –4~3.99, the Ho should be in -2 ~ 1.99)

8.49. Index-10h: EQ Control and Status Register

Default: 0000h

Table 64. Index-10h: EQ Control and Status Register

Bit	Type	Function
15	RW	EQ Block Control 0b: Disable 1b: Enable
14:5	-	Reserved
4	RW	EQ High-Pass Filter (HPF) Control 0: Disabled (bypass) and reset 1: Enabled
3	RW	EQ Band-3 (BP3) Control 0: Disabled and reset 1: Enabled
2	RW	EQ Band-2 (BP2) Control 0: Disabled and reset 1: Enabled
1	RW	EQ Band-1 (BP1) Control 0: Disabled and reset 1: Enabled
0	RW	EQ Low-Pass Filter (LPF) Control 0: Disabled and reset 1: Enabled

Note: Individual EQ coefficients cannot be modified when EQ is enabled.

8.50. Index-11h: EQ Input Volume Control

Default: 0000h

Table 65. Index-11h: EQ Input Volume Control

Bit	Type	Function
15:2	-	Reserved
1:0	RW	7-Bit Volume Unsigned Ratio EQIn-VOL-LR 00b: 0dB 01b: -6dB 10b: -12dB 11b: -18dB

8.51. Index-12h: EQ Output Volume Control

Default: 0001h

Table 66. Index-12h: EQ Output Volume Control

Bit	Type	Function
15:3	-	Reserved
2:0	RW	7-Bit Volume Unsigned Ratio EQOut-VOL-LR 000b: -3dB 001b: 0dB 010b: 3dB 011b: 6dB 100b: 9dB 101b: 12dB 110b: 15dB 111b: 18dB

8.52. Index-20h: Auto Volume Control Register 0

Default: 0050h

Table 67. Index-20h: Auto Volume Control Register 0

Bit	Type	Function
15	RW	Select the Controlled Gain Block for AVC (Default: 00b) 0: Disable AVC 1: Enable AVC to control ADC gain
14:8	-	Reserved
7:3	RW	Monitor Window Control (Unit: 2^(n+1) samples) (Default: 01010b) 00000b: 2^(1) sample 00001b: 2^(2) samples 00010b: 2^(3) samples … 10000b: 2^(17) samples … Others: Reserved. Maximum n=16 *Note: The Monitor Window can only be changed after soft-reset when AVC is enabled.*
2:1	-	Reserved
0	RW	AVC Reference Channel Selection (Default: 0b) 0: Left Channel 1: Right Channel

8.53. Index-21h: Auto Volume Control Register 1

Default: 2710h

Table 68. Index-21h: Auto Volume Control Register 1

Bit	Type	Function
15	-	Reserved
14:0	RW	The Maximum PCM absolute level after AVC, Thmax (=0 ~ 2^15-1)

8.54. Index-22h: Auto Volume Control Register 2

Default: 0BB8h

Table 69. Index-22h: Auto Volume Control Register 2

Bit	Type	Function
15	-	Reserved
14:0	RW	The Minimum PCM absolute level after AVC, Thmin (=0 ~ 2^15-1)

8.55. Index-23h: Auto Volume Control Register 3

Default: 01F4h

Table 70. Index-23h: Auto Volume Control Register 3

Bit	Type	Function
15	-	Reserved
14:0	RW	The Non-active PCM absolute level AVC will keep analog unit gain, Thnonact (=0 ~ 2^15-1)

Note: Initial Index23=0001'h.

8.56. Index-24h: Auto Volume Control Register 4

Default: 0190h

Table 71. Index-24h: Auto Volume Control Register 4

Bit	Type	Function
15:0	RW	The CNTMAXTH1 that controls sensitivity to Gain increase (Unit:2^1) This value should be less than CNTMAXTH2 (Max:2^17)

8.57. Index-25h: Auto Volume Control Register 5

Default: 0200h

Table 72. Index-25h: Auto Volume Control Register 5

Bit	Type	Function
15:0	RW	The CNTMAXTH2 to control the sensitivity to decrease Gain (Unit:2^1) This value should be less than Monitor Window (Optimized: 1/2 Monitor Window) (Max:2^17)

Note: CNTMAXTH1 < CNTMAXTH2.

8.58. Index-39h: Digital Internal Register

Default: 9000h

Table 73. Index-39h: Digital Internal Register

Bit	Type	Function
15	RW	Pad Drive Capability 0b: Weak drive 1b: Strong drive
14:0	RW	Reserved

8.59. Index-4Ah: Class-D Temperature Sensor

Default: 4444h

Table 74. Index-4Ah: Class-D Temperature Sensor

Bit	Type	Function
15	RW	Reserved
14:12	RW	RP Channel Temp. Sensor Threshold Setting 001: 35°C 011: 65°C 101: 95°C 111: 125°C
11	RW	Reserved
10:8	RW	RN Channel Temp. Sensor Threshold Setting 001: 35°C 011: 65°C 101: 95°C 111: 125°C
7	RW	Reserved
6:4	RW	LP Channel Temp. Sensor Threshold Setting 001: 35°C 011: 65°C 101: 95°C 111: 125°C
3	RW	Reserved
2:0	RW	LN Channel Temp. Sensor Threshold Setting 001: 35°C 011: 65°C 101: 95°C 111: 125°C

Note: Tolerance: ± 15℃.

8.60. Index-54h: AD_DA_Mixer_Internal Register

Default: E184h

Table 75. Index-54h: AD_DA_Mixer_Internal Register

Bit	Type	Function
15	RW	Reserved
14:13	RW	DAC Reference Source 01: Internal DAC reference (AVDD & DAC reference cannot be bonded together) 11: External DAC reference (AVDD/AGND as DAC reference) Others: Forbidden
12:3	RW	Reserved
2:0	RW	Temp. Sensor for Threshold Setting 001: 35°C 011: 65°C 101: 95°C 111: 125°C *Note: Tolerance: ± 15℃.*

Note: To reduce DAC power consumption, we suggest that Index54=E184'h be initialized.

8.61. Reg-7Ch: VENDOR ID 1

Default: 10ECh

Table 76. Reg-7Ch: VENDOR ID 1

Name	Bits	Read/Write	Reset State	Description
vender_id1	15:0	R	10EC'h	Vendor ID=10EC

8.62. Reg-7Eh: VENDOR ID 2

Default: 2003h

Table 77. Reg-7Eh: VENDOR ID 2

Name	Bits	Read/Write	Reset State	Description
vender_id	15:8	R	10'h	Device ID=20
device_id2	7:0	R	03'h	Version ID=03

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 78. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DVDD1	-0.3	-	3.63	V
Digital Core	DVDD2	-0.3	-	3.63	V
Analog	AVDD1, AVDD2	-0.3	-	3.63	V
Headphone	HPVDD	-0.3	-	3.63	V
Speaker	SPKVDD	-0.3	-	7[1]	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

Note 1: SPKVDD=5V with 3.5% duty cycle Power bouncing up to SPKVDD=8V is acceptable.

9.1.2. Recommended Operating Conditions

Table 79. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DVDD1	1.8	3.3	3.6	V
Digital Core	DVDD2	1.8	3.3	3.6	V
Analog	AVDD1, AVDD2	2.3	3.3	3.6	V
Headphone	HPVDD	2.3	3.3	3.6	V
Speaker	SPKVDD[1]	2.3	3.3	5	V

Note 1: A 10µF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin of the ALC5624.

9.1.3. Static Characteristics

Table 80. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DVDD	V
High Level Input Voltage	V_{IH}	0.65DVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DVDD	V
Input Leakage Current	-	-1	-	1	µA
Output Leakage Current (Hi-Z)	-	-1	-	1	µA
Output Buffer High Drive Current	-	-	22	-	mA
Output Buffer Low Drive Current	-	-	10	-	mA
V_{MID} Internal Serial Resistor	-	25	50	75	KΩ
V_{MID} Internal Serial Resistor Ratio	-	95	100	105	%

Note: DVDD=3.3V, $T_{ambient}$=25℃, with 50pF external load.

9.2. Analog Performance Characteristics

Table 81. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs	-	1.0	-	Vrms
MIC Inputs (Non-Boost)	-	1.0	-	Vrms
MIC Inputs (Boost 20dB)	-	0.1	-	Vrms
ADC	-	0.7	-	Vrms
Full Scale Output Voltage				
MONO Outputs	-	1.0	-	Vrms
Headphone Amplifiers Outputs	-	1.0	-	Vrms
Speaker Amplifiers Outputs	-	1.3	-	Vrms
DAC	-	1.0	-	Vrms
S/N Ratio (A-Weighted, HPL/R or MONO with 10KΩ/50pF Load)				
Stereo DAC	-	90	-	dB
Stereo ADC	-	85	-	dB
Total Harmonic Distortion + Noise (HPL/R or MONO with 10KΩ/50pF Load)				
Stereo DAC	-	-85	-	dB
Stereo ADC	-	-80	-	dB
MIC Boost Amplifier				
Gain=20dB	18	20	22	dB
Gain=30dB	-	30	-	dB
Gain=40dB	-	40	-	dB
Input Impedance (Gain=0dB, ADC Mixer=On/Off)				
PHONEN (Differential Mode)	-	16	-	KΩ
MIC1N, MIC2N (Differential Mode)	-	16	-	KΩ
MIC1P, MIC2P	-	16	-	KΩ
PHONEP	-	16	-	KΩ
Input Impedance (Gain=0dB, ADC Mixer=On)				
LINE_IN	12.8	16	19.2	KΩ
Input Impedance (Gain=0dB, ADC Mixer=Off)				
LINE_IN	25.6	32	38.4	KΩ
Output Impedance				
MONO_OUT	-	2	-	Ω
HP_OUT	-	2	-	Ω
SPK_OUT (Class-AB)	-	1	-	Ω
SPK_OUT (Class-D)	-	0.3	0.4	Ω
MONO_OUT Amplifier Output Power (32Ω Load)				
Single-Ended Mode	25	-	-	mW
BTL Mode	75	-	-	mW
MONO_OUT Amplifier Quiescent Current (32Ω Load)/CH	-	700	-	µA

Parameter	Min	Typ	Max	Units
MONO_OUT Amplifier Efficiency (f_{IN}=1kHz, 32Ω Load)				
Single-Ended Mode (Output Power=25mW)	50	-	-	%
BTL Mode (Output Power=75mW)	50	-	-	%
MONO_OUT Amplifier THD+N				
Single-Ended Mode (10KΩ Load)				
Output Power=0.1mW	-	0.01	-	%
BTL Mode (10KΩ Load)				
Output Power=0.1mW	-	0.01	-	%
MONO_OUT Amplifier PSRR	-	60	-	dB
Headphone Amplifier Output Power (32Ω Load)	-	-	31.25	mW
Headphone Amplifier Quiescent Current (32Ω Load)	-	700	-	µA
Headphone Amplifier Efficiency (f_{IN}=1kHz, 32Ω Load, Output Power=25mW)	50	-	-	%
Headphone Amplifier THD+N (32Ω Load)				
Output Power=20mW	-	-70	-	dB
Output Power=25mW	-	-70	-	dB
Headphone Amplifier PSRR	-	68	-	dB
Class-D BTL Speaker Amplifier Output Power				
(SPKVDD=5V with 8Ω Load, 1% THD+N)	-	1	-	W
(SPKVDD=5V with 8Ω Load, 10% THD+N)	-	1.2	-	W
(SPKVDD=5V with 4Ω Load, 1% THD+N)	-	1.4	-	W
(SPKVDD=5V with 4Ω Load, 10% THD+N)	-	1.7	-	W
Class-D BTL Speaker Amplifier Output Power				
(SPKVDD=4.2V with 8Ω Load, 1% THD+N)	-	0.7	-	W
(SPKVDD=4.2V with 8Ω Load, 10% THD+N)	-	0.9	-	W
(SPKVDD=4.2V with 4Ω Load, 1% THD+N)	-	1	-	W
(SPKVDD=4.2V with 4Ω Load, 10% THD+N)	-	1.2	-	W
BTL Speaker Amplifier Quiescent Current (8Ω Load, SPKVDD=3.7V)				
Class-AB_Strong	-	7	-	mA
Class-D	-	4	-	mA
BTL Speaker Amplifier Efficiency (f_{IN}=1kHz, 8Ω Load, Output Power=700mW)				
Class-AB	50	-	-	%
Class-D	-	82	-	%
BTL Speaker Amplifier THD+N (8Ω Load, SPKVDD=5V)				
Class-AB_Strong				
Output Power=350mW	-	-70	-	dB
Output Power=600mW	-	-70	-	dB
Class-D				
Output Power=350mW	-	-70	-	dB
Output Power=600mW	-	-60	-	dB
BTL Speaker Amplifier THD+N				
Class-AB_Weak (10KΩ/50pF Load)	-	-85	-	dB

Parameter	Min	Typ	Max	Units
BTL Speaker Amplifier SNR (A-Weighted)				
Class-AB_Weak (10KΩ/50pF Load)	-	90	-	dB
BTL Speaker Amplifier PSRR	-	65	-	dB
Quiescent Playback Current (DAC to HP_OUT with 16Ω Load)	-	7.4	-	mA
Quiescent Record Current (LINE_IN to ADC)	-	11.3	-	mA
Power Down Current				
I_{DDA} (Analog Block)	-	-	10	µA
I_{DDD} (Digital Block)	-	-	1	µA
MICBIAS1 Output Voltage				
0.75*AVDD Setting	-	2.475	-	V
0.9*AVDD Setting	-	2.97	-	V
MICBIAS1 and MICBIAS2 Drive Current	-	16	-	mA
MICBIAS2 Output Voltage				
0.75*AVDD Setting	-	2.475	-	V
0.9*AVDD Setting	-	2.97	-	V
Vref Pull Up Resistor	-	50	-	KΩ

Note: Standard test conditions:
$T_{ambient}$=25℃, DVDD=AVDD1=AVDD2=HPVDD=3.3V, SPKVDD=4.2V.
1kHz input sine wave; PCM Sampling frequency=48kHz; 0dB=1Vrms, Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation; EQ and 3D disabled.

9.3. Signal Timing

9.3.1. I²C Control Interface

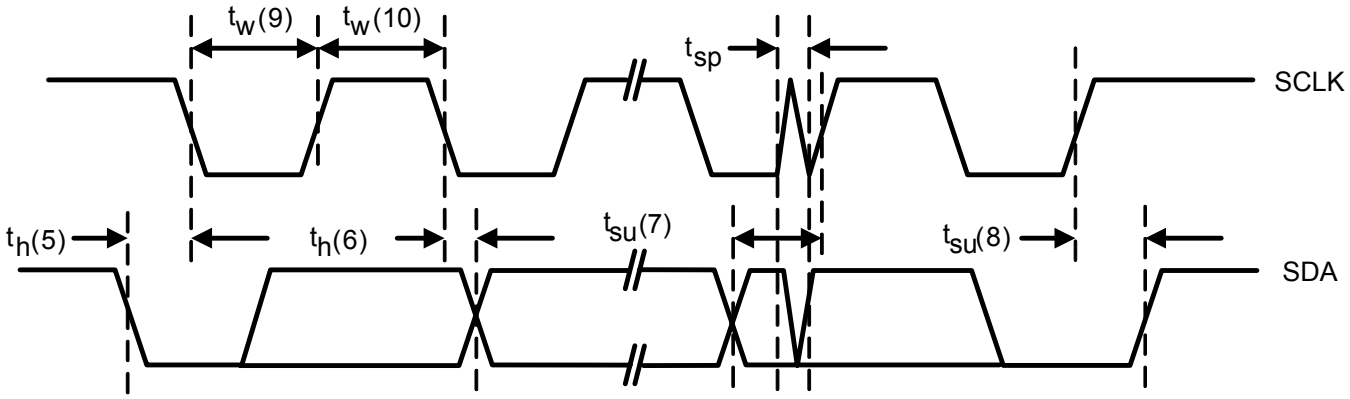


Figure 18. I²C Control Interface

Table 82. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	f	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

Note: Condition: MCLK > 8MHz.

9.3.2. I²S/PCM Interface Master Mode

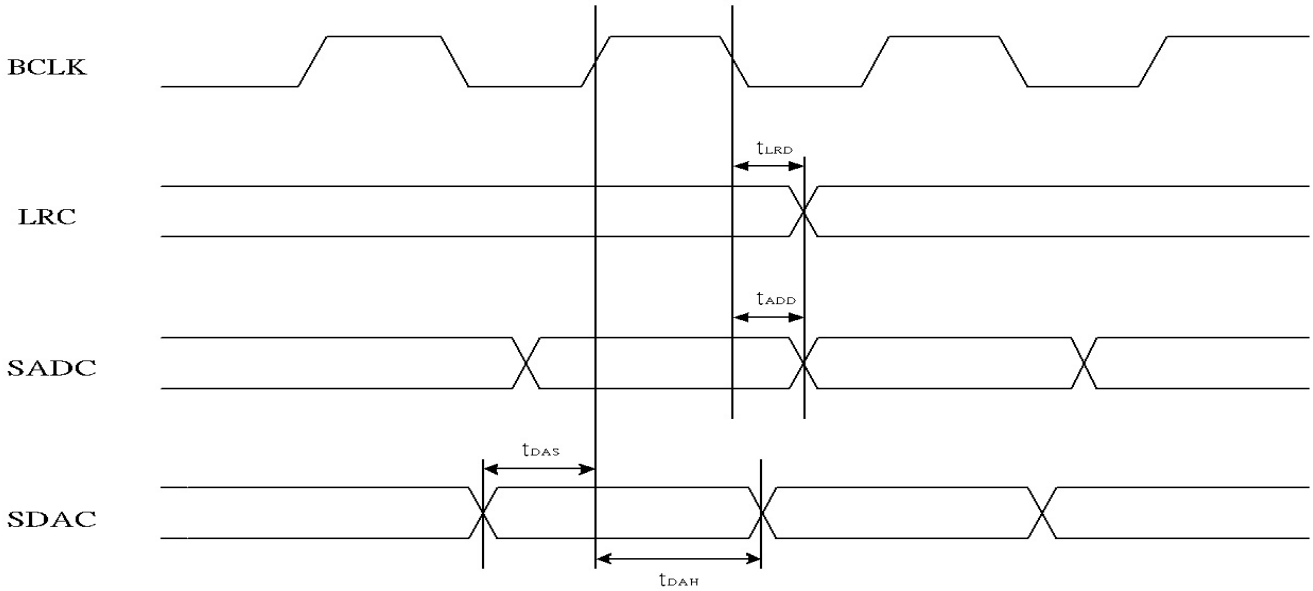


Figure 19. Timing of I²S/PCM Master Mode

Table 83. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

9.3.3. I²S/PCM Interface Slave Mode

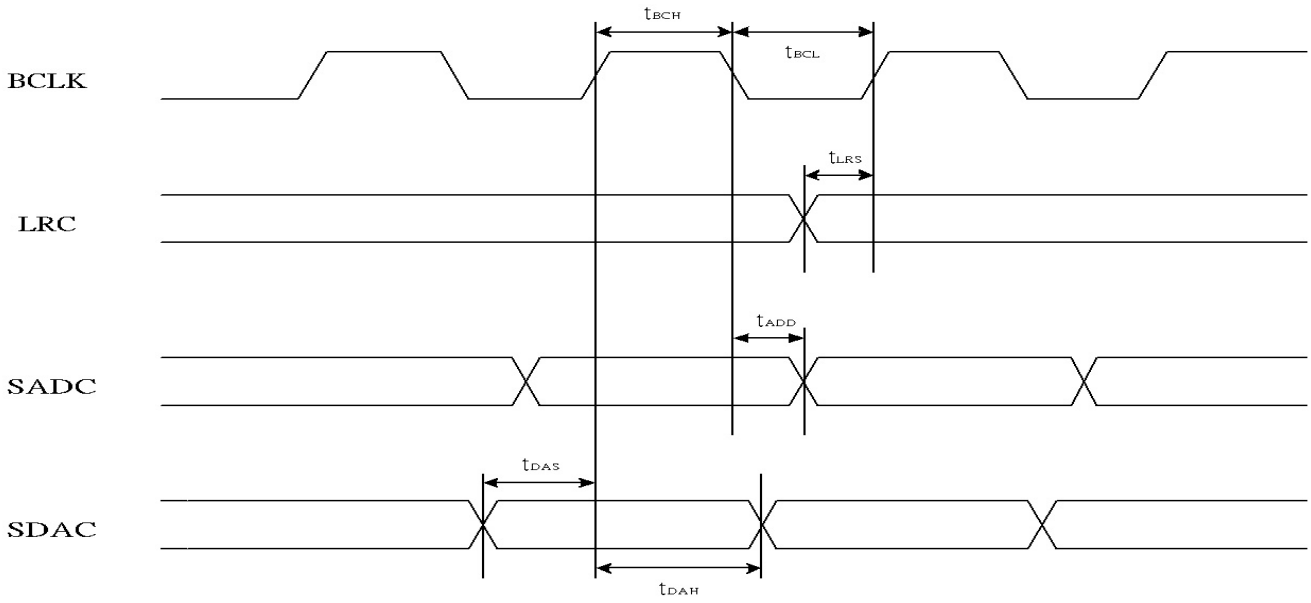
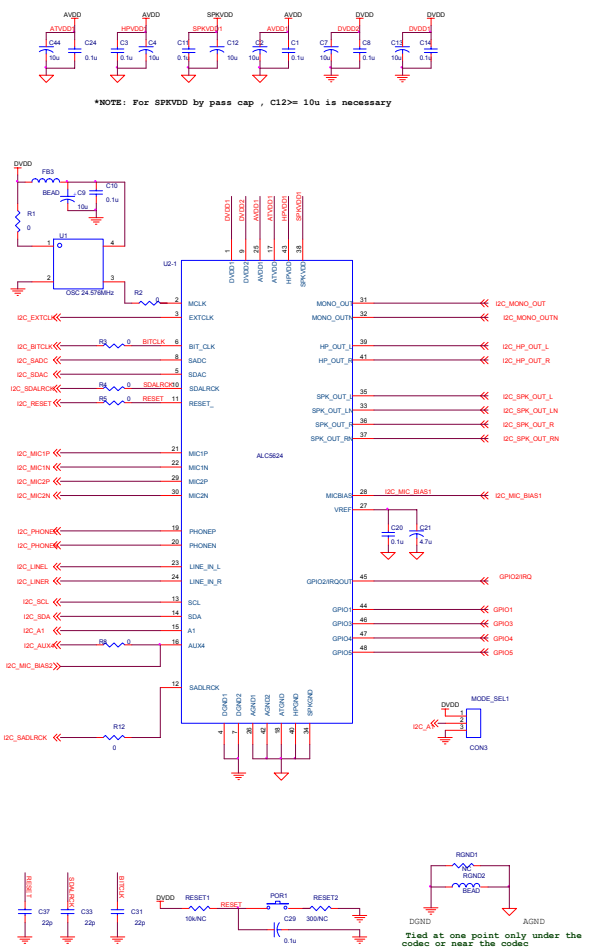


Figure 20. I²S/PCM Slave Mode Timing

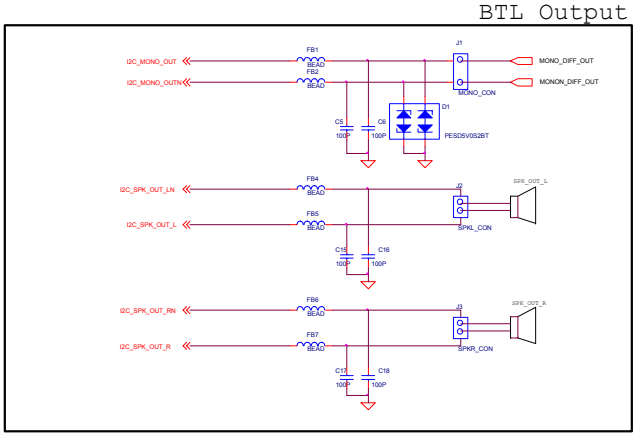
Table 84. I²S/PCM Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

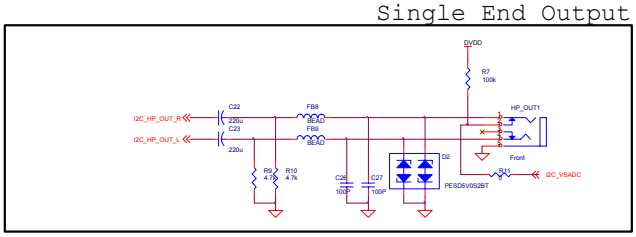
10. Application Circuits



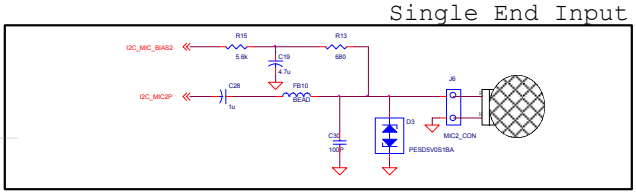
BTL Output



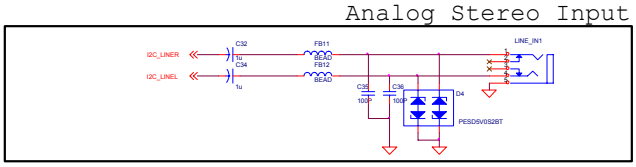
Single End Output



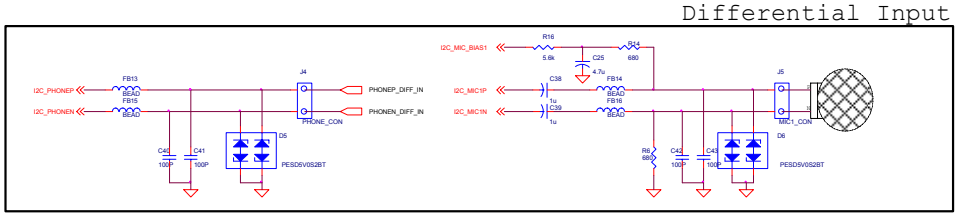
Single End Input



Analog Stereo Input

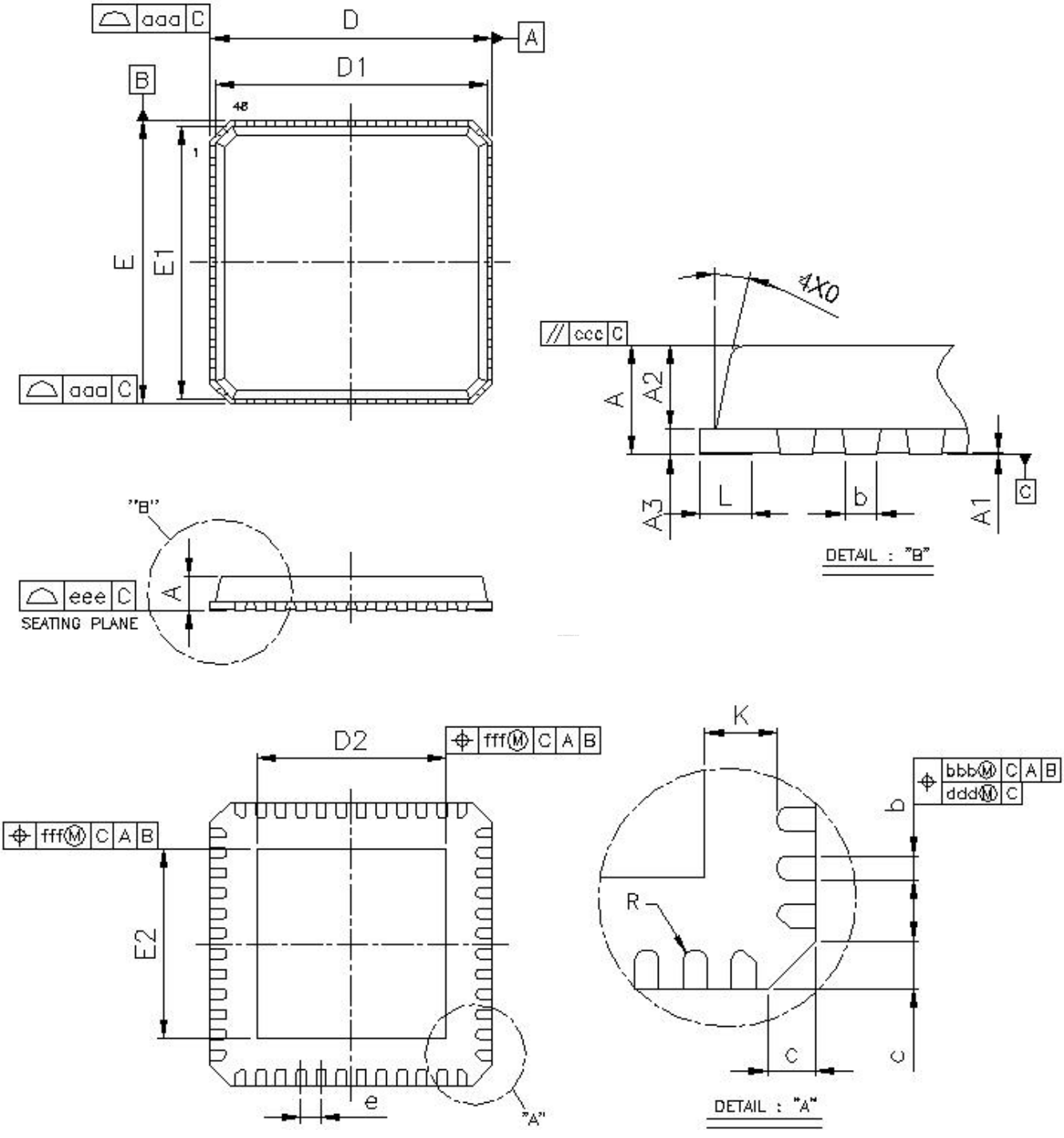


Differential Input



11. Mechanical Dimensions

Plastic Quad Flat No-Lead Package 48 Leads 7x7mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
c	-	-	0.6	-	-	0.024
D/E	7.00BSC			0.276BSC		
D_1/E_1	6.75BSC			0.266BSC		
D_2/E_2	4.80	5.05	5.30	0.189	0.199	0.209
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.2	-	-	0.008	-	-
θ	0^o	-	14^o	0^o	-	14^o
aaa	-	-	0.15	-	-	0.006
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.08	-	-	0.003
fff	-	-	0.10	-	-	0.004

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Appendix A: Stereo I²S Clock Table

12.1. Master/Slave Mode

MCLK or PLL Output❶	DAC Sample Rate	Sel_ sysclk	Stereo_i2s_ da_filter_div	Stereo_i2s_ sclk_div	Stereo_i2s_ da_wclk_div	ADC Sample Rate	Stereo_i2s_ ad_filter_div	Stereo_i2s_ ad_wclk_div
	SDALRCK❷	Reg40[15]	Reg62[15:12] *Reg62[11:9]	Reg60[15:12] *Reg60[10:8]	Reg60[0]	SADLRCK❷	Reg62[7:4] *Reg62[3:1]	Reg60[7:4] *Reg60[3:1]
24576000	8000	0'b/1'b	24	48/96	1'b/0'b	8000	24	64/32
24576000	16000	0'b/1'b	12	24/48	1'b/0'b	16000	/12	64/32
24576000	16000	0'b/1'b	12	24/48	1'b/0'b	8000	24	128/64
24576000	48000	0'b/1'b	4	8/16	1'b/0'b	48000	4	64/32
24576000	48000	0'b/1'b	4	8/16	1'b/0'b	32000	6	96/48
24576000	48000	0'b/1'b	4	8/16	1'b/0'b	16000	12	192/96
24576000	48000	0'b/1'b	4	8/16	1'b/0'b	8000	24	384/192
22579200	11025	0'b/1'b	16	32/64	1'b/0'b	11025	16	64/32
22579200	11025	0'b/1'b	16	32/64	1'b/0'b	8000	22	88/44
22579200	22050	0'b/1'b	8	16/32	1'b/0'b	22050	8	64/32
22579200	22050	0'b/1'b	8	16/32	1'b/0'b	11025	16	128/64
22579200	22050	0'b/1'b	8	16/32	1'b/0'b	8000	22	176/88
22579200	44100	0'b/1'b	4	8/16	1'b/0'b	44100	4	64/32
22579200	44100	0'b/1'b	4	8/16	1'b/0'b	22050	8	128/64
22579200	44100	0'b/1'b	4	8/16	1'b/0'b	11025	16	256/128
22579200	44100	0'b/1'b	4	8/16	1'b/0'b	8000	22	352/176

❶: PLL output as System Clock only supports Master Mode.
❷: SDALRCK and SADLRCK are output in Master Mode, and are input in Slave Mode.

13. Ordering Information

Table 85. Ordering Information

Part Number	Package	Status
ALC5624-GR	QFN-48 in 'Green' Package (Tray)	MP
ALC5624-GRT	QFN-48 in 'Green' Package (Tape & Reel)	MP

Note 1: See page 6 for Green package and version identification.
Note 2: Above parts are tested under AVDD1=AVDD2 =3.3V.

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