ALC5625

I2S AUDIO CODEC + VOICE PCM INTERFACE + ACOUSTIC ECHO CANCELLATION

DATASHEET

Rev. 0.60
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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC5625 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.60	2009/9/17	First released

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1. General Description

The ALC5625 is a Acoustic Echo Cancellation embedded highly-integrated dual I^2S/PCM interface audio codec with multiple input/output ports and is designed for mobile computing and communications. It provides a dual-channel Hi-Fi codec for playback, and dual-channel ADC for recording via an I^2S interface. In addition, an Independent Voice DAC is provided with PCM interface for Bluetooth applications.

Both Stereo audio and voice functions are supported via the I^2S/PCM configurable interface. To reduce component count, the device can connect directly to:

- Mono or Stereo differential analog inputs
- Stereo headphone
- Mono (Bridge-Tied Load) or Stereo Single-ended AUXOUT output
- Mono (Bridge-Tied Load) or Stereo Single-ended Speaker output

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality. Class-AB or Class-D amplifiers are easily swapped via simple register configuration, and the 2.3 Watt speaker removes the need for an additional amplifier, further cutting both cost and required board area. Additionally, a flexible hardware 5-band equalizer with configurable gain, bandwidth, and center frequency, and enriches the sound experience.

ALC5625 can support 1 microphone acoustic processing including acoustic echo cancellation and noise suppression without beam-forming. The AEC function of ALC5625 removes echo from a voice communication in order to improve voice quality to the far end. And BrightVoice™ function enhances the speaker output of playback.

ALC5625 Digital power operates at supply voltages from 1.8V to 3.6V. Analog power operates from 2.3V to 3.6V, and Speaker power operates from 2.3V to 5V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10μA.

The ALC5625 is available in a 7x7mm ‘Green’ QFN package, making it ideal for use in handheld portable systems.

2. Features

- High Performance I^2S Codec
  - 24-bit stereo DAC SNR 97dB, THD+N -93dB
  - 24-bit stereo ADC SNR 90dB, THD+N -85dB
  - Supports I^2S/PCM input and output interface
- One analog stereo input (LINE-IN)
- One analog MONO single-ended or differential input (PHONE and PHONEN input)
- Stereo, single-ended MONO, or differential analog microphone inputs, with boost pre-amplifiers (+20/+30/+40dB)
- BTL (Bridge-Tied Load) Max. output with on-chip 2.3W speaker driver (10% THD+N, SPKVDD=5V, 4Ω load)
- Stereo headphone output with on-chip 45mW headphone driver (HPVDD=3.3V, 16Ω load)
- Mono BTL (Bridge-Tied Load) or Stereo single-ended output support
- Microphone switch detection
- Integrated 24-bit I^2S/PCM interface voice DAC for blue-tooth and other external devices
- Power management and enhanced power saving
- Supports digital 5 band equalizer (EQ)
- Supports digital spatial sound and pseudo stereo effect
- Supports pop noise suppression
- Internal PLL can receive wide range of clock input (Digital IO power > 1.8V)
- Digital power supplies from 1.8V to 3.6V, speaker amplifier power supplies from 2.3V to 5V
- Analog power and headphone power supplies from 2.3V to 3.6V
- Acoustic Echo Cancellation supported
- 7 x 7mm 48-pin QFN package

3. System Applications

- Tablet PC system/Ultra-Mobile PC (UMPC)
- GPS/Personal Navigation Device (PND) or Multi-Media phone
- PDA Phone/Smartphone
- Personal Media Player (PMP)

4. Function Block Diagram

4.1. Function Block

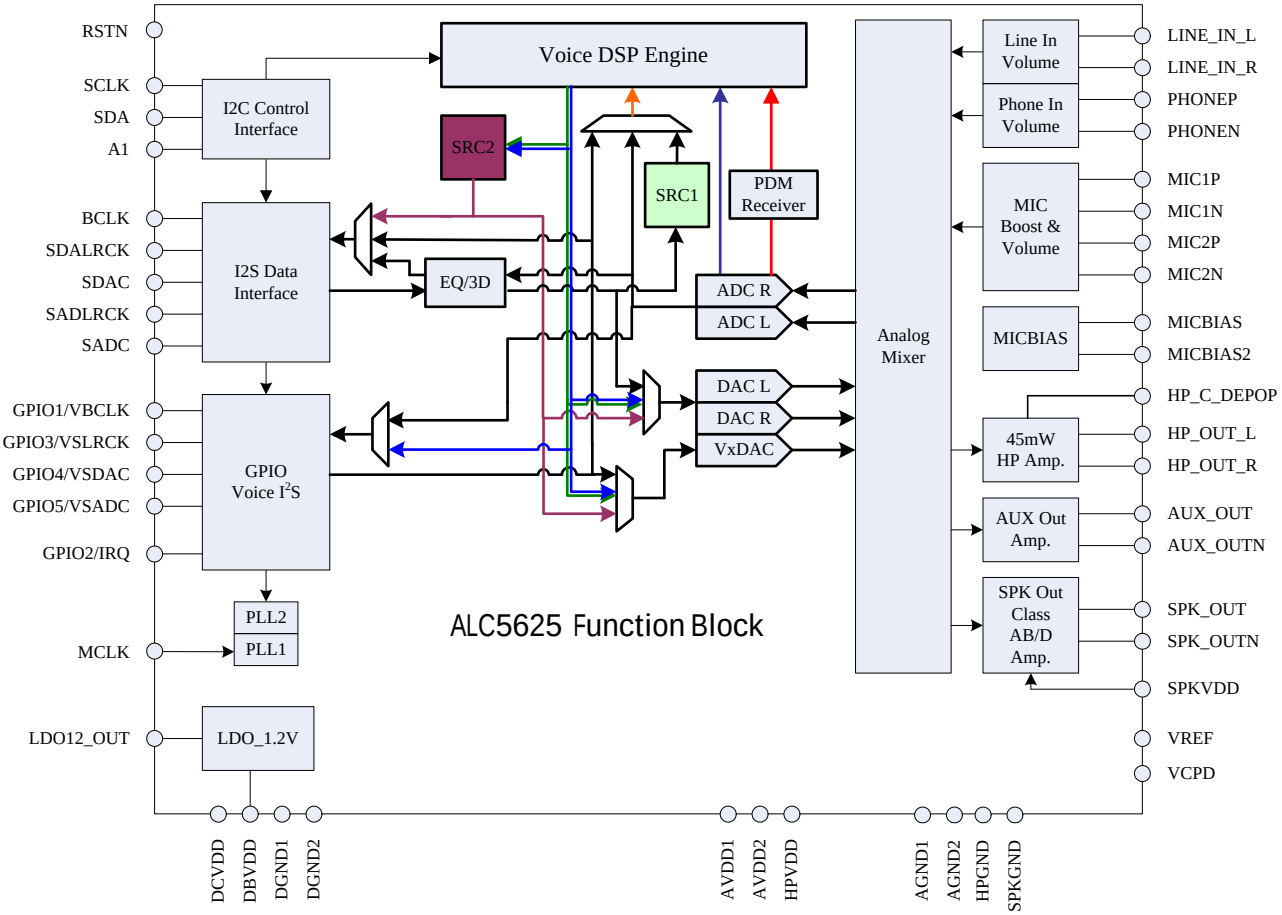


Figure 1. Block Diagram

4.2. Audio Mixer Path

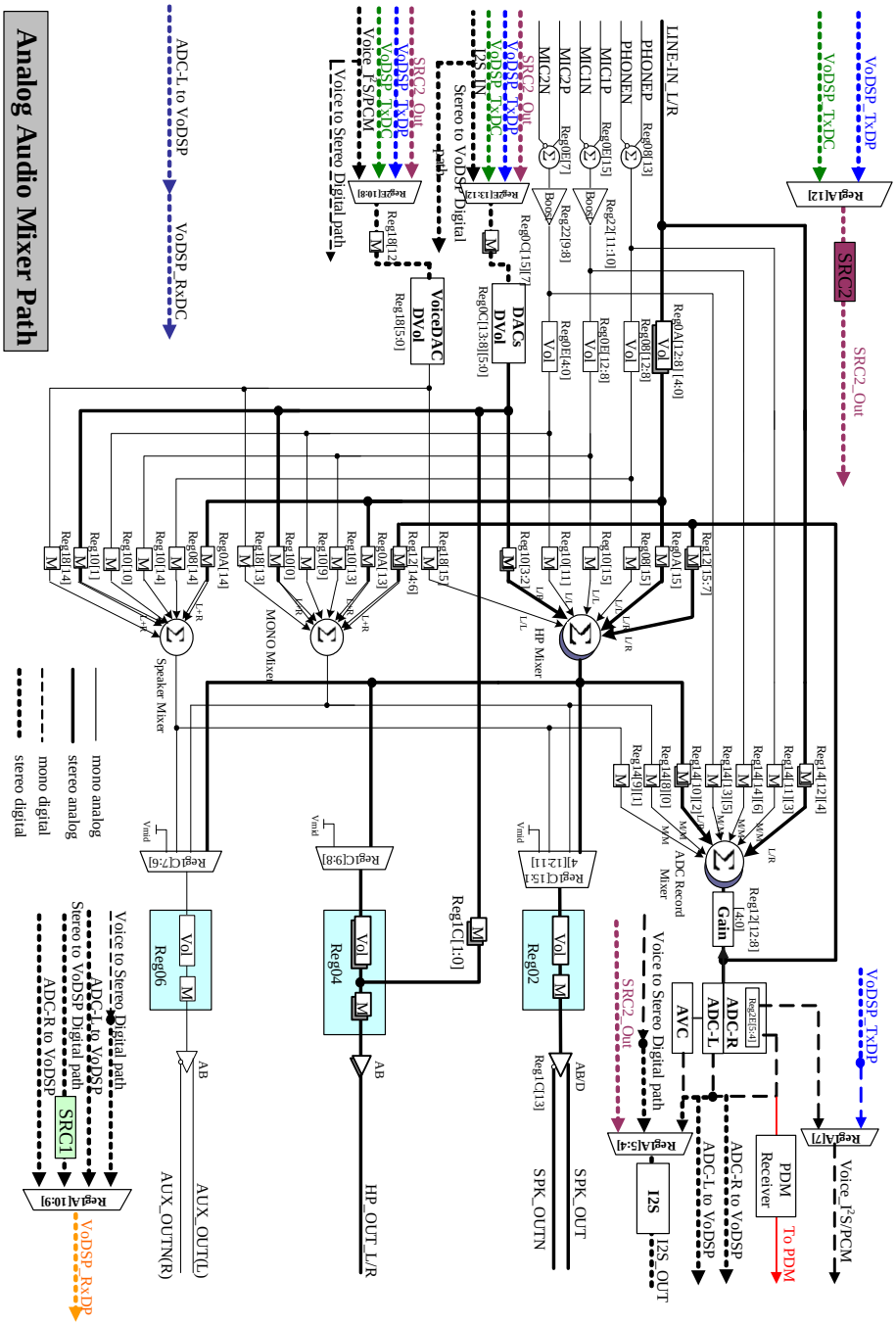


Figure 2. Audio Mixer Path

5. Pin Assignments

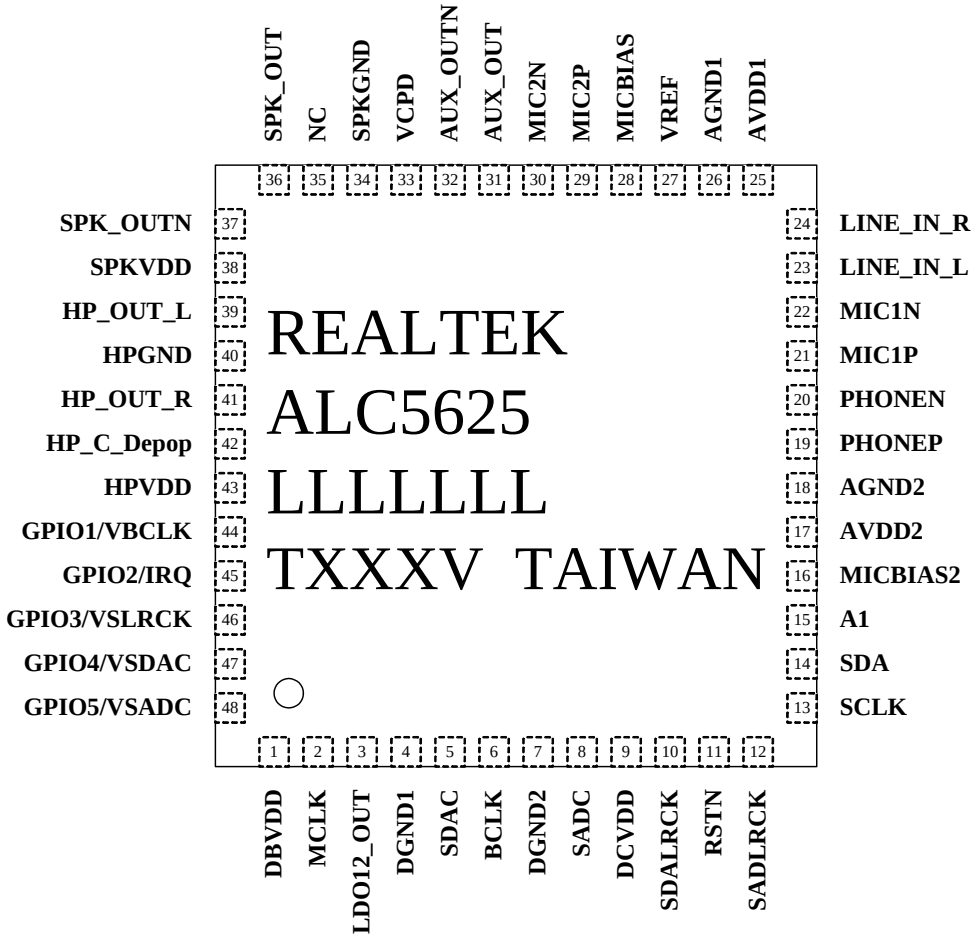


Figure 3. Pin Assignments

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. Pin Assignments. The version number is shown in the location marked 'V'.

6. Pin Descriptions

6.1. I2S Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MCLK	DI	2	Master Clock Input	Schmitt trigger
SDAC	DI	5	Stereo I^2S/PCM DAC Data Input	Schmitt trigger
BCLK	DIO	6	Stereo I^2S/PCM Bit Clock	Master: V_{OL}=0.1*DVDD, V_{OH}=0.9*DVDD Slave: Schmitt trigger
SADC	DO	8	Stereo I^2S/PCM ADC Data Output	V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD
SDALRCK	DIO	10	Stereo I^2S/PCM DAC Synchronous Signal	Master: V_{OL}=0.1*DVDD, V_{OH}=0.9*DVDD Slave: Schmitt trigger
RSTN	DI	11	H/W Reset Input (Low Active)	Schmitt trigger
SADLRCK	DIO	12	Stereo I^2S/PCM ADC Synchronous Signal	Master: V_{OL}=0.1*DVDD, V_{OH}=0.9*DVDD Slave: Schmitt trigger
SCLK	DI	13	I^2C Clock	Schmitt trigger
SDA	DIO	14	I^2C Data	Schmitt trigger
A1	DI	15	I2C address selection. Directly connect to VDD or GND	Schmitt trigger
NC	-	35	Non Connected, Have to keep floating	NC
GPIO1 / VBCLK	DIO	44	General Purpose Input and Output 1 / Voice I^2S interface clock	GPIO: Input / Output VBCLK: Slave input / Master output
GPIO2 / IRQ	DIO	45	General Purpose Input and Output 2 / Interrupt Output	GPIO: Input / Output IRQOUT: Output
GPIO3 / VSLRCK	DIO	46	General Purpose Input and Output 3 / Voice I^2S interface frame signal	GPIO: Input / Output VSLRCK: Slave input / Master output
GPIO4 / VSDAC	DIO	47	General Purpose Input and Output 4 / Voice I^2S interface serial data input	GPIO: Input / Output VSDAC: Voice DAC Data Input
GPIO5 / VSADC	DIO	48	General Purpose Input and Output 5 / Voice I^2S interface serial data output	GPIO: Input / Output VSADC: Voice ADC Data Output
				Total: 16 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MICBIAS2	AO	16	MICBIAS2 voltage output	
PHONEP	AI	19	Phone Positive Input	Analog Input (1Vrms)
PHONEN	AI	20	Phone Negative Input	Analog Input (1Vrms)
MIC1P	AI	21	First Mic Positive Input	Analog Input (1Vrms)
MIC1N	AI	22	First Mic Negative Input	Analog Input (1Vrms)

Name	Type	Pin	Description	Characteristic Definition
LINE_IN_L	AI	23	Line Input Left Channel	Analog Input (1Vrms)
LINE_IN_R	AI	24	Line Input Right Channel	Analog Input (1Vrms)
MICBIAS	AO	28	MIC BIAS Voltage Output	
MIC2P	AI	29	Second Mic Positive Input	Analog Input (1Vrms)
MIC2N	AI	30	Second Mic Negative Input	Analog Input (1Vrms)
AUX_OUT	AO	31	Positive AUX Output (external series connect 300Ω)	Analog Output (1Vrms)
AUX_OUTN	AO	32	Negative AUX Output (external series connect 300Ω)	Analog Output (1Vrms)
SPK_OUT	AO	36	Speaker Output	Analog Output (1.3Vrms@SPKVDD= 4.2V)
SPK_OUTN	AO	37	Negative Speaker Output	Analog Output (1.3Vrms@SPKVDD= 4.2V)
HP_OUT_L	AO	39	Headphone Output Left Channel	Analog Output (1Vrms)
HP_OUT_R	AO	41	Headphone Output Right Channel	Analog Output (1Vrms)
				Total: 16 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
VCPD	AO	33	External Capacitor for stabilizes 1.2V core voltage of VoDSP	Pin for connecting external 0.1uF capacitor to Digital ground
LDO12_OUT	AO	3	1.2V LDO output for VoDSP	Pin for connecting external 1uF capacitor to Digital ground
VREF	O	27	Internal Reference Voltage	4.7μF capacitor to analog ground
HP_C_DEPOP	AIO	42	Headphone de-pop capacitor	Pin for connecting external 1uF capacitor to analog ground
				Total: 4 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
DBVDD	P	1	Digital I/O VDD	1.8V~3.6V
DGND1	P	4	Digital GND	-
DGND2	P	7	Digital GND	-
DCVDD	P	9	Digital Core VDD	1.8V~3.6V
AVDD2	P	17	Analog VDD	2.3V~3.6V
AGND2	P	18	Analog GND	-
AVDD1	P	25	Analog VDD	2.3V~3.6V
AGND1	P	26	Analog GND	-

Name	Type	Pin	Description	Characteristic Definition
SPKGND	P	34	Analog GND for Speaker Amps	-
SPKVDD	P	38	Analog VDD for Speaker Amps External connect 10uF to SPKGND	2.3V~5V
HPGND	P	40	Analog GND of Headphone	-
HPVDD	P	43	Analog VDD of Headphone	2.3V~3.6V
LFGND	P	49	Thermal Pad, Connect to SPKGND. Have to be connect to system GND	-
				Total: 13 Pins

Note: DBVDD ≧ DCVDD, SPKVDD ≧ HPVDD ≧ AVDD1 = AVDD2 ≧ DCVDD
Note: SPDVDD connect 10μF Capacitor to SPKGND is required, and should be placed as close as possible to the SPKVDD pin of the ALC5625.
Note: SPDGND can share with AGND plane when Class-AB Speaker Amplifier is applied, and share with DGND plane when Class-D Speaker Amplifier is applied

7. Functional Description

7.1. Power

The ALC5625 has many power blocks. SPKVDD operates between 2.3V and 5V. HPVDD, AVDD1, and AVDD2 operate between 2.3V and 3.6V. DBVDD and DCVDD operate between 1.8V and 3.6V.
The power supply limit condition are DBVDD ≧ DCVDD, SPKVDD ≧ HPVDD ≧ AVDD1 = AVDD2 ≧ DCVDD

7.2. Reset

There are 3 types of reset operation: Power-On Reset (POR), Cold, and Register reset.

Table 5. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Cold Reset	Assert RESET# for a specified period	Reset all hardware logic and all registers to default values.
Register Reset	Write Reg-00h	Reset all registers to default values except PLL1, PLL2 power and Reg-44, Reg-46.

7.2.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC5625 (V_{POR_ON} ~V_{POR_OFF}). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 6. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: V_{POR_OFF} must be below V_{POR_ON}.

7.3. Power Management

The ALC5625 supports detailed Power Management control registers within Reg3A, 3C, and 3E. Each particular block will be active only when individual bits of Reg3A, 3C, and 3E are set to enable. In addition, The ALC5625 supports a grouped power down control register which is located in Reg26. The relationship between Reg26 and Reg3A/3C/3E is AND function.

7.4. Clocking

The Main_SYSCLK (512Fs) which provide clock into Stereo DAC/ADC, Voice DAC/ADC and Voice DSP Engine block can be selected from MCLK or PLL1. This means MCLK is always provided externally, and the driver have to arrange the clock of each block and setup each divider to fit the required clock rate of each block. Refer to Figure 4. ALC5625 Clock distributions

The Voice_SYSCLK which provide clock into Stereo DAC/ADC, Voice DAC/ADC and VoDSP block can be selected from MCLK (Master mode), PLL1/PLL2 (Master mode) or VBCLK (Slave mode). The driver should arrange the clock of each block and setup each divider to fit the required clock rate of each block. Refer to Figure 4. ALC5625 Clock distributions

Driver has to make sure that source clock of Stereo_SYSCLK and Voice_SYSCLK is ready before switch.

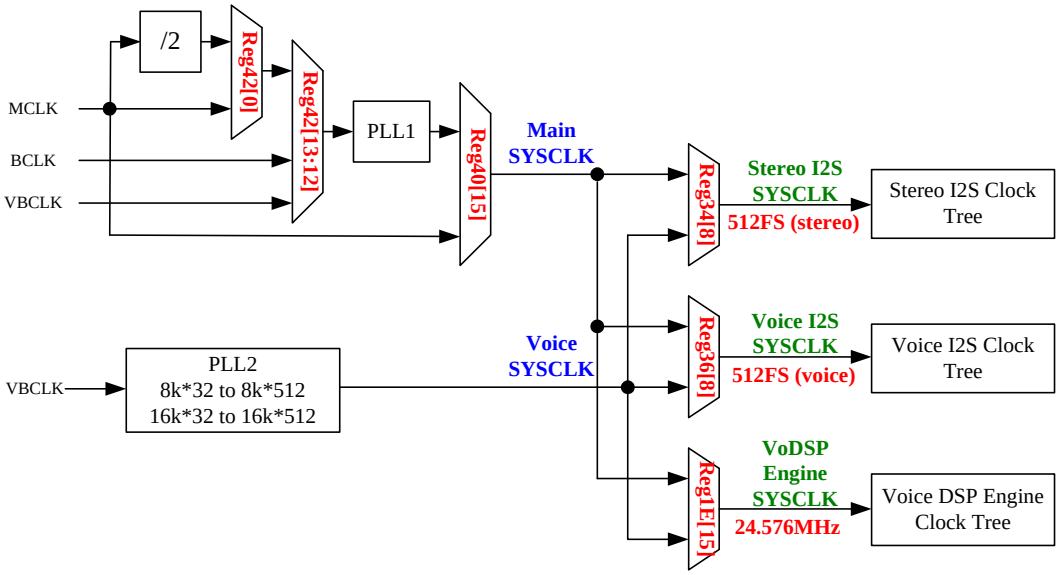


Figure 4. ALC5625 Clock distributions

7.4.1. Phase-Locked Loop

There are two Phase-Locked Loop (PLL) in ALC5625.

7.4.1.1 PLL1

PLL1 is main used to provide a flexible input clock from 2.048MHz to 40MHz for Main_SYSCLK. The source of the PLL can be set from MCLK, BCLK or VBCLK by setting **sel_sysclk.** The driver can set up the PLL1 to output a frequency in order to match the requirement of Main_SYSCLK.

The PLL1 transmit formula is:

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 7. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

Table 8. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

After a Cold Reset, PLL1 related Registers are reset to default values, however, they are not reset to default values after a soft-reset (write Reg00). Driver should not power down PLL1 when the PLL1 output is used as Main_SYSCLK.

7.4.1.2 PLL2

PLL2 is used to provide a flexible input clock for Voice_SYSCLK during Voice CODEC is in slave mode. The source of the PLL2 only can be from VBCLK**.** The output of PLL2 provides 8* or 16* input frequency by **pll2_n** in order to match the requirement of Voice_SYSCLK (512Fs).

7.4.2. I²C and Stereo I²S

The ALC5625 supports I²C for the digital control interface, and Stereo I²S/PCM for the digital data interface. The Stereo I²S/PCM audio digital interface is used to input data to a stereo DAC or output data from a stereo ADC. The I²S/PCM Audio Digital Interface can be configured to Master mode or Slave mode.

Master Mode

In master mode BCLK/SDALRCK/SADLRCK are configured as output. When PLL1 is disabled and sel_sysclk=0, MCLK is used as Stereo SYSCLK. When PLL1 is enabled, MCLK is suggested to provide frequency between 2.048MHz to 40MHz, and PLL1 should be configured to support 512*Fs. The driver should set each divider (Reg60 & Reg62) to arrange the clock distribution. Refer to section 12Appendix A: Stereo I2S Clock for details.

Note: The ALC5625 supports different sample rates between SDALRCK and SADLRCK in Master mode.

Slave Mode

In slave mode , BCLK and SDALRCK are configured as input. The Main_SYSCLK can be input from MCLK by provide BCLK synchronized clock externally. The driver should set each divider to arrange the clock distribution. Refer to section 12 Appendix A: Stereo I2S Clock for details.

Note: In Slave mode, the ALC5625 do NOT support different sample rates between SDALRCK and SADLRCK. Only SDALRCK is used in slave mode.

7.4.3. Voice_I²S/PCM Interface

The ALC5625 supports an independent digital interface for Voice Audio. The voice audio digital interface is used to input digital data to the voice DAC, or output digital data from the voice ADC. The Voice Audio Digital Interface can be configured to Master mode or Slave mode. The Sample rate of Voice ADC and Voice DAC is the same by setting Reg64 no matter in Master mode or Slave mode.

Master Mode

In Master mode the Voice_I2S_SYSCLK can be input selected from MCLK (with or without a PLL1). VBCLK and VSLRCK will be configured as output. The driver should set each divider (Reg64) to arrange the clock distribution. See section 13Appendix B: Voice I2S Clock for details.

Slave Mode

In Slave mode the Voice_I2S_SYSCLK can be input from MCLK by provide VBCLK synchronized externally. Alternatively, Voice_I2S_SYSCLK can be provided by output of PLL2 which input from VBCLK externally (**sel_vx_sysclk**) which is named BCLK Slave Mode. VBCLK and VSLRCK should be configured as input. The driver should set each divider (Reg64) to arrange the clock distribution (see section 13Appendix B: Voice I2S Clock for more information.

7.4.4. Voice ADC

The ALC5625 supports Voice ADC for transmitting voice data to a Bluetooth device. The Voice ADC is implemented by sharing from the Right Channel of the Stereo ADC and Left channel of stereo ADC still input stereo sample. (by setting **adcr_function_sel** = 01'b).

When **adcr_function_sel** = 01'b, the sample rate of the Left channel is still set by the stereo sample rate (Reg60 & Reg62). The sample rate of the Right channel is set by the voice sample rate (Reg64). The Left channel ADC data is output to the Left frame and duplicated to the Right frame of the Stereo I2S/PCM interface. The Right channel of the Stereo ADC data is then used as a Voice ADC and is output to voice_I²S/PCM.

7.5. Digital Data Interface

7.5.1. Stereo and Voice I²S/PCM Interface

The stereo and voice I²S/PCM interface can be configured as Master mode or Slave mode. Three audio data formats are supported:

- PCM mode
- Left justified mode

- I^2S mode

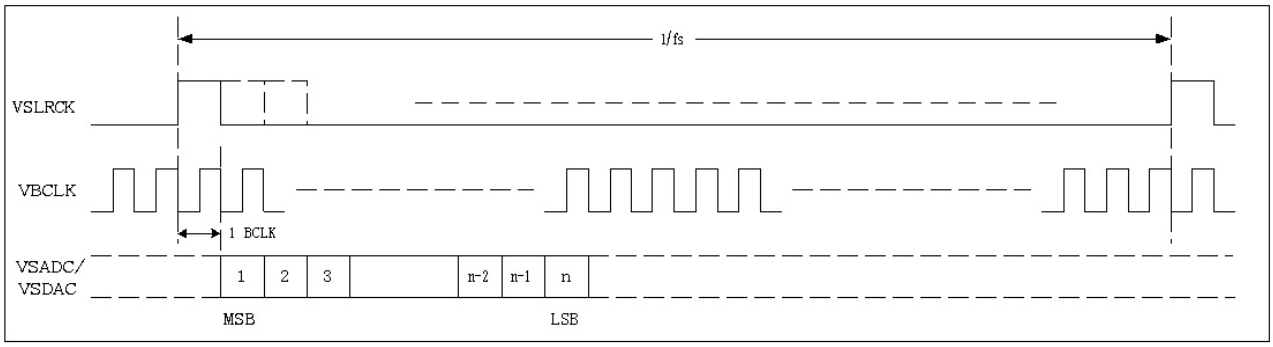


Figure 5. PCM MONO Data Mode A Format (bclk_polarity=0)

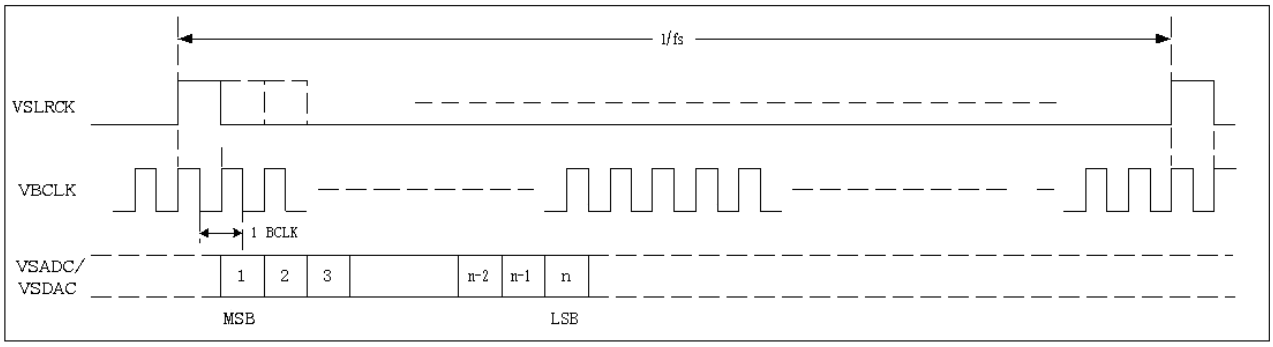


Figure 6. PCM MONO Data Mode A Format (bclk_polarity=1)

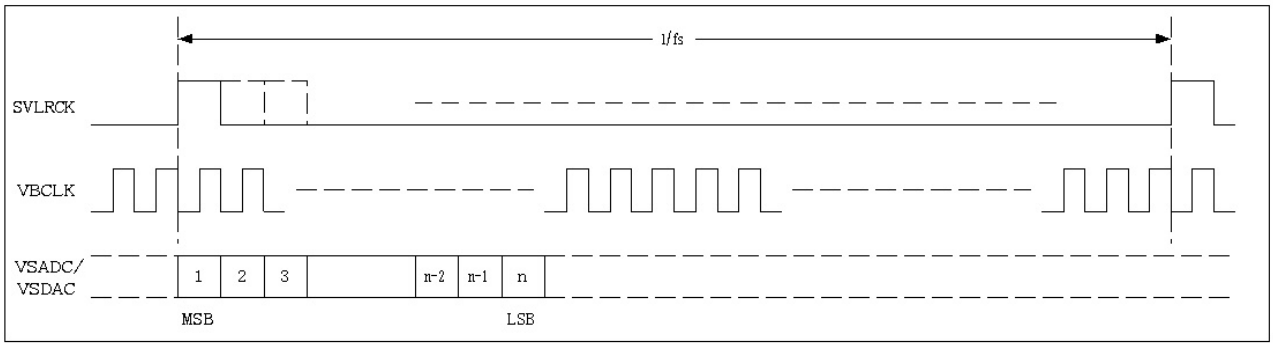


Figure 7. PCM MONO Data Mode B Format (bclk_polarity=0)

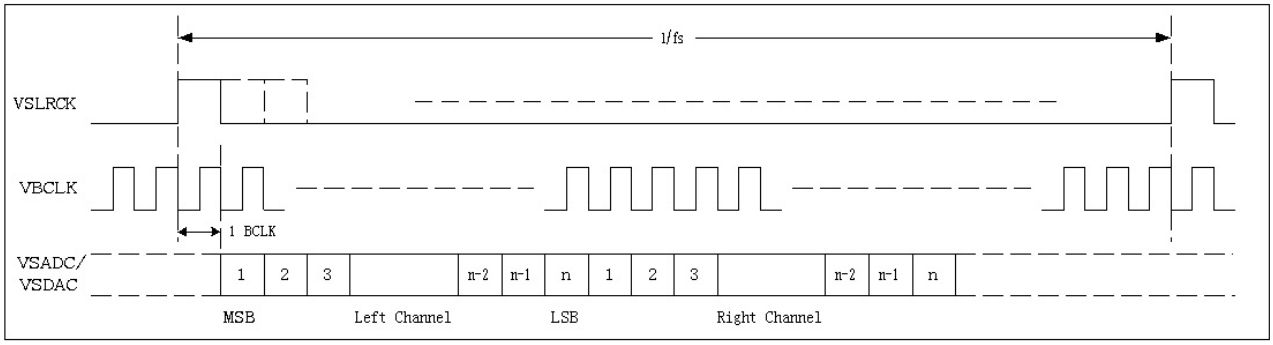


Figure 8. PCM Stereo Data Mode A Format (bclk_polarity=0)

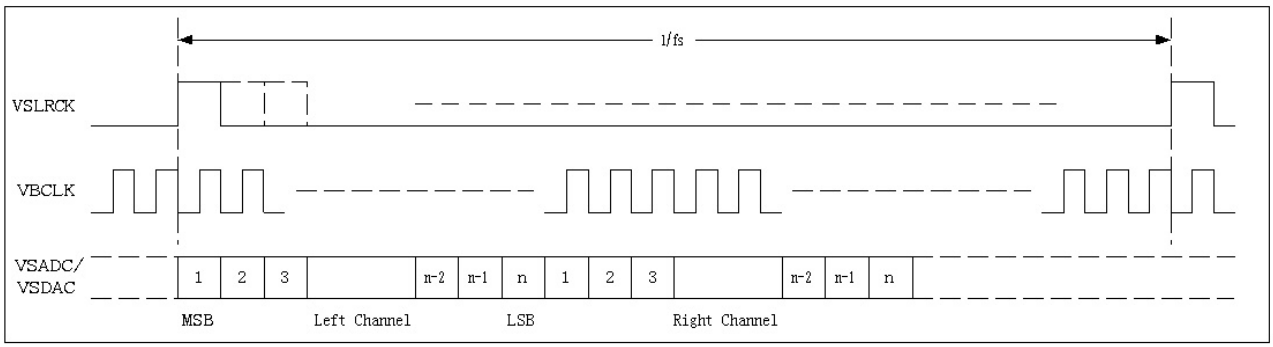


Figure 9. PCM Stereo Data Mode B Format (bclk_polarity=0)

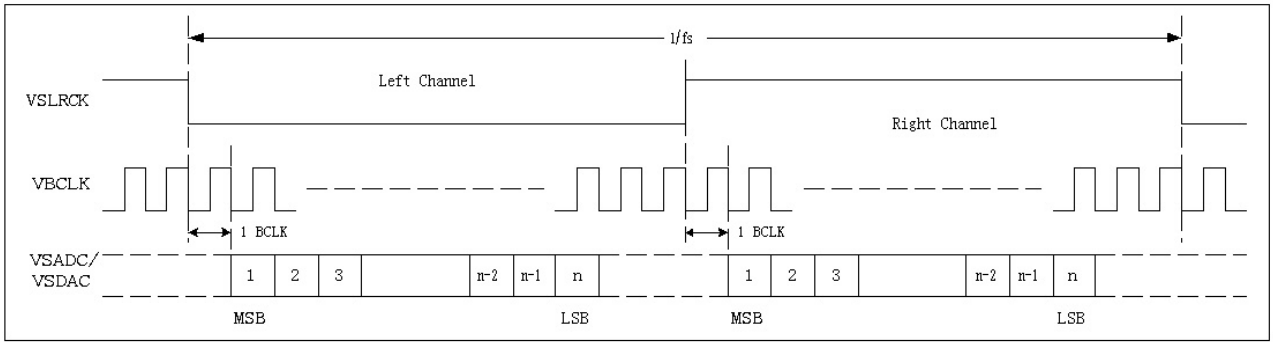


Figure 10. I²S Data Format (bclk_polarity=0)

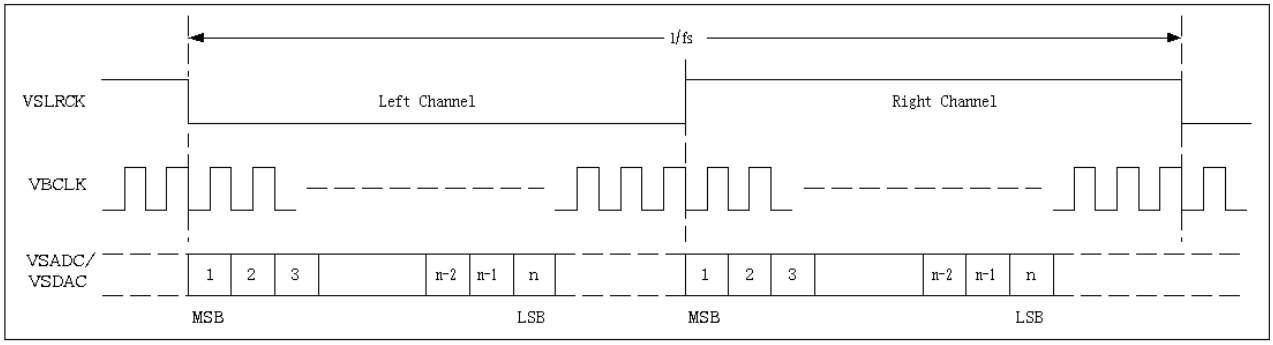


Figure 11. Left-Justified Data Format (bclk_polarity=0)

7.6. Audio Data Path

ALC5625 provides 2 channels Stereo audio DAC for playback, 1 channel Mono DAC for Voice and 2 channels ADC for record. It is suggest that Voice_AD/DA have the same clock source as Main_AD/DA in order to reach best performance.

7.6.1. Stereo ADC and Voice ADC

The stereo ADC is used for recording stereo sound or, by setting **adcr_function_sel** = 01'b, can be configured to mono Main_ADC (Left channel of stereo ADC) + mono Voice_ADC (Right channel of stereo ADC) when using bluetooth and recording at the same time.

- When adcr_function_sel = 00'b and adcl_function_sel=0'b, the sample rate of the stereo ADC can be configured via setting Reg60 & Reg62.
- When adcr_function_sel = 01'b and adcl_function_sel=0', the sample rate of the voice ADC is set by Reg64, and the sample rate of the MONO PCM ADC is set by Reg60 & Reg62.

The sample rate of the stereo ADC is independent of the stereo DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting **pow_adc_l** and **pow_adc_r**

The volume control of the stereo ADC is set via **adc_l_vol** and **adc_r_vol**

7.6.2. Stereo DAC

The stereo DAC can be configured to different sample rate by setting the stereo I^2S clock divider (Reg60).

dac2hp_mute, **dac2spk_mute** and **dac2MONO_mute** can be used to mute the output of Stereo to each Mixer. **dac_l_vol** and **dac_r_vol** can be used to control the volume of DAC output

pow_dac_l can be enabled Left channel of DAC whilt **pow_dac_r** can be enabled Right channel of DAC, Furthermore.

7.6.3. Voice to Stereo Digital Path

The ALC5625 supports a voice to digital stereo path for voice command through Bluetooth by setting **record_source_sel**=01'b. The Voice data will be transferred from the voice I^2S/PCM to the Main I^2S/PCM directly. This function is only supported when both Voice I^2S/PCM and Stereo I^2S/PCM are in Master Mode. The driver should set the same sample rate between the Voice DAC and the Stereo ADC.

When a voice to stereo digital path is enabled, the signal from Voice_I^2S/PCM is direct output to Left frame and is duplicated to Right frame of the Stereo I^2S/PCM interface.

The Voice to Stereo Digital Path and Voice ADC functions can exist at the same time.

7.6.4. Voice DAC

The Voice DAC is dedicated for playback of received voice signals from the voice_I^2S/PCM interface. Typically, it is used at an 8kHz sample rate.

In Voice I^2S/PCM Master mode, the sample rate is set by the VoDAC clock Divider (Reg64). In addition, **Reg64[7:4][3:1]** is used to set the over-sample rate clock divider of the Voice ADC/DAC filter to 128Fs or 64Fs. **Reg64[0]** must be set according to the over-sample rate clock.

Performance at 128Fs is better than 64Fs, but with higher power consumption. The higher frequency will cause better performance. **.** Besides, the frequency of the Voice DAC Sigma Delta clock must be equal to, or higher than the Voice DA filter over-sampling rate.

The volume control of the Voice DAC is set via **voice_vol.**

7.7. Mixers

The ALC5625 supports four mixers for all audio function requirements:

- Headphone mixer for 2 channels
- MONO mixer

- Speaker mixer
- ADC record mixer

7.7.1. Headphone Mixer

The Headphone mixer is used to drive stereo output, including HP_OUT_L/R, SPK_OUT(SPK_OUTN) and AUX_OUT (AUX_OUTN). In addition, the output of the Headphone mixer can be input to the ADC record mixer.

The following signals can be mixed into the headphone mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- Voice DAC output (Controlled by Reg18)
- ADC record mixer output (Controlled by Reg12 & Reg14).

*Note: The Headphone mixer can be powered down by setting **pow_hp_l_mix** and **pow_hp_r_mix**.*

7.7.2. MONO Mixer

The MONO mixer is used to drive AUX_OUT (AUX_OUTN) and SPK_OUT (SPK_OUTN). The output of the MONO mixer can be input to the ADC record mixer. The output of the MONO mixer is two channels with the same signal.

The following signals can be mixed into the MONO mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- Voice DAC output (Controlled by Reg18)
- ADC record mixer output (Controlled by Reg12 & Reg14).

*Note: The MONO mixer can be powered down by setting **pow_mono_mix**.*

7.7.3. Speaker Mixer

The speaker mixer is the same as the MONO mixer and is used to drive AUX_OUT(AUX_OUTN) and SPK_OUT (SPK_OUTN). The output of the speaker mixer can be input to ADC record mixer. The output of the Speaker mixer is two channels with the same signal.

The following signals can be mixed into the Speaker mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- Voice DAC output (Controlled by Reg18)

*Note: The Speaker mixer can be powered down by setting **pow_spk_mix**.*

7.7.4. ADC Record Mixer

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. Output of the ADC record mixer can be input to the headphone mixer, MONO mixer, and Speaker mixer.

The following signals can be mixed into the ADC record mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- PHONEP/N (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Headphone mixer output
- MONO mixer output
- Speaker mixer output

*Note: The ADC record mixer can be powered down by setting **pow_adc_rec_l** and **pow_adc_rec_r.***

7.8. Analog Audio Input Path

The ALC5625 supports four Analog Audio Input paths:

- LINE_IN_L/R

- PHONEP/N
- MIC1P/N
- MIC2P/N

7.8.1. Line Input

LINE_IN_L and LINE_IN_R provide 2-channel stereo single-ended input that can be mixed into the MONO mixer, Headphone mixer, Speaker mixer, or the ADC record mixer.

The LINE_IN_L/R volume and mute are controlled by Reg0A. **pow_li_l_vol** and **pow_li_r_vol** can be used to power down the LINE_IN volume control.

7.8.2. Phone Input

PHONEP/N provides one-channel MONO differential or single-ended input configured by **phone_diff_ctrl** that can be mixed into the ADC record mixer, or any analog output mixer except MONO mixer. PHONEP is main input when differential mode is disabled.

The PHONEP/N volume and mute are controlled by Reg08.

pow_phone_vol and **pow_phone_admixer** can be used to power down PHONEP/N volume control and mixer.

7.8.3. Microphone Input

MIC1P/N and MIC2P/N provide two-channel stereo differential or single-ended input via **mic1_diff_ctrl** and **mic2_diff_ctrl**, that can be mixed into the ADC record mixer, or any analog output mixer. MIC1P and MIC2P are main inputs when differential mode is disabled.

The ALC5625 Microphone input provides 20/30/40dB boost, set by **mic1_boost_ctrl** and **mic2_boost_ctrl.** The MIC1/2 volume and mute are controlled by Reg0E.

For detailed power management of MIC1/2, **pow_mic1_vol** and **pow_mic2_vol** can be used to power down the MIC1/2 volume control. **pow_mic2_boost** and **pow_mic2_boost** can be used to power down boost of MIC1 and MIC2.

7.9. Analog Audio Output Data Path

The ALC5625 supports three Analog Audio output paths:

- SPK_OUT_L/R
- HP_OUT_L/R
- AUX_OUT

7.9.1. Speaker Output

SPK_OUT provides one channel differential output.

The volume source of SPK_OUT_P/N can be select from **spk_vol_in_sel** as below.

- Vmid
- Headphone mixer
- Speaker mixer
- Mono mixer

The path SPK_OUTN can be select from **spk_outn_source** as below

- RN (Speaker Right Volume output N-side)
- RP (Speaker Right Volume output P-side)
- LN (Speaker Left Volume output N-side)

The Speaker out of ALC5625 supports ClassAB and Class D type amplifier and can be select at **spk_out_type_sel.** Owing to the power of voltage of SPKVDD is usually higher than AVDD, ALC5625 have to set Class AB/D Vmid ratio at **spk_amp_ctrl** in order to extend the output level.

The SPK_OUT volume and mute are controlled by Reg02. Besides, **pow_spk_l_vol** and **pow_spk_r_vol** can be used to power down SPK volume output

SPK_OUT supports zero corss detect function which can be enable at **spk_dezero.**

7.9.2. Headphone Output

HP_OUT_L/R provides two-channel single-ended output. And the source of HP_OUT_L/R can be select from **hp_l_in_sel** and **hp_r_in_sel.** Sources are shown below:

- Vmid
- Headphone mixer

In addition, ALC5625 support Direct HP_Out for providing better performance of playback. DAC output

can be direct output to HP_OUT_L/R be setting **dac_l_to_hp** and **dac_l_to_hp.**

The HP_OUT_L/R volume and mute are controlled by Reg04.

pow_hp_l_vol and **pow_hp_r_vol** can be used to power down the volume of HP output.

HP_OUT supports the zero-cross detect function which can be enabled by **hp_l_dezero** and **hp_r_dezero**.

7.9.3. AUX Output

AUX_OUT provide one-channel differential or two-channel single-ended output configured by **se_diff_auxout.** The AUX_OUT source is set in **aux_in_sel**. Sources of AUX_OUT are shown as below:

- Vmid
- Headphone mixer :
- Speaker mixer
- MONO mixer

If signal source of AUX_OUT is from Headphone mixer (**aux_in_sel=01'b**) and AUX_OUT is set to differential output (se_diff_auxout=0'b), the output of AUX_OUT will be HP Left mixer output signal + HP Right mixer output signal and the AUX_OUTN will be inverter of HP Left mixer output signal + HP Right mixer output signal.

If signal source of AUX_OUT is from Headphone mixer (**aux_in_sel=01'b**) and AUX_OUT is set to single-ended output (se_diff_auxout=1'b), AUX_OUT will be HP Left mixer output signal and AUX_OUT_N will be HP Right mixer output signal

The AUX_OUT volume and mute are controlled by Reg06. In addition, **pow_aux_out_vol** can be used to power down the volume of AUX_OUT.

AUX_OUT supports the zero-cross detect function which can be enable at **aux_l_dezero** and **aux_r_dezero.**

7.10. AVC Control

ALC5625 supports independent Automatic Volume Control (AVC) for both ADC (**avc_adc_en**) and DAC (**avc_dac_en**). The AVC function dynamically adjusts the input signal quantized by ADC and DAC to an expected sound level by setting Thmax, THmin and Thnonact.

When the average level of input signal quantized by ADC and DAC is higher than the THmax, AVC will decrease the selected analog gain to attenuate the quantized PCM has lower amplitude than THmax.

When the average level of input signal quantized by ADC and DAC is lower than the THmin, the AVC will increase the selected analog gain to amplify the input signal its quantized PCM by ADC and DAC will higher than THmin. The quantized PCM has average level between THmin and THmax.

In order not to output big amplified signal while input level of gain detector is transit from very small signal to normal signal, the DAC_AVC block can be set to keep pervious gain or limit the selected analog gain to unit gain (=0dB) by setting **avc_dac_gain_action** and **avc_adc_gain_action** when input level of gain detector is lower than THnonact.

The Architecture of ADC_AVC and DAC_AVC is shown as below.

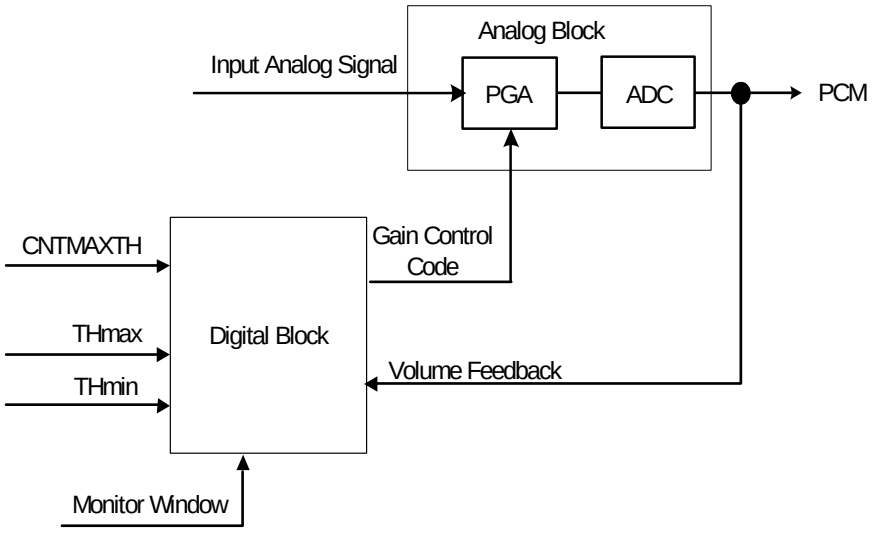


Figure 12. Auto Volume Control Block Diagram

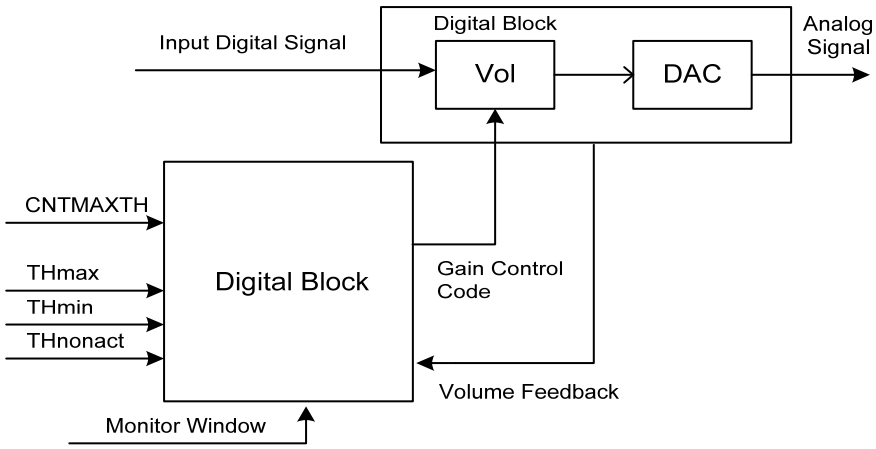


Figure 13. AVC Block of DAC Module

7.11. Hardware Sound Effects

The Sound Effect block is composed of Pseudo Stereo, Spatial 3D, and Equalizer blocks. The Pseudo Stereo block is used to convert a MONO source into virtualized stereo output. The Spatial 3D block is a surround sound generator with adjustable amplitude (Gain) and surround depth (Ratio). The Equalizer block can be used to compensate for speaker response, or to make environment sound effects, e.g., 'Pub', 'Live', 'Rock',… etc..

7.11.1. Equalizer Block

The Equalizer block cascades 5 bands of equalizer to compensate for speaker response and to emulate environment sound. One high-pass filter cascaded in the front end is used to drop low frequency tone, which has a larger amplitude and may damage a mini speaker.

The high-pass filter can also be used to adjust Treble strength with gain control. A low-pass filter with gain control can adjust the Bass strength. Three bands of bi-quad bandpass filters are used to emulate environment sounds.

To avoid PCM sample saturation, the digital volume control has up to 18dB of attenuation before the equalizer. A 0~+18dB digital gain after the equalizer is used to correct PCM output to a suitable level.

7.11.2. Pseudo Stereo and Spatial 3D Sound

There are two spatial effects in post-processing; the Pseudo-Stereo Effect + Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect converts a MONO signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhancing the spatial effect. The Stereo Expansion Effect enhances the spatial effect when the input signal is Stereo.

7.12. Voice DSP Engine

ALC5625 implemented a voice processor includes a high performance and low power DSP (Digital Signal Processor) that comes with a hardware accelerator, an internal ROM and a RAM. The Voice DSP Engine supports Acoustic Echo Cancellation (AEC) and BrightVoice™ signal processing technology.

1.2V-LDO have to be enabled by setting **ldo_en** = 1'b and **pow_main_bias** = 1'b in order to provide core power to Voice DSP Engine. In addition, internal interface have to be enable by setting **pow_src_vodspif** = 1'b, **pow_i2c_vodsp** = 1'b and **i2s_module_en** =1'b. After 1.2V-LDO and internal interface built, Voice DSP Engine can be communicated by read/write to Reg-70, Reg-72 and Reg74.

PDM interface is used as Near End input of Voice DSP Engine which output from ADCR of Audio CODEC. Reg1A and Reg2E are used to select the internal path for AEC and BrightVoice feature. For the detail register setting of Voice DSP Engine, please refer to ALC5625 Application Note.

7.12.1. Acoustic Echo Cancellation

ALC5625 implemented a voice processor includes a high performance and low power DSP (Digital Signal Processor) that comes with a hardware accelerator, an internal ROM and a RAM. The new BrightVoice™ signal processing technology enhances the playback intelligibility by monitoring the ambient noise and enhancing the speaker output.

RxDP of Voice DSP Engine is used to input reference signal of echo from Audio CODEC while TxDP of Voice DSP Engine is used to output acoustic echo cancelled signal from Voice DSP Engine to Audio CODEC. RxDP and TxDP supports 8KHz or 16KHz sample rate which have to be set according to Far End samle rate of application, The performance of 16KHz sample rate is better than 8KHz.

Figure 14 and Figure 15 are two AEC examples that can be supported by ALC5625.

In Figure 14, Far End signal is input from Voice interface and Near End signal is input from MIC1/MIC2. The echo path is: Speaker **è** MIC1/MIC2 and echo cancelled signal is output to Voice interface. This scheme is used on Bluetooth and mobile phone application.

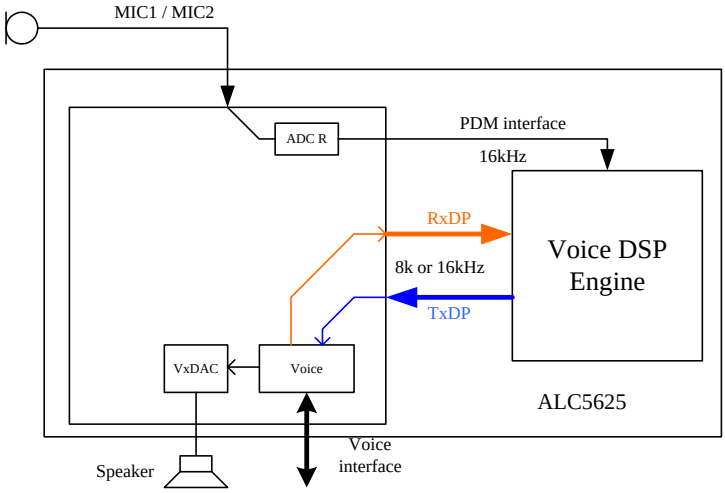


Figure 14 AEC scheme 1 (Far End signal is from Voice interface and Near End signal is from MIC1/MIC2)

In Figure 15, Far End signal is input from from SDAC of I2S (Playback) and Near End signal is input from MIC1/MIC2. The echo path is: Speaker è MIC1/MIC2 and echo cancelled signal is output to SADC of I2S (Recording). This scheme is used on Voice commanding while playback.

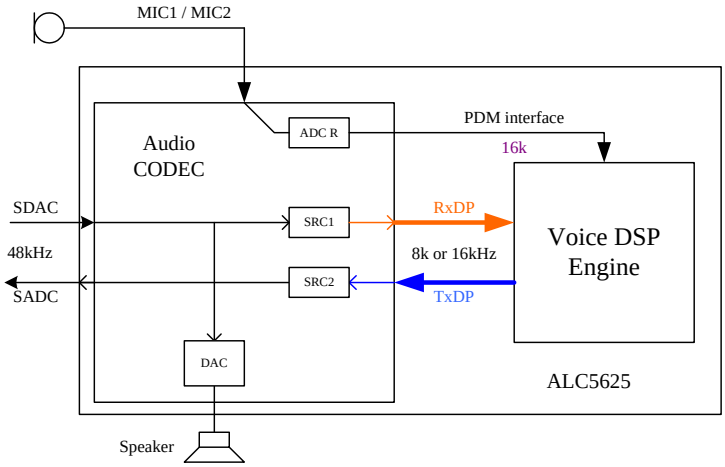


Figure 15 AEC scheme 2 (Far End signal is from Playback and Near End signal is from MIC1/MIC2)

7.12.2. BrightVoice (BVE)

BrightVoice™ signal processing technology enhances the playback intelligibility by monitoring the ambient noise and enhancing the speaker output. When this feature is enabled, BVE actively monitors local background ambient noise levels of 5 individual frequency bands, refer to Table 9. Then apply different output IIR gains filter to each band based on noise level. The gain can range from -23.5dB ~ +24 dB.

Table 9: The Frequency of 5 Bands Used in Bright Voice Engine

Sampling Rate	Band A	Band B	Band C	Band D	Band E
8 kHz	100~160 Hz	245~365 Hz	545~810 Hz	1210~1800 Hz	2690~4000 Hz
16 kHz	100~160 Hz	245~365 Hz	545~810 Hz	1210~1800 Hz	2690~8000 Hz

RxDP of Voice DSP Engine is used to input reference signal of echo from Audio CODEC while TxDC of Voice DSP Engine is used to output BrightVoice signal from Voice DSP Engine to Audio CODEC. In addition, AEC and BVE can be enabled at the same time.

Figure 16, Figure 17 and Figure 18 are 3 examples of AEC + BVE that can be supported by ALC5625

In Figure 16, Far End signal is input from Voice interface and Near End signal is input from MIC1/MIC2. The echo path is: Speaker **è** MIC1/MIC2. The echo cancelled signal is output to Voice interface and BVE processed signal is output to Speaker. This scheme is used on Bluetooth and mobile phone application.

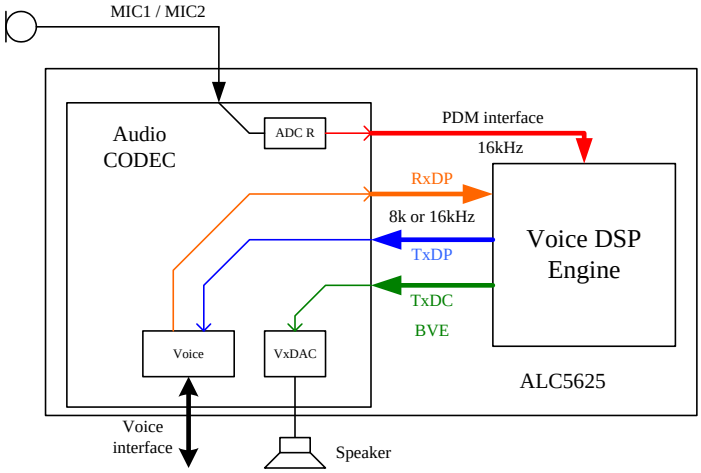


Figure 16 AEC+BVE scheme 1 (Far End signal is from Voice interface and Near End signal is from MIC1/MIC2)

In Figure 17, Far End signal is input from PHONE_IN and Near End signal is input from MIC1/MIC2. The echo path is: Speaker è MIC1/MIC2. The echo cancelled signal is output to AUXOUT and BVE processed signal is output to Speaker. This scheme is used on mobile phone application.

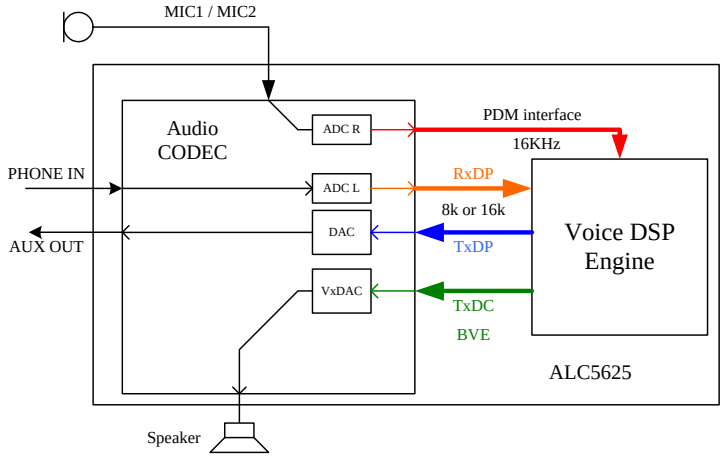


Figure 17 AEC+BVE scheme 2 (Far End signal is from PHONEIN and Near End signal is from MIC1/MIC2)

In Figure 18 , Far End signal is input from SDAC of I2S (Playback) and Near End signal is input from MIC1/MIC2. The echo path is: Speaker è MIC1/MIC2. The echo cancelled signal is output to SADC of I2S (Recording) and BVE processed signal is output to Speaker. This scheme is used on Voice commanding while playback.

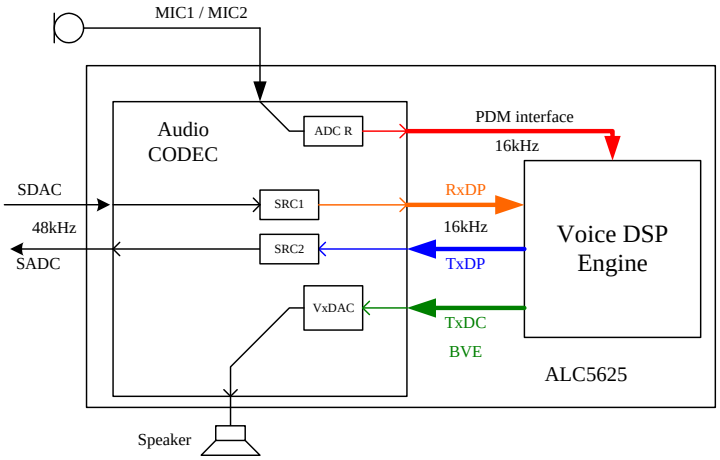


Figure 18 AEC+BVE scheme 3 (Far End signal is from Playback and Near End signal is from MIC1/MIC2)

7.13. GPIO and Interrupt

The ALC5625 supports up to five GPIOs. Each GPIO can be configured as Input/Output by Reg4C. When GPIOs are configured as Input, the status will be indicated in Reg54. When GPIOs are configured as Output, Reg5C is used to drive GPIOs to High (1b) or Low (0b). The status can be read in Reg54.

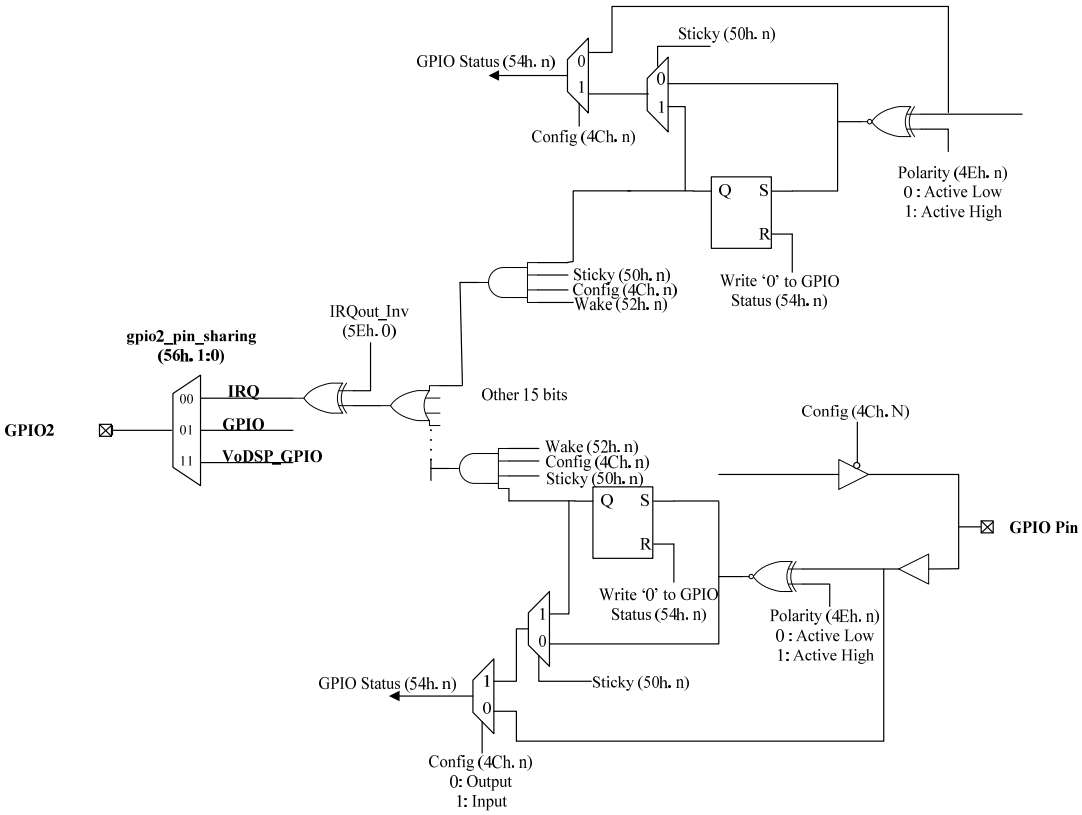
GPIO and Interrupt request (IRQ) can be configured as:

- Sticky by setting Reg50
- Changed polarity by setting Reg4E
- Wake-up by setting Reg52

The driver can write each bit of Reg54=1 to clear each IRQ status flag.

When **VoPCM_En** =1, GPIOs 1, 3, 4, and 5 will be dedicated as VoDAC_I^{2}S/PCM interface, regardless of GPIO Pin Configuration (Reg4C[5:3,1]). These pins cannot be used as GPIOs in this case.

GPIO pin2 can be configured and pin-shared with IRQ_Output by setting Reg56.



Independent to GPIO, there are some Internal Event Signals (MICBIAS short detect..) which the same as GPIO input and can be treat as Interrupts source. The application of Internal Event Signal is the same as GPIO and located in Reg4C, Reg4E, Reg 50, Reg 52 and Reg 54.

7.14. Headphone Depop

The ALC5625 provides a headphone depop mechanism in order to eliminate the pop noise of headphone out. An external 1µF Capacitor is required in this application. Refer to the ALC5625 Application Note for details.

7.15. I²C Control Interface

I²C is a 2-wires half-duplex serial communication interface, supporting only slave mode. The host must support MCLK during register access.

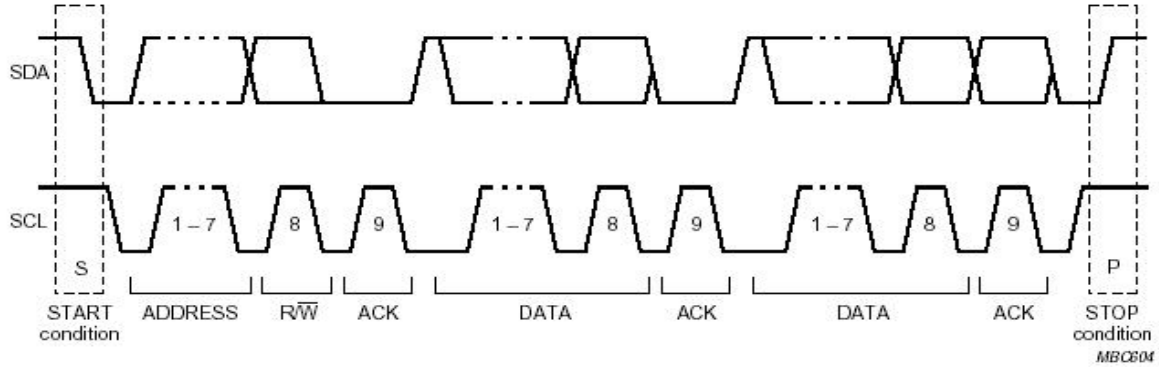
7.15.1. Addressing setting:

(MSB)			BIT				(LSB)
0	0	1	1	1	1	A1	R/W

Note: For A1: determined by directly connect to VDD or GND

7.15.2. Complete Data Transfer

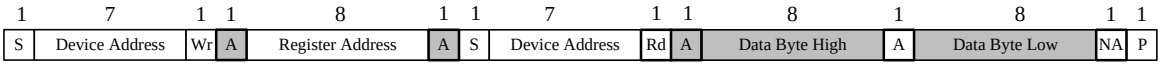
Data transfer over I2C control interface:



Write WORD Protocol:

1	7	1	1	8	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	Data Byte High	A	Data Byte Low	A	P

Read WORD Protocol:



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Mixer Address
A: 0 FOR ACK, 1 FOR NACK
Data Byte: 16-bit Mixer data
£ :Master-to-Slave
£ :Slave-to-Master

7.16. Odd Addressed Register Access

ALC5625 will return “0000h” when those odd-addressed registers and unimplemented registers are read.

8. Mixer Registers List

Accessing odd numbered registers, or reading unimplemented registers, will return with 0.

8.1. Reg-00h: Reset

Default: 59B4h

Table 10. Reg-00h: Reset

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved, read as 0
REG-00_b14_b10	14:10	R	16'h	SE[4:0]=10110b. (Support Realtek HW 3D)
REG-00_b9	9	R	0'h	Not support 20-bit ADC
REG-00_b8	8	R	1'h	Support 16-bit ADC
REG-00_b7	7	R	1'h	Support 16-bit DAC
REG-00_b6	6	R	0'h	Not support 18-bit DAC
REG-00_b5	5	R	1'h	Support for SPK_AMP
REG-00_b4	4	R	1'h	Headphone output support
Reserved	3	R	0'h	Not simulated stereo, for analog 3D block use
REG-00_b2	2	R	1'h	Support EQ
Reserved	1:0	R	0'h	Reserved, read as 0

Note: Writes to this register will reset all registers to their default values except PLL related Register. The written data will be ignored

8.2. Reg-02h: Speaker Output Volume

Default: 8080h

Table 11. Reg-02h: Speaker Output Volume

Name	Bits	Read/Write	Reset State	Description
spk_mute_l	15	R/W	1'h	Speak mute control 0: On 1: Mute (-∞dB)
spk_dezero	14	R/W	0'h	Speaker zero cross detector control 0: Disable 1: Enable
Reserved	13	R	0'h	Reserved
spk_vol_l	12:8	R/W	0'h	Speak Output Volume (SPKV) in 1.5dB step
spk_mute_r	7	R/W	1'h	Speak mute control 0: On 1: Mute (-∞dB) Note: no use when spk_outn_source = 1x'b
Reserved	6:5	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
spk_vol_r	4:0	R/W	0'h	Speak Output Volume in 1.5dB step Note: no use when spk_outn_source = 1x'b

Note: For SPKV, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.3. Reg-04h: Headphone Output Volume

Default: 8080h

Table 12. Reg-04h: Headphone Output Volume

Name	Bits	Read/Write	Reset State	Description
hp_l_mute	15	RW	1'h	Mute HP Left Control 0: On 1: Mute Left Channel (-∞dB)
hp_l_dezero	14	RW	0'h	HP Left Zero-Cross Detector Control 0: Disable 1: Enable
Reserved	13	R	0'h	Reserved. Read as 0
hp_l_vol	12:8	RW	0'h	Headphone Output Left Volume (HPLV) in 1.5dB Steps
hp_r_mute	7	RW	1'h	Mute HP Right Control 0: On 1: Mute Right Channel (-∞dB)
hp_r_dezero	6	RW	0'h	HP Right Zero-Cross Detector Control 0: Disable 1: Enable
Reserved	5	R	0'h	Reserved. Read as 0
hp_r_vol	4:0	RW	0'h	Headphone Output Right Volume (HPRV) in 1.5dB Steps

Note: For HPRV/HPLV, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.4. Reg-06h: AUXOUT Volume

Default: 8080h

Table 13. Reg-06h: AUXOUT Volume

Name	Bits	Read/Write	Reset State	Description
auxo_l_mute	15	R/W	1'h	AUXOUT Left Mute Control 0: On 1: Mute
auxo_l_dezero	14	R/W	0'h	AUXOUT Left zero cross detector control 0: Disable 1: Enable
Reserved	13	R	0'h	Reserved
auxo_l_vol	12:8	R/W	0'h	AUX Output Left Volume (AUXLV) in 1.5dB step
auxo_r_mute	7	R/W	1'h	AUXOUT Right Mute Control 0: On 1: Mute Note: no use when differential mode (Reg1C[4])
auxo_r_dezero	6	R/W	0'h	AUXOUT Right zero cross detector control 0: Disable 1: Enable Note: no use when differential mode (Reg1C[4])

Name	Bits	Read/Write	Reset State	Description
Reserved	5	R	0'h	Reserved
auxo_r_vol	4:0	R/W	0'h	AUX Output Right Volume (AUXRV) in 1.5dB step Note: no use when differential mode (Reg1C[4])

Note: For AUXRV/AUXLV, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.5. Reg-08h: Phone Input

Default: C800h

Table 14. Reg-08h: Phone Input

Name	Bits	Read/Write	Reset State	Description
phone2hp_mute	15	R/W	1'h	Mute Phone Input to Headphone mixer Control 0: On 1: Mute
phone2spk_mute	14	R/W	1'h	Mute Phone Input to Speaker mixer Control 0: On 1: Mute
phone_diff_ctrl	13	R/W	0'h	Phone Differential Input Control 0: Disable 1: Enable
phone_vol	12:8	R/W	08'h	Phone Input Volume (PIV) in 1.5dB step
Reserved	7:0	R	00'h	Reserved

Note: For PIV, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.6. Reg-0Ah: LINE_IN Volume

Default: E808h

Table 15. Reg-0Ah: LINE_IN Volume

Name	Bits	Read/Write	Reset State	Description
li2hp_mute	15	RW	1'h	Mute Volume Output to Headphone Mixer Control 0: On 1: Mute
li2spk_mute	14	RW	1'h	Mute Volume Output to Speaker Mixer Control 0: On 1: Mute
li2mono_mute	13	RW	1'h	Mute Volume Output to MONO Mixer Control 0: On 1: Mute
li_l_vol	12:8	RW	08'h	LINE_IN Left Volume (NILV[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
li_r_vol	4:0	RW	8'h	LINE_IN Right Volume (NIRV[4:0]) in 1.5dB Steps

Note: For NIRV/NILV, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.7. Reg-0Ch: STEREO DAC Input Volume

Default: 1010h

Table 16. Reg-0Ch: STEREO DAC Input Volume

Name	Bits	Read/Write	Reset State	Description
main_dac_l_mute	15	R/W	0'h	Mute Main DAC Left Input 0: On 1: Mute
main_dac_l_dezero	14	R/W	0'h	Main DAC Left channel zero cross detector control 0: Disable 1: Enable
dac_l_vol	13:8	R/W	10'h	DAC Left Volume (DACLV) in 0.75dB step
main_dac_r_mute	7	R/W	0'h	Mute Main DAC Right Input 0: On 1: Mute
main_dac_r_dezero	6	R/W	0'h	Main DAC Right channel zero cross detector control 0: Disable 1: Enable
dac_r_vol	5:0	R/W	10'h	DAC Right Volume (DACRV) in 0.75dB step

Note: For DACRV/DACLV,: 00h: +12dB gain 10h: 0dB attenuation 3Fh: 35.25dB attenuation

8.8. Reg-0Eh: MIC Input Volume

Default: 0808h

Table 17. Reg-0Eh: MIC Input Volume

Name	Bits	Read/Write	Reset State	Description
mic1_diff_ctrl	15	R/W	0'h	MIC1 Differential Input Control 0: Disable 1:Enable
Reserved	14:13	R	0'h	Reserved
mic1_vol	12:8	RW	08'h	MIC1 Volume (M1V[4:0]) in 1.5dB Steps
mic2_diff_ctrl	7	R/W	0'h	MIC2 Differential Input Control 0: Disable 1:Enable
Reserved	6:5	R	0'h	Reserved
mic2_vol	4:0	RW	8'h	MIC2 Volume (M2V[4:0]) in 1.5dB Steps

For M2V/M1V, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.9. Reg-10h: Stereo DAC and MIC Routing Control

Default: EE0Fh

Table 18. Reg-10h: Stereo DAC and MIC Routing Control

Name	Bits	Read/Write	Reset State	Description
mic12hp_mute	15	RW	1'h	Mute MIC1 Volume Output to Headphone Mixer 0: On 1: Mute

Name	Bits	Read/Write	Reset State	Description
mic12spk_mute	14	RW	1'h	Mute MIC1 Volume Output to Speaker Mixer 0: On 1: Mute
mic12mono_mute	13	RW	1'h	Mute MIC1 Volume Output to MONO Mixer 0: On 1: Mute
Reserved	12	R	0'h	Reserved
mic22hp_mute	11	RW	1'h	Mute MIC2 Volume Output to Headphone Mixer 0: On 1: Mute
mic22spk_mute	10	RW	1'h	Mute MIC2 Volume Output to Speaker Mixer 0: On 1: Mute
mic22mono_mute	9	RW	1'h	Mute MIC2 Volume Output to MONO Mixer 0: On 1: Mute
Reserved	8:4	R	0'h	Reserved
dacl2hp_mute	3	R/W	1'h	Mute DAC Left Volume Out to Headphone L mixer Control 0: On 1: Mute
dacr2hp_mute	2	R/W	1'h	Mute DAC Right Volume Out to Headphone R mixer Control 0: On 1: Mute
dac2spk_mute	1	R/W	1'h	Mute DAC Left Volume Out to Speaker mixer Control 0: On 1: Mute
dac2mono_mute	0	R/W	1'h	Mute DAC Left Volume Out to Mono mixer Control 0: On 1: Mute

8.10. Reg-12h: ADC Record Gain

Default: CBCBh

Table 19. Reg-12h: ADC Record Gain

Name	Bits	Read/Write	Reset State	Description
adc2hp_l_mute	15	R/W	1'h	Mute ADC Left Gain Output to headphone mixer Control 0: On 1: Mute
adc2mono_l_mute	14	R/W	1'h	Mute ADC Left Gain Output to mono mixer Control 0: On 1: Mute
adc_l_dezero	13	R/W	0'h	ADC Left Zero cross detector Control 0: Disable 1: Enable
adc_l_vol	12:8	R/W	0B'h	ADC Left Channel Record Gain in 1.5dB Step 00'h: -16.5dB attenuation 0B'h: 0dB gain 1F'h: 30dB gain
adc2hp_r_mute	7	R/W	1'h	Mute ADC Right Gain Output to headphone mixer Control 0: On 1: Mute
adc2mono_r_mute	6	R/W	1'h	Mute ADC Right Gain Output to mono mixer Control 0: On 1: Mute
adc_r_dezero	5	R/W	0'h	ADC Right Zero cross detector Control 0: Disable 1: Enable

Name	Bits	Read/Write	Reset State	Description
adc_r_vol	4:0	R/W	0B'h	ADC Right Channel Record Gain in 1.5dB Step 00'h: -16.5dB attenuation 0B'h: 0dB gain 1F'h: 30dB gain

8.11. Reg-14h: ADC Record Mixer Control

Default: 7F7Fh

Table 20. Reg-14h: ADC Record Mixer Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
adcrec_l_mute	14:8	RW	7F'h	Left Mixer Mute Control 0: On 1: Mute (-∞dB) Bit 14: MIC1 Bit 13: MIC2 Bit 12: LINE_IN_L Bit 11: PHONE Bit 10: Headphone Mixer Left Channel Bit 9: Speaker Mixer Bit 8: MONO Mixer
Reserved	7	R	0'h	Reserved
adcrec_r_mute	6:0	RW	7F'h	Right Mixer Mute Control 0: On 1: Mute (-∞dB) Bit 6: MIC1 Bit 5: MIC2 Bit 4: LINE_IN_R Bit 3: PHONE Bit 2: Headphone Mixer Right Channel Bit 1: Speaker Mixer Bit 0: MONO Mixer

8.12. Reg-18h: Voice DAC Volume

Default: E010h

Table 21. Reg-18h: Voice DAC Volume

Name	Bits	Read/Write	Reset State	Description
voice2hp_mute	15	R/W	1'h	Mute Voice DAC Volume Out to headphone mixer Control 0: On 1: Mute
voice2spk_mute	14	R/W	1'h	Mute Voice DAC Volume Out to speaker mixer Control 0: On 1: Mute
voice2mono_mute	13	R/W	1'h	Mute Voice DAC Volume Out to mono mixer Control 0: On 1: Mute
voice_dac_mute	12	R/W	0'h	Mute Voice DAC 0: On 1: Mute
Reserved	11:7	R	00'h	Reserved
voice_dac_dezero	6	R/W	0'h	Voice DAC zero cross detector control 0: Disable 1: Enable
voice_vol	5:0	RW	10'h	VoDAC Output Volume (VV) in 0.75dB Steps

Note: For VV, 00h: +12dB gain 10h: 0dB attenuation 3Fh: 35.25dB attenuation

8.13. Reg-1Ah: VoDSP & PDM Control

Default: 0000h

Table 22. Reg-1Ah: VoDSP Control

Name	Bits	Read/Write	Reset State	Description
src1_pow	15	R/W	0'h	SRC1 (48K to 16K) Power 0: Disable 1: Enable
Reserved	14	R	0'h	Reserved
src2_pow	13	R/W	0'h	SRC2 (16K to 48K) Power 0: Disable 1: Enable
src2_source_sel	12	R/W	0'h	SRC2 (16K to 48K) Source Select 0'b: VoDSP_TxDP 1'b: VoDSP_TxDC
vodsp_rxdp_pow	11	R/W	0'h	VoDSP RxDP Power 0: Disable 1: Enable
vodsp_rxdp_source_sel	10:9	R/W	0'h	VoDSP_RxDP Source Select 00'b: SRC1 Output 01'b: ADC Left to VoDSP Digital Path 10'b: Voice to Stereo Digital Path 11'b: ADC Right to VoDSP Digital Path
vodsp_rxdc_pow	8	R/W	0'h	VoDSP_RxDC Power 0'b: Disable 1'b: Enable
vsadc_pcm	7	R/W	0'h	VSADC PCM Interface Source Select 0: ADC R 1: VoDSP_TxDP
Reserved	6	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
record_source_sel	5:4	R/W	0'h	Main Stereo Record I2S Source Select 00'b: ADC L / ADC R 01'b: Voice to Stereo Digital Path 10'b: SRC2 Out 11'b: Reserved
Reserved	3:1	R	0'h	Reserved
pdm_edge	0	R/W	0'h	PDM latch edge 0: Rising edge 1: Falling edge

8.14. Reg-1Ch: Output Mixer Control

Default: 8008h

Table 23. Reg-1Ch: Output Mixer Control

Name	Bits	Read/Write	Reset State	Description
spk_outn_source	15:14	R/W	2'h	Speaker Out N Source Select from HP Mixer (include Class AB & Class D) 00: RN 01: RP 10: LN 11: Mute Note: SPK Out is dedicated for LP Note:spk_outn_source function only work when spk_vol_in_sel = 01'b
spk_out_type_sel	13	R/W	0'h	SPK Output Type Select 0: Class AB 1: Class D
clsab_amp_sel	12	R/W	0'h	Class AB Output Amplifier Select 0: Strong Amp 1: Weak Amp
spk_vol_in_sel	11:10	R/W	0'h	SPK Volume Input Select 00'b: VMID (No input) 01'b: HP Mixer 10'b: SPK Mixer (differential out) 11'b: Mono Mixer (differential out)
hp_l_in_sel	9	R/W	0'h	HP Left Volume Input Select 0: VMID (No input) 1: HP Left Mixer
hp_r_in_sel	8	R/W	0'h	HP Right Volume Input Select 0: VMID (No input) 1: HP Right Mixer
aux_in_sel	7:6	R/W	0'h	AUX Volume Input Select 00'b: VMID (No input) 01'b: HP Left + Right Mixer 10'b: SPK Mixer 11'b: Mono Mixer

Name	Bits	Read/Write	Reset State	Description
Reserved	5	R	0'h	Reserved
se_diff_auxout	4	R/W	0'h	Single End & Differential of AUXOUT Select 0: Differential Mode (AUX_OUT P/N) 1: Single End Mode (AUX_OUT L/R)
en_spk_vol_diff	3	R/W	1'h	Speaker volume N-side OP power 0: Disable 1: Enable
se_btl_clsab	2	R/W	0'h	Single End & BTL of Class AB Amplifier Select 0: Differential Mode 1: Single End Mode
dac_l_to_hp	1	R/W	0'h	DAC Left Volume Output to HP Left Amplifier 0: Mute (Normal Path) 1: On (DAC L Direct Path)
dac_r_to_hp	0	R/W	0'h	DAC Right Volume Output to HP Right Amplifier 0: Mute (Normal Path) 1: On (DAC R Direct Path)

8.15. Reg-1Eh: VoDSP Control

Default: 2007h

Table 24. Reg-1Eh: VoDSP Control

Name	Bits	Read/Write	Reset State	Description
vodsp_sysclk_source_sel	15	R/W	0'h	VoDSP SYSCLK Source Select 0'b: Main SYSCLK 1'b: Voice SYSCLK
vodsp_lrck_sel	14:13	R/W	1'h	VoDSP LRCK Select 00: 8KHz (VoDSP SYSCLK=24.576MHz) 01: 16KHz (VoDSP SYSCLK=24.576MHz) 1x: (VoDSP SYSCLK=512*Fs_{VoDSP})
Reserved	12:4	R	0'h	Reserved
vodsp_test	3	R/W	0'h	VoDSP TEST Pin Control Output to VoDSP 0'b: normal 1'b: test mode
vodsp_bp	2	R/W	1'h	VoDSP BP Pin Control Output to VoDSP 0'b: bypass mode 1'b: normal
vodsp_pwdn	1	R/W	1'h	VoDSP Power Down Pin Control Output to VoDSP 0'b: power down 1'b: normal
vodsp_reset	0	R/W	1'h	VoDSP Resest Pin Control Output to VoDSP 0'b: reset 1'b: normal

8.16. Reg-22h: Microphone Control

Default: 0000h

Table 25. Reg-22h: Microphone Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0'h	Reserved
mic1_boost_ctrl	11:10	RW	0'h	MIC1 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: +40dB
mic2_boost_ctrl	9:8	RW	0'h	MIC2 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: +40dB
Reserved	7:6	R	0'h	Reserved. Read as 0
mic1_bias_voltage_ctrl	5	RW	0'h	MICBIAS1 Output Voltage Control 0: 0.9 * AVDD 1: 0.75 * AVDD
mic2_bias_voltage_ctrl	4	RW	0'h	MICBIAS2 Output Voltage Control 0: 0.9 * AVDD 1: 0.75 * AVDD
Reserved	2:3	R	0'h	Reserved. Read as 0
mic_bias_threshold	1:0	RW	0'h	MICBIAS1/2 Short Current Detector Threshold 00: 600µA 01: 1500µA 1x: 2000µA

8.17. Reg-24h: Digital Boost Control

Default: 00C0h

Table 26. Reg-24h: Digital Boost Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:3	R	0018'h	Reserved
digital_boost_ctrl	2:0	R/W	0'h	DMIC Boost Control (ADC Digital Boost) 000'b: Bypass 001'b: +6dB 010'b: +12dB 011'b: +18dB 100'b: +24dB 101'b: +30dB 110'b: +36dB 111'b: +42dB

8.18. Reg-26h: Power Down Control/Status

Default: EF00h

Table 27. Reg-26h: Power Down Control/Status

Name	Bits	Read/Write	Reset State	Description
pr7	15	R/W	1'h	PR7 Speaker Amplifier 0: Normal 1: Power Down
pr6	14	R/W	1'h	PR6 HP Out and AUXOUT 0: Normal 1: Power Down
pr5	13	R/W	1'h	PR5 Internal Clock (without PLL1) 0: Normal 1: Power Down
Reserved	12	R/W	0'h	Reserved
pr3	11	R/W	1'h	PR3 Mixer (Vref / Vrefout Off) 0: Normal 1: Power Down
pr2	10	R/W	1'h	PR2 Mixer (Vref / Vrefout are still On) 0: Normal 1: Power Down
pr1	9	R/W	1'h	PR1 Stereo DAC 0: Normal 1: Power Down
pr0	8	R/W	1'h	PR0 Stereo ADC and Input MUX 0: Normal 1: Power Down
Reserved	7:4	R	0'h	Reserved
vref_status	3	R	0'h	Vref Status 0: Not yet 1: Vref is up to Normal Level
analog_mixer_status	2	R	0'h	Analog Mixer Status 0: Not yet 1: Ready
dac_status	1	R	0'h	DAC Power Status 0: Not yet 1: Ready
adc_status	0	R	0'h	ADC Power Status 0: Not yet 1: Ready

Table 28. Truth Table for Power Down Mode (PD=Power Down)

	ADC	DAC	Mixer	Vref	Int CLK	HP-OUT	AUXOUT	SPK-OUT
PR0=1	PD	-	-	-	-	-	-	-
PR1=1	-	PD	-	-	-	-	-	-
PR2=1	-	-	PD	-	-	PD	-	-
PR3=1	PD	PD	PD	PD	-	PD	-	-
PR5=1	PD	PD	-	-	PD	-	-	-
PR6=1	-	-	-	-	-	PD	PD	-
PR7=1	-	-	-	-	-	-	-	PD

8.19. Reg-2Eh: Stereo DAC / Voice DAC / Stereo ADC Function Select

Default: 0000h

Table 29. Reg-2Eh: Stereo DAC / Voice DAC / Stereo ADC Function Select

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R	0'h	Reserved
dac_function_sel	13:12	R/W	0'h	DAC Function Selection 00'b: Stereo DAC (refer to DAC divider in I2S mode) 01'b: SRC2_Out 10'b: VoDSP_TxDP 11'b: VoDSP_TxDC
Reserved	11	R	0'h	Reserved
vodac_source_sel	10:8	R/W	0'h	Voice DAC Source Select 000'b: Voice PCM interface 001'b: SRC2_Out 010'b: VoDSP_TxDP 011'b: VoDSP_TxDC Other: Reserved
Reserved	7:6	R	0'h	Reserved
adcr_function_sel	5:4	R/W	0'h	ADCR Function Selection 00'b: Stereo ADC 01'b: Voice ADC 10'b: VoDSP Interface 11'b: PDM Slave Interface
Reserved	3:1	R	0'h	Reserved
adcl_function_sel	0	R/W	0'h	ADCL Function Select 0: Stereo ADC 1: VoDSP Interface

8.20. Reg-34h: Main Serial Data Port Control (Stereo I^2S)

Default: 8000h

Table 30. Reg-34h: Main Serial Data Port Control (Stereo I^2S)

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_mode_sel	15	R/W	1'h	Main Serial Data Port Mode Select 0: Master 1: Slave

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_sadlrck_ctrl_en	14	R/W	0'h	SADLRCK Control: Set '1' when ADC and DAC are different sampling rate 0: Disable, ADC and DAC use the same Fs 1: Enable Note: frame clock have to input from SDALRCK when this bit set to '0'
Reserved	13:9	R	00'h	Reserved
stereo_i2s_sysclk_sel	8	R/W	0'h	Stereo I2S SYSCLK Source Select 0: Main SYSCLK 1: Voice SYSCLK
stereo_i2s_bclk_polarity_ctrl	7	R/W	0'h	Stereo I2S BCLK Polarity Control 0: Normal 1: Invert
stereo_i2s_lr_inv	6	R/W	0'h	Stereo I2S LRCK Inverter 0: Normal (SADLRCK / SDALRCK) 1: Invert (SADLRCK / SDALRCK) Note: Only support when stereo_i2s_sadlrck_ctrl_en = 1'b0
Reserved	5:4	R	0'h	Reserved
stereo_i2s_data_len_sel	3:2	R/W	0'h	Data Length Select 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
stereo_i2s_data_format_sel	1:0	R/W	0'h	Stereo PCM Data Format Select 00'b: I2S Format 01'b: Left justified 10'b: PCM Mode A 11'b: PCM Mode B

8.21. Reg-36h: Extend Serial Data Port Control (VoDAC_I2S/PCM)

Default: 0000h

Table 31. Reg-36h: Extend Serial Data Port Control (VoDAC_I²S/PCM)

Name	Bits	Read/Write	Reset State	Description
vopcm_en	15	R/W	0'h	Enable Voice I2S / PCM Interface on GPIO 1,3,4,5 0: GPIO function 1: Voice PCM Interface
voice_mode_sel	14	R/W	0'h	Extend Serial Data Mode Select 0: Master 1: Slave
vodac_hpf_clk_ctrl	13	R/W	0'h	HPF auto clock control for BCLK Slave mode 0: Disable 1: Enable
Reserved	12:9	R	0'h	Reserved
voice_i2s_sysclk_sel	8	R/W	0'h	Voice I2S SYSCLK Source Select 0: Main SYSCLK 1: Voice SYSCLK

Name	Bits	Read/Write	Reset State	Description
voice_vbclk_polarity_ctrl	7	R/W	0'h	Voice I2S VBCLK Polarity Control 0: Normal 1: Invert
voice_i2s_lr_inv	6	R/W	0'h	Voice I2S LRCK Inverter 0: Normal VSLRCK 1: Invert VSLRCK
Reserved	5:4	R	0'h	Reserved
voice_data_len_sel	3:2	R/W	0'h	Data Length Select 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
voice_data_format_sel	1:0	R/W	0'h	Stereo PCM Data Format Select 00'b: I2S Format 01'b: Left justified 10'b: PCM Mode A 11'b: PCM Mode B

8.22. Reg-3Ah: Power Management Addition 1

Default: 0000h

Table 32. Reg-3Ah: Power Management Addition 1

Name	Bits	Read/Write	Reset State	Description
pow_dacl2mixer	15	R/W	0'h	Stereo DAC L **channel to mixer** 0: Power Down 1: Power On
pow_dacr2mixer	14	R/W	0'h	Stereo DAC R **channel to mixer** 0: Power Down 1: Power On
pow_zcd	13	R/W	0'h	All Zero Cross Detect Power Down 0: Power Down 1: Power On
Reserved	12	R/W	0'h	Reserved
i2s_module_en	11	R/W	0'h	Main I2S and VoDSP Digital Interface Enable 0: Disable 1: Enable
pow_spk_amp	10	R/W	0'h	Speaker amplifier power (ClassAB / ClassD) 0: Power Down 1: Power On
en_hp_out_amp	9	R/W	0'h	Headphone Output Buffer for Light Loading (K ohm) Used to drive high Impedance 0: Disable 1: Enable

Name	Bits	Read/Write	Reset State	Description
en_hp_enhance_amp	8	R/W	0'h	Headphone Enhance Output Buffer for High Loading (ohm) 0: Disable 1: Enable
pow_voicedac2mixer	7	R/W	0'h	Voice DAC **to mixer** 0: Power Down 1: Power On
pow_softgen	6	R/W	0'h	Softgen power control 0: Disable 1: Enable
pow_mic1_bias_det_ctrl	5	R/W	0'h	MICBIAS1 Short Current Detect Control 0: Disable 1: Enable
pow_mic2_bias_det_ctrl	4	R/W	0'h	MICBIAS2 Short Current Detect Control 0: Disable 1: Enable
pow_mic1_bias	3	R/W	0'h	MICBIAS1 Power 0: Disable 1: Enable
pow_mic2_bias	2	R/W	0'h	MICBIAS2 Power 0: Disable 1: Enable
pow_main_bias	1	R/W	0'h	Main Bias Power 0: Power Down 1: Power On
pow_dac_ref	0	R/W	0'h	DAC reference voltage power 0: Power Down 1: Power On

en_hp_out_amp	en_hp_enhance_amp	Description
0'b	**0'b**	HP output OFF
0'b	**1'b**	No suggest
1'b	**0'b**	HP output for Hi Impendance Loading (>KOhm)
1'b	**1'b**	HP output for Low Impendance Loading (<100Ohm)

8.23. Reg-3Ch: Power Management Addition 2

Default: 0000h

Table 33. Reg-3Ch: Power Management Addition 2

Name	Bits	Read/Write	Reset State	Description
pow_pll1	15	R/W	0'h	Power On PLL1 0: Power Down 1: Power On

Name	Bits	Read/Write	Reset State	Description
pow_pll2	14	R/W	0'h	Power On PLL2 0: Power Down 1: Power On
pow_vref	13	R/W	0'h	Power On VREF of all analog circuit (Vref pin) 0: Power Down 1: Power On
pow_ovt_detect	12	R/W	0'h	Over Temperature sensor Power 0: Power Down 1: Power On
Reserved	11	R/W	0'h	Reserved
pow_voice_dac	10	R/W	0'h	Power Voice DAC / ADC, VoDAC / VoADC clock will be disable while Disable (Include Voice Interface) 0: Power Down 1: Power On
pow_dac_l	9	R/W	0'h	Stereo Left DAC power and filter clock 0: Power Down 1: Power On
pow_dac_r	8	R/W	0'h	Stereo Right DAC power and filter clock 0: Power Down 1: Power On
pow_adc_l	7	R/W	0'h	Stereo Left ADC power and filter clock 0: Power Down 1: Power On
pow_adc_r	6	R/W	0'h	Stereo Right ADC power and filter clock 0: Power Down 1: Power On
pow_hp_l_mix	5	R/W	0'h	HP Left Mixer Power 0: Power Down 1: Power On
pow_hp_r_mix	4	R/W	0'h	HP Right Mixer Power 0: Power Down 1: Power On
pow_spk_mix	3	R/W	0'h	Speaker Mixer Power 0: Power Down 1: Power On
pow_mono_mix	2	R/W	0'h	Mono Mixer Power 0: Power Down 1: Power On
pow_adc_rec_l	1	R/W	0'h	ADC Record Left Mixer Power 0: Power Down 1: Power On
pow_adc_rec_r	0	R/W	0'h	ADC Record Left Mixer Power 0: Power Down 1: Power On

8.24. Reg-3Eh: Power Management Addition 3

Default: 8000h

Table 34. Reg-3Eh: Power Management Addition 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R/W	1'h	Reserved
pow_aux_out_vol	14	R/W	0'h	AUX OUT Volume Power 0: Power Down 1: Power On
pow_spk_l_vol	13	R/W	0'h	Power On SPK OUT L Volume (Class AB & Class D Amp.) 0: Power Down 1: Power On
pow_spk_r_vol	12	R/W	0'h	Power On SPK OUT R Volume (Class AB & Class D Amp.) 0: Power Down 1: Power On
pow_hp_l_vol	11	R/W	0'h	Power On HP Out Left Volume (Amp) 0: Power Down 1: Power On
pow_hp_r_vol	10	R/W	0'h	Power On HP Out Right Volume (Amp) 0: Power Down 1: Power On
pow_src_vodspif	9	R/W	0'h	SRC1, SRC2 and VoDSP sound interface (Tx/Rx-DP, Tx/Rx-DC) power 0: Power Down 1: Power On
pow_i2c_vodsp	8	R/W	0'h	Power On VoDSP controller Interface 0: Power Down 1: Power On
pow_li_l_vol	7	R/W	0'h	Power On Line In Left Volume 0: Power Down 1: Power On
pow_li_r_vol	6	R/W	0'h	Power On Line In Right Volume 0: Power Down 1: Power On
pow_phone_vol	5	R/W	0'h	Power On Phone Volume 0: Power Down 1: Power On
pow_phone_admixer	4	R/W	0'h	Power On Phone ADmixer 0: Power Down 1: Power On
pow_mic1_vol	3	R/W	0'h	Power On Microphone1 Volume and Boost 0: Power Down 1: Power On
pow_mic2_vol	2	R/W	0'h	Power On Microphone2 Volume and Boost 0: Power Down 1: Power On

Name	Bits	Read/Write	Reset State	Description
pow_mic1_boost	1	R/W	0'h	Power On Microphone1 Boost 0: Power Down 1: Power On
pow_mic2_boost	0	R/W	0'h	Power On Microphone2 Boost 0: Power Down 1: Power On

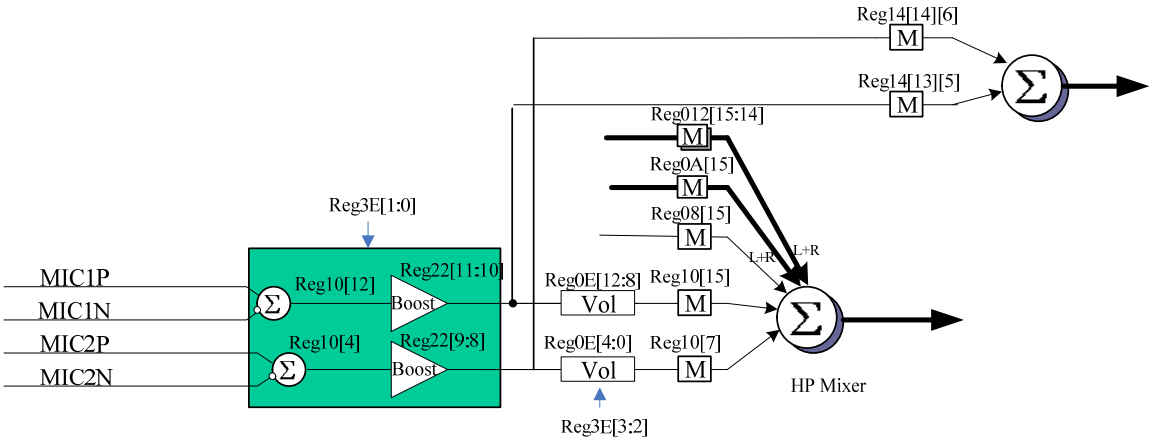


Figure 19 Power Control to MIC Input

8.25. Reg-40h: General Purpose Control Register 1

Default: 0C0Ah

Table 35. Reg-40h: General Purpose Control Register 1

Name	Bits	Read/Write	Reset State	Description
sel_sysclk	15	R/W	0'h	Main SYSCLK Source Select 0: MCLK 1: PLL1 Output
Reserved	14:11	R/W	1'h	Reserved
dac_hpf_en	10	R/W	1'h	Stereo DAC High Pass Filter Enable 0: Disable (Bypass) 1: Enable (Normal operation)
Reserved	9:4	R/W	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
spk_amp_ctrl	3:1	R/W	5'h	Speaker Class AB/D Amplifier Vmid ratio Control 000'b: 2.25 Vdd 001'b: 2.00 Vdd 010'b: 1.75 Vdd 011'b: 1.50 Vdd 100'b: 1.25 Vdd 101'b: 1.00 Vdd Other: Not allowed
Reserved	0	R/W	0'h	Reserved

8.26. Reg-42h: General Purpose Control Register 2

Default: 0000h

Table 36. Reg-42h: General Purpose Control Register 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R	0'h	Reserved
pll1_source_sel	13:12	R/W	0'h	PLL1 Source Select 0x: From MCLK 10: From BCLK 11: From VBCLK
Reserved	11:1	R	00'h	Reserved
pll1_pre_div	0	R/W	0'h	PLL1 Pre-divider 0: ÷ 1 1: ÷ 2

8.27. Reg-44h: PLL1 Control

Default: 0000h

Table 37. Reg-44h: PLL1 Control

Name	Bits	Read/Write	Reset State	Description
Pll1_n_code	15:8	RW	00'h	N[7:0] Code for Analog PLL 00000000: Div 2 00000001: Div 3 …….. 11111111: Div 257
Pll1_m_bypass	7	RW	0'h	Bypass PLL M 0b: No bypass 1b: Bypass

Name	Bits	Read/Write	Reset State	Description
Pll1_k_code	6:4	RW	0'h	K[2:0] Code for Analog PLL 000: Div 2 001: Div 3 …… 111: Div 9
Pll1_m_code	3:0	RW	0'h	M[3:0] Code for Analog PLL 0000: Div 2 0001: Div 3 …… 1111: Div 17

*Note: The PLL transmit formula is FOUT = (MCLK * (N+2))/((M+2) * (K+2)) {Typical K=2}*

8.27.1. PLL1 Clock Setting Table for 48K: (Unit: MHz)

Table 38. PLL Clock Setting Table for 48K: (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

8.27.2. PLL Clock Setting Table for 44.1K: (Unit: MHz)

Table 39. PLL Clock Setting Table for 44.1K: (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

8.28. Reg-46h: PLL2 Control

Default: 0000h

Table 40. Reg-46h: PLL2 Control

Name	Bits	Read/Write	Reset State	Description
pll2_en	15	R/W	0'h	PLL2 Enable 0: Disable 1: Enable
Reserved	14:1	R	0000'h	Reserved
pll2_n	0	R/W	0'h	PLL2 Ratio 0'b: 8 x 1'b: 16 x

8.29. Reg-48h: LDO Control

Default: 0029h

Table 41. Reg-48h: LDO Control

Name	Bits	Read/Write	Reset State	Description
ldo_en	15	R/W	0'h	LDO Enable 0: Disable 1: Enable
Reserved	14:4	R	002'h	Reserved
LDO_output_voltage_ctrl	3:0	R/W	9'h	LDO output Voltage control 0000'b: 0.75V 0001'b: 0.80V 0010'b: 0.85V 0011'b: 0.90V 0100'b: 0.95V 0101'b: 1.00V 0110'b: 1.05V 0111'b: 1.15V 1000'b: 1.20V 1001'b: 1.25V 1010'b: 1.30V 1011'b: 1.35V 1100'b: 1.40V 1101'b: 1.45V 1110'b: 1.50V 1111'b: 1.55V

Note: Driver have to enable 1.2V-LDO in order to provide core power to VoDSP.

Note: It is suggest that LDO_output_voltage _ctrl set to 1000'b in order to provide 1.2V to Voice DSP Engine.

8.30. Reg-4Ch: GPIO Pin Configuration

Default: BE3Eh

Table 42. Reg-4Ch: GPIO Pin Configuration

Name	Bits	Read/Write	Reset State	Description
vodsp_gpio_internal_conf	15	R/W	1'h	VoDSP GPIO Configuration 0: Output 1: Input
Reserved	14:13	R	01'b	Reserved
over_curr_spk_conf	12	R/W	1'h	SPK Over Current Status Source Configure 0: Bypass 1: Normal
over_temp_conf	11	RW	1'h	Over-Temperature Status Source Configuration 0: Bypass 1: Normal
mic1_short_det_conf	10	RW	1'h	MICBIAS1 Short Current Status Source Configuration 0: Bypass 1: Normal
mic2_short_det_conf	9	RW	1'h	MICBIAS2 Short Current Status Source Configuration 0: Bypass 1: Normal
Reserved	8:6	R	0'h	Reserved
gpio5_conf	5	RW	1'h	GPIO5 Pin Configuration 0: Output 1: Input
gpio4_conf	4	RW	1'h	GPIO4 Pin Configuration 0: Output 1: Input
gpio3_conf	3	RW	1'h	GPIO3 Pin Configuration 0: Output 1: Input
gpio2_conf	2	RW	1'h	GPIO2 Pin Configuration 0: Output 1: Input
gpio1_conf	1	RW	1'h	GPIO1 Pin Configuration 0: Output 1: Input
Reserved	0	R	0'h	Reserved. Read as 0

8.31. Reg-4Eh: GPIO Pin Polarity

Default: BE3Eh

Table 43. Reg-4Eh: GPIO Pin Polarity

Name	Bits	Read/Write	Reset State	Description
vodsp_gpio_polarity	15	R/W	1'h	VoDSP GPIO Internal Signal Polarity 0: Low Active 1: High Active
Reserved	14:13	R	01'b	Reserved
over_curr_spk_polarity	12	R/W	1'h	SPK Over Current Polarity 0: Low Active 1: High Active
over_temp_polarity	11	RW	1'h	Over-Temperature Polarity 0: Low Active 1: High Active
mic1_short_det_polarity	10	RW	1'h	MICBIAS1 Short Current Detect Polarity 0: Low Active 1: High Active
mic2_short_det_polarity	9	RW	1'h	MICBIAS2 Short Current Detect Polarity 0: Low Active 1: High Active
Reserved	8:6	R	0'h	Reserved. Read as 0
gpio5_polarity	5	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio4_polarity	4	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio3_polarity	3	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio2_polarity	2	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
gpio1_polarity	1	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
Reserved	0	R	0'h	Reserved. Read as 0

8.32. Reg-50h: GPIO Pin Sticky

Default: 0000h

Table 44. Reg-50h: GPIO Pin Sticky

Name	Bits	Read/Write	Reset State	Description
vodsp_gpio_sticky_en	15	R/W	0'h	VoDSP GPIO Internal Signal Sticky Enable 0: No Sticky 1: Sticky
Reserved	14:13	R	0'h	Reserved
over_curr_spk_sticky_en	12	R/W	0'h	SPK Over Current Sticky Enable 0: No Sticky 1: Sticky
over_temp_sticky_En	11	RW	0'h	Over-Temperature Sticky Enable 0: Not sticky 1: Sticky
mic1_short_det_sticky_En	10	RW	0'h	MICBIAS1 Short Current Detect Sticky Enable 0: Not sticky 1: Sticky
mic2_short_det_sticky_En	9	RW	0'h	MICBIAS2 Short Current Detect Sticky Enable 0: Not sticky 1: Sticky
Reserved	8:6	R	0'h	Reserved. Read as 0
gpio5_sticky_En	5	RW	0'h	GPIO5 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio4_sticky_En	4	RW	0'h	GPIO4 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio3_sticky_En	3	RW	0'h	GPIO3 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio2_sticky_En	2	RW	0'h	GPIO2 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio1_sticky_En	1	RW	0'h	GPIO1 Pin Sticky Enable 0: Not sticky 1: Sticky
Reserved	0	R	0'h	Reserved. Read as 0

8.33. Reg-52h: GPIO Pin Wake Up

Default: 0000h

Table 45. Reg-52h: GPIO Pin Wake Up

Name	Bits	Read/Write	Reset State	Description
vodsp_gpio_wakeup_en	15	R/W	0'h	VoDSP GPIO Internal Signal Wake Up Enable 0: No Wake Up 1: Wake Up
Reserved	14:13	R	0'h	Reserved
over_curr_spk_wakeup_en	12	R/W	0'h	SPK Over Current Wake Up Enable 0: No Wake Up 1: Wake Up
over_temp_wakeup_en	11	R/W	0'h	Over Temperature Wake Up Enable 0: No Wake Up 1: Wake Up
mic1_short_det_wakeup_en	10	R/W	0'h	MICBIAS1 Short Current Wake Up Enable 0: No Wake Up 1: Wake Up
mic2_short_det_wakeup_en	9	R/W	0'h	MICBIAS2 Short Current Wake Up Enable 0: No Wake Up 1: Wake Up
Reserved	8:6	R	0'h	Reserved
gpio5_wakeup_en	5	R/W	0'h	GPIO5 Pin Wake Up Enable 0: No Wake Up 1: Wake Up
gpio4_wakeup_en	4	R/W	0'h	GPIO4 Pin Wake Up Enable 0: No Wake Up 1: Wake Up
gpio3_wakeup_en	3	R/W	0'h	GPIO3 Pin Wake Up Enable 0: No Wake Up 1: Wake Up
gpio2_wakeup_en	2	R/W	0'h	GPIO2 Pin Wake Up Enable 0: No Wake Up 1: Wake Up
gpio1_wakeup_en	1	R/W	0'h	GPIO1 Pin Wake Up Enable 0: No Wake Up 1: Wake Up
Reserved	0	R	0'h	Reserved

8.34. Reg-54h: GPIO Pin Status

Default: 803Ah

Table 46. Reg-54h: GPIO Pin Status

Name	Bits	Read/Write	Reset State	Description
vodsp_gpio_status	15	R	1'h	VoDSP GPIO Internal Signal Status Read: Return Status Write: Write '0' to clear sticky bit
Reserved	14:13	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
over_curr_spk_status	12	R	0'h	SPK Over Current Status Read: Return Status Write: Write '0' to clear sticky bit
over_temp_status	11	R	0'h	Over-Temperature Status Read: Return status Write: Writing '0' clears the sticky bit
mic1_short_det_status	10	R	0'h	MICBIAS1 Short Current Detect Status Read: Return status Write: Writing '0' clears the sticky bit
mic2_short_det_status	9	R	0'h	MICBIAS2 Short Current Detect Status Read: Return status Write: Writing '0' clears the sticky bit
Reserved	8:6	R	0'h	Reserved. Read as 0
gpio5_status	5	R	1'h	GPIO5 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears the sticky bit
gpio4_status	4	R	1'h	GPIO4 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears the sticky bit
gpio3_status	3	R	1'h	GPIO3 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears the sticky bit
gpio2_status	2	R	1'h	GPIO2 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears the sticky bit
gpio1_status	1	R	1'h	GPIO1 Pin Status Read: Return status of each GPIO pin Write: Writing '0' clears the sticky bit
Reserved	0	R	0'h	Reserved. Read as 0

8.35. Reg-56h: Pin Sharing

Default: 0000h

Table 47. Reg-56h: Pin Sharing

Name	Bits	Read/Write	Reset State	Description
Reserved	15:2	R	0000'h	Reserved
gpio2_pin_sharing	1:0	R/W	0'h	GPIO2 Pin Sharing 00'b: IRQ_Out 01'b: GPIO enable 10'b: Reserved 11'b: VoDSP Bypass

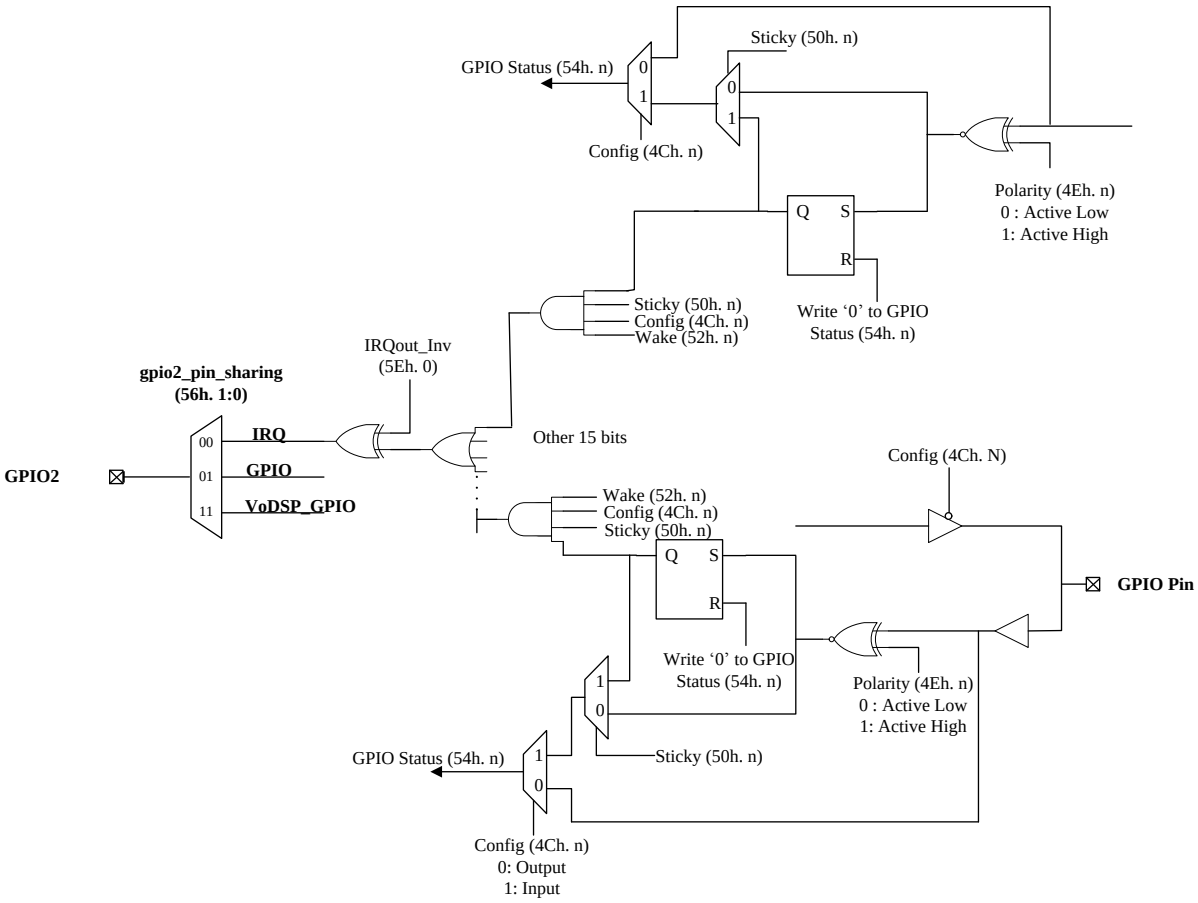


Figure 20 GPIO and IRQ Logic

8.36. Reg-58h: Over-Temp/Current Status

Default: 0000h

Table 48. Reg-58h: Over-Temp/Current Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15:11	R	0'h	Reserved
ovt_status	10	R	0'h	Over Temperature Status 0: Normal 1: Over
ovc_micbias1_status	9	R	0'h	MICBIAS1 Over Current Status 0: Normal 1: Over
ovc_micbias2_status	8	R	0'h	MICBIAS2 Over Current Status 0: Normal 1: Over
Reserved	7:5	R	0'h	Reserved
ovc_spk	4	R	0'h	Speaker Over Current Status (Class AB | Class D) 0: Normal 1: Over
Reserved	3:0	R	0'h	Reserved

8.37. Reg-5Ah: Soft Volume Control Setting

Default: 0009h

Table 49. Reg-58h: Soft Volume Control Setting

Name	Bits	Read/Write	Reset State	Description
softvol_ctrl_en	15	R/W	0'h	Soft Volume Control Enable 0: Disable 1: Enable
Reserved	14:4	R	000'h	Reserved
sel_sync_softvol	3:0	R/W	9'h	Soft volume change delay time 0000'b: 1 SVSYNC 0001'b: 2 SVSYNC 0010'b: 4 SVSYNC 0011'b: 8 SVSYNC 0100'b: 16 SVSYNC 0101'b: 32 SVSYNC 0110'b: 64 SVSYNC 0111'b: 128 SVSYNC 1000'b: 256 SVSYNC 1001'b: 512 SVSYNC 1010'b: 1024 SVSYNC Other: Reserved Note: SVSYNC = 1/Fs. Step: One step

8.38. Reg-5Ch: GPIO_Output Pin Control

Default: 0000h

Table 50. Reg-5Ch: GPIO_Output Pin Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	000'h	Reserved
gpio5_out_status	5	RW	0'h	GPIO5 Output Pin Control 0b: Drive Low 1b: Drive High
gpio4_out_status	4	RW	0'h	GPIO4 Output Pin Control 0b: Drive Low 1b: Drive High
gpio3_out_status	3	RW	0'h	GPIO3 Output Pin Control 0b: Drive Low 1b: Drive High
gpio2_out_status	2	RW	0'h	GPIO2 Output Pin Control 0b: Drive Low 1b: Drive High
gpio1_out_status	1	RW	0'h	GPIO1 Output Pin Control 0b: Drive Low 1b: Drive High
Reserved	0	R	0'h	Reserved. Read as 0

8.39. Reg-5Eh: MISC Control

Default: 3000h

Table 51. Reg-5Eh: MISC Control

Name	Bits	Read/Write	Reset State	Description
en_vref_fast	15	R/W	0'h	Enable fast Vref (This bit have to be disable before play back & record) 0: Enable fast Vref 1: Disable fast Vref
Reserved	14	R	0'h	Reserved
avc_target_sel	13:12	R/W	3'h	AVC target select (ADC AVC volume control target) 00'b: Reserved (No AVC) 01'b: R Channel 10'b: L Channel 11'b: Both Channel
Reserved	11:10	R	0'h	Reserved
en_dp1_hp	9	R/W	0'h	Enable depop mode1 of Headphone 0: Disable 1: Enable
en_dp2_hp	8	R/W	0'h	Enable depop mode2 of Headphone 0: Disable 1: Enable
en_smt_hp_l	7	R/W	0'h	Enable Headphone L mute-unmute de-pop 0: Disable 1: Enable
en_smt_hp_r	6	R/W	0'h	Enable Headphone R mute-unmute de-pop 0: Disable 1: Enable
smt_trig	5	R/W	0'h	Enable mute-unmute de-pop 0: Disable 1: Enable

Name	Bits	Read/Write	Reset State	Description
Reserved	4:2	R	0’h	Reserved
gpio_wakeup_ctrl	1	R/W	0’h	GPIO Wake Up Control 0: Disable 1: Enable
irqout_inv_ctrl	0	R/W	0’h	IRQOUT Inverter Control 0: Normal 1: Inverter

The Jack-insert-detect pull up resistor is implemented via an external circuit (see Figure 21 below).

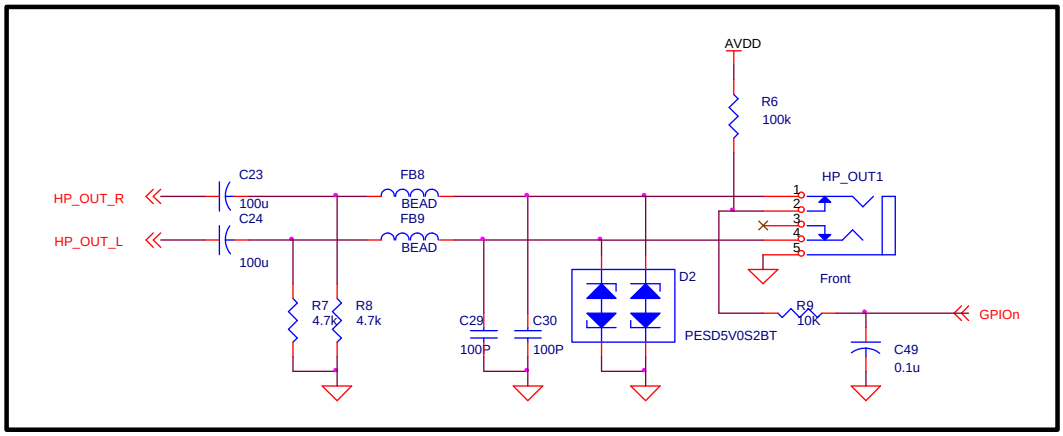


Figure 21 Jack-Insert-Detect Pull Up Resistor Implemented via an External Circuit

8.40. Reg-60h: Stereo DAC Clock Control_1

Default: 3075h

Table 52. Reg-60h: Stereo DAC Clock Control_1

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_bclk_div1	15:12	R/W	3’h	stereo_i2s_bclk_div1 0000’b: ÷ 1 0001’b: ÷ 2 …… 1111’b: ÷ 16
Reserved	11	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_bclk_div2	10:8	R/W	0'h	stereo_i2s_bclk_div2 000'b: ÷ 2 001'b: ÷ 4 010'b: ÷ 8 011'b: ÷ 16 100'b: ÷ 32 Others: Reserved
stereo_i2s_ad_lrck_div1	7:4	R/W	7'h	stereo_i2s_ad_lrck_div1 0000'b: ÷ 1 0001'b: ÷ 2 …… 1111'b: ÷ 16
stereo_i2s_ad_lrck_div2	3:1	R/W	2'h	stereo_i2s_ad_lrck_div2 000'b: ÷ 2 001'b: ÷ 4 010'b: ÷ 8 011'b: ÷ 16 100'b: ÷ 32 Others: Reserved
stereo_i2s_da_lrck_div	0	R/W	1'h	stereo_i2s_da_lrck_div 0: ÷ 32 1: ÷ 64

8.41. Reg-62h: Stereo DAC Clock Control_2

Default: 1010h

Table 53. Reg-62h: Stereo DAC Clock Control_2

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_da_filter_clk_div1	15:12	R/W	1'h	stereo_i2s_da_filter_clk_div1 0000'b: ÷ 1 0001'b: ÷ 2 …… 1111'b: ÷ 16
stereo_i2s_da_filter_clk_div2	11:9	R/W	0'h	stereo_i2s_da_filter_clk_div2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 4 011'b: ÷ 8 100'b: ÷ 16 101'b: ÷ 32 Others: Reserved
stereo_da_64osr	8	R/W	0'h	Stereo DA Sigma Delta Filter Select 0: 128X (256fs / 2) 1: 64X (256fs / 4)

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_ad_filter_clk_div1	7:4	R/W	1'h	stereo_i2s_ad_filter_clk_div1 0000'b: ÷ 1 0001'b: ÷ 2 …… 1111'b: ÷ 16
stereo_i2s_ad_filter_clk_div2	3:1	R/W	0'h	stereo_i2s_ad_filter_clk_div2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 4 011'b: ÷ 8 100'b: ÷ 16 101'b: ÷ 32 Others: Reserved
stereo_ad_64osr	0	R/W	0'h	Stereo AD Sigma Delta Filter Select 0: 128X (256fs / 2) 1: 64X (256fs / 4)

8.42. Reg-64h: VoDAC_PCM Clock Control_1

Default: 3110h

Table 54. Reg-64h: VoDAC_PCM Clock Control_1

Name	Bits	Read/Write	Reset State	Description
voice_i2s_bclk_div1	15:12	R/W	3'h	voice_i2s_bclk_div1 0000'b: ÷ 1 0001'b: ÷ 2 …… 1111'b: ÷ 16
voice_i2s_bclk_div2	11:9	R/W	0'h	voice_i2s_bclk_div2 000'b: ÷ 2 001'b: ÷ 4 010'b: ÷ 8 011'b: ÷ 16 100'b: ÷ 32 Others: Reserved
voice_i2s_lrck_div	8	R/W	1'h	voice_i2s_lrck_div 0: ÷ 32 1: ÷ 64
voice_i2s_filter_clk_div1	7:4	R/W	1'h	voice_i2s_filter_clk_div1 0000'b: ÷ 1 0001'b: ÷ 2 …… 1111'b: ÷ 16

Name	Bits	Read/Write	Reset State	Description
voice_i2s_filter_clk_div2	3:1	R/W	0'h	voice_i2s_filter_clk_div2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 4 011'b: ÷ 8 100'b: ÷ 16 101'b: ÷ 32 Others: Reserved
voice_64osr	0	R/W	0'h	Voice DA / AD Sigma Delta Filter Select 0: 128X (256fs / 2) 1: 64X (256fs / 4)

Note: The driver must determine the Voice AD/DA filter clock, and select the filter by setting Voice_64osr

8.43. Reg-68h: Pseudo Stereo and Spatial Effect Block Control

Default: 0553h

Table 55. Reg-68h: Pseudo Stereo and Spatial Effect Block Control

Name	Bits	Read/Write	Reset State	Description
spatial_ctrl_en	15	R/W	0'h	Spatial Effect Enable 0: Disable 1: Enable
apf_en	14	R/W	0'h	Enable All Pass Filter (EN APF) 0: Disable 1: Enable The coefficient a1 is loaded from apf_parm_a1
pseudo_stereo_en	13	R/W	0'h	Enable Pseudo Stereo (EN-Pseudo) 0: Disable 1: Enable
en_3d	12	R/W	0'h	Enable Stereo Extension (EN-3D) 0: Disable 1: Enable load 3D ratio from ratio_parm_3d and 3D Gain from gain_parm_3d
gain1_parm_3d	11:10	R/W	1'h	3D Gain1 Parameter (SEGn) 00'b: Gain = 1.0 01'b: Gain = 1.5 10'b: Gain = 2.0 11'b: Reserved
ratio1_parm_3d	9:8	R/W	1'h	3D Ratio1 Parameter (DPn) 00'b: Ratio = 0.0 01'b: Ratio = 0.66 10'b: Ratio = 1.0 11'b: Reserved
gain2_parm_3d	7:6	R/W	1'h	3D Gain2 Parameter (SEGn) 00'b: Gain = 1.0 01'b: Gain = 1.5 10'b: Gain = 2.0 11'b: Reserved

Name	Bits	Read/Write	Reset State	Description
ratio2_parm_3d	5:4	R/W	1'h	3D Ratio2 Parameter (DPn) 00'b: Ratio = 0.0 01'b: Ratio = 0.66 10'b: Ratio = 1.0 11'b: Reserved
Reserved	3:2	R	0'h	Reserved
apf_parm_a1	1:0	R/W	3'h	All Pass Filter parameter a1 00'b: 0 01'b: -0.85 (for 32KHz sample rate or lower) 10'b: -0.90 (for 44.1KHz sample rate) 11'b: -0.95 (for 48KHz sample rate)

Note: Writes to SEGn and DPn will be ignored when the Spatial effect control bit is enabled. This means individual Spatial coefficients cannot be modified when Spatial is enabled.

8.44. Reg-6Ah: Private Register Address

Default: 0000h

Table 56. Reg-6Ah: Private Register Address

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	00'h	Reserved
private_addr	7:0	R/W	00'h	Private Register Address

8.45. Reg-6Ch: Private Register Data

Default: 0000h

Table 57. Reg-6Ch: Private Register Data

Name	Bits	Read/Write	Reset State	Description
private_data	15:0	R/W	0000'h	Private Register Data

Note: It is strong suggest not writting to un-available Hiden Register.

8.46. Reg-6Eh: EQ Control and Status / ADC HPF Control

Default: 0000h

Table 58. Reg-6Eh: EQ Control and Status / ADC HPF Control

Name	Bits	Read/Write	Reset State	Description
eq_en	15	R/W	0'h	EQ Block Enable Control 0: Disable 1: Enable
eq_source_sel	14	R/W	0'h	EQ Source Select 0: DAC path 1: ADC path
eq_hpf_sel	13	R/W	0'h	EQ High Pass Filter Control 0: High Frequency Shelving Filter 1: High Pass Filter
eq_hpf_status	12	R	0'h	EQ High Pass Filter Status 0: Normal 1: Overflow This bit is set if overflow had ever occurred. Write '1' to clear
eq_bpf3_status	11	R	0'h	EQ Band-3 Pass Filter Status 0: Normal 1: Overflow This bit is set if overflow had ever occurred. Write '1' to clear
eq_bpf2_status	10	R	0'h	EQ Band-2 Pass Filter Status 0: Normal 1: Overflow This bit is set if overflow had ever occurred. Write '1' to clear
eq_bpf1_status	9	R	0'h	EQ Band-1 Pass Filter Status 0: Normal 1: Overflow This bit is set if overflow had ever occurred. Write '1' to clear
eq_lpf_status	8	R	0'h	EQ Low Pass Filter Status 0: Normal 1: Overflow This bit is set if overflow had ever occurred. Write '1' to clear
eq_para_update	7	R/W	0'h	EQ parameter update control (EQ LPF, BPF, HPF) 0: No action 1: Update parameter
adc_hpf_ctrl	6	R/W	0'h	ADC High Pass Filter Control 0: Disable 1: Enable
adc_hpf_sel	5	R/W	0'h	ADC High Pass Filter Control 0: High Frequency Shelving Filter 1: High Pass Filter
hpf_en	4	R/W	0'h	EQ HPF Control 0: Disable 1: Enable
bpf3_en	3	R/W	0'h	EQ BPF3 Control 0: Disable 1: Enable
bpf2_en	2	R/W	0'h	EQ BPF2 Control 0: Disable 1: Enable
bpf1_en	1	R/W	0'h	EQ BPF1 Control 0: Disable 1: Enable
lpf_en	0	R/W	0'h	EQ LPF Control 0: Disable 1: Enable

8.47. Private-00h: EQ Low Pass Filter Cofficient (LPF a1)

Default: 0000’h

Table 59. EQ Low Pass Filter Cofficient (LPF a1)

Name	Bits	RW	Default	Description
lpf_a1	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a1 should be in –2 ~ 1.99)

8.48. Private-01h: EQ Low Pass Filter Gain (LPF Ho)

Default: 0000’h

Table 60. EQ Low Pass Filter Gain (LPF Ho)

Name	Bits	RW	Default	Description
lpf_h0	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the ho should be in –4 ~ 3.99)

8.49. Private-02h: EQ Band-1 Pass Filter Cofficient (BPF1 a1)

Default: 0000’h

Table 61. EQ Band-1 Pass Filter Cofficient (BPF1 a1)

Name	Bits	RW	Default	Description
bpf1_a1	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a1 should be in –2 ~ 1.99)

8.50. Private-03h: EQ Band-1 Pass Filter Cofficient (BPF1 a2)

Default: 0000’h

Table 62. EQ Band-1 Pass Filter Cofficient (BPF1 a2)

Name	Bits	RW	Default	Description
bpf1_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a2 should be in –2 ~ 1.99)

8.51. Private-04h: EQ Band-1 Pass Filter Gain (BPF1 Ho)

Default: 0000’h

Table 63. EQ Band-1 Pass Filter Gain (BPF1 Ho)

Name	Bits	RW	Default	Description
bpf1_h0	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the ho should be in –4 ~ 3.99)

8.52. Private-05h: EQ Band-2 Pass Filter Cofficient (BPF2 a1)

Default: 0000’h

Table 64. EQ Band-2 Pass Filter Cofficient (BPF2 a1)

Name	Bits	RW	Default	Description
bpf2_a1	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a1 should be in –2 ~ 1.99)

8.53. Private-06h: EQ Band-2 Pass Filter Cofficient (BPF2 a2)

Default: 0000’h

Table 65. EQ Band-2 Pass Filter Cofficient (BPF2 a2)

Name	Bits	RW	Default	Description
bpf2_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a2 should be in –2 ~ 1.99)

8.54. Private-07h: EQ Band-2 Pass Filter Gain (BPF2 Ho)

Default: 0000’h

Table 66. EQ Band-2 Pass Filter Gain (BPF2 Ho)

Name	Bits	RW	Default	Description
bpf2_h0	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the ho should be in –4 ~ 3.99)

8.55. Private-08h: EQ Band-3 Pass Filter Cofficient (BPF3 a1)

Default: 0000’h

Table 67. EQ Band-3 Pass Filter Cofficient (BPF3 a1)

Name	Bits	RW	Default	Description
bpf3_a1	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a1 should be in –2 ~ 1.99)

8.56. Private-09h: EQ Band-3 Pass Filter Cofficient (BPF3 a2)

Default: 0000’h

Table 68. EQ Band-3 Pass Filter Cofficient (BPF3 a2)

Name	Bits	RW	Default	Description
bpf3_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a2 should be in –2 ~ 1.99)

8.57. Private-0Ah: EQ Band-3 Pass Filter Gain (BPF3 Ho)

Default: 0000’h

Table 69. EQ Band-3 Pass Filter Gain (BPF3 Ho)

Name	Bits	RW	Default	Description
bpf3_h0	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the ho should be in –4 ~ 3.99)

8.58. Private-0Bh: EQ High Pass Filter Cofficient (HPF a1)

Default: 0000’h

Table 70. EQ High Pass Filter Cofficient (HPF a1)

Name	Bits	RW	Default	Description
hpf_a1	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a1 should be in –2 ~ 1.99)

8.59. Private-0Ch: EQ High Pass Filter Gain (HPF Ho)

Default: 0000’h

Table 71. EQ High Pass Filter Gain (HPF Ho)

Name	Bits	RW	Default	Description
hpf_h0	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the ho should be in –4 ~ 3.99)

8.60. Private-11h: EQ Input Volume Control

Default: 0000’h

Table 72. EQ Input Volume Control

Name	Bits	RW	Default	Description
Reserved	15:2	R	0000’h	Reserved
eq_in_vol	1:0	R/W	0’h	EQ Input Volume (7-bit Volume Unsigned Ratio) 00’b: 0dB 01’b: -6dB 10’b: -12dB 11’b: -18dB

8.61. Private-12h: EQ Output Volume Control

Default: 0000’h

Table 73. EQ Output Volume Control

Name	Bits	RW	Default	Description
Reserved	15:3	R	0000’h	Reserved
eq_out_vol	2:0	R/W	1’h	EQ Output Volume (7-bit Volume Unsigned Ratio) 000’b: -3dB 001’b: 0dB 010’b: 3dB 011’b: 6dB 100’b: 9dB 101’b: 12dB 110’b: 15dB 111’b: 18dB

8.62. Private-13h: ADC High Pass Filter Cofficient (ADC HPF

a1)

Default: 0000’h

Table 74. ADC High Pass Filter Cofficient (ADC HPF a1)

Name	Bits	RW	Default	Description
adc_hpf_a1	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the a1 should be in –2 ~ 1.99)

8.63. Private-14h: ADC High Pass Filter Gain (ADC HPF Ho)

Default: 0000’h

Table 75. ADC High Pass Filter Gain (HPF Ho)

Name	Bits	RW	Default	Description
adc_hpf_h0	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4 ~ 3.99, the ho should be in –4 ~ 3.99)

8.64. Private-20h: ADC Auto Volume Control Register 0

Default: 000A’h

Table 76. ADC Auto Volume Control Register 0

Name	Bits	RW	Default	Description
avc_adc_en	15	R/W	0’h	AVC Enable (Select the controlled gain block for AVC) 0: Disable 1: Enable
avc_adc_gain_action	14	R/W	0’h	Gain Action of Non active region 0: Keep pervious gain 1: Unit Gain
avc_adc_feedback	13	R/W	0’h	Non-act threshold gain feedback selection 0: without gain feedback 1: with gain feedback
Reserved	12:8	R	0’h	Reserved
avc_adc_ref_sel	7	R/W	0’h	AVC Reference Channel Select 0: Left Channel 1: Right Channel
Reserved	6:5	R	0’h	Reserved

monitor_window_adc_ctrl	4:0	R/W	0A'h	Monitor Window Control (Unit: 2^(n+1) samples) (default: 01010'b) 00000'b: 2^1 sample 00001'b: 2^2 samples 00010'b: 2^3 samples ..... 10000'b: 2^17 samples Others: Reserved The maximum n = 16 **à** 100000000000000000 = 2^17 Note: Monitor Window can only be changed after soft-reset once AVC Enable

8.65. Private-21h: ADC Auto Volume Control Register 1

Default: 0400'h

Table 77. ADC Auto Volume Control Register 1

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
avc_adc_thmax	14:0	R/W	0400'h	The Maximum PCM absolute level after AVC, Thmax (= 0 ~ 2^15-1)

8.66. Private-22h: ADC Auto Volume Control Register 2

Default: 0390'h

Table 78. ADC Auto Volume Control Register 2

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
avc_adc_thmin	14:0	R/W	0390'h	The Minimum PCM absolute level after AVC, Thmin (= 0 ~ 2^15-1)

8.67. Private-23h: ADC Auto Volume Control Register 3

Default: 0001'h

Table 79. ADC Auto Volume Control Register 3

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
avc_adc_thnon	14:0	R/W	0001'h	The Non-active PCM absolute level after AVC, Thnonact (= 0 ~ 2^15-1)

8.68. Private-24h: ADC Auto Volume Control Register 4

Default: 01FF'h

Table 80. ADCAuto Volume Control Register 4

Name	Bits	RW	Default	Description
avc_adc_cntmaxth1	15:0	R/W	01FF'h	The CNTMAXTH1 to control the sensitivity to decrease Gain (unit: 2^1) This value should be less than CNTMAXTH2 (Max: 2^17-2)

8.69. Private-25h: ADC Auto Volume Control Register 5

Default: 0200'h

Table 81. ADCAuto Volume Control Register 5

Name	Bits	RW	Default	Description
avc_adc_cntmaxth2	15:0	R/W	0200'h	The CNTMAXTH2 to control the sensitivity to decrease Gain (unit: 2^1) This value should be less than Monitor Window. (Optimum: 1/2 Monitor window) (Max: 2^18-2)

8.70. Private-26h: DAC Auto Volume Control Register 0

Default: 200A'h

Table 82. DAC Auto Volume Control Register 0

Name	Bits	RW	Default	Description
avc_dac_en	15	R/W	0'h	AVC Enable (Select the controlled gain block for AVC) 0: Disable 1: Enable
avc_dac_gain_action	14	R/W	0'h	Gain Action of Non active region 0: Keep pervious gain 1: Unit Gain

avc_dac_feedback	13	R/W	1'h	Non-act threshold gain feedback selection 0: After Digital volume 1: Before Digital volume
Reserved	12:8	R	0'h	Reserved
avc_dac_ref_sel	7	R/W	0'h	AVC Reference Channel Select 0: Left Channel 1: Right Channel
Reserved	6:5	R	0'h	Reserved
monitor_window_dac_ctrl	4:0	R/W	0A'h	Monitor Window Control (Unit: 2^(n+1) samples) (default: 01010'b) 00000'b: 2^1 sample 00001'b: 2^2 samples 00010'b: 2^3 samples ..... 10000'b: 2^17 samples Others: Reserved The maximum n = 16 **à** 100000000000000000 = 2^17 Note: Monitor Window can only be changed after soft-reset once AVC Enable

8.71. Private-27h: DAC Auto Volume Control Register 1

Default: 0400'h

Table 83. DAC Auto Volume Control Register 1

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
avc_dac_thmax	14:0	R/W	0400'h	The Maximum PCM absolute level after AVC, Thmax (= 0 ~ 2^15-1)

8.72. Private-28h: DAC Auto Volume Control Register 2

Default: 0390'h

Table 84. DAC Auto Volume Control Register 2

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
avc_dac_thmin	14:0	R/W	0390'h	The Minimum PCM absolute level after AVC, Thmin (= 0 ~ 2^15-1)

8.73. Private-29h: DAC Auto Volume Control Register 3

Default: 0001'h

Table 85. DAC Auto Volume Control Register 3

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
avc_dac_thnon	14:0	R/W	0001'h	The Non-active PCM absolute level after AVC, Thnonact (= 0 ~ 2^15-1)

8.74. Private-2Ah: DACAuto Volume Control Register 4

Default: 01FF'h

Table 86. DACAuto Volume Control Register 4

Name	Bits	RW	Default	Description
avc_dac_cntmaxth1	15:0	R/W	01FF'h	The CNTMAXTH1 to control the sensitivity to decrease Gain (unit: 2^1) This value should be less than CNTMAXTH2 (Max: 2^17-2)

8.75. Private-2Bh: DACAuto Volume Control Register 5

Default: 0200'h

Table 87. DACAuto Volume Control Register 5

Name	Bits	RW	Default	Description
avc_dac_cntmaxth2	15:0	R/W	0200'h	The CNTMAXTH2 to control the sensitivity to decrease Gain (unit: 2^1) This value should be less than Monitor Window. (Optimum: 1/2 Monitor window) (Max: 2^18-2)

8.76. Private-38h: Digital Reset

Default: 0000’h

Table 88. Digital Reset

Name	Bits	RW	Default	Description
Reserved	15:3	R	0000’h	Reserved
rst_voice_dac_filter	2	R/W	0’h	Voice DAC filter reset 0: Normal 1: Reset
rst_stereo_adc_filter	1	R/W	0’h	Stereo ADC filter reset 0: Normal 1: Reset
rst_stereo_dac_filter	0	R/W	0’h	Stereo DAC filter reset 0: Normal 1: Reset

8.77. Private-39h: Digital Internal Register

Default: 9000’h

Table 89. PR39 Digital Internal Register

Name	Bits	RW	Default	Description
pad_drive	15	R/W	1’h	Pad drive capability 0: 5mA 1: 12mA
Reserved	14:11	R/W	2’h	Reserved, must keep 02’h
i2s_adc_dir	10	R/W	0’h	Main I2S SADC pin direct 0: Output 1: Hi-Z for multi- I2S
Reserved	9:0	R	000’h	Reserved

8.78. Private-4Eh: VoDSP Microphone source select

Default: 0000’h

Table 90. PR4E VoDSP Microphone source select

Name	Bits	RW	Default	Description
Reserved	15:7	R/W	0’h	Reserved
vodsp_mic_sel	6:4	R/W	0’h	VoDSP Microphone source select 000’b: only from ADCR (Default) 101’b: from ADCL / ADCR Others: reserved
Reserved	3:0	R/W	0’h	Reserved

8.79. Reg-70h: VoDSP Register Address

Table 91. Reg-70h: VoDSP Register Address

Name	Bits	Read/Write	Reset State	Description
vodsp_addr	15:0	R/W	0000’h	VoDSP Register Address

8.80. Reg-72h: VoDSP Register Data

Default: 0000h

Table 92. Reg-72h: VoDSP Register Data

Name	Bits	Read/Write	Reset State	Description
vodsp_data	15:0	R	0000’h	VoDSP Register Data

8.81. Reg-74h: VoDSP Register Command

Default: 0000h

Table 93. Reg-74h: VoDSP Register Command

Name	Bits	Read/Write	Reset State	Description
vodsp_busy	15	R	0’h	VoDSP I2C Busy flag
vodsp_mx72_source	14	R/W	0’h	VoDSP_data Read source select 0: From VoDSP read back register 1: From Reg72 write temp register
vodsp_clk_sel	13:12	R/W	0’h	VoDSP internal clock select (VoDSP SYSCLK=24.576MHz) 2’b00: 12.288MHz 2’b01: 6.144MHz 2’b10: 3.072MHz 2’b11: 2.048MHz
Reserved	11:10	R	0’h	Reserved
vodsp_read	9	R/W	0’h	VoDSP Read Enable
vodsp_write	8	R/W	0’h	VoDSP Write Enable
vodsp_cmd	7:0	R/W	00’h	Command Entry Ex: 3B’h: Memory Write 37’h: Memory Read 60’h: Register Read 68’h: Register Write etc.

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 94. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	3.63	V
Analog	AVDD	-0.3	-	3.63	V
Headphone	HPVDD	-0.3	-	3.63	V
Speaker	SPKVDD	-0.3	-	7	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 95. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer Power	DBVDD	1.8	3.3	3.6	V
Digital Core Power	DCVDD	1.8	3.3	3.6	V
Headphone Power	HPVDD	2.3	3.3	3.6	V
Analog Power	AVDD	2.3	3.3	3.6	V
Speaker Power	SPKVDD	2.3	3.3	5	V

9.1.3. Static Characteristics

Table 96. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Low Level Input Voltage	V_{IL}	-	-	0.35DVDD	V
High Level Input Voltage	V_{IH}	0.65DVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DVDD	V
Input Leakage Current	-	-1	-	1	µA
Output Leakage Current (Hi-Z)	-	-1	-	1	µA
Output Buffer High Drive Current	-	-	22	-	mA
Output Buffer Low Drive Current	-	-	10	-	mA
V_{MID} Internal Serial Resistor	-	25	50	75	KΩ
V_{MID} Internal Serial Resistor Ratio	-	95	100	105	%

Note: DVDD=3.3V, $T_{ambient}$=25°C, with 50pF external load.

9.2. Analog Performance Characteristics

Table 97. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs	-	1.0	-	Vrms
MIC Inputs (Non-Boost)	-	1.0	-	Vrms
MIC Inputs (Boost 20dB)	-	0.1	-	Vrms
ADC	-	0.7	-	Vrms
Full Scale Output Voltage				
MONO Outputs	-	1.0	-	Vrms
Headphone Amplifiers Outputs	-	1.0	-	Vrms
Speaker Amplifiers Outputs	-	1.3	-	Vrms
S/N Ratio (A-weighted, HPL/R or MONO with 10KΩ/50pF load)				
STEREO DAC	-	97	-	dB
STEREO ADC	-	90	-	dB
Voice DAC	-	94	-	dB
Total Harmonic Distortion + Noise (A-weighted, HPL/R or MONO with 10KΩ/50pF load)				
STEREO DAC	-	-93	-	dB
STEREO ADC	-	-85	-	dB
Voice DAC	-	-90	-	dB
MIC Boost Amplifier				
Gain=20dB	-	20	-	dB
Gain=30dB	-	30	-	dB
Gain=40dB	-	40	-	dB
Input Impedance (Gain=0dB, ADC Mixer=On)				
PHONEN (Differential Mode)	-	16	-	KΩ
MIC1N, MIC2N (Differential Mode)	-	76	-	KΩ
MIC1P, MIC2P	-	76	-	KΩ
PHONEP	-	16	-	KΩ
LINE_IN		16		
Input Impedance (Gain=0dB, ADC Mixer=Off)				
PHONEN (Differential Mode)		16		KΩ
MIC1N, MIC2N (Differential Mode)		76		KΩ
MIC1P, MIC2P		76		KΩ
PHONEP		32		KΩ
LINE_IN		32		KΩ
Output Impedance				
AUX_OUT	-	300	-	Ω
HP_OUT	-	3	-	Ω
SPK_OUT (Class AB)	-	1	-	Ω
SPK_OUT (Class D)	-	0.8	-	Ω

Parameter	Min	Typ	Max	Units
AUX_OUTAmplifier Quiescent Current (32Ω Load)/CH	-	0.4	-	μA
AUX_OUTAmplifier THD+N Single End Mode (10KΩ Load) Output Power=0.1mW BTL Mode (10KΩ Load) Output Power=0.1mW	- -	0.01 0.01	- -	% %
AUX_OUTAmplifier PSRR (217Hz)	-	-70	-	dB
Headphone Amplifier Output Power (THD+N=60dB, 32Ω Load)	-	-	31.25	mW
Headphone Amplifier Quiescent Current (32Ω Load)	-	1	-	μA
Headphone Amplifier THD+N (32Ω Load) Output Power=20mW Output Power=25mW	 - -	 -80 -80	 - -	 dB dB
Headphone Amplifier PSRR (217Hz)	-	-55	-	dB
BTL Class-AB/D Speaker Amplifier Output Power (SPKVDD=5V with 8Ω Load) THD+N=-40dB THD+N=-20dB	-	 1.2 1.5	-	W
BTL Class-AB/D Speaker Amplifier Output Power (SPKVDD=5V with 4Ω Load) THD+N=-40dB THD+N=-20dB	-	 1.8 2.3	-	W
BTL Speaker Amplifier Quiescent Current Class AB_Strong (8Ω Load) Class D	 - -	 - -	 2.8 1.2	 mA mA
BTL Speaker Amplifier THD + N (8Ω Load) Class AB_Strong (8Ω Load) Output Power=350mW Output Power=600mW Class D Output Power=350mW Output Power=600mW	 - - - -	 -58 -58 -80 -75	 - - - -	 dB dB dB dB
BTL Speaker Amplifier THD + N Class AB_Weak (10KΩ/50pF Load)	 -	 -85	 -	 dB
BTL Speaker Amplifier SNR Class AB_Weak (10KΩ/50pF Load)	 -	 88	 -	 dB
BTL Speaker Amplifier PSRR (217Hz)	-	-70	-	dB
Power Supply Current (32Ω HP playback 1KHz –3dB sine wave) I_{DDA} (Analog Block) I_{DDD} (Digital Block)	 - -	 - -	 25 7	 mA mA

Parameter	Min	Typ	Max	Units
Power Down Current				
I_{DDA} (Analog Block)	-	-	10	µA
I_{DDD} (Digital Block)	-	-	1	µA
MICBIAS1 Output Voltage				
0.75*Avdd Setting	-	2.475	-	V
0.9*Avdd Setting	-	2.97	-	V
MICBIAS1 and MICBIAS2 Drive Current	-	16	-	mA
MICBIAS2 Output Voltage				
0.75*Avdd Setting	-	2.475	-	V
0.9*Avdd Setting	-	2.97	-	V

Note: Standard test conditions
$T_{ambient}$ = 25°C, DVDD = AVDD = AVDD2=HPVDD=3.3V, SPKVDD = 4.2V
1kHz input sine wave; PCM Sampling frequency = 48kHz; 0dB = 1Vrms, Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation; EQ and 3D disabled

9.3. AC Timing Characteristics

9.3.1. I²C Control Interface

Table 98. I²C Control Interface Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Clock Pulse Duration	$t_{w(9)}$	1.3	-	-	µs
Clock Pulse Duration	$t_{w(10)}$	600	-	-	ns
Clock Frequency	f	0	-	400K	Hz
Re-Start Setup Time	$t_{su(6)}$	600	-	-	ns
Start Hold Time	$t_{h(5)}$	600	-	-	ns
Data Setup Time	$t_{su(7)}$	100	-	-	ns
Data Hold Time	$t_{h(6)}$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su(8)}$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

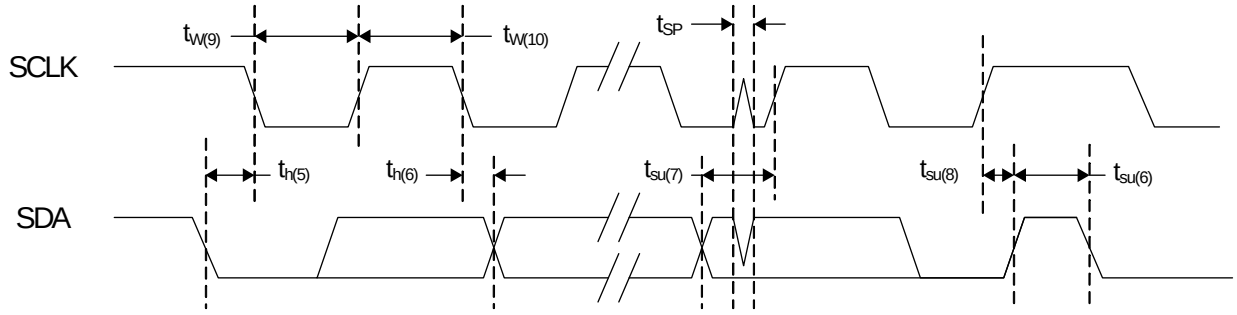


Figure 22 I²C Control Interface Waveform

9.3.2. I²S/PCM Interface Master Mode

Table 99. I²S Master Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

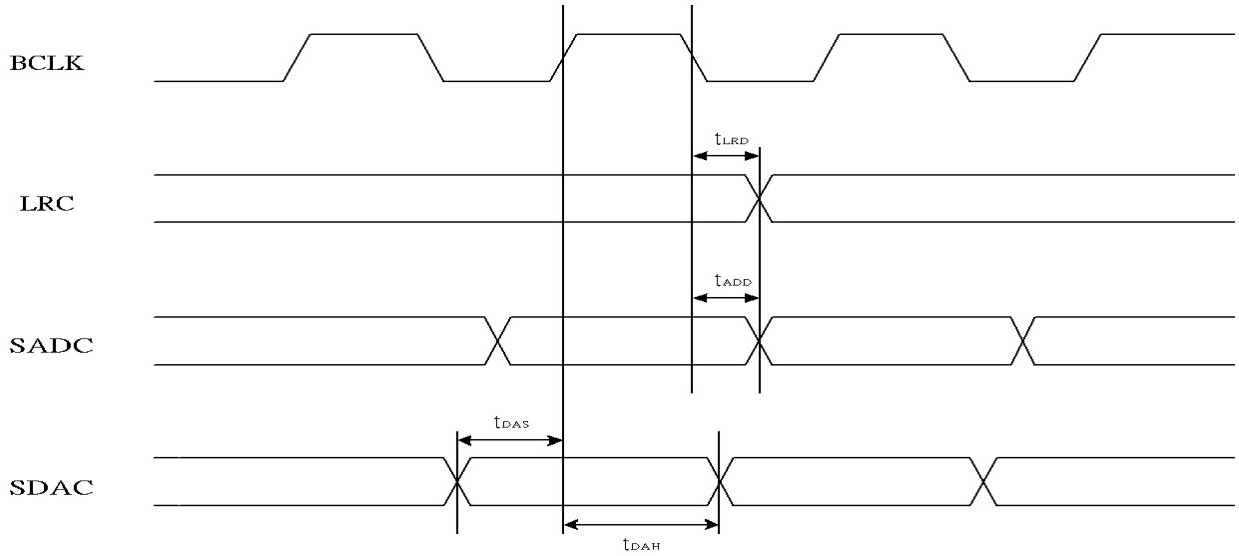


Figure 23 I²S Master Mode Waveform

9.3.3. I²S/PCM Interface Slave Mode

Table 100. I²S Slave Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

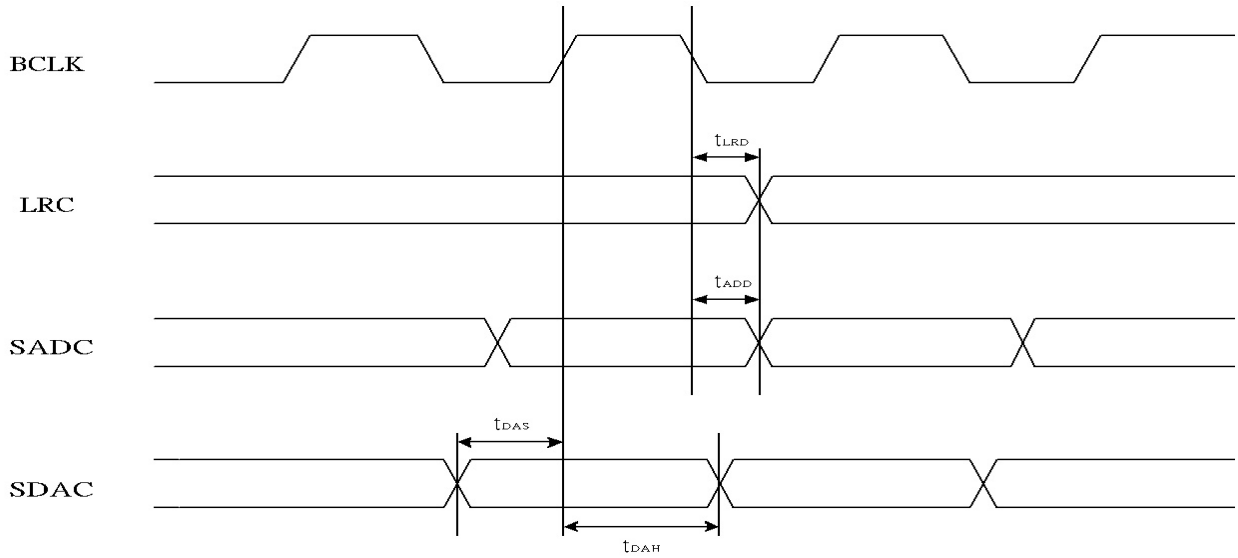
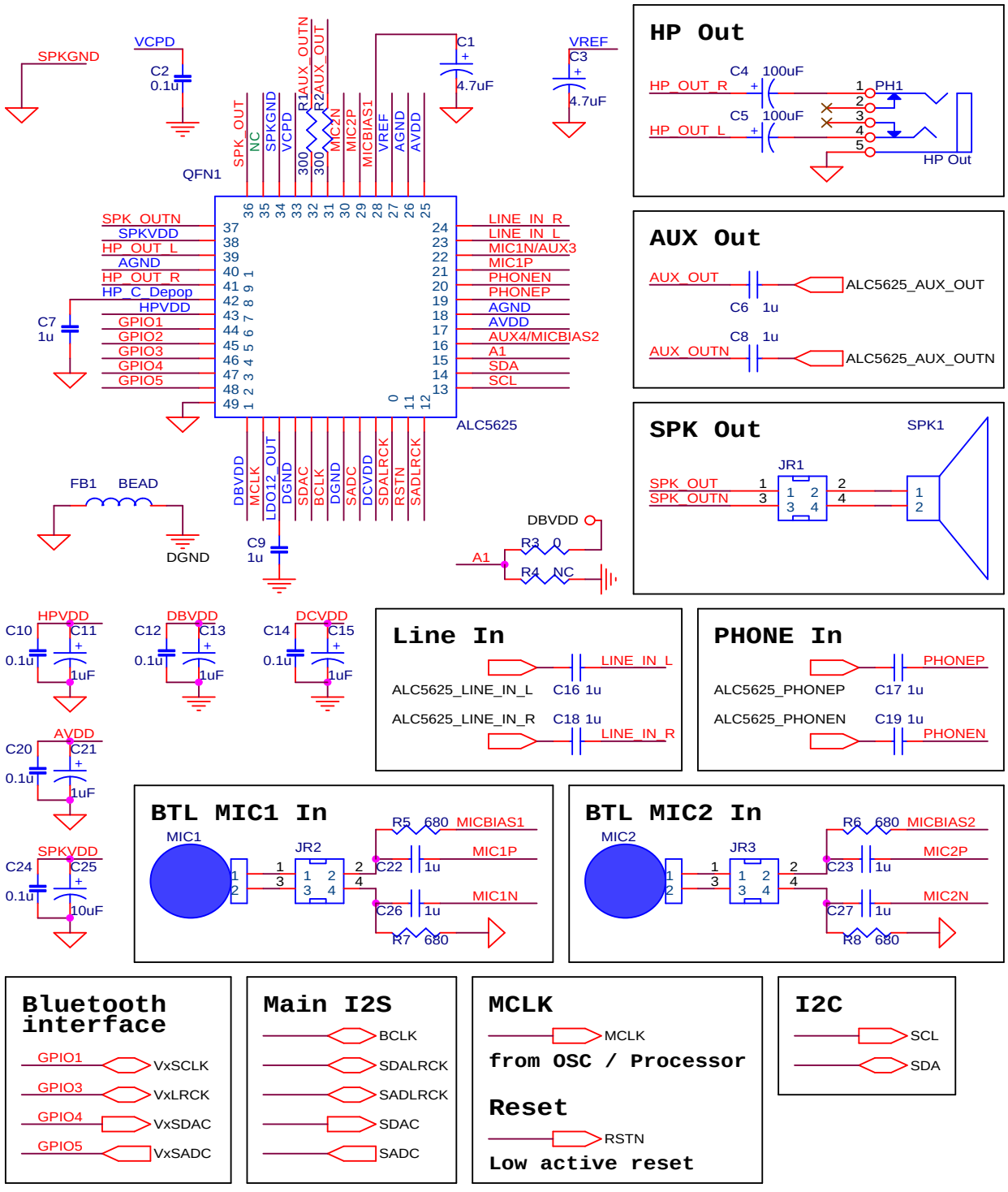
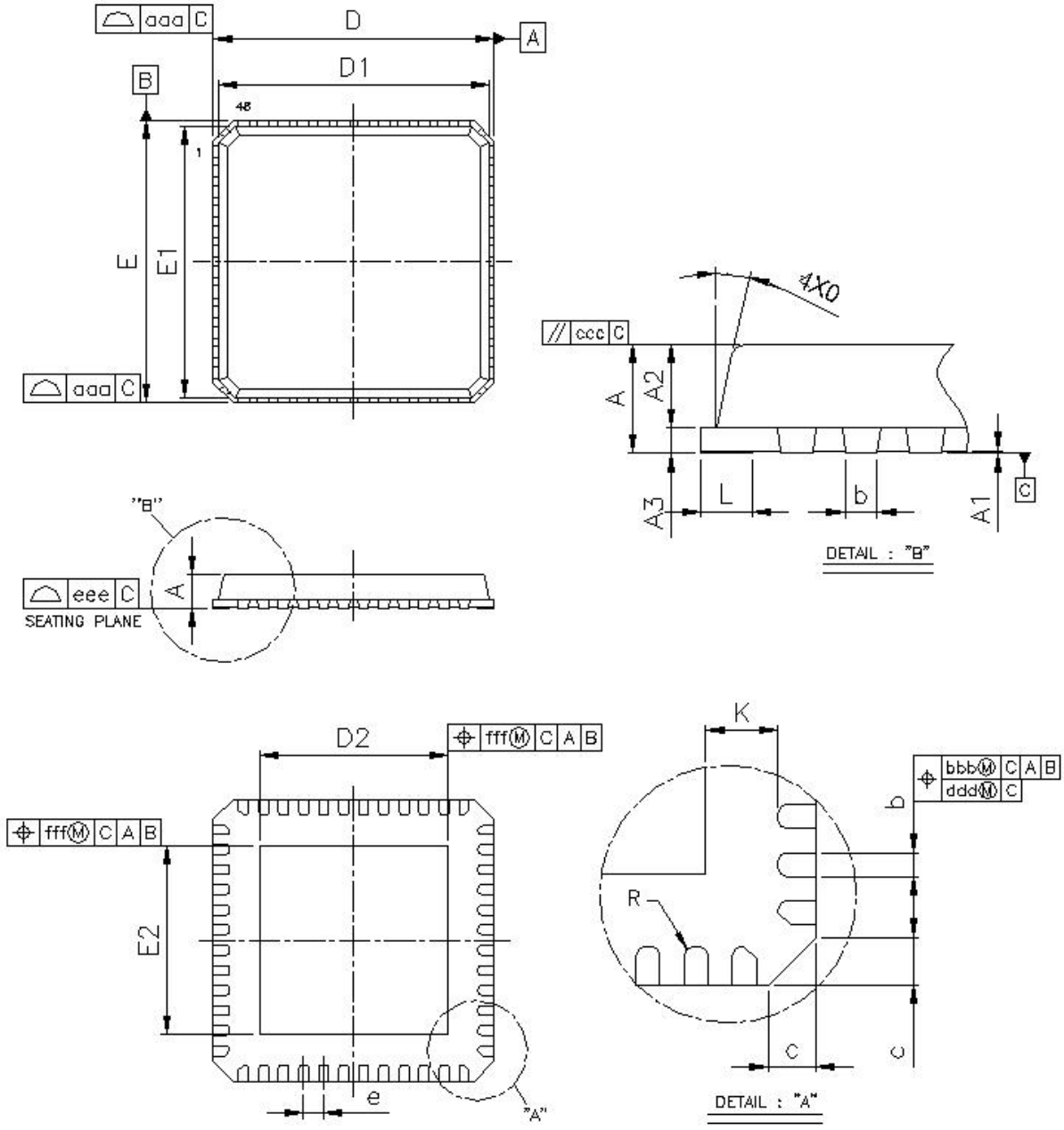


Figure 24 I²S Slave Mode Waveform

10. Application Circuits



11. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
c	—	—	0.6	—	—	0.024
D/E	7.00BSC			0.276BSC		
D_1/E_1	6.75BSC			0.266BSC		
D_2/E_2	4.80	5.05	5.30	0.189	0.199	0.209
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.2	—	—	0.008	—	—
θ	0^o	—	14^o	0^o	—	14^o
aaa	—	—	0.15	—	—	0.006
bbb	—	—	0.10	—	—	0.004
ccc	—	—	0.10	—	—	0.004
ddd	—	—	0.05	—	—	0.002
eee	—	—	0.08	—	—	0.003
fff	—	—	0.10	—	—	0.004

12. Appendix A: Stereo I2S Clock

12.1. Stereo I2S Interface Clock Setting

Stereo I2S SYSCLK	SCLK Freq.	DAC Sample Rate	ADC Sample Rate	Reg34 [14]	Reg60	Reg62
24.576MH	512KHz	8KHz	8KHz	0'h	B175'h	2424'h
24.576MH	256KHz	8KHz	8KHz	0'h	B274'h	2424'h
24.576MH	1.024MH	16KHz	16KHz	0'h	B075'h	2222'h
24.576MH	512KHz	16KHz	16KHz	0'h	B174'h	2222'h
24.576MH	1.024MH	16KHz	8KHz	1'h	B077'h	2224'h
24.576MH	512KHz	16KHz	8KHz	1'h	B174'h	2224'h
24.576MH	3.072MH	48KHz	48KHz	0'h	3075'h	1010'h
24.576MH	1.536MH	48KHz	48KHz	0'h	3174'h	1010'h
24.576MH	3.072MH	48KHz	16KHz	1'h	30B7'h	1022'h
24.576MH	1.536MH	48KHz	16KHz	1'h	31B4'h	1022'h
24.576MH	3.072MH	48KHz	8KHz	1'h	30B9'h	1024'h
24.576MH	1.536MH	48KHz	8KHz	1'h	31B6'h	1024'h
22.5792M	705.6KH	11.025K	11.025KHz	0'h	3275'h	1414'h
22.5792M	352.8KH	11.025K	11.025KHz	0'h	3374'h	1414'h
22.5792M	1.4112M	22.05KH	22.05KHz	0'h	3175'h	1212'h
22.5792M	705.6KH	22.05KH	22.05KHz	0'h	3274'h	1212'h
22.5792M	1.4112M	22.05KH	11.025KHz	1'h	3177'h	1214'h
22.5792M	705.6KH	22.05KH	11.025KHz	1'h	3274'h	1214'h
22.5792M	2.8224M	44.1KHz	44.1KHz	0'h	3075'h	1010'h
22.5792M	1.4112M	44.1KHz	44.1KHz	0'h	3174'h	1010'h
22.5792M	2.8224M	44.1KHz	22.05KHz	1'h	3077'h	1012'h
22.5792M	1.4112M	44.1KHz	22.05KHz	1'h	3174'h	1012'h
22.5792M	2.8224M	44.1KHz	11.025KHz	1'h	3079'h	1014'h
22.5792M	1.4112M	44.1KHz	11.025KHz	1'h	3176'h	1014'h

13. Appendix B: Voice I2S Clock

13.1. Voice I2S Clock Setting

Voice I2S SYSCLK	VxSCLK Freq.	DAC SR	Reg64
24.576MHz	512KHz	8KHz	2724'h
24.576MHz	256KHz	8KHz	2824'h
24.576MHz	1.024MHz	16KHz	2522'h
24.576MHz	512KHz	16KHz	2622'h
24.576MHz	1.536MHz	24KHz	2312'h
24.576MHz	768KHz	24KHz	2412'h
24.576MHz	2.048MHz	32KHz	2320'h
24.576MHz	1.024MHz	32KHz	2420'h
24.576MHz	3.072MHz	48KHz	3110'h
24.576MHz	1.536MHz	48KHz	3210'h
22.5792MHz	705.6KHz	11.025KHz	3514'h
22.5792MHz	352.8KHz	11.025KHz	3615'h
22.5792MHz	1.4112MHz	22.05KHz	3312'h
22.5792MHz	705.6KHz	22.05KHz	3412'h
22.5792MHz	2.8224MHz	44.1KHz	3110'h
22.5792MHz	1.4112MHz	44.1KHz	3210'h
512 * VoFs	X	VoFs	3110'h

14. Ordering Information

Table 101. Ordering Information

Part Number	Package	Status
ALC5625-GR	QFN-48 in 'Green' Package (Tray)	Mass Production
ALC5625-GRT	QFN-48 in 'Green' Package (Tape & Reel)	Mass Production

Note 1: See page 5 for Green package and version identification.
Note 2: Above parts are tested under AVDD=3.3V.

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