ALC5629

I²S/PCM AUDIO DAC

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5629 Audio DAC IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/06/26	First release.

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1. General Description

The ALC5629 is a highly-integrated I^2S/PCM interface audio DAC with single-ended stereo LINE_OUT that can be configured to drive Headphones, and is designed for Multimedia and Communication handheld devices. It provides a Stereo Hi-Fi DAC for playback via the I^2S/PCM interface and is controlled by the I^2C interface.

The ALC5629 AVDD operates at supply voltages from 2.3V to 3.6V. DCVDD and DBVDD operate from 1.8V to 3.6V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10μA.

The ALC5629 is available in a 4x4mm 'Green' QFN-24 package, making it ideal for use in handheld portable systems.

2. Features

- Digital-to-Analog Converter with 100dB SNR and –86dB THD+N at 3.3V
- Supports playback soft-mute and digital volume
- Supports pop noise suppression with external capacitor
- Digital power supplied from 1.8V to 3.6V
- Analog power supplied from 2.3V to 3.6V
- Stereo LINE_OUT can be configured to drive 45mW Headphone OUT
- Power management and enhanced power saving
- Internal PLL can receive wide range of clock inputs
- Supports crystal oscillator
- Supports sampling rate 8KHz ~ 192KHz
- Supports I^2C control interface
- Supports three programmable data interfaces
  - I^2S, left justified, and PCM interface
  - 16/20/24-bit word lengths
  - Master or Slave clock mode
- 24-pin QFN 4x4mm package for small footprint

3. System Applications

- Portable media player
- MP3 player
- Bluetooth A2DP (Advanced Audio Distribution Profile) headsets
- Portable Navigation Device (PND)
- Multimedia phone

4. Block Diagram

4.1. Function Block

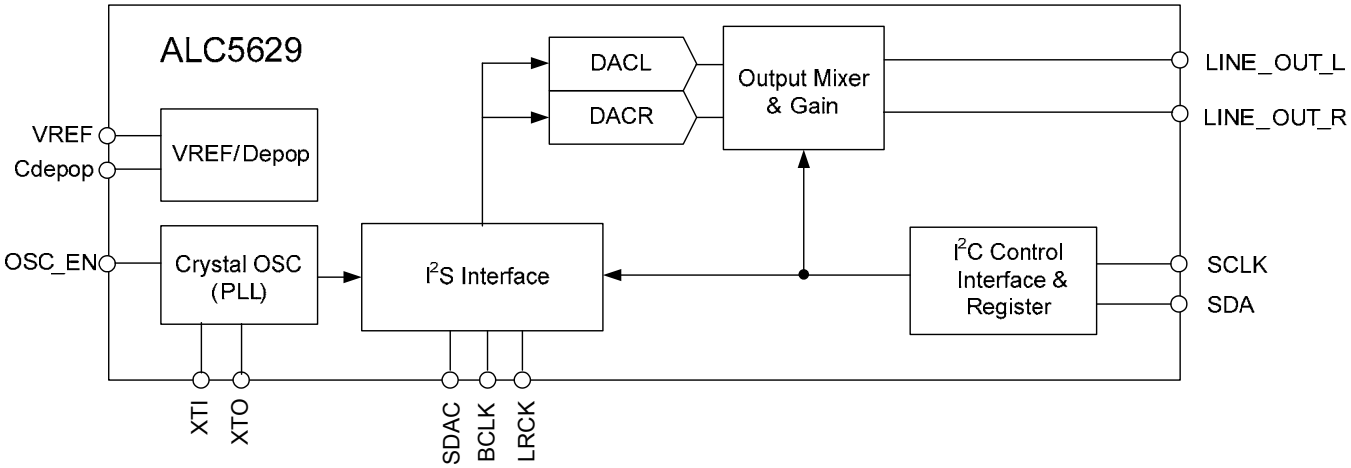


Figure 1. Block Diagram

4.2. Audio Mixer Path

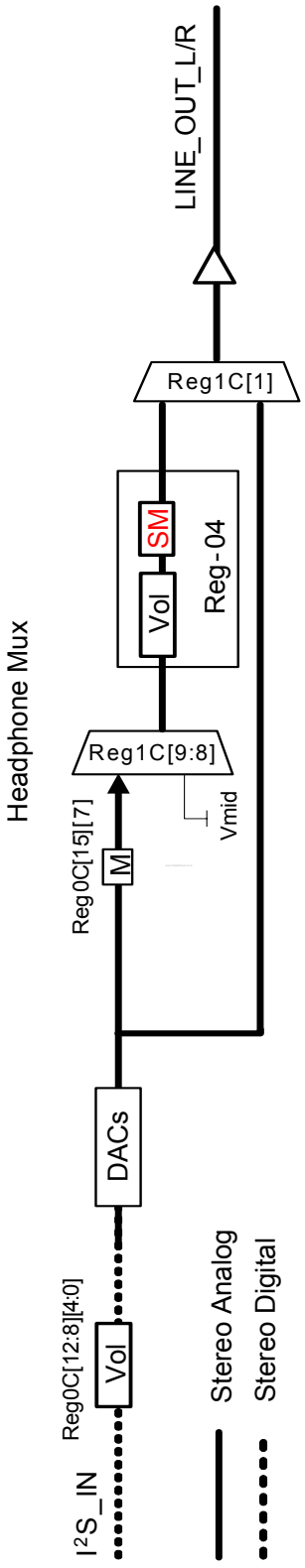


Figure 2. Audio Mixer Path

5. Pin Assignments

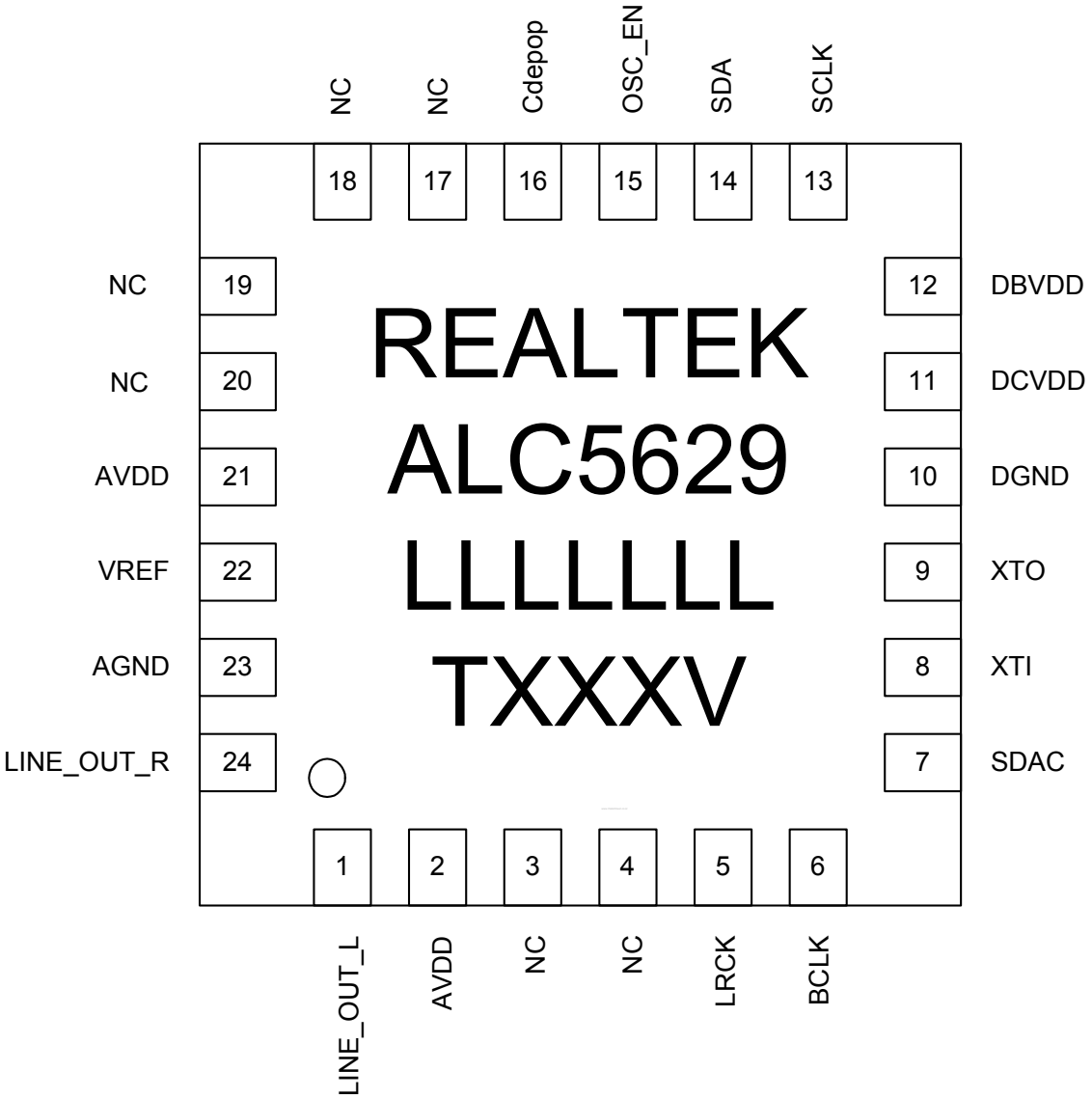


Figure 3. Pin Assignments

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3.

6. Pin Descriptions

6.1. Digital I/O

Table 1. Digital I/O Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
LRCK	IO	5	Digital Audio Input Frame Sync	Schmitt Trigger Input, Output
BCLK	IO	6	Digital Audio Serial Clock	Schmitt Trigger Input, Output
SDAC	I	7	Digital Audio Serial Data Input	Schmitt Trigger Input
XTI	I	8	Crystal Input	Schmitt Trigger Input
XTO	O	9	Crystal Output	Schmitt Trigger Output
SCLK	I	13	I^2C: Clock Input	Schmitt Trigger Input
SDA	IO	14	I^2C: Data Input And Output	Schmitt Trigger Input, Output
OSC_EN	I	15	Crystal Oscillator Enable Control, Connect to VDD or GND VDD: Crystal enabled GND: Crystal disabled	Schmitt Trigger Input

6.2. Analog I/O

Table 2. Analog I/O Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
LINE_OUT_L	O	1	Line Output Left Channel	Analog Amplifier Output
LINE_OUT_R	O	24	Line Output Right Channel	Analog Amplifier Output

6.3. Filter/Reference

Table 3. Filter/Reference Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
Cdepop	IO	16	De-Pop Capacitor, Connect 1µF Capacitor to Analog GND	Capacitor to Analog Ground
VREF	O	22	Reference Voltage Output, Connect 4.7µF Capacitor to Analog GND	Capacitor to Analog Ground

6.4. Power/Ground

Table 4. Power/Ground Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
DGND	P	10	Digital GND	-
DCVDD	P	11	Digital VDD	1.8V~3.6V (Core)
DBVDD	P	12	Digital VDD	1.8V~3.6V (IO Buffer)
AGND	P	23	Analog GND	-
AVDD	P	2, 21	Analog VDD	2.3V~3.6V
DGND	P	Exposed Pad	Digital GND	-

6.5. Not Connected (NC)

Table 5. Not Connected (NC) Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
NC	-	3, 4, 17, 18, 19, 20	Not Connected	-

7. Functional Description

7.1. Power

The ALC5629 has many power blocks. The power supply limit conditions are DBVDD≥DCVDD and AVDD≥DCVDD. To prevent pop noise, we suggest that DCVDD is powered on before AVDD.

7.2. Reset

There are two types of reset operation: Power-On-Reset (POR) and Register reset.

Table 6. Reset Operation

Reset Type	Trigger Condition	Codec Response
POR	Monitor Digital Power Supply Voltage Reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write Reg00	Reset all registers to default values.

7.2.1. Power-On Reset (POR)

When power is on, DCVDD passes through the V_{POR} band of the ALC5629 (V_{PORH}~V_{PORL}). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 7. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: The V_{POR_OFF} must be below V_{POR_ON}.

7.3. Clocking

The ALC5629 supports a Crystal as internal system clock. When the OSC_EN pin is kept high, the audio system clock can be selected from XTI/XTO or PLL. When a crystal is applied, 256/384/512/768Fs is required from XTI/XTO. If using internal PLL as audio internal clock, set the PLL output to 512Fs.

A Phase-Lock Loop (PLL) is used to provide a flexible input clock from 2.048MHz (64Fs of 32kHz) to 40MHz. Typical choices are 2.048MHz, 4.096MHz, and 13MHz. The source of the PLL can be set to XTI or BCLK by setting sel_pll_sour (Reg42[14]). Firmware can setup the PLL to output the desired frequency for the system clock.

The PLL transmit formula is: F_{OUT} = (XTI*(N+2)) / ((M+2)*(K+2)) (Typical K=2)

Table 8. PLL Clock Setting Table for 48K (Unit: MHz)

XTI	M Code	N Code	Fvco	K Code	Fout
2.048	0	94	98.304	2	24.576
3.6864	1	78	98.304	2	24.576
4.096	0	46	98.304	2	24.576
12	14	129	98.25	2	24.5625
13	14	119	98.3125	2	24.57812
15.36	3	30	98.304	2	24.576
16	5	41	98.28571	2	24.57143
19.2	15	85	98.25882	2	24.5647
19.68	0	8	98.4	2	24.6

Table 9. PLL Clock Setting Table for 44.1K (Unit: MHz)

XTI	M Code	N Code	Fvco	K Code	Fout
2.048	0	86	90.112	2	22.528
3.6864	0	47	90.3168	2	22.5792
4.096	9	241	90.48436	2	22.62109
12	15	126	90.35294	2	22.58824
13	15	116	90.23529	2	22.55882
15.36	15	98	90.35294	2	22.58824
16	12	77	90.28571	2	22.57143
19.2	15	78	90.35294	2	22.58824
19.68	15	76	90.29647	2	22.57412

7.4. I²C Control Interface

I²C is a 2-wire half-duplex serial communication interface, supporting only slave mode.

7.4.1. Addressing Setting

(MSB)			BIT				(LSB)
0	0	1	1	0	0	0	RW

7.4.2. Complete Data Transfer

Data Transfer over I²C Control Interface

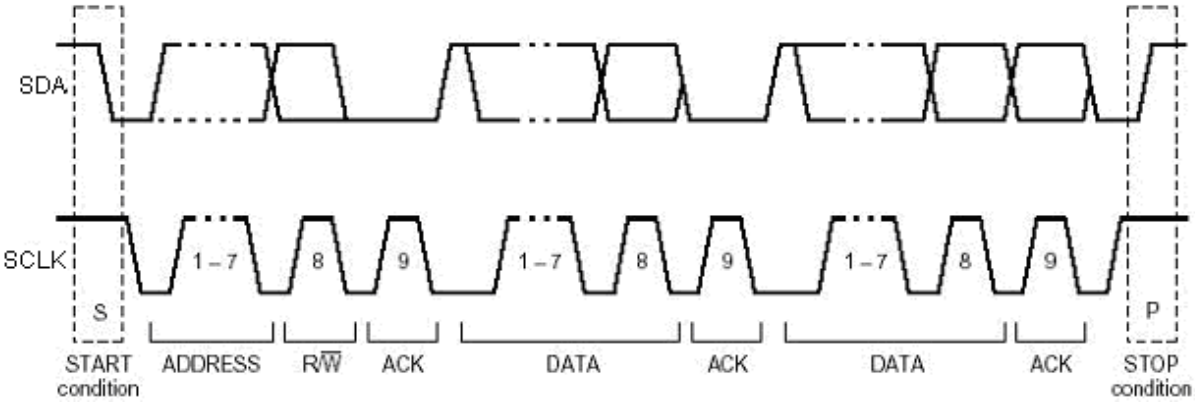


Figure 4. Data Transfer Over I²C Control Interface

Write WORD Protocol

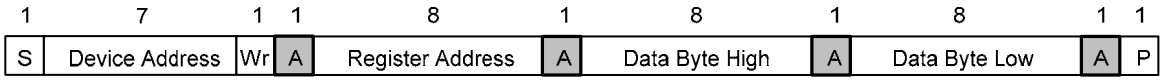
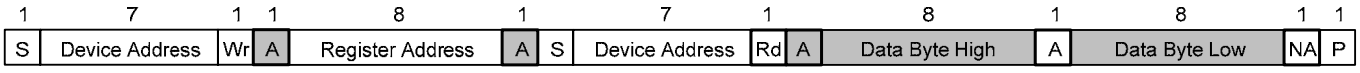


Figure 5. Write WORD Protocol

Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

Figure 6. Read WORD Protocol

7.4.3. Odd-Addressed Register Access

The ALC5629 will return '0000h' when odd-addressed and unimplemented registers are read.

7.5. Digital Data Interface

7.5.1. I²S/PCM Interface

The Digital to Analog Converter (DAC) serial data is input via the SDAC pin. The serial data is shifted in on the rising edge of BCLK (ctrl_i2s_bclk_polarity=0'b) or the falling edge (ctrl_i2s_bclk_polarity=1'b). The Left/Right Clock (LRCK) signal is the frame sync signal. Left/Right data can be swapped by en_dac_lrck_swap.

The ALC5629 I²S/PCM interface can be configured to Master mode or Slave mode. In Master mode (sel_i2s_mode=0'b), BCLK and LRCK are configured as output. In Slave mode (sel_i2s_mode=1'b), BCLK and LRCK are configured as input. The XTI provides BCLK synchronized clock externally as Stereo System Clock.

The ALC5629 supports three independent I²S/PCM interfaces for Stereo Audio data formats:

- PCM/DSP mode
- Left justified mode
- I²S mode

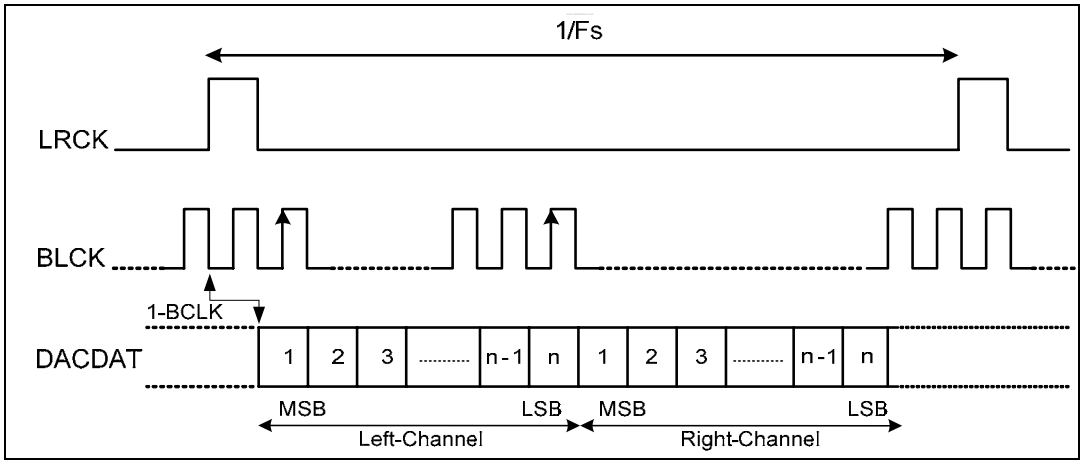


Figure 7. PCM Stereo Data Mode A Format-1 (sel_i2s_data_format=10'b, ctrl_i2s_bclk_polarity=0'b)

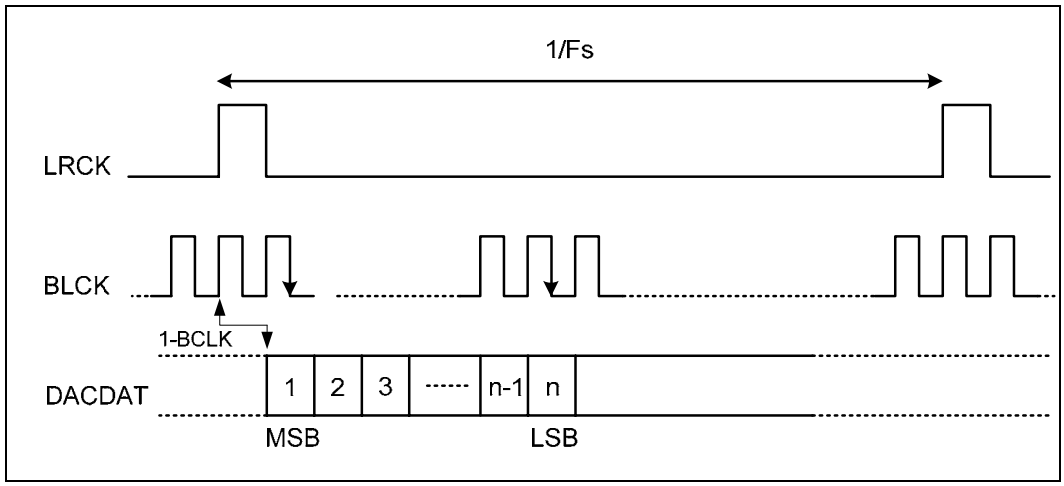


Figure 8. PCM Stereo Data Mode A Format-2 (sel_i2s_data_format=10'b, ctrl_i2s_bclk_polarity=1'b)

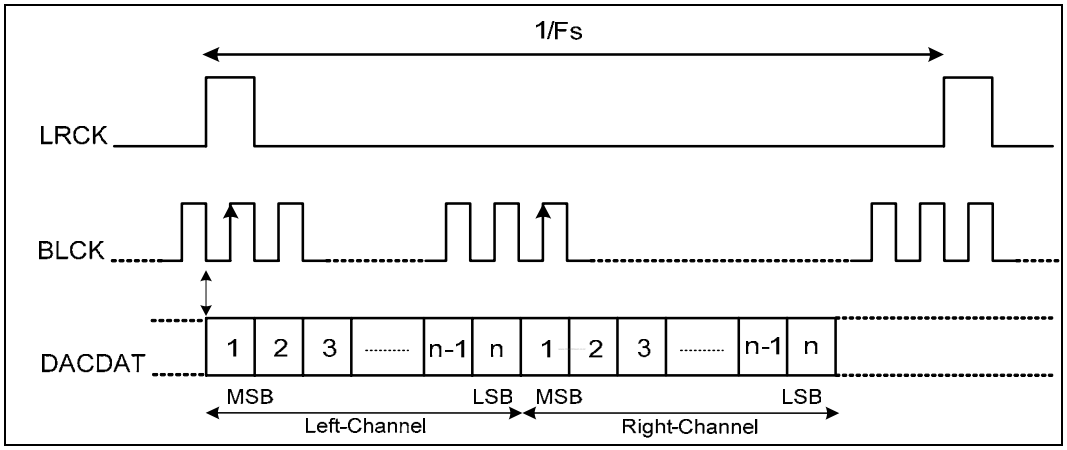


Figure 9. PCM Stereo Data Mode B Format (sel_i2s_data_format=11'b, ctrl_i2s_bclk_polarity=0'b)

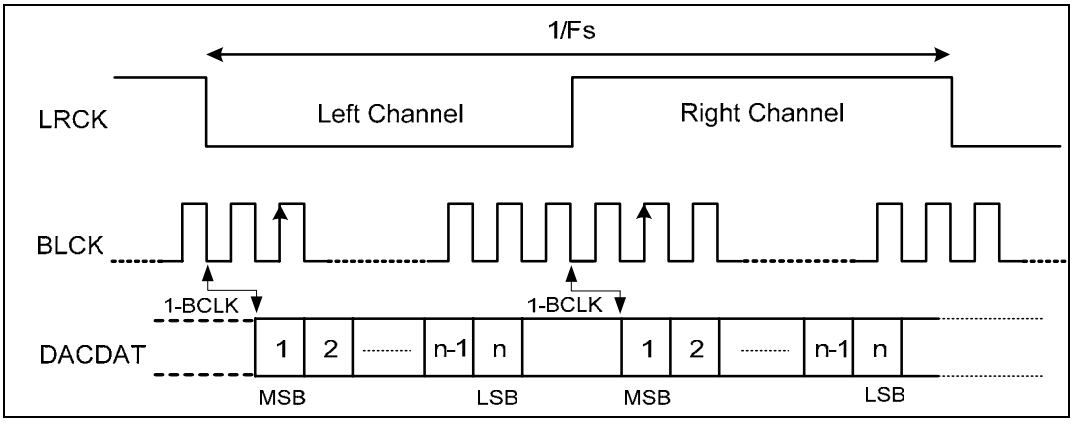


Figure 10. I²S Data Format (sel_i2s_data_format=00'b)

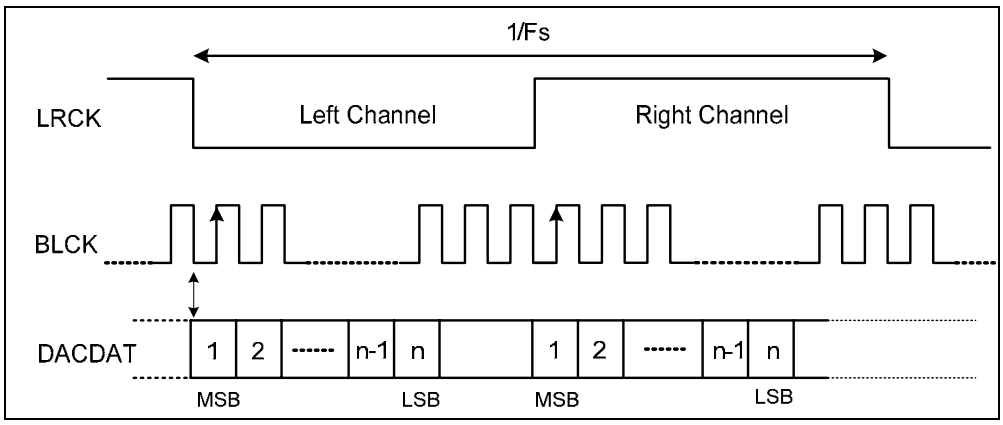


Figure 11. Left-Justified Data Format (sel_i2s_data_format=01'b, ctrl_i2s_bclk_polarity=0'b)

7.6. Analog Signal Path

7.6.1. Line Output

LINE_OUT_L/R provides 2-channel single-ended output. The source of LINE_OUT_L/R can be selected from sel_lo_l_in & sel_lo_r_in, as shown below.

- V_{MID}
- DAC R/L channel

The LINE_OUT_L/R volume and mute are controlled by Reg04. Besides, Reg3E[10]: pow_lo_l_vol and Reg3E[9]: pow_lo_r_vol can be used to power down the LINE_OUT volume.

LINE_OUT supports 'Soft Volume Delay Mute' and 'Zero-Crossing Detect' functions which can be enabled by Reg5C[11]: en_lo_l_dezero, Reg5C[10]: en_lo_l_softvol, Reg5C[9]: en_lo_r_dezero, and Reg5C[8]: en_lo_r_softvol.

LINE_OUT_L/R source can be selected from DAC Stereo output (Reg1C[1]: en_dac_lo) for high quality performance playback.

LINE_OUT_L/R can be configured to drive Headphone by setting en_hp_enhance_amp=1.

7.6.2. Stereo DAC

The stereo DAC can be configured to different sample rates by driving 256Fs/384Fs into audio SYSCLK, and individually set by sel_i2s_bclk_ms (Reg38[12]).

dac_l_vol & dac_r_vol can be used to control the DAC output volume.

7.7. Power Management

The ALC5629 supports detailed Power Management control registers within Reg3A, 3C, and 3E. Each particular block will be active only when individual bits of Reg3A, 3C, and 3E are set to enable.

7.8. Line Output Depop

The ALC5629 provides a LINE_OUT depop mechanism in order to eliminate the pop noise of LINE_OUT when LINE_OUT acts as Headphone output, by setting en_lo_out_amp=1 and en_lo_enhance_amp=1. An external 1µF Capacitor is required in this application. Refer to the ALC5629 Application Notes (separate document) for details.

7.9. Zero Cross

When Zero-Cross detect is enabled, the ALC5629 will change each output volume or mute only if the signal swing crosses the zero point. This function can avoid pop noise when volume is changed or muted.

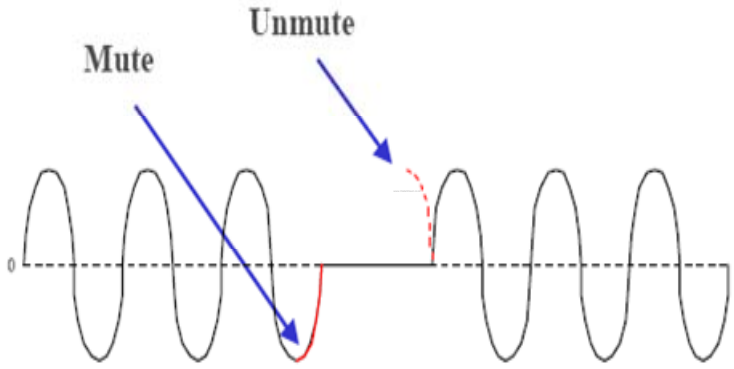


Figure 12. Zero Cross Disabled when Output Muted

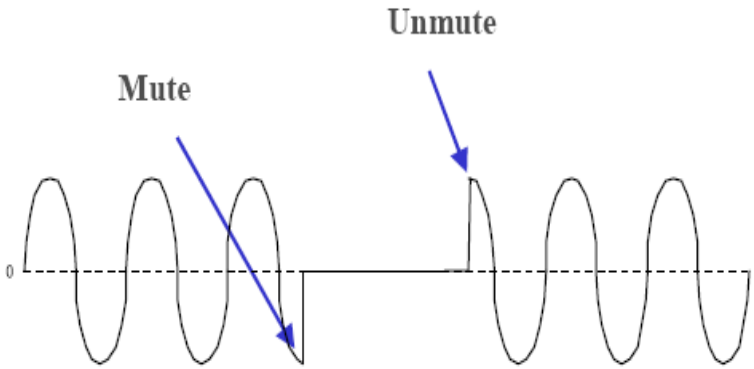


Figure 13. Zero Cross Enabled when Output Muted

8. Register Descriptions

8.1. Reg-00h: Software Reset

Default: 0003'h

Table 10. MX00 Software Reset

Name	Bits	RW	Default	Description
id	15:8	R	00'h	Chip ID
Reserved	7:0	R	03'h	Reserved

8.2. Reg-04h: Line Output Volume

Default: 9F9F'h

Table 11. MX04 Line Output Volume

Name	Bits	RW	Default	Description
mute_lo_l	15	RW	1'h	Mute Line Output Left Channel 0: On 1: Mute (-∞ dB)
Reserved	14:13	R	0'h	Reserved
sel_lo_l_vol	12:8	RW	1F'h	Line Output Left Volume (HPL[4:0]) in 1.5dB Steps
mute_lo_r	7	RW	1'h	Mute Line Output Right Channel 0: On 1: Mute (-∞ dB)
Reserved	6:5	R	0'h	Reserved
sel_lo_r_vol	4:0	RW	1F'h	Line Output Right Volume (HPR[4:0]) in 1.5dB Steps *Note: For HPR/HPL: 00h: 0dB attenuation.* *1Fh: 46.5dB attenuation.*

8.3. Reg-0Ch: Stereo DAC Digital Volume

Default: FFFF'h

Table 12. MX0C Stereo DAC Digital Volume

Name	Bits	RW	Default	Description
mute_dacl2hp	15	RW	1'h	Mute DAC Left Channel Digital Volume Output to Headphone Mux Control 0: On 1: Mute (-∞ dB)
mute_dacl2spk	14	RW	1'h	Mute DAC Left Channel Digital Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞ dB)
dac_l_vol	13:8	RW	3F'h	DAC Left Channel Digital Volume (PLV[5:0]) in 0.75dB Steps

Name	Bits	RW	Default	Description
mute_dacr2hp	7	RW	1'h	Mute Right Channel DAC Digital Volume Output to Headphone Mux Control 0: On 1: Mute (-∞ dB)
mute_dacr2spk	6	RW	1'h	Mute Right Channel DAC Digital Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞ dB)
dac_r_vol	5:0	RW	3F'h	DAC Right Channel Digital Volume (PRV[5:0]) in 0.75dB Steps *Note: For PRV/PLV: 00h: +12dB gain.* *10h: 0dB attenuation.* *3Fh: 35.25dB attenuation.*

8.4. Reg-16h: Soft Delay Volume Control Time

Default: 0009'h

Table 13. MX16 Soft Delay Volume Control Time

Name	Bits	RW	Default	Description
Reserved	15:4	R	0'h	Reserved
sel_sync_softvol	3:0	RW	1001'b	Soft Volume Change Delay Time (Default=1001b) 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved

Note: SVSYNC=1/Fs, Step: -1.5dBFS.

8.5. Reg-1Ch: Output Mixer Control

Default: 8004'h

Table 14. MX1C Output Mixer Control

Name	Bits	RW	Default	Description
Reserved	15:10	R	10'h	Reserved
sel_lo_l_in	9	RW	0'h	Line Out Left Volume Output Source Select 0: VMID (No input) 1: DAC Left Channel
sel_lo_r_in	8	RW	0'h	Line Out Right Volume Output Source Select 0: VMID (No input) 1: DAC Right Channel
Reserved	7:2	R	01'h	Reserved
en_dac_lo	1	RW	0'b	DAC Direct Output to LINE_OUT Control 0: Normal 1: Enable direct output
Reserved	0	R	0'b	Reserved

8.6. Reg-34h: Stereo Audio Serial Data Port Control

Default: 8000'h

Table 15. MX34 Stereo Audio Serial Data Port Control

Name	Bits	RW	Default	Description
sel_i2s_mode	15	RW	1'h	Main Serial Data Port Mode Selection 0: Master 1: Slave
Reserved	14:8	R	0'h	Reserved
ctrl_i2s_bclk_polarity	7	RW	0'h	Stereo I²S BCLK Polarity Control 0: Normal 1: Invert
Reserved	6:5	R	0'h	Reserved
en_dac_lrck_swap	4	RW	0'h	DAC Data L/R Swap 0: DAC data appears at left phase of LRCK 1: DAC data appears at right phase of LRCK *Note: Support to I²S & PCM.*
sel_i2s_data_len	3:2	RW	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
sel_i2s_data_format	1:0	RW	0'h	Stereo PCM Data Format Selection 00: I²S format 01: Left justified 10: PCM Mode A (LRCK One Plus at Master Mode) 11: PCM Mode B (LRCK One Plus at Master Mode)

8.7. Reg-38h: Stereo DAC Clock Control

Default: 2000'h

Table 16. MX38 Stereo DAC Clock Control

Name	Bits	RW	Default	Description
sel_i2s_pre_div	15:13	RW	1'h	I²S Pre-Divider 000b: ÷1 001b: ÷2 010b: ÷4 011b: ÷8 100b: ÷16 101b: ÷32 Others: Reserved
sel_i2s_bclk_ms	12	RW	0'b	Master Mode Clock Relative to BCLK and LRCK 0b: 32bits (64FS) 1b: 16bits (32FS)
Reserved	11:3	R	0'h	Reserved
sel_dac_filter_clk	2	RW	0'b	Stereo DAC Filter Clock Select 0b: 256Fs 1b: 384Fs
Reserved	1:0	R	0'h	Reserved

8.8. Reg-3Ah: Power Management Addition 1

Default: 0000'h

Table 17. MX3A Power Management Addition 1

Name	Bits	RW	Default	Description
en_main_i2s	15	RW	0'h	I^2S Digital Interface Enable 0: Disable 1: Enable
pow_zcd	14	RW	0'h	All Zero Cross Detect Power Down (Including Digital) 0: Disable 1: Enable
Reserved	13:9	R	0'h	Reserved
pow_softgen	8	RW	0'h	Power on Softgen 1: Power on 0: Power down *Note: When pow_softgen=1, whether the LINE_OUT can be driven depends on the level on Cdepop (depneds on depop mode selection)*
Reserved	7:6	R	0'h	Reserved
en_lo_out_amp	5	RW	0'h	1: Enable LINE_OUT 0: Disable
en_lo_enhance_amp	4	RW	0'h	1: Enable LINE_OUT enhance output amplifier 0: Disable (DPOP mode or normal loading mode)
Reserved	3:0	R	0'h	Reserved

The following table describes Bit 4 & Bit 5:

Table 18. LINE_OUT Drive Ability Selection

en_lo_out_amp	en_lo_enhance_amp	Description
0'b	0'b	LINE Output Off
0'b	1'b	Not Used
1'b	0'b	LINE Output for High-Impedance Loading (>KOhm)
1'b	1'b	LINE Output for Low-Impedance Loading (<100Ohm), acts as Headphone Amplifier

8.9. Reg-3Ch: Power Management Addition 2

Default: 0000’h

Table 19. MX3C Power Management Addition 2

Name	Bits	RW	Default	Description
Reserved	15:14	R	0’h	Reserved
pow_vref	13	RW	0’h	0: Disable 1: Enable VREF for All analog circuit
pow_pll	12	RW	0’h	0: Disable 1: Enable PLL
Reserved	11	RW	0’h	Reserved (Must be Set to ‘0’)
pow_dac_ref	10	RW	0’h	0: Disable 1: Enable DAC reference circuit
pow_dac_l	9	RW	0’h	0: Disable 1: Enable left STEREO DAC and its filter clock
pow_dac_r	8	RW	0’h	0: Disable 1: Enable right STEREO DAC and its filter clock
pow_dacl2hpmux_direct	7	RW	0’h	0: Disable 1: Enable left DAC to hpmux and direct path power
pow_dacr2hpmux_direct	6	RW	0’h	0: Disable 1: Enable Right DAC to hpmux and direct path power
pow_lo_l	5	RW	0’h	0: Disable 1: Enable left LINE_OUT
pow_lo_r	4	RW	0’h	0: Disable 1: Enable right LINE_OUT
Reserved	3:0	R	0’h	Reserved

8.10. Reg-3Eh: Power Management Addition 3

Default: 0000’h

Table 20. MX3E Power Management Addition 3

Name	Bits	RW	Default	Description
pow_main_bias	15	RW	0’h	0: Disable 1: Enable Main bias of analog circuit
Reserved	14:11	R	0’h	Reserved
pow_lo_l_vol	10	RW	0’h	0: Disable 1: Enable LINE_OUT_L volume control
pow_lo_r_vol	9	RW	0’h	0: Disable 1: Enable LINE_OUT_R volume control
Reserved	8:0	R	0’h	Reserved

8.11. Reg-40h: General Purpose Control

Default: 0100'h

Table 21. MX40 General Purpose Control

Name	Bits	RW	Default	Description
Reserved	15:9	R	0'h	Reserved
en_dac_hpf	8	RW	1'h	STEREO DAC High Pass Filter 0: Disable 1: Enable
Reserved	7:0	R	0'h	Reserved

8.12. Reg-42h: Global Clock Control

Default: 0000'h

Table 22. MX42 Global Clock Control

Name	Bits	RW	Default	Description
sel_sysclk	15	RW	0'h	Clock Source MUX Control 0: XTI 1: PLL
sel_pll_sour	14	RW	0'h	PLL Source Select 0: From XTI 1: From BIT_CLK
Reserved	13:3	R	0'h	Reserved
sel_pll_pre_div	0	RW	0'b	PLL Pre Divider 0b: ÷1 1b: ÷2

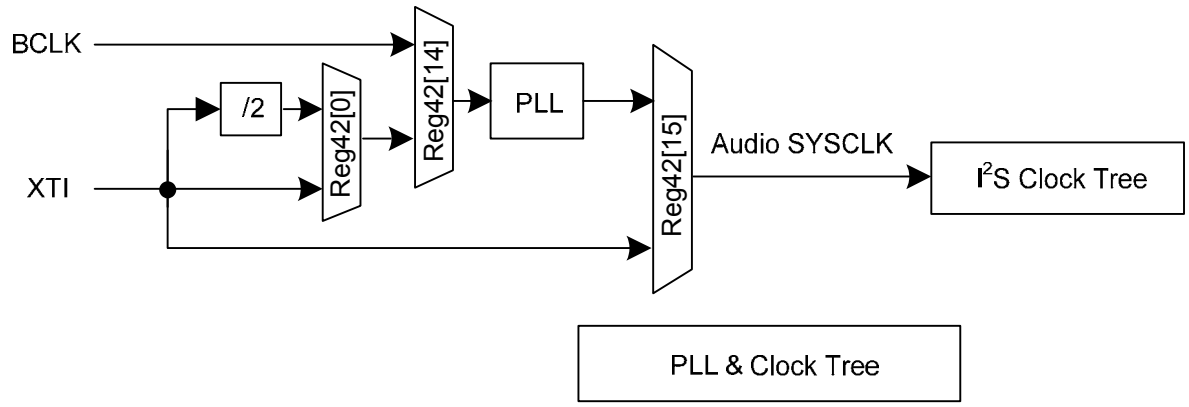


Figure 14. Global Clock Control

8.13. Reg-44h: PLL M/N Code Control

Default: 0000'h

Table 23. MX44 PLL M/N Code Control

Name	Bits	RW	Default	Description
sel_pll_n_code	15:8	RW	00'h	N[7:0] Code for Analog PLL 00000000: Div 2 00000001: Div 3 …… 11111111: Div 257
sel_pll_m_bypass	7	RW	0'h	Bypass PLL M 0b: No bypass 1b: Bypass
sel_pll_k_code	6:4	RW	0'h	K[2:0] Code for Analog PLL 000: Div 2 001: Div 3 …… 111: Div 9
sel_pll_m_code	3:0	RW	0'h	M[3:0] Code for Analog PLL 0000: Div 2 0001: Div 3 …… 1111: Div 17

8.14. Reg-5Ch: MISC1 Control

Default: 0000'h

Table 24. MX5C MISC1 Control

Name	Bits	RW	Default	Description
Reserved	15:12	R	0'h	Reserved
en_lo_l_dezero	11	RW	0'h	LINE Out Left Zero Cross Detector Control 0: Disable 1: Enable
en_lo_l_softvol	10	RW	0'h	LINE Out Left Soft Volume Change Control 0: Disable 1: Enable
en_lo_r_dezero	9	RW	0'h	LINE Out Right Zero Cross Detector Control 0: Disable 1: Enable
en_lo_r_softvol	8	RW	0'h	LINE Out Right Soft Volume Control 0: Disable 1: Enable
Reserved	7:4	R	0'h	Reserved
en_dac_zc	3	RW	0'b	Enable DAC Digital Volume Zero Crossing Detect 0: Disable 1: Enable
en_dac_soft_vol	2	RW	0'b	Enable DAC Digital Soft Volume 0: Disable 1: Enable
Reserved	1:0	R	0'h	Reserved

Note: When zero cross detector is enabled, change mute volume only on zero crossing or after timeout.

8.15. Reg-5Eh: MISC2 Control

Default: 0000'h

Table 25. MX5E MISC2 Control

Name	Bits	RW	Default	Description
en_vref_fastb	15	RW	0'b	Enable Fast Vref (This Bit must be Disabled in Normal Use) 0: Enable fast Vref 1: Disable fast Vref
en_thermal_shutdown	14	RW	0'b	Thermal Shut Down Enable 0: Disable 1: Enable
Reserved	13:10	R	0'h	Reserved
en_dp2_lo	9	RW	0'h	Enable De-Pop Mode 2 of Line Out 0: Disable 1: Enable
en_dp1_lo	8	RW	0'h	Enable De-Pop Mode 1 of Line Out 0: Disable 1: Enable
en_smt_lo_l	7	RW	0'h	Enable Line Out Left Mute-Unmute Depop 0: Disable 1: Enable
en_smt_lo_r	6	RW	0'h	Enable Line Out Right Mute-Unmute Depop 0: Disable 1: Enable
smt_en	5	RW	0'h	Mute-Unmute Depop 0: Disable 1: Enable
Reserved	4	R	0'h	Reserved
mute_dac_l	3	RW	0'h	Mute Main DAC Left Input 0: On 1: Mute (-∞ dB)
mute_dac_r	2	RW	0'h	Mute Main DAC Right Input 0: On 1: Mute (-∞ dB)
Reserved	1:0	R	0'h	Reserved

8.16. Reg-6Ah: Private Register Index

Default: 0000'h

Table 26. MX6A Private Register Index

Name	Bits	RW	Default	Description
Reserved	15:7	R	0'h	Reserved
private_reg_index	6:0	RW	0'h	Private Register Index

8.17. Reg-6Ch: Private Register Data

Default: 0000’h

Table 27. MX6C Private Register Data

Name	Bits	RW	Default	Description
private_reg_data	15:0	RW	0’h	Private Register Data Port

8.18. Private-39h: Digital Internal Register

Default: 8800’h

Table 28. PR39 Digital Internal Register

Name	Bits	RW	Default	Description
sel_pad_drive	15	RW	1’h	Pad Drive Capability 0b: 5mA 1b: (5+6) 11mA
Reserved	14:12	R	0’b	Reserved
osc_curr	11:9	RW	100’b	Oscillator Drive Current Control 000: 1x bias current 001: 2x 010: 4x 011: 8x 100: 16x …….. 111: 128x *Note: The oscillator startup current is set to maximum, and controlled by osc_curr after 512 clocks. The digital clock input is enabled after 1024 clocks.*
Reserved	8:0	R	0’b	Reserved

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 29. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DCVDD	-0.3	-	3.63	V
Digital Power for IO and PLL	DBVDD	-0.3	-	3.63	V
Analog Power	AVDD	-0.3	-	3.63	V
Ambient Operating Temperature	Ta	-20	-	+85	°C
Storage Temperature	Ts	-40	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 30. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.8	3.3	3.6	V
Digital Core	DCVDD	1.8	3.3	3.6	V
Analog	AVDD	2.3	3.3	3.6	V

Note: A 1μF Capacitor must be connected from AVDD to AGND, and should be placed as close as possible to the AVDD pin of the ALC5629.

9.1.3. Static Characteristics

DBVDD= 3.3V, $T_{ambient}$=25°C, with 25pF external load.

Table 31. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DBVDD +0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.33*DBVDD	V
High Level Input Voltage	V_{IH}	0.66*DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9*DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1*DBVDD	V
Low Level Input Voltage (JD2)	V_{IL}	-	-	0.33*AVDD	V
High Level Input Voltage (JD2)	V_{IH}	0.66*AVDD	-	-	V

9.2. Analog Performance Characteristics

Standard Test Conditions

- $T_{ambient}$=25°C, DBVDD=DCVDD=1.8V, AVDD=3.3V, 1kHz input sine wave; Sampling Frequency=48kHz; 0dB=1Vrms, 10KΩ/50pF load; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation

Table 32. Analog Performance Characteristics

Parameter	Minimum	Typical	Maximum	Units
Full-Scale Output Voltage LINE_OUT Outputs	-	1.0	-	Vrms
S/N (A Weighted) LINE_OUT	-	95	-	dBFS
THD+N LINE_OUT	-	-80	-	dBFS
Power Supply Rejection (217Hz)	-	-50	-	dB
Amplifier Gain Step	-	1.5	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
LINE_OUT Output Power (RL=16Ω) (en_hp_enhance_amp='1')	25	45	-	mW
Digital Power Supply Current (Power Down Mode) DCVDD=1.8V, DBVDD=1.8V (Include POR Circuit)	-	-	10	µA
Analog Power Supply Current (DAC to Headphone Without Load) AVDD=DCVDD=DBVDD=3.3V	-	8	-	mA
Analog Power Supply Current (Power Down Mode) AVDD=3.3V	-	-	1	µA
VREF Output Voltage	-	0.5	-	AVDD
VREF Rising Time at Fast Mode (C=4.7µF)	-	-	50	ms

9.3. AC Timing Characteristics

9.3.1. I²C Control Interface

Table 33. I²C Control Interface Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Clock Pulse Duration	$t_{w(9)}$	1.3	-	-	µs
Clock Pulse Duration	$t_{w(10)}$	600	-	-	ns
Clock Frequency	f	0	-	400K*	Hz
Re-Start Setup Time	$t_{su(6)}$	600	-	-	ns
Start Hold Time	$t_{h(5)}$	600	-	-	ns
Data Setup Time	$t_{su(7)}$	100	-	-	ns
Data Hold Time	$t_{h(6)}$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su(8)}$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

Note: '' indicates the host must provide MCLK higher than 4MHz to the ALC5629 during I²C control interface access. If MCLK provides 128*8KHz, the I²C clock frequency can only support 100KHz.*

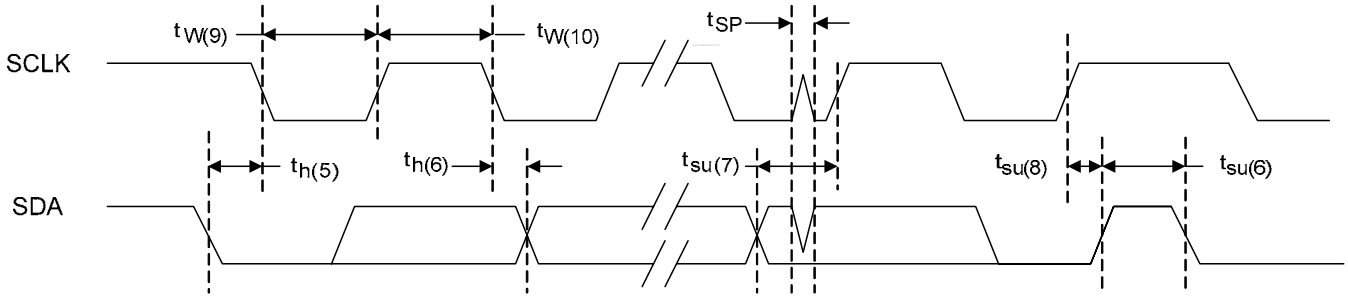


Figure 15. I²C Control Interface Waveform

9.3.2. I²S/PCM Interface Master Mode

Table 34. I²S Master Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

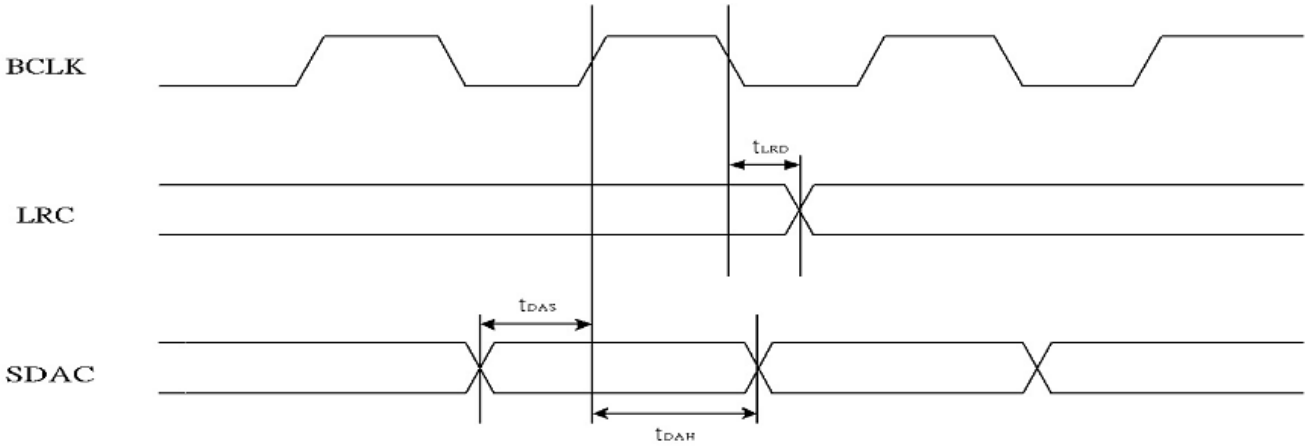


Figure 16. I²S Master Mode Waveform

9.3.3. I²S/PCM Interface Slave Mode

Table 35. I²S Slave Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

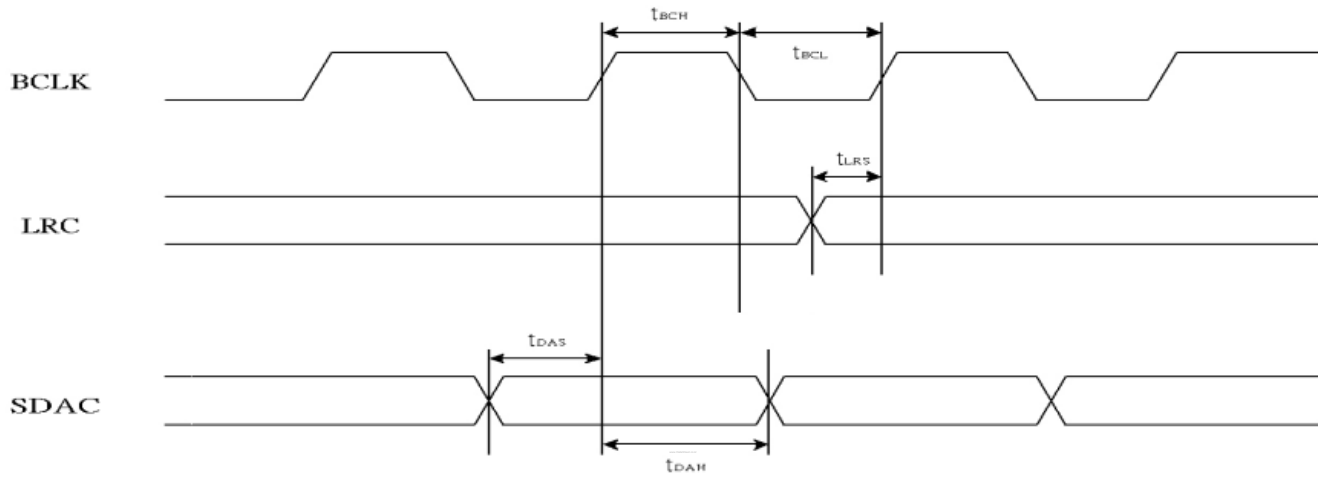


Figure 17. I²S Slave Mode Waveform

10. Application Circuits

Application circuits are for design reference only. System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, Realtek should confirm modifications of application circuits.

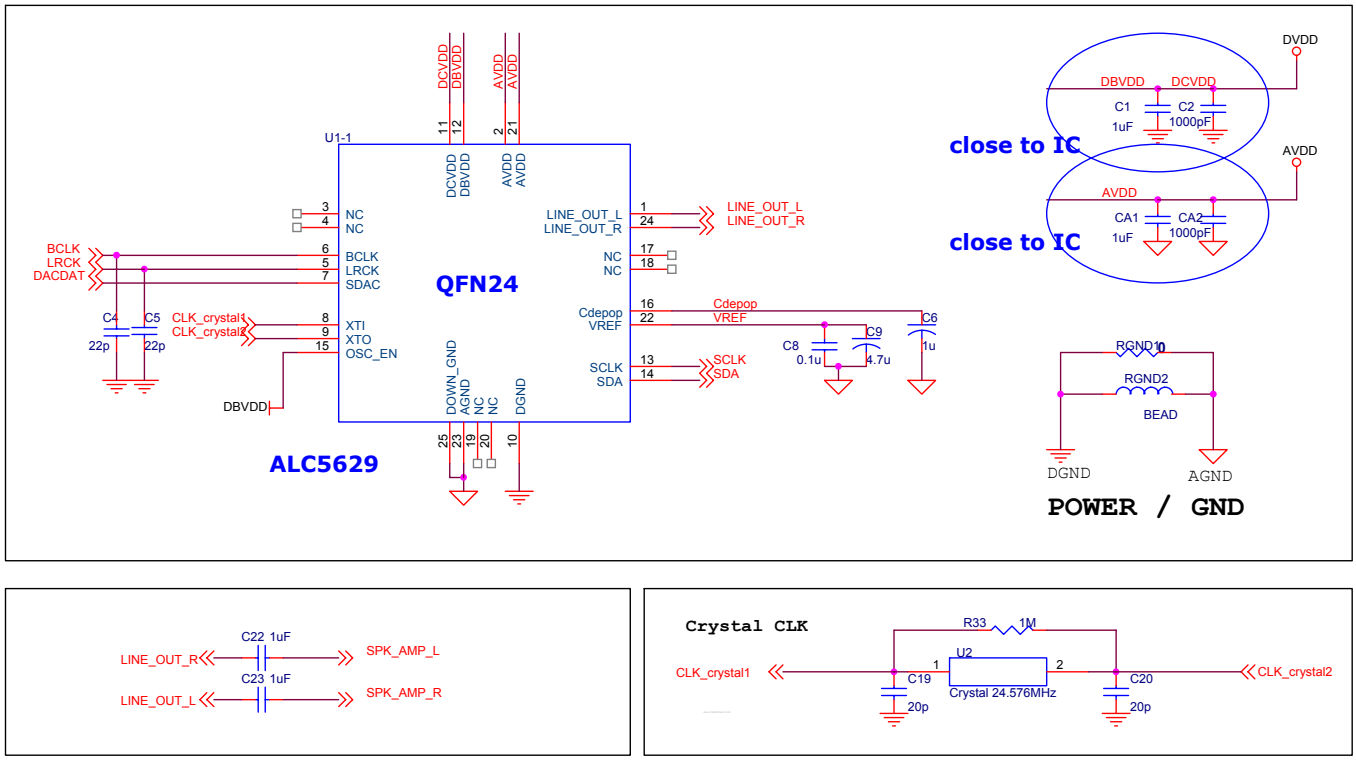
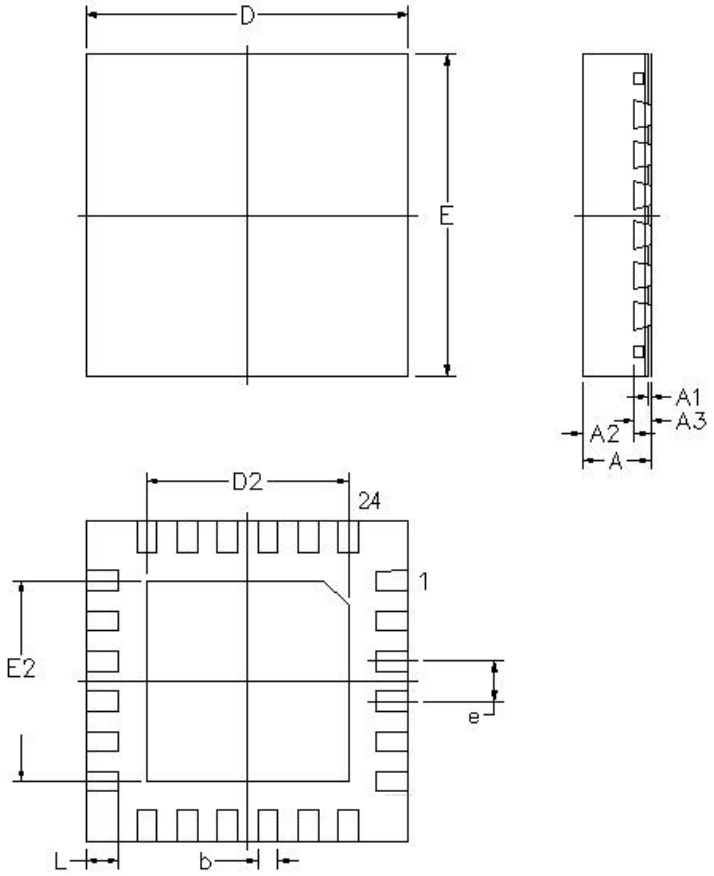


Figure 18. Application Circuits

11. Mechanical Dimensions

QFN-24 Package; 4x4mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	-	0.65	0.70	-	0.026	0.028
A_3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.00 BSC			0.158 BSC		
D_2/E_2	2.00	2.25	2.50	0.078	0.088	0.098
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Ordering Information

Table 36. Ordering Information

Part Number	Package	Status
ALC5629-GR	QFN-24 in 'Green' Package (Tray)	Mass Production
ALC5629-GRT	QFN-24 in 'Green' Package (Tape & Reel)	Mass Production

Note: See page 6 for package and version identification.

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