REALTEK

ALC5633Q

I^2C + I^2S Stereo Audio Codec
Mono Class-AB/D Amp

Datasheet

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC5633Q Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2010/06/24	Preliminary version

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1. General Description

The ALC5633Q is a high performance I^{2}S/PCM interface audio codec. The main functions have Stereo Codec, Stereo Headphone Output, Stereo Differential Input, Stereo Line Input and Mono Class-AB/D Speaker Amplifier.

For audio inputs, one stereo differential microphone inputs, one stereo single-ended line inputs and stereo digital microphone inputs. For audio outputs, one stereo line outputs and mono differential speaker output or stereo single-ended headphone outputs.

The powerful Auto-Level-Control (ALC) function is for playback and record. For playback, it will keep the same output level when different input level. And prevent the output signal be clipped when speaker power is dropping or huge input signal. For record, it can boost recorded data when small signal input or limit recorded data when large signal input. For noise gate function of ALC, it can effective to reduce the background noise when no speaking voice for voice recording. A flexible hardware 7-band equalizer with configurable gain, bandwidth and center frequency that enriches the sound experience.

Low power consumption design on ALC5633Q is suitable for portable devices. Also the ALC5633Q is available in a 5x5mm 'Green' QFN-32 package.

2. Features

- Digital-to-Analog Converter with 98dBA SNR and –90dB THD+N
- Analog-to-Digital Converter with 93dBA SNR and –90dB THD+N
- Mono BTL (Bridge-Tied Load) / Stereo SE (Single-Ended) Class-AB/D amplifier and with
  650mW/Ch output power (SPKVDD=3.6V, THD = 1%, 8Ω load, Class-D Mode)
  2W/Ch output power (SPKVDD=5.0V, THD = 1%, 4Ω load, Class-D Mode)
- Stereo differential analog microphone inputs with multi-step boost pre-amplifiers and low noise microphone bias
- Audio jack insert detection and microphone switch detection
- Power management and enhanced power saving
- Support flexible digital 7 bands equalizer (EQ) and wind filter
- Support analog to analog path with EQ function
- Support digital spatial sound and pseudo stereo effect
- Zero detection and soft volume for pop noise suppression
- Inside PLL can receive wide range clock input
- Digital beep generator
- Support I^{2}C control interface
- 24bit/8kHz ~ 192kHz I^{2}S/PCM interface for stereo DAC
- 24bit/8kHz ~ 96kHz I^{2}S/PCM interface for stereo ADC
- Support enhanced Auto Level Control (ALC) function for playback and record
- QFN-32 (5mm x 5mm) package

3. System Application

- Tablet PC system/Ultra-Mobile PC (UMPC)
- Portable Navigation Device

4. Function Block and Mixer Path

4.1. Function Block

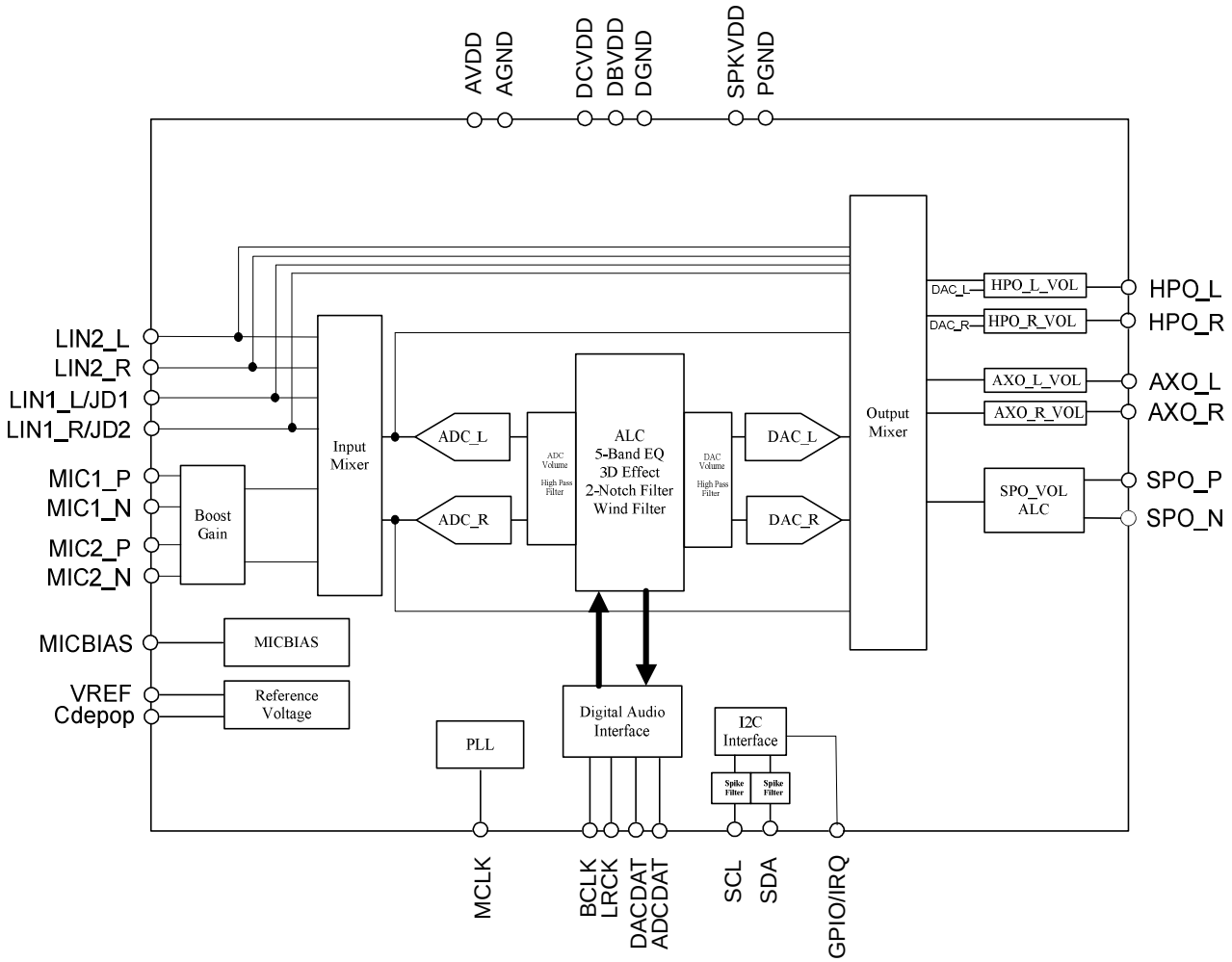


Figure 1. Block Diagram

4.2. Audio Mixer Path

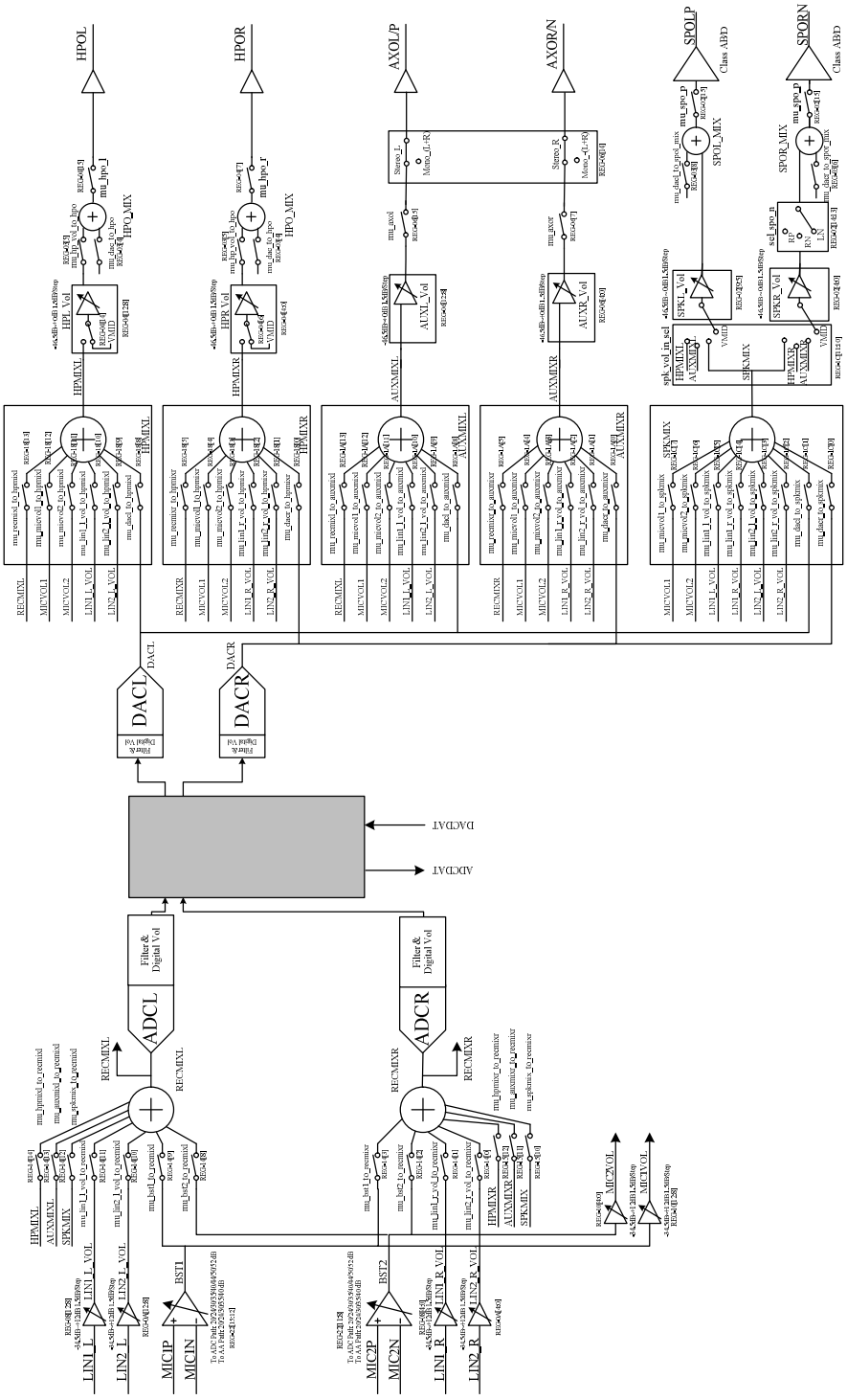


Figure 2. Audio Mixer Path

5. Pin Assignments

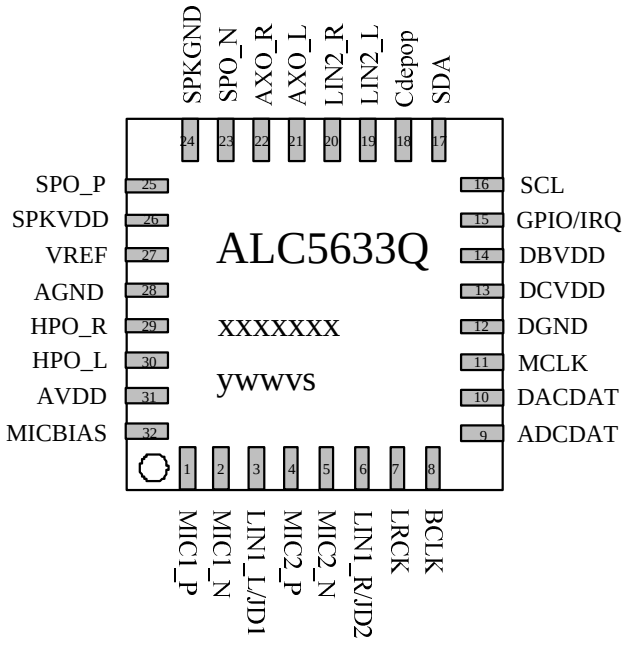


Figure 3. Pin Assignments

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LRCK	I/O	7	Digital audio synchronous signal	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
BCLK	I/O	8	Digital audio serial clock	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
ADCDAT	O	9	Serial ADC data output	V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD
DACDAT	I	10	Serial DAC data input	Schmitt trigger
MCLK	I	11	Master clock input	Schmitt trigger
GPIO/IRQ	I/O	15	General purpose input/output Interrupt output	Output: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Input: Schmitt trigger
SCL	I	16	I^2C clock	Schmitt trigger
SDA	I/O	17	I^2C data	Open Drain
				Total: 8 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MIC1P	I	1	Microphone 1 differential positive input	Analog input
MIC1N	I	2	Microphone 1 differential negative input	Analog input
MIC2P	I	4	Microphone 2 differential positive input	Analog input
MIC2N	I	5	Microphone 2 differential negative input	Analog input
LIN1_L/JD1	I	3	Line 1 left channel input Jack detection input 1	Analog input
LIN1_R/JD2	I	6	Line 1 right channel input Jack detection input 2	Analog input
LIN2_L	I	19	Line 2 left channel input	Analog input
LIN2_R	I	20	Line 2 right channel input	Analog input
AXO_L	O	21	Auxiliary left channel output	Analog output
AXO_R	O	22	Auxiliary right channel output	Analog output
SPO_N	O	24	Right speaker negative output	Analog output
SPO_P	O	25	Left speaker positive output	Analog output
HPO_R	O	29	Headphone right channel output	Analog output
HPO_L	O	30	Headphone left channel output	Analog output
				Total: 14 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition

VREF	O	27	Internal Reference voltage	2.2uf capacitor to analog ground
MICBIAS	O	32	MIC BIAS Voltage output	Programmable Analog DC output with 3mA drive
Cdepop	O	18	Depop capacitor for headphone output	Capacitor to analog ground
				Total: 3 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
DGND	P	12	Digital ground	Ground
SPKGND	P	24	Speaker ground	Ground
AGND	P	28	Analog ground	Ground
DCVDD	P	13	Digital power for digital core	1.71V~3.6V
DBVDD	P	14	Digital power for digital I/O	1.71V~3.6V
SPKVDD	P	26	Speaker power	3.0V~5.5V
AVDD	P	31	Analog power	2.3V~3.6V
				Total: 7 Pins

7. Function Description

7.1. Power

There are different power types in ALC5633Q. DBVDD is for digital I/O power, DCVDD is for digital core power, AVDD is for analog power (include analog I/Os, Video Buffer and Touch Panel Controller) and SPKVDD is for speaker amplifier power.

The power supplier limit condition is DBVDD ≧ DCVDD and SPKVDD ≧ AVDD, AVDD ≧ DCVDD, and for the best performance, our design setting is show on below.

Table 5. Power Supply for Best Performance

Power	DBVDD	DCVDD	AVDD	SPKVDD
Setting	3.3V	3.3V	3.3V	4.2V

7.2. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 5. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write REG-MX00h	Reset all registers to default values except some specify control registers and logic.

7.2.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC5633Q (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 6. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: V_{POR_OFF} must be below V_{POR_ON}.

7.2.2. Software Reset

When REG-MX00h is wrote, all registers become to default value.

7.3. Clocking

The system clock of ALC5633Q can be selected from MCLK or PLL. MCLK is always provided externally while the reference clock of PLLs can be selected from MCLK or BCLK.

The I2S_SYSCLK(Main SYSCLK) provides clocks into ADC that can be selected from MCLK or PLL. The driver should arrange the clock of each block and setup each divider in order to provide I2S_SYSCLK=256 or 384*Fs set by sel_adc_filter_clk as Audio internal system clock. Refer to Figure 3. Audio SYSCLK

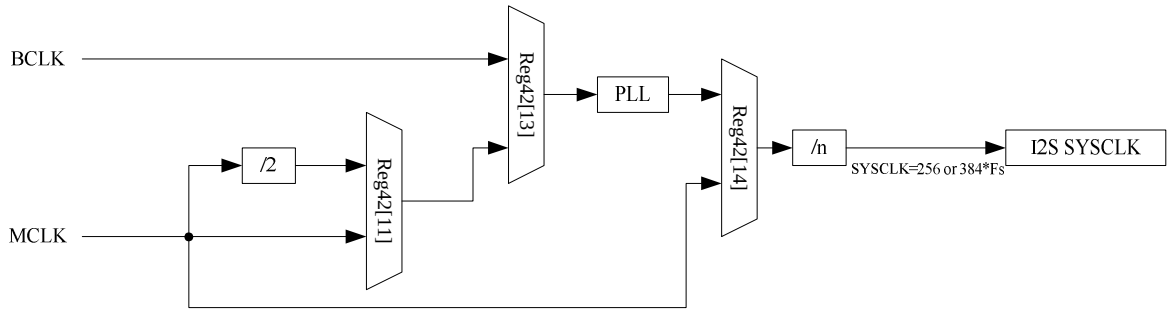


Figure 4. Audio Clock

7.3.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. The source of the PLL can be set to MCLK or BCLK by setting register.

The driver can set up the PLL to output a frequency close to the system clock.

The PLL transmit formula is:

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 7. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6

MCLK	N	M	F_{VCO}	K	F_{OUT}
19.68	78	14	98.4	2	24.6

Table 8. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

After a POR Reset, PLL related Registers are reset to default values, however, they are not reset to default values after a soft-reset (write REG-MX00). Firmware should not power down the PLL when the PLL output is used as system clock.

7.3.2. I^2C and Stereo I^2S

The ALC5633Q supports I^2C for the digital control interface, and has I^2S/PCM for the digital data interface. The I^2S/PCM audio digital interface is used to input data to a stereo DAC or output data from a stereo ADC. The I^2S/PCM audio digital interface can be configured to Master mode or Slave mode.

Master Mode

In master mode BCLK and LRCK are configured as output.

When MCLK is used as I2S SYSCLK source, PLL can be disabled and sel_sysclk=0'b. The MCLK is used as system clock.

When PLL output is used as I2S SYSCLK source PLL enabled and sel_sysclk=1'b, PLL should be configured to support 256 or 384*Fs onto I2S SYSCLK.

Slave Mode

In slave mode BCLK and LRCK are configured as input. The I2S SYSCLK can be input from MCLK by providing BCLK synchronized clock externally or from BCLK with PLL to generate 256 or 384*Fs as I2S SYSCLK. The driver should set each divider to arrange the clock distribution.

7.4. Digital Data Interface

7.4.1. Stereo I²S/PCM Interface

The stereo I²S/PCM interface can be configured as master mode or slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- I²S mode

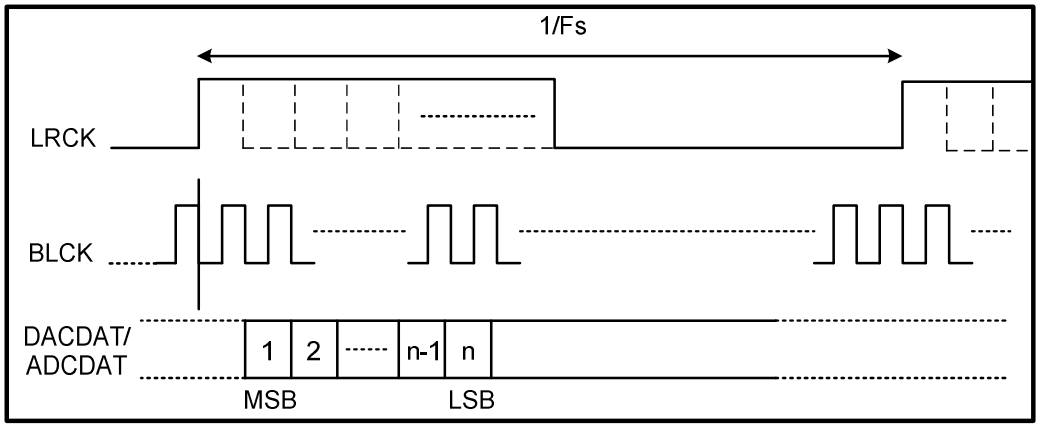


Figure 4. PCM MONO Data Mode A Format (BCLK POLARITY=0)

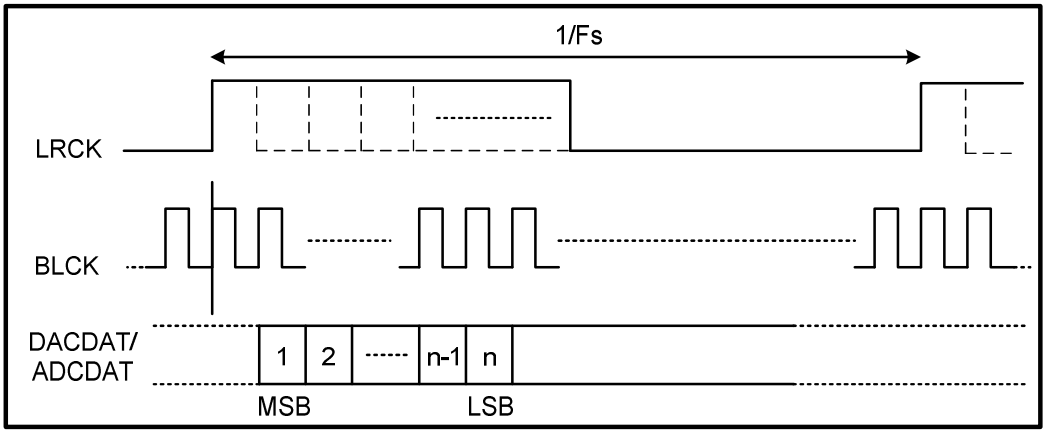


Figure 5. PCM MONO Data Mode A Format (BCLK POLARITY=1)

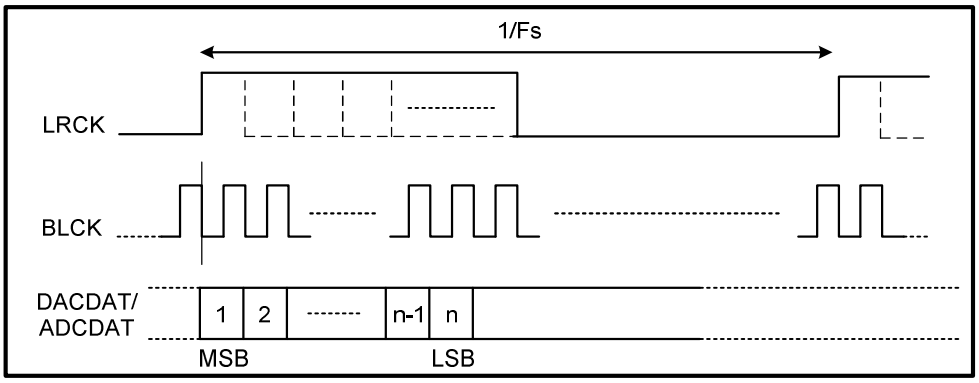


Figure 6. PCM MONO Data Mode B Format (BCLK POLARITY=0)

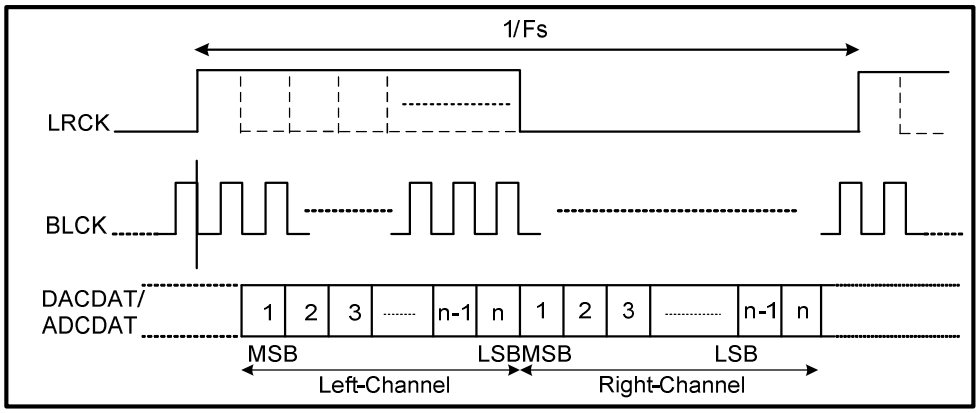


Figure 7. PCM Stereo Data Mode A Format (BCLK POLARITY=0)

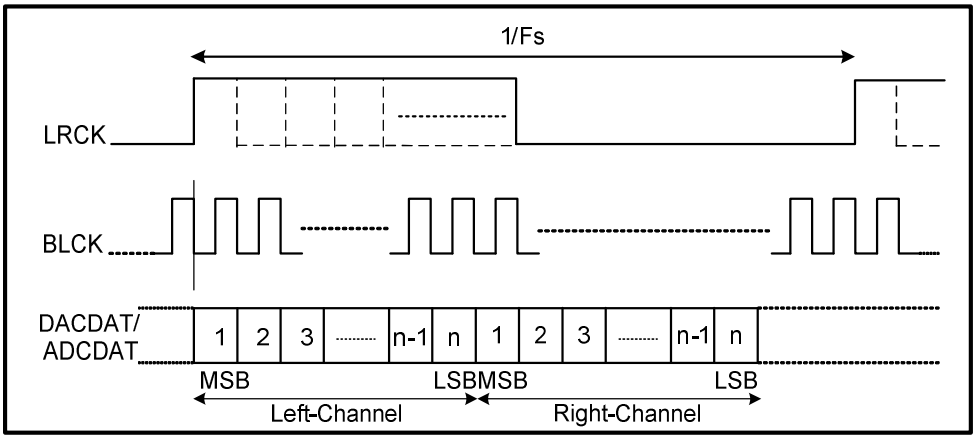


Figure 8. PCM Stereo Data Mode B Format (BCLK POLARITY=0)

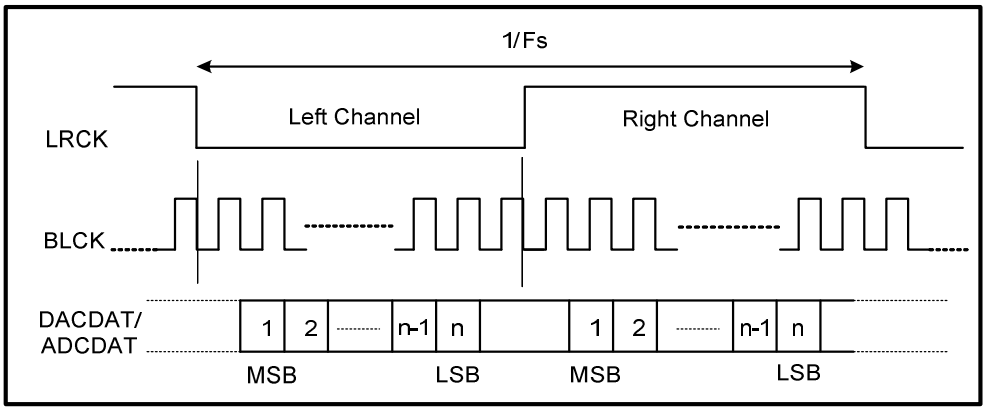


Figure 9. I²S Data Format (BCLK POLARITY=0)

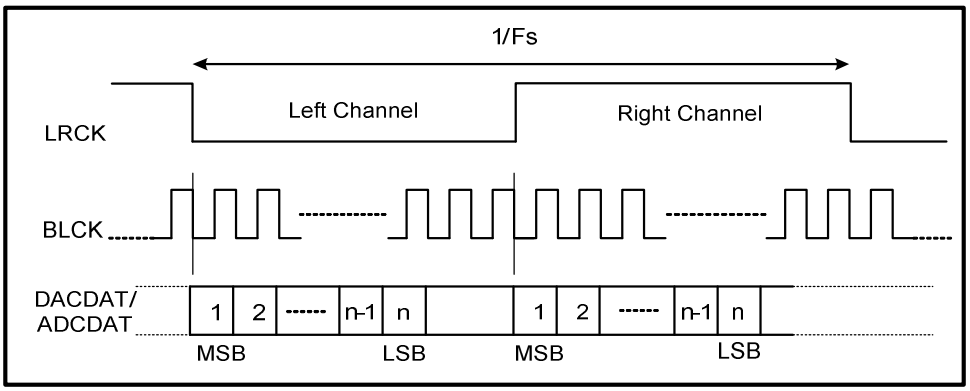


Figure 10. Left-Justified Data Format (BCLK POLARITY=0)

7.5. Audio Data Path

7.5.1. Stereo ADC

The stereo ADC is a high performance ADC. The full scale input of ADC is 1Vrms at AVDD is 3.3V. In order to save power, the left and right ADC can be powered down separately by setting the related register. The volume control of the stereo ADC is also can set by registers.

7.5.2. Stereo DAC

The stereo DAC is a high performance DAC. The sampling rate can be configured by setting the stereo I^2S clock divider. The volume control of the stereo DAC is set by registers.

7.5.3. Mixers

There are seven analog mixers in ALC5633Q.

- **Headphone mixer - HPMIXL/R**

  The stereo headphone mixer can do mixing for DAC outputs and analog inputs. The mixer output is mainly for headphone output. Each input path has mute function to the mixer block.

  At headphone output has another mixer for headphone volume output and direct DAC output. From headphone volume output has it's volume control and from DAC is also has it's volume control – digital volume. For different source and independent volume control, can use this mixer to implement.

- **Speaker mixer – SPKMIX**

  The speaker mixer can do mixing for DAC outputs and analog inputs. The mixer output is for speaker output. Each input path has it's mute function to the mixer block.

- **Aux Output mixer – AUXMIXL/R**

  The stereo analog mixer can do mixing for analog input and DAC output. The mixer output is for line-out output for drive external amplifier. Each input path has individual mute function to the mixer block.

- **Record mixer – RECMIXL/R**

  The stereo analog mixer can do mixing for analog input and output mixer. The mixer output is for ADC input. Each input path has it's mute function to the mixer block.

  # Each mixer has it's power down control by register. And can power down single channel of stereo mixer independent. It can easy to control the power management to achieve enhance power saving.

7.6. Analog Audio Input Path

The ALC5633Q supports four analog audio input ports:

- **MIC1P/N**

  The microphone input port-1 can configure as mono differential input or mono single-ended input. The microphone input port has it's microphone bias and microphone boost. High performance microphone bias can improve the recording performance and increase the microphone sensitivity. Multi-steps microphone boost gain can easy to use for microphone application.

- **MIC2P/N**

  The microphone input port-2 can configure as mono differential input or mono single-ended input. The microphone input port has it's microphone bias and microphone boost. High performance microphone bias can improve the recording performance and increase the microphone sensitivity. Multi-steps microphone boost gain can easy to use for microphone application.

- **LIN1_L/R**

  The input port is a stereo single-ended input. It has input volume for tuning. The volume range is from +12dB to -34.5dB and with 1.5dB/step.

- **LIN2_L/R**

  The input port is a stereo single-ended input. It has input volume for tuning. The volume range is from +12dB to -34.5dB and with 1.5dB/step.

7.7. Analog Audio Output Path

The ALC5633Q supports three type output paths:

- **SPO_L/R_P/N**

  The speaker output of ALC5633Q can configured as a mono BTL output or stereo single-end outputs. The power of speaker amplifier is an individual power pin and higher than AVDD. So the input and output of speaker amplifier has a gain ratio to enlarge or reduce the income analog signal. The gain ratio setting can be controlled by auto-mode or manual-mode. The input source of the speaker output port is mixing from DAC and SPKVOL.

- **HPO_L/R**

  The headphone output of ALC5633Q is a stereo output headphone amplifier. The headphone output's source can mix from HPVOL and DAC output.

- **AXO_L/R_P/N**

  The output type is line output. The output can configure as a mono differential output or stereo single-end outputs. For mono differential output, the data will get from L channel plus R channel.

7.8. ALC Function

The Automatic Level Control (ALC) function is dynamically adjusts the input signal by ALC block to let the output signal to achieve the target level. The ALC5633Q supports playback ALC for DAC and record ALC for ADC.

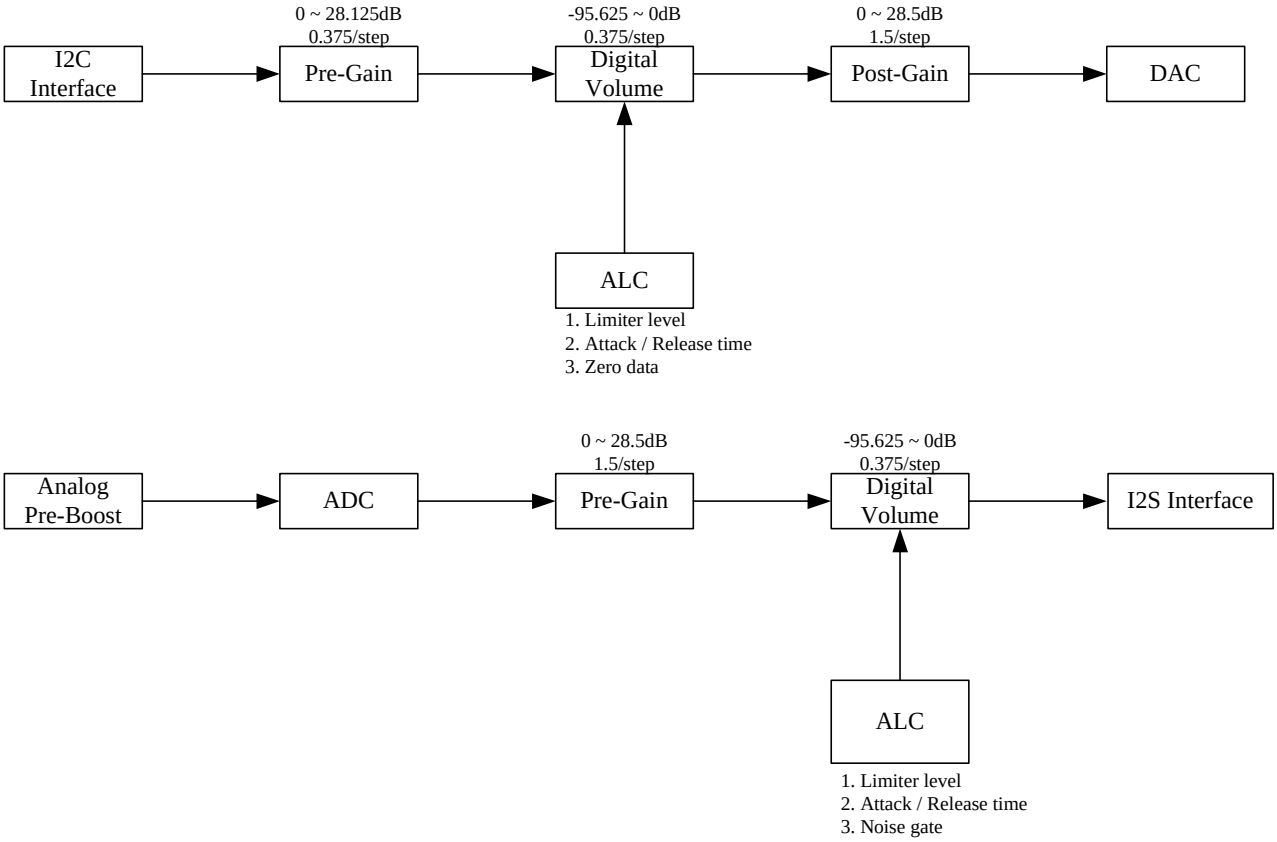


Figure 11. Auto Level Control Block Diagram

Playback Mode:

For DAC playback mode, when the input signal exceeds target threshold, the signal will decrease "ALC Digital Volume" (0.375dB/step at every zero-crossing) until drop to target level then keep the digital volume. When input signal is below the target threshold, the signal will step-up "ALC Digital Volume" (0.375dB/step every zero-crossing) until return to original level. If want to return to the target level, need to set the pre-gain to achieve.

Fine tune parameters:

- Limiter Threshold: 0 ~ -46.5dB, 1.5dB/step
- Attack Rate: T=(4*2^n)/sample rate, n=REG-0x64[12:8]
- Recovery Rate: T=(4*2^n)/sample rate, n=REG-0x64[4:0]

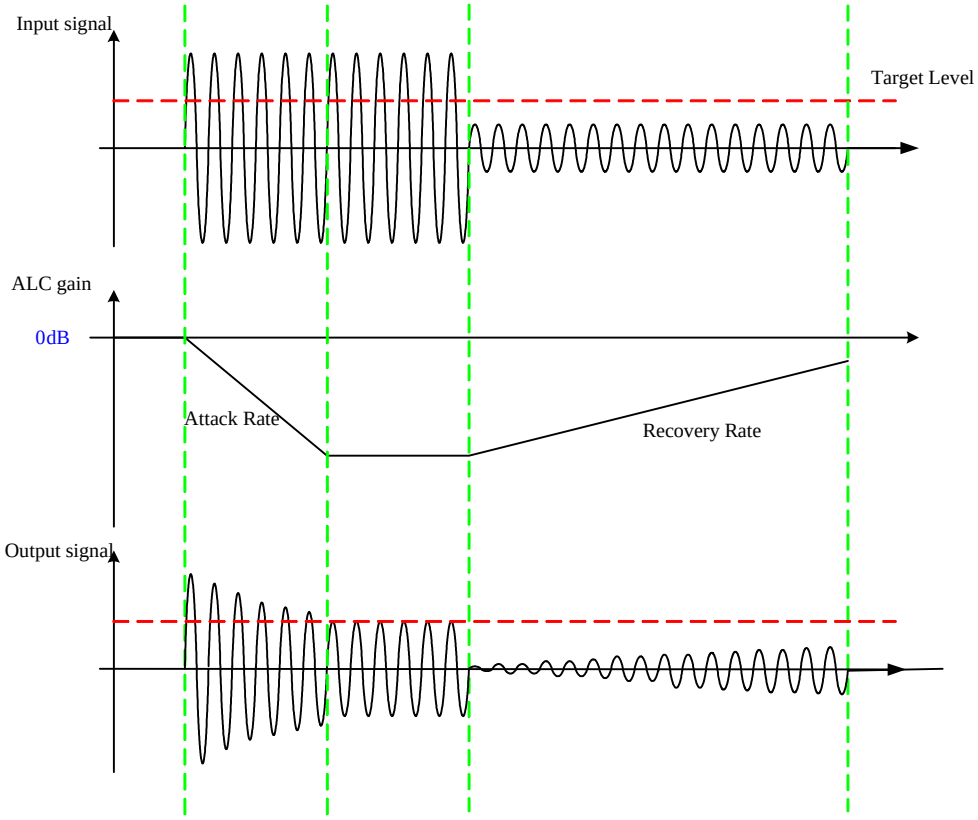


Figure 13. ALC for Playback Mode

Recording Mode:

For ADC recording mode, when the input signal exceeds target threshold, the signal will decrease "ALC Digital Volume" (0.375dB/step at every zero-crossing) until drop to target level then keep the digital volume. When input signal is below the target threshold, the signal will step-up "ALC Digital Volume" (0.375dB/step every zero-crossing) until return to original level. If want to return to the target level, need to set the pre-gain to achieve.

When input signal is below noise gate, the input signal will be reduced and to suppress the background noise. The reducing level can be set by register. And when input signal is above noise gate, the input signal will be boosted to target level.

Fine tune parameters:

- Limiter Threshold: 0 ~ -46.5dB, 1.5dB/step
- Attack Rate: T=(4*2^n)/sample rate, n=REG0x64[12:8]
- Recovery Rate: T=(4*2^n)/sample rate, n=REG0x64[12:8]
- Noise Gate Threshold: -36 ~ -82.5dB, 1.5dB/step
- Reducing Noise Level: 0 ~ 45dB, 3dB/step

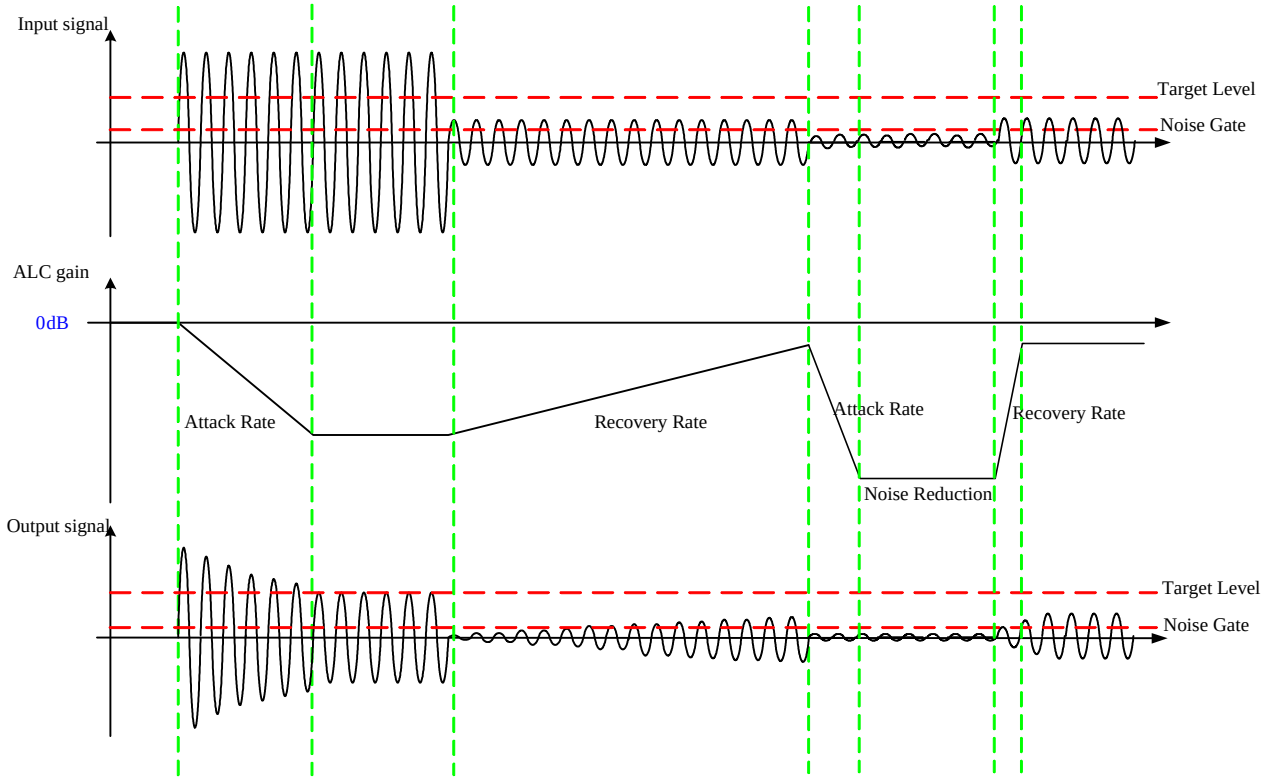


Figure 14. ALC for Recording Mode

7.9. Speaker Amplifier Ratio Gain

Owing to speaker power (SPKVDD) and analog power (AVDD) is different power domain. And normally the speaker power is higher than analog power. So the audio input signal is need to be boost or reduce by a gain and then output from speaker amplifier. When SPKVDD is dropping, the gain need to be reduced to prevent the signal is clipped. And when SPKVDD is rising, the gain need to be boosted to prevent the signal is to small.

Table 10. Ration Gain Table for SPKVDD

SPKVDD	SPKVDD Code	AVDD = 3.3V Ratio Gain	AVDD = 2.5V Ratio Gain
4.6	**111'b**	**TBD**	**TBD**
4.2	**110'b**	**TBD**	**TBD**
4.1	**101'b**	**TBD**	**TBD**
4.0	**100'b**	**TBD**	**TBD**
3.9	**011'b**	**TBD**	**TBD**
3.8	**010'b**	**TBD**	**TBD**
3.6	**001'b**	**TBD**	**TBD**
3.3	**000'b**	**TBD**	**TBD**

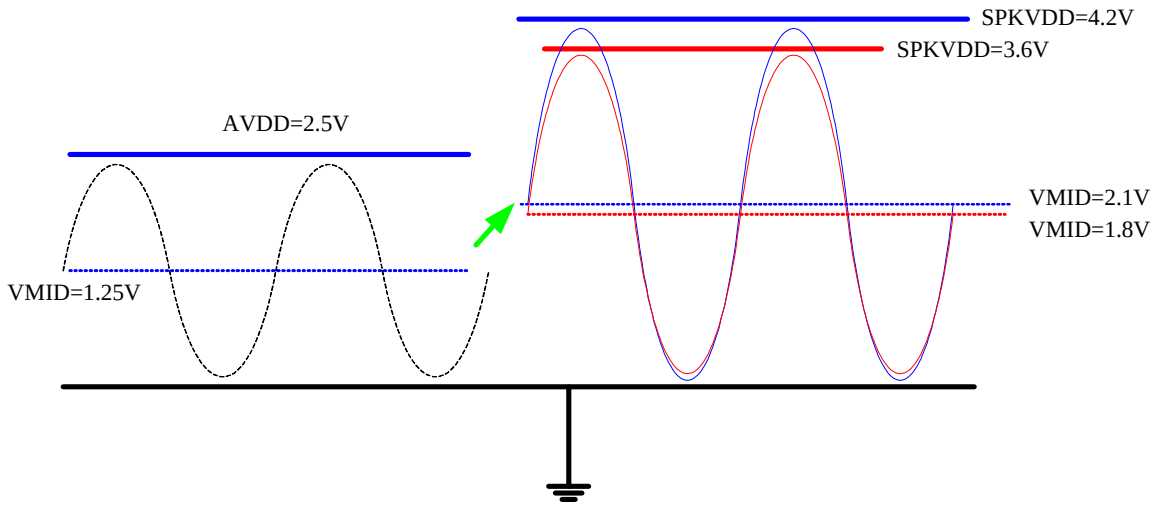


Figure 15. Ratio Gain for SPKVDD and AVDD

7.10. Hardware Sound Processing

The Sound Effect block is composed of Pseudo Stereo, Spatial 3D, and Equalizer blocks. The Pseudo Stereo block is used to convert a MONO source into virtualized stereo output. The Spatial 3D block is a surround sound generator with adjustable amplitude (Gain) and surround depth (Ratio). The Equalizer block can be used to compensate for speaker response, or to make environment sound effects, e.g., 'Pub', 'Live', 'Rock',… etc..

7.10.1. Equalizer Block

The equalizer block cascades 7 bands of equalizer to compensate for speaker response and to emulate environment sound. The 7 bands equalizer are include two high pass filter, four band pass filter and one low pass filter. One high pass filter cascaded in the front end is used to drop low frequency tone, the tone has a large amplitude and may damage a mini speaker.

The high pass filter can also be used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength. Three bands of bi-quad band pass filters are used to emulate environment sounds.

7.10.2. Pseudo Stereo and Spatial 3D Sound

There are two spatial effects in post-processing; the Pseudo-Stereo Effect + Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect converts a MONO signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhancing the spatial effect. The Stereo Expansion Effect enhances the spatial effect when the input signal is Stereo.

7.10.3. Wind Noise Reduction Filter

The wind filter is implemented by a high pass filter equalizer. The wind filter is mainly for ADC recording used. The bandwidth of wind filter is programmable and varies with sample rate. The filter is used to remove DC offset at normal condition, and wind noise reduction at application mode.

Wind Filter fc decision by filter coefficient

The setting procedure of wind filter:

Step1: disable wind filter - REG-0x40[1:0]

Step2: fine tune wind filter coefficient - REG-0x40[7:2]

Step3: enable win filter - REG-0x40[1:0]

If want to change the coefficient, is also need to follow the procedure.

Table 11. Sample Rate with bandwidth for Wind Filter

Fc (Hz) / n	Sample Rate (KHz)										
	8K Hz	11.025 KHz	12 KHz	16 KHz	22.05 KHz	24 KHz	32 KHz	44.1 KHz	48 KHz	88 KHz	96 KHZ
000000'b	0.968	1.334	1.452	1.936	2.668	2.906	3.872	5.336	5.808	10.672	11.616
000001'b	4.84	6.67	7.26	9.68	13.34	14.52	19.36	26.681	29.04	53.361	58.08
000010'b	8.68	11.962	13.02	17.36	23.924	26.04	34.72	47.848	52.08	95.697	104.16
000011'b	12.48	17.199	18.72	24.96	34.398	37.44	49.92	68.796	74.88	137.592	149.76
000100'b	16.28	22.436	24.42	32.56	44.872	48.84	65.12	89.743	97.68	179.487	195.36
000101'b	20.08	27.673	30.12	40.16	55.346	60.24	80.32	110.691	120.48	221.382	240.96
000110'b	23.84	32.855	35.76	47.68	65.709	71.52	95.36	131.418	143.04	262.836	286.08
000111'b	27.6	38.036	41.4	55.2	76.073	82.8	110.4	152.145	165.6	304.29	331.2
001000’b	31.32	43.163	46.98	62.64	86.326	93.96	125.28	172.652	187.92	345.303	375.84
001001’b	35.04	48.29	52.56	70.08	96.579	105.12	140.16	193.158	210.24	386.316	420.48
001010’b	38.76	53.416	58.14	77.52	106.832	116.28	155.04	213.665	232.56	427.329	465.12
001011’b	42.44	58.488	63.66	84.88	116.975	127.32	169.76	233.951	254.64	467.901	509.28
001100’b	46.12	63.559	69.18	92.24	127.118	138.36	184.48	254.237	276.72	508.473	553.44
001101’b	49.76	68.575	74.64	99.52	137.151	149.28	199.04	274.302	298.56	548.604	597.12
001110’b	53.4	73.592	80.1	106.8	147.184	160.2	213.6	294.368	320.4	588.735	640.8
001111’b	57.04	78.608	85.56	114.08	157.217	171.12	228.16	314.433	342.24	628.866	684.48
010000’b	60.64	83.569	90.96	121.28	167.139	181.92	242.56	334.278	363.84	668.556	727.68
010001’b	64.24	88.531	96.36	128.48	177.062	192.72	256.96	354.123	385.44	708.246	770.88
010010’b	67.8	93.437	101.7	135.6	186.874	203.4	271.2	373.748	406.8	747.495	813.6
010011’b	71.36	98.343	107.04	142.72	196.686	214.08	285.44	393.372	428.16	786.744	856.32
010100’b	74.92	103.249	112.38	149.84	206.498	224.76	299.68	412.996	449.52	825.993	899.04
010101’b	78.44	108.1	117.66	156.88	216.2	235.32	313.76	432.401	470.64	864.801	941.28
010110’b	81.96	112.951	122.94	163.92	225.902	245.88	327.84	451.805	491.76	903.609	983.52
010111’b	85.44	117.747	128.16	170.88	235.494	256.32	341.76	470.988	512.64	941.976	1025.28
011000’b	88.96	122.598	133.44	177.92	245.196	266.88	355.84	490.392	533.76	980.784	1067.52

011001’b	92.4	127.339	138.6	184.8	254.678	277.2	369.6	509.355	554.4	1018.71	1108.8
011010’b	95.88	132.135	143.82	191.76	264.269	287.64	383.52	528.539	575.28	1057.077	1150.56
011011’b	99.32	136.875	148.98	198.64	273.751	297.96	397.28	547.502	595.92	1095.003	1191.84
011100’b	102.76	141.616	154.14	205.52	283.232	308.28	411.04	566.465	616.56	1132.929	1233.12
011101’b	106.16	146.302	159.24	212.32	292.604	318.48	424.64	585.207	636.96	1170.414	1273.92
011110’b	109.56	150.987	164.34	219.12	301.975	328.68	438.24	603.949	657.36	1207.899	1314.72
011111’b	112.94	155.673	169.44	225.92	311.346	338.88	451.84	622.692	677.76	1245.384	1355.52
100000’b	116.36	160.359	174.54	232.72	320.717	349.08	465.44	641.434	698.16	1282.869	1396.32
100001’b	119.72	164.989	179.58	239.44	329.978	359.16	478.88	659.957	718.32	1319.913	1436.64
100010’b	123.04	169.565	184.56	246.08	339.129	369.12	492.16	678.258	738.24	1356.516	1476.48
100011’b	126.4	174.195	189.6	252.8	348.39	379.2	505.6	696.78	758.4	1393.56	1516.8
100100’b	129.72	178.77	194.58	259.44	357.541	389.16	518.88	715.082	778.32	1430.163	1556.64
100101’b	133.04	183.346	199.56	266.08	366.692	399.12	532.16	733.383	798.24	1466.766	1596.48
100110’b	136.32	187.866	204.48	272.64	375.732	408.96	545.28	751.464	817.92	1502.928	1635.84
100111’b	139.64	192.441	209.46	279.28	384.883	418.92	558.56	769.766	837.84	1539.531	1675.68
101000’b	142.88	196.906	214.32	285.76	393.813	428.64	571.52	787.626	857.28	1575.252	1714.56
101001’b	146.16	201.427	219.24	292.32	402.854	438.48	584.64	805.707	876.96	1611.414	1753.92
101010’b	149.4	205.892	224.1	298.8	411.784	448.2	597.6	823.568	896.4	1647.135	1792.8
101011’b	152.64	210.357	228.96	305.28	420.714	457.92	610.56	841.428	915.84	1682.856	1831.68
101100’b	155.88	214.822	233.82	311.76	429.644	467.64	623.52	859.289	935.28	1718.577	1870.56
101101’b	159.08	219.232	238.62	318.16	438.464	477.24	636.32	876.928	954.48	1753.857	1908.96
101110’b	162.28	223.642	243.42	324.56	447.284	486.84	649.12	894.568	973.68	1789.137	1947.36
101111’b	165.48	228.052	248.22	330.96	456.104	496.44	661.92	912.209	992.88	1824.417	1985.76
110000’b	168.68	232.462	253.02	337.36	464.924	506.04	674.72	929.849	1012.08	1859.697	2024.16
110001’b	171.84	236.817	257.76	343.68	473.634	515.52	687.36	947.268	1031.04	1894.536	2062.08
110010’b	175	241.172	262.5	350	482.344	525	700	964.688	1050	1929.375	2100
110011’b	178.16	245.527	267.24	356.32	491.054	534.48	712.64	982.107	1068.96	1964.214	2137.92
110100’b	181.28	249.827	271.92	362.56	499.653	543.84	725.12	999.306	1087.68	1998.612	2175.36
110101’b	184.4	254.162	276.6	368.8	508.253	553.2	737.6	1016.505	1106.4	2033.01	2212.8
110110’b	187.52	258.426	281.28	375.04	516.852	562.56	750.08	1033.704	1125.12	2067.408	2250.24

110111'b	190.64	262.726	285.96	381.28	525.452	571.92	762.56	1050.903	1143.84	2101.806	2287.68
111000'b	193.72	266.97	290.58	387.44	533.941	581.16	774.88	1067.882	1162.32	2135.763	2324.64
111001'b	196.8	271.215	295.2	393.6	542.43	590.4	787.2	1084.86	1180.8	2169.72	2361.6
111010'b	199.88	275.46	299.82	399.76	550.919	599.64	799.52	1101.839	1199.28	2203.677	2398.56
111011'b	202.92	279.649	304.38	405.84	559.298	608.76	811.68	1118.597	1217.52	2237.193	2435.04
111100'b	206	283.894	309	412	567.788	618	824	1135.575	1236	2271.15	2472
111101'b	209.04	288.083	313.56	418.08	576.166	627.12	836.16	1152.333	1254.24	2304.666	2508.48
111110'b	212.08	292.273	318.12	424.16	584.546	636.24	848.32	1169.091	1272.48	2338.182	2544.96
111111'b	215.08	296.407	322.62	430.16	592.814	645.24	860.32	1185.629	1290.48	2371.257	2580.96

*This table is for 2nd filter

7.10.4. Analog to Analog Path with EQ Function

In order to let analog audio input with EQ function, ALC5633Q use ADC and DAC to implement EQ function on analog to analog path. The analog input will be converted to digital signal and sum with I2S input then pass EQ block and convert to analog signal for analog output.

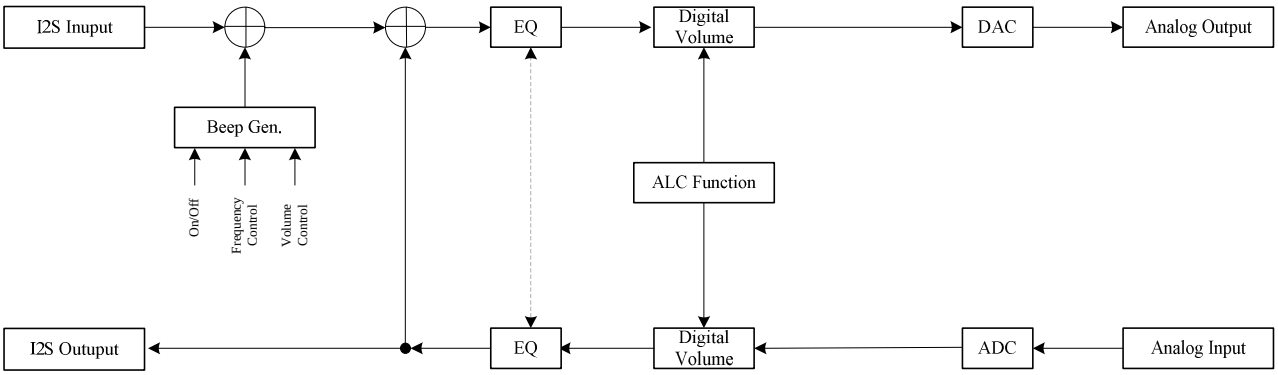


Figure 16. Analog to Analog Path with EQ Function

7.10.5. Digital Beep Generator

The build in digital beep generator will produce vary frequency tones and tone level is also can be controlled by register. The beep sound can sum with I2S input and convert to analog output. It can mix sound from I2S and tone from beep generator.

Table 12. Beep Frequency and Volume

REG-48[11:8]	Frequency	REG-48[7:5]	Volume
0000'b	500Hz	000'b	0dB
0001'b	600Hz	001'b	-3dB
0010'b	750Hz	010'b	-6dB
0011'b	800Hz	011'b	-9dB
0100'b	1kHz	100'b	-12dB
0101'b	1.2kHz	101'b	-15dB
0110'b	1.5kHz	110'b	-18dB
0111'b	1.6kHz	111'b	-21dB
1000'b	2kHz		
1001'b	2.4kHz		
1010'b	3kHz		
1011'b	3.2kHz		
1100'b	4kHz		
1101'b	4.8kHz		
1110'b	6kHz		
1111'b	6.4kHz		

7.11. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400KHz rate and SDA data is a open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

7.11.1. Address Setting

Table 13. Address Setting (0x3Ah)

(MSB)			BIT				(LSB)
0	0	1	1	1	0	1	R/W

7.11.2. Complete Data Transfer

Data Transfer over I²C Control Interface

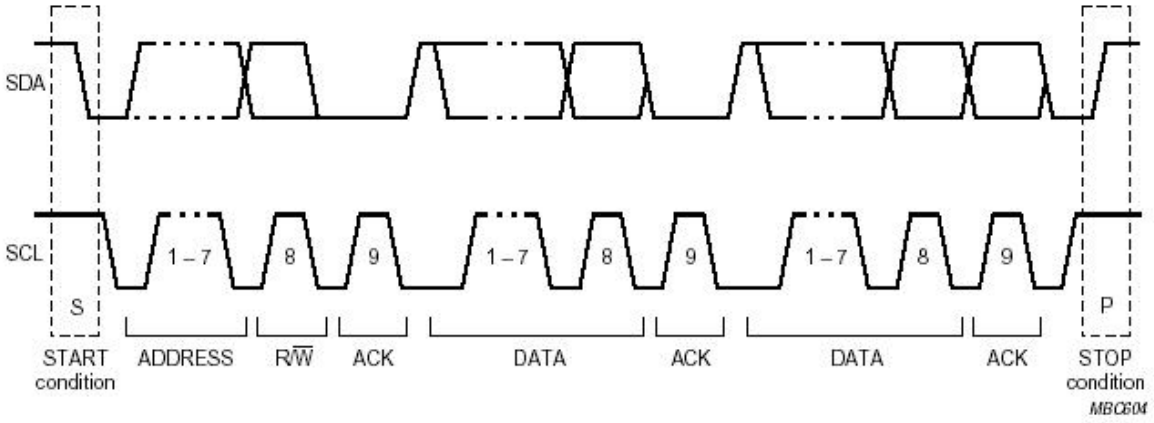


Figure 17. Data Transfer Over I²C Control Interface

Write WORD Protocol

Table 14. Write WORD Protocol

1	7	1	1	8	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	Data Byte High	A	Data Byte Low	A	P

Read WORD Protocol

Table 15. Read WORD Protocol

1	7	1	1	8	1	7	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	S	Device Address	Rd	A	Data Byte High	A	Data Byte Low	NA	P

S:	Start Condition	A:	0 for ACK, 1 for NACK
Slave Address:	7-bit Device Address	Data Byte:	16-bit Mixer data
Wr:	0 for Write Command	£:	Master-to-Slave
Rd:	1 for Read Command	£:	Slave-to-Master
Command Code:	8-bit Register Address		

7.12. GPIO, Interrupt and Jack Detection

The ALC5633Q supports one digital GPIO. The GPIO can as IRQ output and triggered by trigger sources. The trigger sources can from over-current status, over-temperature status and jack detection. Each of these is trigged and the GPIO will output a flag as interrupt signal.

There are two pins can as jack detect pins, JD1 and JD2. And the JD pins is share with Line1 pins. The jack detect function is use to turn-on or turn-off output port. When jack detect pin has been trigged, the selected output ports will be turn-on or turn-off. When GPIO is as IRQ function then will not as jack detect pin.

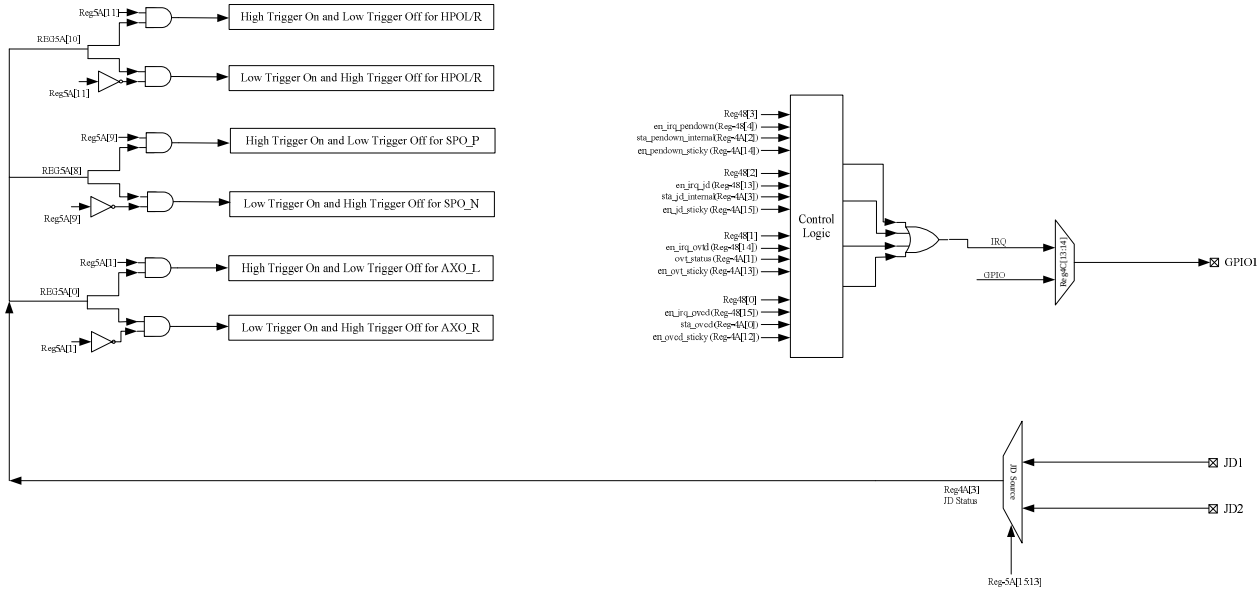


Figure 18. IRQ/Jack Detection Function Block

8. Registers List

Access unimplemented registers will return a 0.

8.1. Reg-00h: Software Reset

Default: 0001'h

Table 16. MX00 Software Reset

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:0	R	0'h	Reserved

Note: Writing any data into this register will reset all registers to their default value. The written data is ignored.

8.2. Reg-02h: Speaker Output Control

Default: E000'h

Table 17. MX02 Speaker Output Control

Port Name	Bits	Read/Write	Reset Status	Description
mu_spo_p	15	R/W	1'h	Output Control for SPOLP/SPORN 0'b: Mute 1'b: Un-Mute
Spkon_source	14:13	R/W	3'h	Output Control for SPO_R/N 00'b: RN 01'b: RP 10'b: RN 11'b: LN
reserved	12:10	R	0'h	Reserved
vol_spol	9:5	R/W	0'h	Speaker Left Channel Volume Control (SPKL_Vol) 00'h: 0dB ~ 1F'h: -46.5dB, with 1.5dB/step
vol_spor	4:0	R/W	0'h	Speaker Right Channel Volume Control (SPKR_Vol) 00'h: 0dB ~ 1F'h: -46.5dB, with 1.5dB/step

8.3. Reg-03h: Speaker/HP Output Mixer Control

Default: 0000’h

Table 18. MX03 Speaker/HP Output Mixer Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:9	R	0’h	Reserved
Sel_dacl_to_spo_l	8	R/W	0’h	Mute Control of SPOL_MIX for DACL to SPOL_MIX 0’b: Mute 1’b: Un-Mute
Reserved	7	R	0’h	Reserved
Sel_dacr_to_spo_r	6	R/W	0’h	Mute Control of SPOR_MIX for DACR to SPOR_MIX 0’b: Mute 1’b: Un-Mute
Sel_dac _to_hpo	5	R/W	0’h	Mute Control of HPO_MIX for DAC to HPO 0’b: Mute 1’b: Un-Mute
Sel_hp_vol_to_hpo	4	R/W	0’h	Mute Control of HPO_MIX for HP_Vol to HPO 0’b: Mute 1’b: Un-Mute
Reserved	3:0	R	0’h	Reserved

8.4. Reg-04h: Headphone Output Volume Control

Default: 8080’h

Table 14. MX04 Headphone Output Volume Control

Port Name	Bits	Read/Write	Reset Status	Description
mu_hpo_l	15	R/W	1’b	Mute Control for HPOL 0’b: Un-mute 1’b: Mute
sel_hpovoll_in	14	R/W	0’h	HP Left Channel Volume Input Select 0’b: VMID (No input) 1’b: HPMIXL
Reserved	13	R	0’h	Reserved
vol_hpo_l	12:8	R/W	00’h	HPO Left Channel Volume Control 00’h: 0dB

				~ 1F'h: -46.5dB, with 1.5dB/step
mu_hpo_r	7	R/W	1'b	Mute Control for HPOR 0'b: Un-mute 1'b: Mute
sel_hpovolr_in	6	R/W	0'h	HP Right Channel Volume Input Select 0'b: VMID (No input) 1'b: HPMIXR
Reserved	5	R	0'h	Reserved
vol_hpo_r	4:0	R/W	00'h	HPO Right Channel Volume Control 00'h: 0dB ~ 1F'h: -46.5dB, with 1.5dB/step

8.5. Reg-06h: AUX Output Control

Default: C080'h

Table 19. MX06 AUX Output Control

Port Name	Bits	Read/Write	Reset Status	Description
mu_axol	15	R/W	1'b	Mute Control for AXOLP 0'b: Un-mute 1'b: Mute
sel_axo_mode	14	R/W	1'h	AUX Output Mode Control 0'b: Mono differential output => (L+R) / -(L+R) 1'b: Stereo single-ended output => L / R
Reserved	13	R	0'b	Reserved
auxl_vol	12:8	R/W	00'h	AUX Left Channel Volume Control 00'h: 0dB ~ 1F'h: -46.5dB, with 1.5dB/step
mu_axor	7	R/W	1'b	Mute Control for AXORN 0'b: Un-mute 1'b: Mute
Reserved	6:5	R	0'h	Reserved

auxr_vol	4:0	R/W	00’h	AUX Right Channel Volume Control 00’h: 0dB ~ 1F’h: -46.5dB, with 1.5dB/step

8.6. Reg-08h: LINE1 Input Volume Control

Default: 0808’h

Table 20. MX08 LINE1 Input Volume Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:13	R	0’h	Reserved
lin1_l_vol	12:8	R/W	08’h	LINE1 Input Left Channel Volume Control 00’h: 12dB ~ 08’h: 0dB ~ 1F’h: -34.5dB, with 1.5dB/step
Reserved	7:5	R	0’h	Reserved
lin1_r_vol	4:0	R/W	08’h	LINE1 Input Right Channel Volume Control 00’h: 12dB ~ 08’h: 0dB ~ 1F’h: -34.5dB, with 1.5dB/step

8.7. Reg-0Ah: LINE2 Input Volume Control

Default: 0808’h

Table 20. MX0A LINE2 Input Volume Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:13	R	0’h	Reserved
Lin2_l_vol	12:8	R/W	08’h	LINE2 Input Left Channel Volume Control 00’h: 12dB ~

				08’h: 0dB ~ 1F’h: -34.5dB, with 1.5dB/step
Reserved	7:5	R	0’h	Reserved
Lin2_r_vol	4:0	R/W	08’h	LINE2 Input Right Channel Volume Control 00’h: 12dB ~ 08’h: 0dB ~ 1F’h: -34.5dB, with 1.5dB/step

8.8. Reg-0Ch: DAC Control

Default: 0000’h

Table 21. MX0C DAC Control

Port Name	Bits	Read/Write	Reset Status	Description
mu_dac_l	15	R/W	0’b	Digital Mute for Left DAC 0’b: Un-Mute 1’b: Mute
mu_da2mix	14	R/W	0’b	Mute Control for I2S Data to Digital Mixer of DAC 0’b: Un-Mute 1’b: Mute
en_a2a_path	13	R/W	0’b	Enable Control for ADC Data to Digital Mixer of DAC 0’b: Disable 1’b: Enable
Reserved	12:8	R	0’h	Reserved
mu_dac_r	7	R/W	0’b	Digital Mute for Right DAC 0’b: Un-Mute 1’b: Mute
sel_dac_pre_bst	6:0	R/W	0’h	DAC Digital Pre-Boost Gain 00’h= 0dB 01’h= 0.375dB 02’h= 0.75dB 03’h= 1.125dB ……..

				4B'h= 28.125dB, with 0.375dB/step Others: Reserved

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	0	16	10	6	32	20	12	48	30	18	64	40	24
1	1	0.375	17	11	6.375	33	21	12.375	49	31	18.375	65	41	24.375
2	2	0.75	18	12	6.75	34	22	12.75	50	32	18.75	66	42	24.75
3	3	1.125	19	13	7.125	35	23	13.125	51	33	19.125	67	43	25.125
4	4	1.5	20	14	7.5	36	24	13.5	52	34	19.5	68	44	25.5
5	5	1.875	21	15	7.875	37	25	13.875	53	35	19.875	69	45	25.875
6	6	2.25	22	16	8.25	38	26	14.25	54	36	20.25	70	46	26.25
7	7	2.625	23	17	8.625	39	27	14.625	55	37	20.625	71	47	26.625
8	8	3	24	18	9	40	28	15	56	38	21	72	48	27
9	9	3.375	25	19	9.375	41	29	15.375	57	39	21.375	73	49	27.375
10	A	3.75	26	1A	9.75	42	2A	15.75	58	3A	21.75	74	4A	27.75
11	B	4.125	27	1B	10.125	43	2B	16.125	59	3B	22.125	75	4B	28.125
12	C	4.5	28	1C	10.5	44	2C	16.5	60	3C	22.5			
13	D	4.875	29	1D	10.875	45	2D	16.875	61	3D	22.875			
14	E	5.25	30	1E	11.25	46	2E	17.25	62	3E	23.25			
15	F	5.625	31	1F	11.625	47	2F	17.625	63	3F	23.625			

8.9. Reg-0Eh: DAC Digital Volume Control

Default: 0000'h

Table 22. MX0E DAC Digital Volume Control

Port Name	Bits	Read/Write	Reset Status	Description
vol_dac_l	15:8	R/W	0'h	DAC Left Channel Digital Volume 00'h: 0dB ~ FF'h: -95.625dB, with 0.375dB/step
vol_dac_r	7:0	R/W	0'h	DAC Right Channel Digital Volume 00'h: 0dB ~ FF'h: -95.625dB, with 0.375dB/step

8.10. Reg-10h: Microphone Input Control

Default: 0808'h

Table 23. MX10 Microphone Input Control

Port Name	Bits	Read/Write	Reset Status	Description
en_mic1_df	15	R/W	0'b	MIC1 Input Mode Control 0'b: Single-ended input (From MIC1P for Input) 1'b: Differential input
Reserved	14:13	R	0'h	Reserved
mic1vol	12:8	R/W	08'h	MIC1 Volume Control 00'h: 12dB ~ 08'h: 0dB ~ 1F'h: -34.5dB, with 1.5dB/step
en_mic2_df	7	R/W	0'b	MIC2 Input Mode Control 0'b: Single-ended input (From MIC2P for Input) 1'b: Differential input
Reserved	6:5	R	0'h	Reserved
mic2vol	4:0	R/W	08'h	MIC2 Volume Control 00'h: 12dB ~ 08'h: 0dB ~ 1F'h: -34.5dB, with 1.5dB/step

8.11. Reg-12h: ADC Control

Default: 0000'h

Table 24. MX12 ADC Control

Port Name	Bits	Read/Write	Reset Status	Description
mu_adc_l	15	R/W	0'b	Digital Mute for ADC Left Channel 0'b: Un-Mute 1'b: Mute
mu_ad2tx	14	R/W	0'b	Mute Control for ADC Data to I2S 0'b: Un-Mute

				1’b: Mute
Reserved	13:8	R	0’h	Reserved
Mu_adc_r	7	R/W	0’h	Digital Mute for ADC Right Channel 0’b: Un-Mute 1’b: Mute
Reserved	6:5	R	0’h	Reserved
Sel_adc_pre_bst	4:0	R/W	0’h	ADC Digital Pre-BOOST 00’h= 0dB 01’h= 1.5dB 02’h= 3dB 03’h= 4.5dB …….. 13’h= 28.5dB, with 1.5dB/step Others: Reserved

8.12. Reg-14h: REC Mixer Control

Default: 7FFF’h

Table 25. MX14 REC Mixer Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15	R	0’h	Reserved
Mu_hpmixl_to_recmixl	14	R/W	1’b	HP Left Mixer to REC Left Mixer 0’b: UnMute 1’b: Mute
mu_auxmixl_to_recmixl	13	R/W	1’b	AUX Left Mixer to REC Left Mixer 0’b: UnMute 1’b: Mute
mu_spkmix_to_recmixl	12	R/W	1’b	Speaker Mixer to REC Left Mixer 0’b: UnMute 1’b: Mute
mu_lin1_l_vol_to_recmixl	11	R/W	1’b	Line In 1 Left Volume to REC Left Mixer 0’b: UnMute 1’b: Mute
mu_lin2_l_vol_to_recmixl	10	R/W	1’b	Line In 2 Left Volume to REC Left Mixer 0’b: UnMute

				1’b: Mute
mu_bst1_to_recmixl	9	R/W	1’b	MIC1 Boost Gain to REC Left Mixer 0’b: UnMute 1’b: Mute
mu_bst2_to_recmixl	8	R/W	1’b	MIC2 Boost Gain to REC Left Mixer 0’b: UnMute 1’b: Mute
Reserved	7	R	0’h	Reserved
Mu_hpmixr_to_recmixr	6	R/W	1’b	HP Right Mixer to REC Right Mixer 0’b: UnMute 1’b: Mute
mu_auxmixr_to_recmixr	5	R/W	1’b	AUX Right Mixer to REC Right Mixer 0’b: UnMute 1’b: Mute
mu_spkmix_to_recmixr	4	R/W	1’b	Speaker Mixer to REC Right Mixer 0’b: UnMute 1’b: Mute
mu_lin1_r_vol_to_recmixr	3	R/W	1’b	Line In 1 Right Volume to REC Right Mixer 0’b: UnMute 1’b: Mute
mu_lin2_r_vol_to_recmixr	2	R/W	1’b	Line In 2 Right Volume to REC Right Mixer 0’b: UnMute 1’b: Mute
mu_bst1_to_recmixr	1	R/W	1’b	MIC1 Boost Gain to REC Right Mixer 0’b: UnMute 1’b: Mute
mu_bst2_to_recmixr	0	R/W	1’b	MIC2 Boost Gain to REC Right Mixer 0’b: UnMute 1’b: Mute

8.13. Reg-16h: ADC Digital Volume Control

Default: 0000’h

Table 26. MX16 ADC Digital Volume Control

Port Name	Bits	Read/Write	Reset Status	Description

vol_adc_l	15:8	R/W	0'h	ADC Left Channel Digital Volume Control 00'h: 0dB ~ FF'h: -95.625dB, with 0.375dB/step
vol_adc_r	7:0	R/W	0'h	ADC Right Channel Digital Volume Control 00'h: 0dB ~ FF'h: -95.625dB, with 0.375dB/step

8.14. Headphone Mixer Control

Default: 3F3F'h

Table 25. MX18 Headphone Mixer Control

Register:: 0x18					**3F3F'h**
Net-list Name	**Bits**	**Read/ Write**	**Reset Status**	**Comment**	**Config**
reserved	15:14	R	0'h	Reserved	
mu_recmixl_to_hpmixl	13	R/W	1'b	REC Left Mixer to Headphone Left Mixer 0'b: Un-Mute 1'b: Mute	
mu_micvol1_to_hpmixl	12	R/W	1'b	MIC 1 volume to Headphone Left Mixer 0'b: Un-Mute 1'b: Mute	
mu_micvol2_to_hpmixl	11	R/W	1'b	MIC 2 volume to Headphone Left Mixer 0'b: Un-Mute 1'b: Mute	
mu_lin1_l_vol_to_hpmixl	10	R/W	1'b	Line In 1 Left volume to Headphone Left Mixer 0'b: Un-Mute 1'b: Mute	
mu_lin2_l_vol_to_hpmixl	9	R/W	1'b	Line In 2 Left volume to Headphone Left Mixer 0'b: Un-Mute 1'b: Mute	
mu_dacl_to_hpmixl	8	R/W	1'b	DAC Left to Headphone Left Mixer 0'b: Un-Mute	

				1’b: Mute	
Reserved	7:6	R	0’h	Reserved	
mu_recmixr_to_hpmixr	5	R/W	1’b	REC Right Mixer to Headphone Right Mixer 0’b: Un-Mute 1’b: Mute	
mu_micvol1_to_hpmixr	4	R/W	1’b	MIC 1 volume to Headphone Right Mixer 0’b: Un-Mute 1’b: Mute	
mu_micvol2_to_hpmixr	3	R/W	1’b	MIC 2 volume to Headphone Right Mixer 0’b: Un-Mute 1’b: Mute	
mu_lin1_r_vol_to_hpmixr	2	R/W	1’b	Line In 1 Right volume to Headphone Right Mixer 0’b: Un-Mute 1’b: Mute	
mu_lin2_r_vol_to_hpmixr	1	R/W	1’b	Line In 2 Right volume to Headphone Right Mixer 0’b: Un-Mute 1’b: Mute	
mu_dacr_to_hpmixr	0	R/W	1’b	DAC Right to Headphone Right Mixer 0’b: Un-Mute 1’b: Mute	

8.15. Reg-1Ah: AUX Mixer Control

Default: 3F3F’h

Table 27. MX1A AUX Mixer Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:14	R	0’h	Reserved
mu_recmixl_to_auxmixl	13	R/W	1’b	REC Left Mixer to AUX Left Mixer 0’b: Un-Mute 1’b: Mute
mu_micvol1_to_auxmixl	12	R/W	1’b	MIC1 Volume to AUX Left Mixer 0’b: Un-Mute 1’b: Mute
mu_micvol2_to_auxmixl	11	R/W	1’b	MIC2 Volume to AUX Left Mixer 0’b: Un-Mute

				1’b: Mute
mu_lin1_l_vol_to_auxmixl	10	R/W	1’b	Line In 1 Left Volume to AUX Left Mixer 0’b: Un-Mute 1’b: Mute
mu_lin2_l_vol_to_auxmixl	9	R/W	1’b	Line In 2 Left Volume to AUX Left Mixer 0’b: Un-Mute 1’b: Mute
mu_dacl_to_auxmixl	8	R/W	1’b	DAC Left Channel to AUX Left Mixer 0’b: Un-Mute 1’b: Mute
Reserved	7:6	R	0’h	Reserved
mu_recmixr_to_auxmixr	5	R/W	1’b	REC Right Mixer to AUX Right Mixer 0’b: Un-Mute 1’b: Mute
mu_micvol1_to_auxmixr	4	R/W	1’b	MIC1 Volume to AUX Right Mixer 0’b: Un-Mute 1’b: Mute
mu_micvol2_to_auxmixr	3	R/W	1’b	MIC2 Volume to AUX Right Mixer 0’b: Un-Mute 1’b: Mute
mu_lin1_r_vol_to_auxmixr	2	R/W	1’b	Line In 1 Right Volume to AUX Right Mixe 0’b: Un-Mute 1’b: Mute
mu_lin2_r_vol_to_auxmixr	1	R/W	1’b	Line In 2 Right Volume to AUX Right Mixe 0’b: Un-Mute 1’b: Mute
mu_dacr_to_auxmixr	0	R/W	1’b	DAC Right Channel to AUX Right Mixer 0’b: Un-Mute 1’b: Mute

8.16. Reg-1Ch: Speaker Mixer Control

Default: 00FF’h

Table 28. MX1C Speaker Mixer Control

Port Name	Bits	Read/Write	Reset Status	Description

Reserved	15:12	R	00’h	Reserved
spk_vol_in_sel	11:10	R/W	0’h	Speaker Volume Input Select 00’b: VMID 01’b: HP mixer 10’b: Speaker mixer 11’b: AUX mixer
Reserved	9:8	R	0’h	Reserved
mu_micvol1_to_spkmix	7	R/W	1’b	MIC1 Volume to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_micvol2_to_spkmix	6	R/W	1’b	MIC2 Volume to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_lin1_l_vol_to_spkmix	5	R/W	1’b	Line In 1 Left Volume to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_lin1_r_vol_to_spkmix	4	R/W	1’b	Line In 1 Right Volume to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_lin2_l_vol_to_spkmix	3	R/W	1’b	Line In 2 Left Volume to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_lin2_r_vol_to_spkmix	2	R/W	1’b	Line In 2 Right Volume to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_dacl_to_spkmix	1	R/W	1’b	DAC Left Channel to Speaker Mixer 0’b: Un-Mute 1’b: Mute
mu_dacr_to_spkmix	0	R/W	1’b	DAC Right Channel to Speaker Mixer 0’b: Un-Mute 1’b: Mute

8.17. Reg-1Eh: Speaker Amplifier Control

Default: 8000’h

Table 29. MX1E Speaker Amplifier Control

Port Name	Bits	Read/Write	Reset Status	Description
Abdmode	15	R/W	1'b	Speaker Amplifier Mode Control 0'b: Class AB 1'b: Class D
clsab_amp_sel	14	R/W	0'b	Class AB Amplifier Driving Control 0'b: Strong Amp 1'b: Weak Amp
reserved	13:0	R	0'h	Reserved

8.18. Reg-22h: Microphone Control

Default: 0000'h

Table 30. MX22 Microphone Control

Port Name	Bits	Read/Write	Reset Status	Description
sel_bst1	15:12	R/W	0'h	MIC 1 Boost Control 0000'b: 0dB (Bypass) 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB (Only for to ADC path) 0111'b: +50dB (Only for to ADC path) 1000'b: +52dB (Only for to ADC path) Others : Reserved
sel_bst2	11:8	R/W	0'h	MIC 2 Boost Control 0000'b: 0dB (Bypass) 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB (Only for to ADC path) 0111'b: +50dB (Only for to ADC path)

				1000’b: +52dB (Only for to ADC path) Others : Reserved
sel_micbias1	7	R/W	0’h	MICBIAS1 Output Voltage Control 0’b: 0.9 * AVDD 1’b: 0.75 * AVDD
pow_mic1_ovcd	6	R/W	0’h	MICBIAS1 Short Current Detector Control 0’b: Disable 1’b: Enable
sel_mic1_ovcd_th	5:4	R/W	0’h	MICBIAS1 Short Current Detector Threshold 00’b: 600uA 01’b: 1500uA 1x’b: 2000uA Note: tolerance is 200uA
sel_micbias2	3	R/W	0’h	MICBIAS2 Output Voltage Control 0’b: 0.9 * AVDD 1’b: 0.75 * AVDD
pow_mic2_ovcd	2	R/W	0’h	MICBIAS2 Short Current Detector Control 0’b: Disable 1’b: Enable
sel_mic2_ovcd_th	1:0	R/W	0’h	MICBIAS2 Short Current Detector Threshold 00’b: 600uA 01’b: 1500uA 1x’b: 2000uA Note: tolerance is 200uA

8.19. Reg-34h: I2S Audio Serial Data Port Control

Default: 8000’h

Table 32. MX34 I2S Audio Serial Data Port Control

Port Name	Bits	Read/Write	Reset Status	Description
Sel_i2s_ms	15	R/W	1’b	I2S Serial Data Port Mode Selection 0’b: Master 1’b: Slave
Copy_adc	14:13	R/W	0’b	Copy ADC Left/Right Channel Digital Data to Right/Left Channel for Mono Recording

				00’b: Normal (Independent) 01’b: Right copy to Left 10’b: Left copy to Right 11’b: Reserved
reserved	12	R	0’h	Reserved
En_adc_comp	11:10	R/W	0’h	ADC Compress (For I2S ADCDAT Output) 00’b: Off 01’b: μ law 10’b: A law 11’b: Reserved
En_dac_comp	9:8	R/W	0’h	DAC Compress (For I2S DACDAT Input) 00’b: OFF 01’b: μ law 10’b: A law 11’b: Reserved
Inv_bclk	7	R/W	0’b	I2S BCLK Polarity Control 0’b: Normal 1’b: Invert
Inv_r_ch	6	R/W	0’b	Inverse I2S Right Channel Data Phase for Differential Output 0’b: Normal 1’b: Invert
Inv_adc_lrck	5	R/W	0’b	ADC Digital Data Left/Right Channel Swap 0’b: Normal 1’b: Swap (Support for I2S and PCM)
Inv_dac_lrck	4	R/W	0’b	DAC Digital Data Left/Right Channel Swap 0’b: Normal 1’b: Swap (Support for I2S and PCM)
Sel_i2s_len	3:2	R/W	0’h	I2S Data Length Selection 00’b: 16-bit 01’b: 20-bit 10’b: 24-bit 11’b: 8-bit
Sel_i2s_format	1:0	R/W	0’h	I2S Data Format Selection 00’b: I2S Format

				01’b: Left justified 10’b: PCM mode A 11’b: PCM mode B

8.20. Reg-38h: Stereo ADC/DAC Clock Control

Default: 2000’h

Table 33. MX38 Stereo ADC/DAC Clock Control

Port Name	Bits	Read/Write	Reset Status	Description
sel_i2s_pre_div1	15:13	R/W	1’h	I2S Pre-Divider 000’b: ÷ 1 001’b: ÷ 2 010’b: ÷ 4 011’b: ÷ 8 100’b: ÷ 16 101’b: ÷ 32 Others: Reserved
sel_i2s_bclk_ms1	12	R/W	0’b	Master Mode Clock Relative of BCLK and LRCK 0’b: 32Bits (64FS) 1’b: 16Bits (32FS)
sel_dac_osr	11:10	R/W	00’b	Stereo DAC Over Sample Rate Select 00’b: 128Fs 01’b: 64Fs 10’b: 32Fs 11’b: 16Fs
sel_adc_osr	9:8	R/W	00’b	Stereo ADC Over Sample Rate Select 00’b: 128Fs 01’b: 64Fs 10’b: 32Fs 11’b: 16Fs
sel_filter_clk1	7	R/W	0’b	Stereo ADC/DAC Filter Clock Select 0’b: 256Fs 1’b: 384Fs
reserved	6:0	R	0’h	Reserved

8.21. Reg-3Ah: Power Management Control 1

Default: 0000’h

Table 34. MX3A Power Management Control 1

Port Name	Bits	Read/Write	Reset Status	Description
en_i2s	15	R/W	0’b	I2S Digital Interface Enable Control 0’b: Power down 1’b: Power on
Reserved	14	R	0’b	Reserved
pow_clsd	13	R/W	0’b	Power On Class D Modulation 0’b: Power down 1’b: Power on
pow_adc_l	12	R/W	0’h	Stereo Analog ADC_L Power Down Control 0’b: Power down 1’b: Power on
pow_adc_r	11	R/W	0’h	Stereo Analog ADC_R Power Down Control 0’b: Power down 1’b: Power on
pow_dac_l	10	R/W	0’b	Stereo Analog DAC_L Power Down Control 0’b: Power down 1’b: Power on
pow_dac_r	9	R/W	0’b	Stereo Analog DAC_R Power Down Control 0’b: Power down 1’b: Power on
pow_dac_ref	8	R/W	0’b	Stereo Analog DAC Reference Power Down Control 0’b: Power down 1’b: Power on
pow_dac_df2se_l	7	R/W	0’b	Stereo Analog DAC_L DF2SE Power Down Control 0’b: Power down 1’b: Power on
pow_dac_df2se_r	6	R/W	0’b	Stereo Analog DAC_R DF2SE Power Down Control 0’b: Power down 1’b: Power on
Powdn_clsab	5	R/W	0’b	Class-AB Amp Power Control 0’b: Power down

				1’b: Power on
reserved	4:0	R	0’h	Reserved

8.22. Reg-3Bh: Power Management Control 2

Default: 0000’h

Table 35. MX3B Power Management Control 2

Port Name	Bits	Read/Write	Reset Status	Description
Pow_hpmixl	15	R/W	0’b	Left HP Mixer Power Down Control 0’b: Power down 1’b: Power on
Pow_hpmixr	14	R/W	0’b	LRight HP Mixer Power Down Control 0’b: Power down 1’b: Power on
pow_auxmixl	13	R/W	0’b	Left AUX Mixer Power Down Control 0’b: Power down 1’b: Power on
pow_auxmixr	12	R/W	0’b	Right AUX Mixer Power Down Control 0’b: Power down 1’b: Power on
pow_recmixl	11	R/W	0’h	Left Record Mixer Power Down Control 0’b: Power down 1’b: Power on
pow_recmixr	10	R/W	0’h	Right Record Mixer Power Down Control 0’b: Power down 1’b: Power on
pow_lin1l	9	R/W	0’b	Line In 1 L Volume Power Down Control 0’b: Power down 1’b: Power on
pow_lin1r	8	R/W	0’b	Line In 1 R Volume Power Down Control 0’b: Power down 1’b: Power on
pow_lin2l	7	R/W	0’b	Line In 2 L Volume Power Down Control 0’b: Power down 1’b: Power on

pow_lin2r	6	R/W	0’b	Lin2 In 2 R Volume Power Down Control 0’b: Power down 1’b: Power on
pow_mic1	5	R/W	0’b	MIC1 Boost Power Down Control 0’b: Power down 1’b: Power on
pow_mic2	4	R/W	0’b	MIC2 Boost Power Down Control 0’b: Power down 1’b: Power on
pow_micbias1	3	R/W	0’h	Microphone Bias 1 Power Down Control 0’b: Power down 1’b: Power on
pow_micbias2	2	R/W	0’h	Microphone Bias 2 Power Down Control 0’b: Power down 1’b: Power on
pow_pll1	1	R/W	0’b	PLL Power Down Control 0’b: Power down 1’b: Power on
pow_spkmix	0	R/W	0’b	Speaker Mixer Power Down Control 0’b: Power down 1’b: Power on

8.23. Reg-3Ch: Power Management Control 3

Default: 0000’h

Table 36. MX3C Power Management Control 3

Port Name	Bits	Read/Write	Reset Status	Description
pow_vref	15	R/W	0’h	Enable Vref voltage for all circuit buffer 0’b: Power down 1’b: Power on
en_fastb	14	R/W	0’h	Fast Vref Control 0’b: Enable

				1’b: Disable
pow_main_bias	13	R/W	0’h	Enable All Analog Circuit Bias 0’b: Power down 1’b: Power on
Reserved	12:4	R	0’b	Reserved
pow_hp	3	R/W	0’b	Power On Headphone Amplifier 0’b: Power Down 1’b: Power On
pow_vcm_hp	2	R/W	0’b	Power On Headphone Common-mode Buffer 0’b: Power Down 1’b: Power On
en_out_hp	1	R/W	0’b	Change Output Mode for Power on Depop 0’b: Depop mode 1’b: Normal mode
en_amp_hp	0	R/W	0’b	Improve HP Amp Driving 0’b: Disable 1’b: Enable

Œ For power on sequence used. After power on and need to disable the Fast Vref Control.

8.24. Reg-3Eh: Power Management Control 4

Default: 0000’h

Table 37. MX3E Power Management Control 4

Port Name	Bits	Read/Write	Reset Status	Description
pow_spkl_vol	15	R/W	0’h	Left Speaker Volume Power Down Control 0’b: Power down 1’b: Power on
pow_spkr_vol	14	R/W	0’h	Right Speaker Volume Power Down Control 0’b: Power down 1’b: Power on
Reserved	13:12	R	0’h	Reserved
pow_hpl_vol	11	R/W	0’h	Left Headphone Volume Power Down Control 0’b: Power down 1’b: Power on

pow_hpr_vol	10	R/W	0’h	Right Headphone Volume Power Down Control 0’b: Power down 1’b: Power on
pow_auxl_vol	9	R/W	0’h	Left AUX Volume Power Down Control 0’b: Power down 1’b: Power on
pow_auxr_vol	8	R/W	0’h	Right AUX Volume Power Down Control 0’b: Power down 1’b: Power on
Reserved	7:0	R	0’h	Reserved

8.25. Reg-40h: General Purpose Control Register 1

Default: 7C00’h

Table 38. MX40 General Purpose Control Register 1

Port Name	Bits	Read/Write	Reset Status	Description
en_spk_auto_ratio	15	R/W	0’h	Speaker Amplifier Auto AC Ratio Gain Control • 0’b: Disable (Manual) 1’b: Enable (Auto)
spk_gain_clsd	14:12	R/W	7’h	Speaker Amplifier AC Ratio Gain Control 000’b: 2.34× 001’b: 2.0× 010’b: 1.68× 011’b: 1.56× 100’b: 1.44× 101’b: 1.27× 110’b: 1.1× 111’b: 1.00×
en_dac_hpf	11	R/W	1’h	Stereo DAC High Pass Filter Control 0’b: Bypass 1’b: Normal operating (With HPF)
en_adc_hpf	10	R/W	1’h	Stereo ADC High Pass Filter Control 0’b: Bypass

				1’b: Normal operating (With HPF)
Reserved	9:8	R	0’h	Reserved
sel_adc_wf_coef	7:2	R/W	0’h	ADC Wind Filter Coefficient Œ 00’h: n=0 ~ 3f’h: n=63
sel_adc_wf_mod	1:0	R/W	0’h	ADC Wind Filter Control 00’b: Disable 01’b: 1st order HPF 10’b: 1st order HPF 11’b: 2nd order HPF

Œ Wind Filter fc decision by filter coefficient

The setting procedure of wind filter:

Step1: disable wind filter

Step2: fine tune wind filter coefficient

Step3: enable win filter

If want to change the coefficient, is also need to follow the procedure.

Fc (Hz) / n	Sample Rate (KHz)										
	8K Hz	11.025 KHz	12 KHz	16 KHz	22.05 KHz	24 KHz	32 KHz	44.1 KHz	48 KHz	88 KHz	96 KHZ
000000'b	0.968	1.334	1.452	1.936	2.668	2.906	3.872	5.336	5.808	10.672	11.616
000001'b	4.84	6.67	7.26	9.68	13.34	14.52	19.36	26.681	29.04	53.361	58.08
000010'b	8.68	11.962	13.02	17.36	23.924	26.04	34.72	47.848	52.08	95.697	104.16
000011'b	12.48	17.199	18.72	24.96	34.398	37.44	49.92	68.796	74.88	137.592	149.76
000100'b	16.28	22.436	24.42	32.56	44.872	48.84	65.12	89.743	97.68	179.487	195.36
000101'b	20.08	27.673	30.12	40.16	55.346	60.24	80.32	110.691	120.48	221.382	240.96
000110'b	23.84	32.855	35.76	47.68	65.709	71.52	95.36	131.418	143.04	262.836	286.08
000111'b	27.6	38.036	41.4	55.2	76.073	82.8	110.4	152.145	165.6	304.29	331.2
001000’b	31.32	43.163	46.98	62.64	86.326	93.96	125.28	172.652	187.92	345.303	375.84
001001’b	35.04	48.29	52.56	70.08	96.579	105.12	140.16	193.158	210.24	386.316	420.48
001010’b	38.76	53.416	58.14	77.52	106.832	116.28	155.04	213.665	232.56	427.329	465.12

001011’b	42.44	58.488	63.66	84.88	116.975	127.32	169.76	233.951	254.64	467.901	509.28
001100’b	46.12	63.559	69.18	92.24	127.118	138.36	184.48	254.237	276.72	508.473	553.44
001101’b	49.76	68.575	74.64	99.52	137.151	149.28	199.04	274.302	298.56	548.604	597.12
001110’b	53.4	73.592	80.1	106.8	147.184	160.2	213.6	294.368	320.4	588.735	640.8
001111’b	57.04	78.608	85.56	114.08	157.217	171.12	228.16	314.433	342.24	628.866	684.48
010000’b	60.64	83.569	90.96	121.28	167.139	181.92	242.56	334.278	363.84	668.556	727.68
010001’b	64.24	88.531	96.36	128.48	177.062	192.72	256.96	354.123	385.44	708.246	770.88
010010’b	67.8	93.437	101.7	135.6	186.874	203.4	271.2	373.748	406.8	747.495	813.6
010011’b	71.36	98.343	107.04	142.72	196.686	214.08	285.44	393.372	428.16	786.744	856.32
010100’b	74.92	103.249	112.38	149.84	206.498	224.76	299.68	412.996	449.52	825.993	899.04
010101’b	78.44	108.1	117.66	156.88	216.2	235.32	313.76	432.401	470.64	864.801	941.28
010110’b	81.96	112.951	122.94	163.92	225.902	245.88	327.84	451.805	491.76	903.609	983.52
010111’b	85.44	117.747	128.16	170.88	235.494	256.32	341.76	470.988	512.64	941.976	1025.28
011000’b	88.96	122.598	133.44	177.92	245.196	266.88	355.84	490.392	533.76	980.784	1067.52
011001’b	92.4	127.339	138.6	184.8	254.678	277.2	369.6	509.355	554.4	1018.71	1108.8
011010’b	95.88	132.135	143.82	191.76	264.269	287.64	383.52	528.539	575.28	1057.077	1150.56
011011’b	99.32	136.875	148.98	198.64	273.751	297.96	397.28	547.502	595.92	1095.003	1191.84
011100’b	102.76	141.616	154.14	205.52	283.232	308.28	411.04	566.465	616.56	1132.929	1233.12
011101’b	106.16	146.302	159.24	212.32	292.604	318.48	424.64	585.207	636.96	1170.414	1273.92
011110’b	109.56	150.987	164.34	219.12	301.975	328.68	438.24	603.949	657.36	1207.899	1314.72
011111’b	112.94	155.673	169.44	225.92	311.346	338.88	451.84	622.692	677.76	1245.384	1355.52
100000’b	116.36	160.359	174.54	232.72	320.717	349.08	465.44	641.434	698.16	1282.869	1396.32
100001’b	119.72	164.989	179.58	239.44	329.978	359.16	478.88	659.957	718.32	1319.913	1436.64
100010’b	123.04	169.565	184.56	246.08	339.129	369.12	492.16	678.258	738.24	1356.516	1476.48
100011’b	126.4	174.195	189.6	252.8	348.39	379.2	505.6	696.78	758.4	1393.56	1516.8
100100’b	129.72	178.77	194.58	259.44	357.541	389.16	518.88	715.082	778.32	1430.163	1556.64
100101’b	133.04	183.346	199.56	266.08	366.692	399.12	532.16	733.383	798.24	1466.766	1596.48
100110’b	136.32	187.866	204.48	272.64	375.732	408.96	545.28	751.464	817.92	1502.928	1635.84
100111’b	139.64	192.441	209.46	279.28	384.883	418.92	558.56	769.766	837.84	1539.531	1675.68
101000’b	142.88	196.906	214.32	285.76	393.813	428.64	571.52	787.626	857.28	1575.252	1714.56

101001'b	146.16	201.427	219.24	292.32	402.854	438.48	584.64	805.707	876.96	1611.414	1753.92
101010'b	149.4	205.892	224.1	298.8	411.784	448.2	597.6	823.568	896.4	1647.135	1792.8
101011'b	152.64	210.357	228.96	305.28	420.714	457.92	610.56	841.428	915.84	1682.856	1831.68
101100'b	155.88	214.822	233.82	311.76	429.644	467.64	623.52	859.289	935.28	1718.577	1870.56
101101'b	159.08	219.232	238.62	318.16	438.464	477.24	636.32	876.928	954.48	1753.857	1908.96
101110'b	162.28	223.642	243.42	324.56	447.284	486.84	649.12	894.568	973.68	1789.137	1947.36
101111'b	165.48	228.052	248.22	330.96	456.104	496.44	661.92	912.209	992.88	1824.417	1985.76
110000'b	168.68	232.462	253.02	337.36	464.924	506.04	674.72	929.849	1012.08	1859.697	2024.16
110001'b	171.84	236.817	257.76	343.68	473.634	515.52	687.36	947.268	1031.04	1894.536	2062.08
110010'b	175	241.172	262.5	350	482.344	525	700	964.688	1050	1929.375	2100
110011'b	178.16	245.527	267.24	356.32	491.054	534.48	712.64	982.107	1068.96	1964.214	2137.92
110100'b	181.28	249.827	271.92	362.56	499.653	543.84	725.12	999.306	1087.68	1998.612	2175.36
110101'b	184.4	254.162	276.6	368.8	508.253	553.2	737.6	1016.505	1106.4	2033.01	2212.8
110110'b	187.52	258.426	281.28	375.04	516.852	562.56	750.08	1033.704	1125.12	2067.408	2250.24
110111'b	190.64	262.726	285.96	381.28	525.452	571.92	762.56	1050.903	1143.84	2101.806	2287.68
111000'b	193.72	266.97	290.58	387.44	533.941	581.16	774.88	1067.882	1162.32	2135.763	2324.64
111001'b	196.8	271.215	295.2	393.6	542.43	590.4	787.2	1084.86	1180.8	2169.72	2361.6
111010'b	199.88	275.46	299.82	399.76	550.919	599.64	799.52	1101.839	1199.28	2203.677	2398.56
111011'b	202.92	279.649	304.38	405.84	559.298	608.76	811.68	1118.597	1217.52	2237.193	2435.04
111100'b	206	283.894	309	412	567.788	618	824	1135.575	1236	2271.15	2472
111101'b	209.04	288.083	313.56	418.08	576.166	627.12	836.16	1152.333	1254.24	2304.666	2508.48
111110'b	212.08	292.273	318.12	424.16	584.546	636.24	848.32	1169.091	1272.48	2338.182	2544.96
111111'b	215.08	296.407	322.62	430.16	592.814	645.24	860.32	1185.629	1290.48	2371.257	2580.96

*The table is for 2nd filter

• At auto mode, the chip will auto detect the PVDD level and auto adjust the AC ration gain. And keep maximum output power.

8.26. Reg-42h: Internal Clock Control

Default: 0000’h

Table 39. MX42 Internal Clock Control

Port Name	Bits	Read/Write	Reset Status	Description
sel_sysclk	15:14	R/W	0’b	System Clock Source MUX Control 00’b: MCLK 01’b: PLL Others: Reserved
sel_pll_sour	13	R/W	0’b	PLL Source Select 0’b: From MCLK 1’b: From BCLK
Reserved	12	R	0’h	Reserved
sel_pll_pre_div1	11	R/W	0’b	PLL Pre-divider 0’b: ÷ 1 1’b: ÷ 2
Reserved	10:0	R	0’h	Reserved

8.27. Reg-44h: PLL Function Control

Default: 0000’h

Table 40. MX44 PLL Function Control

Port Name	Bits	Read/Write	Reset Status	Description
Pll1_n_code	15:8	R/W	00’h	N[7:0] Code for Analog PLL 00000000’b: Div 2 00000001’b: Div 3 … 11111111’b: Div 257
pll1_m_bypass	7	R/W	0’b	Bypass PLL M 0’b : No bypass 1’b : Bypass
Pll1_k_code	6:4	R/W	0’h	K[2:0] Code for Analog PLL 000’b: Div 2 001’b: Div 3 … 111’b: Div 9

Pll1_m_code	3:0	R/W	0'h	M[3:0] Code for Analog PLL 0000'b: Div 2 0001'b: Div 3 …….. 1111'b: Div 17

8.28. Reg-48h: Digital Beep Gen. and IRQ Control

Default: 0240'h

Table 42. MX48 Digital Beep Gen. and IRQ Control

Port Name	Bits	Read/Write	Reset Status	Description
en_irq_ovcd	15	R/W	0'b	IRQ Output Source Configure of Speaker Amplifier Over-Current Status 0'b: Disable 1'b: Enable
en_irq_ovtd	14	R/W	0'b	IRQ Output Source Configure of Over-Temperature Status 0'b: Disable 1'b: Enable
en_irq_jd	13	R/W	0'b	IRQ Output Source Configure of Jack Detection Status 0'b: Disable 1'b: Enable
en_beep_gen	12	R/W	0'b	Digital Beep Generator Control 0'b: Disable 1'b: Enable
beep_gen_freq	11:8	R/W	2'h	Select Frequency for Beep Gen. 0000'b: 500Hz 0001'b: 600Hz 0010'b: 750Hz 0011'b: 800Hz 0100'b: 1kHz 0101'b: 1.2kHz 0110'b: 1.5kHz 0111'b: 1.6kHz 1000'b: 2kHz 1001'b: 2.4kHz 1010'b: 3kHz

				1011’b: 3.2kHz 1100’b: 4kHz 1101’b: 4.8kHz 1110’b: 6kHz 1111’b: 6.4kHz
beep_gen_vol	7:5	R/W	4’h	Select Gain for Beep Gen. 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB 111’b: -21dB
reserved	4:3	R	0’h	Reserved
inv_jd	2	R/W	0’b	Jack Detection Status Polarity 0’b: Normal 1’b: Output Invert
inv_ovtd	1	R/W	0’b	Over Temperature Status Polarity 0’b: Normal 1’b: Output Invert
inv_ovcd	0	R/W	0’b	Speaker Amplifier Over Current Status Polarity 0’b: Normal 1’b: Output Invert

8.29. Reg-4Ah: Internal Status and Sticky Control

Default: 0000’h

Table 43. MX4A Internal Status and Sticky Control

Port Name	Bits	Read/Write	Reset Status	Description
en_jd_sticky	15	R/W	0’b	Sticky Control for Jack Detect 0’b: Disable 1’b: Enable
Reserved	14	R	0’b	Reserved
en_ovt_sticky	13	R/W	0’b	Sticky Control for Over Temperature 0’b: Disable 1’b: Enable
en_ovcd_sticky	12	R/W	0’b	Sticky Control for Over Current of Speaker Amplifier

				0’b: Disable 1’b: Enable
reserved	11	R	0’h	Reserved
Status_jd1_in	10	R	0’b	JD1 Pin Status 0’b: Low 1’b: High
Status_jd2_in	9	R	0’b	JD2 Pin Status 0’b: Low 1’b: High
Reserved	8:6	R	0’h	Reserved
sta_gpio	5	R	0’b	GPIO Pin Status 0’b: Low 1’b: High
Reserved	4	R	0’b	Reserved
sta_jd_internal	3	R	0’b	JD Status Read: Return status of Jack Detect Select output Write: Write ‘0’ to clear stick bit
Reserved	2	R	0’b	Reserved
ovt_status	1	R	0’b	Over Temperature Status Read: return status of each status pin Write: Write ‘0’ to clear stick bit
sta_ovcd	0	R	0’b	Speaker Amplifier Over Current Status Read: return status of each status pin Write: Write ‘0’ to clear stick bit

8.30. Reg-4Ch: GPIO Control 1

Default: 0000’h

Table 44. MX4C GPIO Control 1

Port Name	Bits	Read/Write	Reset Status	Description
reserved	15:14	R	0’h	Reserved
sel_gpio_type	13	R/W	0’h	GPIO/IRQ Function Select 0’b: GPIO 1’b: IRQ Output
reserved	12:0	R	0’h	Reserved

8.31. Reg-4Dh: GPIO Control 2

Default: 0000’h

Table 45. MX4D GPIO Control 2

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:12	R	0’h	Reserved

sel_gpio	11	R/W	0'b	GPIO Pin Configuration 0'b: Input 1'b: Output
sel_gpio_logic	10	R/W	0'b	GPIO Output Pin Control 0'b: Drive low 1'b: Drive high
Reserved	9:0	R	0'h	Reserved

8.32. Reg-52h: General Purpose Control Register 2

Default: 40C0'h

Table 46. MX52 General Purpose Control Register 2

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:10	R	40'h	Reserved
polarity_jd1_out	9	R/W	0'h	JD1 Polarity 0: Normal 1: Invert
polarity_jd2_out	8	R/W	0'h	JD2 Polarity 0: Normal 1: Invert
Reserved	7:0	R	C0'h	Reserved

8.33. Reg-5Ah: Jack Detect Control Register

Default: 0000'h

Table 47. MX5A Jack Detect Control Register

Port Name	Bits	Read/Write	Reset Status	Description
sel_jd_source	15:13	R/W	0'h	Jack Detect Select 000'b: OFF 100'b: Enable JD1 from pin LIN1_L 101'b: Enable JD2 from pin LIN1_R Others are reserved.
reserved	12	R	0'b	Reserved
En_jd_hpo	11	R/W	0'b	Enable Jack Detect Trigger for HPOUT 0'b: Disable 1'b: Enable
Polarity_jd_tri_hpo	10	R/W	0'b	Select Jack Detect Polarity Trigger for HPOUT 0'b: Low trigger 1'b: High trigger
en_jd_spo	9:8	R/W	0'b	Enable Jack Detect Trigger for SPO Œ 00'b: Disable

				01’b: Enable jack detect trigger for SPO_LP/LN 10’b: Enable jack detect trigger for SPO_LP/RP 11’b: Reserved
polarity_jd_tri_spo	7	R/W	0’b	Select Jack Detect Polarity Trigger for SPO 0’b: Low trigger for SPO 1’b: High trigger for SPO
Reserved	6:4	R	0’h	Reserved
Line1_l_pin_share	3	R/W	0’b	Line_In_1_L Pin Share Control 0’b: Line_In 1’b: JD1
Line1_r_pin_share	2	R/W	0’b	Line_In_1_R Pin Share Control 0’b: Line_In 1’b: JD2
en_jd_axo	1	R/W	0’b	Enable Jack Detect Trigger for AXO 0: Disable 1: Enable
polarity_jd_tri_axo	0	R/W	0’b	Select Jack Detect Polarity Trigger for AXO • 0: Low trigger 1: High trigger

Œ When enable jack detection function for speaker output. There are two settings for speaker amplifier:
At Class-D mode, will keep differential output.
At Class-AB mode, will keep single-end output and weak driving power.

• When enable jack detection function for AUX output. That will fix at single-ended output mode.

8.34. Reg-64h: ALC Function Control 1

Default: 0206’h

Table 48. MX64 ALC Function Control 1

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:13	R	0’h	Reserved
sel_alc_atk	12:8	R/W	2’h	Select ALC Attack RateŒ 00’h: 83 uSec 01’h: 0.167 mSec … 10’h: 5.46 Sec Others: Reserved
Reserved	7:5	R	0’h	Reserved
sel_rc_rate	4:0	R/W	6’h	Select ALC Recovery Rate • 00’h: 83 uSec 01’h: 0.167 mSec … 10’h: 5.46 Sec Others: Reserved

Œ Attack time=(4*2^n)/Sample_Rate, n=Reg64[12:8], default=0.33mS, Sample rate is 48kHz

• Recovery time=(4*2^n)/Sample_Rate, n= Reg64 [4:0], default=5.3mS, Sample rate is 48kHz

8.35. Reg-65h: ALC Function Control 2

Default: 0000’h

Table 49. MX65 ALC Function Control 2

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:4	R	0’h	Reserved
noise_gate_boost	3:0	R/W	0’h	Select Compensation Gain When Signal is Below Noise Gate Level. 0’h: 0dB 1’h: 3dB 2’h: 6dB … E’h: 42dB F’h: 45dB

8.36. Reg-66h: ALC Function Control 3

Default: 2000’h

Table 50. MX66 ALC Function Control 3

Port Name	Bits	Read/Write	Reset Status	Description
sel_alc	15:14	R/W	0’h	ALC Enable Control 00’b: Disable ALC 01’b: Enable ALC to DAC Path 10’b: Disable ALC 11’b: Enable ALC to ADC Path
update_alc_param	13	R	1’h	Update ALC Parameter Write 1’b to update all alc parameter
sel_alc_thmax	12:8	R/W	0’h	ALC Signal Limiter Level 00’h= 0dBFS 01’h= -1.5dBFS 02’h= -3dBFS 03’h= -4.5dBFS … 1F’h= -46.5dBFS, with 1.5dB/step
en_alc_noise_gate	7	R/W	0’b	Enable Noise Gate Function 0’b: Diaable 1’b: Enable
en_alc_noise_gate_hold	6	R/W	0’h	Enable Noise Gate Hold Data Function 0’b: Disable 1’b: Enable
Reserved	5	R	0’h	Reserved
sel_alc_noise_th	4:0	R/W	0’h	Noise Gate Threshold 00’h: -36dBFS 01’h: -375dBFS … 1F’h: -82.5 dBFS, with 1.5dB/step

8.37. Reg-68h: Pseudo Stereo & Spatial Effect Control

Default: 0553'h

Table 51. MX68 Pseudo Stereo & Spatial Effect Control

Port Name	Bits	Read/Write	Reset Status	Description
spatial_ctrl_en	15	R/W	0'h	Spatial Effect Enable 0: Disable 1: Enable
apf_en	14	R/W	0'h	Enable All Pass Filter (EN APF) 0: Disable 1: Enable The coefficient a1 is loaded from apf_parm_a1
pseudo_stereo_en	13	R/W	0'h	Enable Pseudo Stereo (EN-Pseudo) 0: Disable 1: Enable
en_3d	12	R/W	0'h	Enable Stereo Expension (EN-3D) 0: Disable 1: Enable Load 3D ratio from ratio_parm_3d and 3D Gain from gain_parm_3d
Gainl_parm_3d	11:10	R/W	1'h	3D Gain1 Parameter (SEGn) 00'b: Gain = 1.0 01'b: Gain = 1.5 10'b: Gain = 2.0 11'b: Reserved
Ratiol_parm_3d	9:8	R/W	1'h	3D Ratio1 Parameter (DPn) 00'b: Ratio = 0.0 01'b: Ratio = 0.66 10'b: Ratio = 1.0 11'b: Reserved
Gainr_parm_3d	7:6	R/W	1'h	3D Gain2 Parameter (SEGn) 00'b: Gain = 1.0 01'b: Gain = 1.5 10'b: Gain = 2.0 11'b: Reserved
ratior_parm_3d	5:4	R/W	1'h	3D Ratio2 Parameter (DPn) 00'b: Ratio = 0.0 01'b: Ratio = 0.66 10'b: Ratio = 1.0 11'b: Reserved
Reserved	3:2	R	0'h	Reserved
apf_parm_a1	1:0	R/W	3'h	All Pass Filter parameter a1 00'b: 0 01'b: -0.85 (for 32KHz sample rate or lower) 10'b: -0.90 (for 44.1KHz sample rate) 11'b: -0.95 (for 48KHz sample rate)

8.38. Reg-6Ah: Private Register Address

Default: 0000'h

Table 52. MX6A Private Register Register

Port Name	Bits	Read/Write	Reset Status	Description
reserved	15:8	R	00'h	Reserved
reg_index	7:0	R/W	00'h	Private Register Address (PRxx)

8.39. Reg-6Ch: Private Register Data

Default: 0000'h

Table 53. MX6C Private Register Data

Port Name	Bits	Read/Write	Reset Status	Description
reg_data	15:0	R/W	00'h	Private Register Data

8.40. Reg-6Eh: EQ Control 1

Default: 1000'h

Table 54. MX6E EQ Control 1

Port Name	Bits	Read/Write	Reset Status	Description
eq_sour	15	R/W	0'b	Select EQ Function for DAC or ADC 0'b: DAC path (Analog input to ADC to EQ to DAC to analog output) 1'b: ADC path
Reserved	14	R	0'b	Reserved
eq_para_update	13	R	0'b	EQ Parameter Update Control 0'b: No action 1'b: Update parameter
En_eq_zcd_para	12	R/W	1'h	Zero Detection for Update EQ Parameter and On/Off EQ 0'b: Disable 1'b: Enable
Reserved	11:8	R	00'h	Reserved
reg_typ_hpf_en	7	R/W	0'b	EQ High Pass Filter Mode Control 0'b: High frequency shelving filter 1'b: 1st order typical HPF (-20dB per decade)
reg_typ_lpf_en	6	R/W	0'b	EQ Low Pass Filter Mode Control 0'b: Low frequency shelving filter 1'b: 1st order typical LPF (-20dB per decade)
Reserved	5:1	R	00'h	Reserved
sta_post_vol	0	R	0'b	EQ Post Volume Status. 0'b: Normal 1'b: Overflow.

				This bit is set if overflow had ever occurred. Write 1 to clear it

Œ For analog input to analog output with EQ function is need to set to DAC path to turn-on EQ function.

8.41. Reg-70h: EQ Control 2

Default: 0000'h

Table 55. MX70 EQ Control 2

Port Name	Bits	Read/Write	Reset Status	Description
sta_hpf2	15	R	0'b	EQ High Pass Filter (HPF2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_hpf1	14	R	0'b	EQ High Pass Filter (HPF1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
reserved	13	R	0'b	Reserved
sta_bpf4	12	R	0'b	EQ Band-4 (BP4) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf3	11	R	0'b	EQ Band-3 (BP3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf2	10	R	0'b	EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf1	9	R	0'b	EQ Band-1 (BP1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_lpf	8	R	0'b	EQ Low Pass Filter (LPF) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
en_hpf2	7	R/W	0'h	EQ High Pass Shelving Filter (HPF2) Control. 0'b: Disable 1'b: Enable
en_hpf1	6	R/W	0'b	EQ High Pass Shelving Filter (HPF1) Control.

				0’b: Disable 1’b: Enable
reserved	5	R	0’b	Reserved
en_bpf4	4	R/W	0’b	EQ Band-4 (BP4) Shelving Filter Control. 0’b: Disable 1’b: Enable
en_bpf3	3	R/W	0’b	EQ Band-3 (BP3) Shelving Filter Control. 0’b: Disable 1’b: Enable
en_bpf2	2	R/W	0’b	EQ Band-2 (BP2) Shelving Filter Control. 0’b: Disable 1’b: Enable
en_bpf1	1	R/W	0’b	EQ Band-1 (BP1) Shelving Filter Control. 0’b: Disable 1’b: Enable
en_lpf	0	R/W	0’b	EQ Low Pass Filter (LPF) Shelving Filter Control. 0’b: Disable 1’b: Enable

8.42. Private-00h: EQ Low Pass Filter Coefficient (LPF: a1)

Default: 0000’h

Table 56. PR00 EQ Low Pass Filter Coefficient (LPF: a1)

Port Name	Bits	Read/Write	Reset Status	Description
lpf_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.43. Private-01h: EQ Low Pass Filter Gain (LPF: H0)

Default: 0000’h

Table 57. PR01 EQ Low Pass Filter Gain (LPF: H0)

Port Name	Bits	Read/Write	Reset Status	Description
lpf_h0	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.44. Private-02h: EQ Band Pass Filter 1 Coefficient (BPF1: a1)

Default: 0000’h

Table 58. PR02 EQ Band Pass Filter 1 Coefficient (BPF1: a1)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.45. Private-03h: EQ Band Pass Filter 1 Coefficient (BPF1: a2)

Default: 0000'h

Table 59. PR03 EQ Band Pass Filter 1 Coefficient (BPF1: a2)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.46. Private-04h: EQ Band Pass Filter 1 Gain (BPF1: H0)

Default: 0000'h

Table 60. PR04 EQ Band Pass Filter 1 Gain (BPF1: H0)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.47. Private-05h: EQ Band Pass Filter 2 Coefficient (BPF2: a1)

Default: 0000'h

Table 61. PR05 EQ Band Pass Filter 2 Coefficient (BPF2: a1)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.48. Private-06h: EQ Band Pass Filter 2 Coefficient (BPF2: a2)

Default: 0000’h

Table 62. PR06 EQ Band Pass Filter 2 Coefficient (BPF2: a2)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.49. Private-07h: EQ Band Pass Filter 2 Gain (BPF2: H0)

Default: 0000’h

Table 63. PR07 EQ Band Pass Filter 2 Gain (BPF2: H0)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.50. Private-08h: EQ Band Pass Filter 3 Coefficient (BPF3: a1)

Default: 0000’h

Table 64. PR08 EQ Band Pass Filter 3 Coefficient (BPF3: a1)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.51. Private-09h: EQ Band Pass Filter 3 Coefficient (BPF3: a2)

Default: 0000’h

Table 65. PR09 EQ Band Pass Filter 3 Coefficient (BPF3: a2)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.52. Private-0Ah: EQ Band Pass Filter 3 Gain (BPF3: H0)

Default: 0000’h

Table 66. PR0A EQ Band Pass Filter 3 Gain (BPF3: H0)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.53. Private-0Bh: EQ High Pass Filter 1 Coefficient (HPF1: a1)

Default: 0000’h

Table 67. PR0B EQ High Pass Filter 1 Coefficient (HPF1: a1)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.54. Private-0Ch: EQ High Pass Filter 1 Gain (HPF1: H0)

Default: 0000’h

Table 68. PR0C EQ High Pass Filter 1 Gain (HPF1: H0)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.55. Private-0Dh: EQ High Pass Filter 2 Coefficient (HPF2: a1)

Default: C01E’h

Table 69. PR0D EQ High Pass Filter 2 Coefficient (HPF2: a1)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.56. Private-0Eh: EQ High Pass Filter 2 Coefficient (HPF2: a2)

Default: 1FE2’h

Table 70. PR0E EQ High Pass Filter 2 Coefficient (HPF2: a2)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.57. Private-0Fh: EQ High Pass Filter 2 Gain (HPF2: H0)

Default: 1FF1’h

Table 71. PR0F EQ High Pass Filter 2 Gain (HPF2: H0)

Port Name	Bits	Read/Write	Reset Status	Description
bpf1_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.58. Private-11h: EQ Input Volume Control

Default: 0000’h

Table 72. PR11 EQ Input Volume Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:3	R	0’h	Reserved
reg_eq_pre_vol	2:0	R/W	000’b	EQ Input Volume 000b:0dB 001b:-3dB 010b:-6dB 011b:-9dB 100b:-12dB 101b:-15dB 110b:-18dB 111b:-21dB

8.59. Private-12h: EQ Output Volume Control

Default: 0003'h

Table 73. PR12 EQ Output Volume Control

Port Name	Bits	Read/Write	Reset Status	Description
Reserved	15:4	R	0'h	Reserved
reg_eq_post_vol	3:0	R/W	0011'b	EQ Output Volume 0000'b: -4.5dB 0001'b: -3dB 0010'b: -1.5dB 0011'b: 0dB 0100'b: 1.5dB 0101'b: 3dB 0110'b: 4.5dB 0111'b: 6dB 1000'b: 7.5dB 1001'b: 9dB 1010'b: 10.5dB 1011'b: 12dB 1100'b: 13.5dB 1101'b: 15dB 1110'b: 16.5dB 1111'b: 18dB

8.60. Private-13h: EQ Band Pass Filter 4 Coefficient (BPF4: a1)

Default: 0000'h

Table 74. PR13 EQ Band Pass Filter 4 Coefficient (BPF4: a1)

Port Name	Bits	Read/Write	Reset Status	Description
bpf4_a1	15:0	R/W	0'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.61. Private-14h: EQ Band Pass Filter 4 Coefficient (BPF4: a2)

Default: 0000'h

Table 75. PR14 EQ Band Pass Filter 4 Coefficient (BPF4: a2)

Port Name	Bits	Read/Write	Reset Status	Description
bpf4_a1	15:0	R/W	0'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.62. Private-15h: EQ Band Pass Filter 4 Gain (BPF4: H0)

Default: 0000’h

Table 76. PR15 EQ Band Pass Filter 4 Gain (BPF4: H0)

Port Name	Bits	Read/Write	Reset Status	Description
bpf4_a1	15:0	R/W	0’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.63. Private-21h: ALC Function Control 4

Default: 0000’h

Table 77. PR21 ALC Function Control 4

Port Name	Bits	Read/Write	Reset Status	Description
Sel_dac_post_bst	8:4	R/W	0’h	DAC Digital Post Gain 00’h= 0dB 01’h= 1.5dB 02’h= 3dB 03’h= 4.5dB …….. 13’h= 28.5dB, with 1.5dB/step Others: Reserved

8.64. Reg-7Ah: Version ID

Default: 0000’h

Table 78. MX7A Version ID

Register:: 0x7A					**0000’h**
Net-list Name	**Bits**	**Read / Write**	**Reset Status**	**Comment**	**Config**
Reserved	15:8	R	00’h	Reserved	
version_id	7:0	R	00’h	Version ID	

8.65. Reg-7C: Vender ID

Default: 0000’h

Table 79. MX7C Vender ID

Register:: 0x7C					10EC’h
Net-list Name	**Bits**	**Read / Write**	**Reset Status**	**Comment**	**Config**
vender_id	15:0	R	10EC’h	Vender ID “10EC”	

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 80. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	3.63	V
Analog	AVDD	-0.3	--	3.63	V
Speaker	SPKVDD	-0.3	-	7[1]	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

Note 1: SPKVDD=5V with 3.5% duty cycle Power bouncing up to SPKVDD=8V is acceptable.

9.1.2. Recommended Operating Conditions

Table 81. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.71	3.3	3.6	V
Digital Core	DCVDD	1.71	3.3	3.6	V
Analog	AVDD	2.3	3.3	3.6	V
Speaker	SPKVDD[1]	2.5	3.3	5	V

Note 1: A 10µF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin.

9.1.3. Static Characteristics

Table 82. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Input Leakage Current	-	-1	-	1	µA
Output Leakage Current (Hi-Z)	-	-1	-	1	µA
Output Buffer High Drive Current	-	-	22	-	mA
Output Buffer Low Drive Current	-	-	10	-	mA
V_{MID} Internal Serial Resistor	-	25	50	75	KΩ
V_{MID} Internal Serial Resistor Ratio	-	95	100	105	%

Note: DVDD=3.3V, $T_{ambient}$=25°C, with 50pF external load.

9.2. Analog Performance Characteristics

Table 83. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs (Single-ended)	-	1.0	-	Vrms
Line Inputs (Differential)	-	TBD	-	Vrms
MIC Inputs (Single-ended)	-	1.0	-	Vrms
MIC Inputs (Differential)	-	TBD	-	Vrms
Full Scale Output Voltage				
Line Outputs (Single-ended)	-	1.0	-	Vrms
Line Outputs (Differential)	-	TBD	-	Vrms
Headphone Amplifiers Outputs	-	TBD	-	Vrms
Speaker Amplifiers Outputs (SPKVDD=3.6V with 8Ω Load, 1% THD+N)		2.3		
S/N Ratio (A-weighted, HPL/R or MONO with 10KΩ/50pF Load)				
STEREO DAC	-	96	98	dB
STEREO ADC	-	92	93	dB
Total Harmonic Distortion + Noise (HPL/R or MONO with 10KΩ/50pF Load)				
STEREO DAC	-	-90	-	dB
STEREO ADC	-	-90	-	dB
MIC Boost Amplifier				
Gain=20dB	-	20	-	dB
Gain=24dB	-	24	-	dB
Gain=30dB	-	30	-	dB
Gain=35dB	-	35	-	dB
Gain=40dB	-	40	-	dB
Gain=44dB	-	44	-	dB
Gain=50dB	-	50	-	dB
Gain=52dB	-	52	-	dB
Input Impedance (Gain=0dB, ADC Mixer=On/Off)				
MIC1 Inputs	-	16	-	KΩ
Input Impedance (Gain=0dB, ADC Mixer=On)				
LINE_IN	-	16	-	KΩ
Input Impedance (Gain=0dB, ADC Mixer=Off)				
LINE_IN	-	32	-	KΩ
Output Impedance				
AUX_OUT	--	2	--	Ω
HP_OUT	-	TBD	-	Ω
SPK_OUT (Class-D)	-	0.4	-	Ω
Headphone Amplifier Output Power (32Ω Load)	-	-	31.25	mW
Headphone Amplifier Quiescent Current (32Ω Load)	-	TBD	-	µA
Headphone Amplifier Efficiency (f_{IN}=1kHz, 32Ω Load, Output Power=25mW)	TBD	-	-	%

Parameter	Min	Typ	Max	Units
Headphone Amplifier THD+N (32Ω Load)				
Output Power=20mW	-	-70	-	dB
Output Power=25mW	-	-70	-	dB
Class-D BTL Speaker Amplifier Output Power				
(SPKVDD=5.0V with 8Ω Load, 1% THD+N)	-	TBD	-	W
(SPKVDD=5.0V with 8Ω Load, 10% THD+N)	-	TBD	-	W
(SPKVDD=5.0V with 4Ω Load, 1% THD+N)	-	TBD	-	W
(SPKVDD=5.0V with 4Ω Load, 10% THD+N)	-	TBD	-	W
Class-AB BTL Speaker Amplifier Output Power				
(SPKVDD=5.0V with 8Ω Load, 1% THD+N)	-	TBD	-	W
(SPKVDD=5.0V with 8Ω Load, 10% THD+N)	-	TBD	-	W
(SPKVDD=5.0V with 4Ω Load, 1% THD+N)	-	TBD	-	W
(SPKVDD=5.0V with 4Ω Load, 10% THD+N)	-	TBD	-	W
BTL Speaker Amplifier Quiescent Current (8Ω Load, SPKVDD=3.7V)				
Class-D	-	4	-	mA
BTL Speaker Amplifier Efficiency (f_{IN}=1kHz, 8Ω Load, Output Power=700mW)				
Class-D	-	88	-	%
Quiescent Playback Current (DAC to HP_OUT with 16Ω Load)	-	TBD	-	mA
Quiescent Record Current (LINE_IN to ADC)	-	TBD	-	mA
Power Down Current				
I_{DD}	-	-	10	μA
Stand-By Current (AVDD=DBVDD=DCVDD=3.3V, SPKVDD=3.6V) Condition: I2S+DAC+AUX_MIX+AUX_OUT				
I_{DD_AVDD}	-	TBD	-	mA
$I_{DD\_DCVDD+DBVDD}$	-	TBD	-	mA
Stand-By Current (AVDD=DBVDD=DCVDD=3.3V, SPKVDD=3.6V) Condition: I2S+ADC+REC_MIX+MIC_IN				
I_{DD_AVDD}	-	TBD	-	mA
$I_{DD\_DCVDD+DBVDD}$	-	TBD	-	mA
MICBIAS Output Voltage				
0.75*AVDD Setting	-	2.475	-	V
0.9*AVDD Setting	-	2.97	-	V
MICBIAS Drive Current	-	TBD	-	mA
Vref Pull Up Resistor	-	50	-	KΩ

Note: Standard test conditions:
$T_{ambient}$=25°C, DBVDD=DCVDD=AVDD=CPVDD=3.3V, SPKVDD=3.6V.
1kHz input sine wave; PCM Sampling frequency=48kHz; 0dB=1Vrms, Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation; EQ and 3D disabled.

9.3. Signal Timing

9.3.1. I²C Control Interface

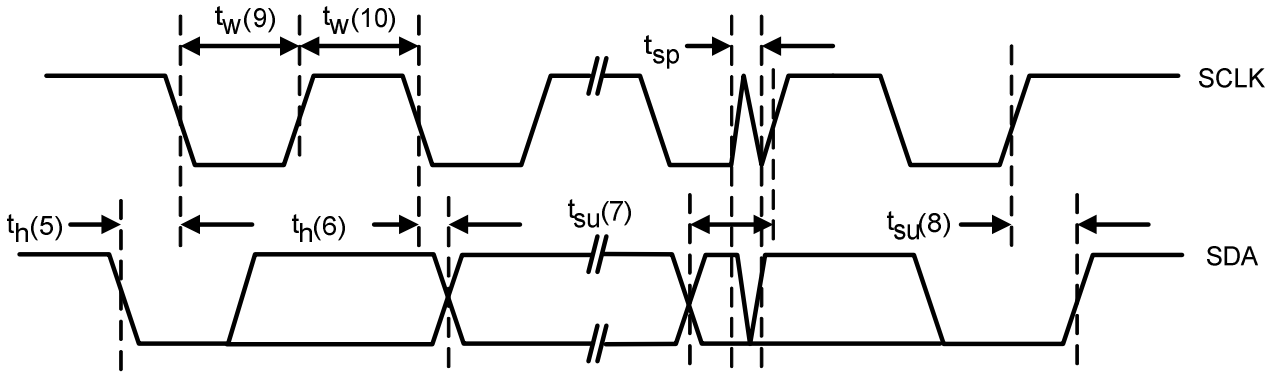


Figure 15. I²C Control Interface

Table 84. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	f	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

Note: Condition: MCLK > 8MHz.

9.3.2. I²S/PCM Interface Master Mode

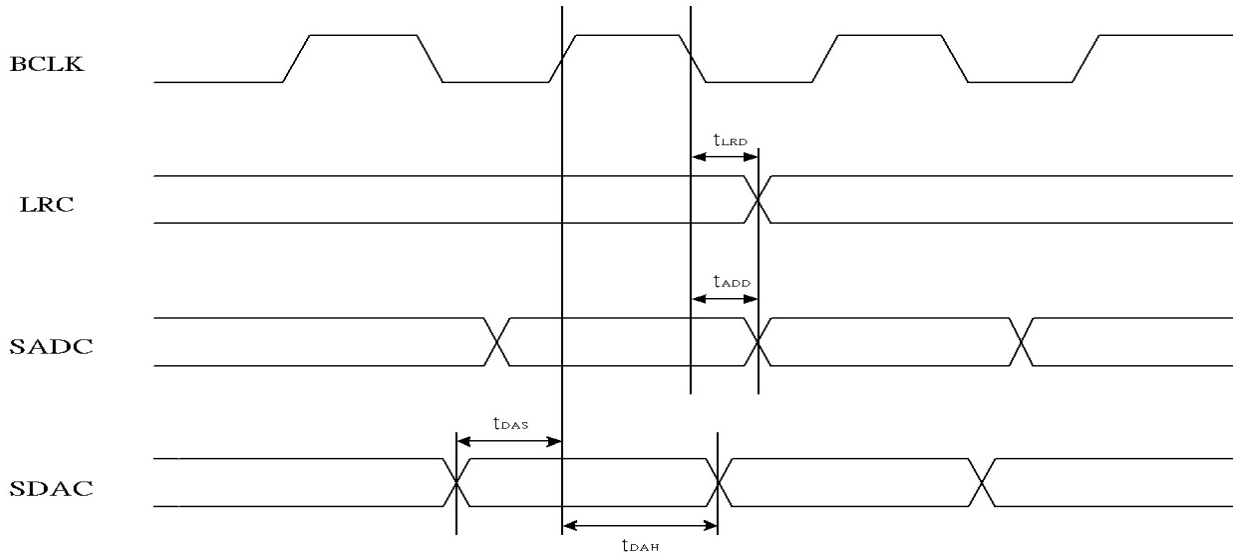


Figure 16. Timing of I²S/PCM Master Mode

Table 85. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

9.3.3. I²S/PCM Interface Slave Mode

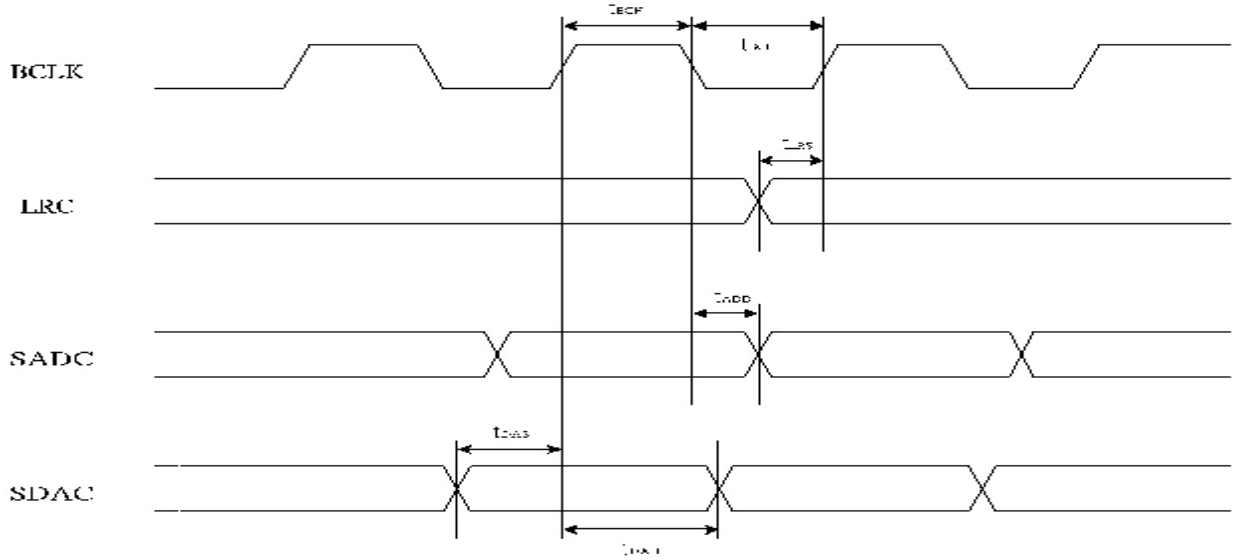
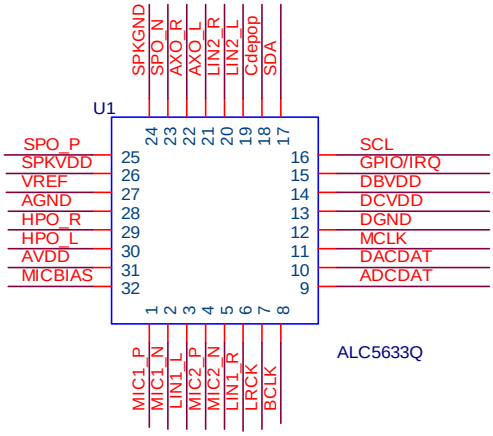


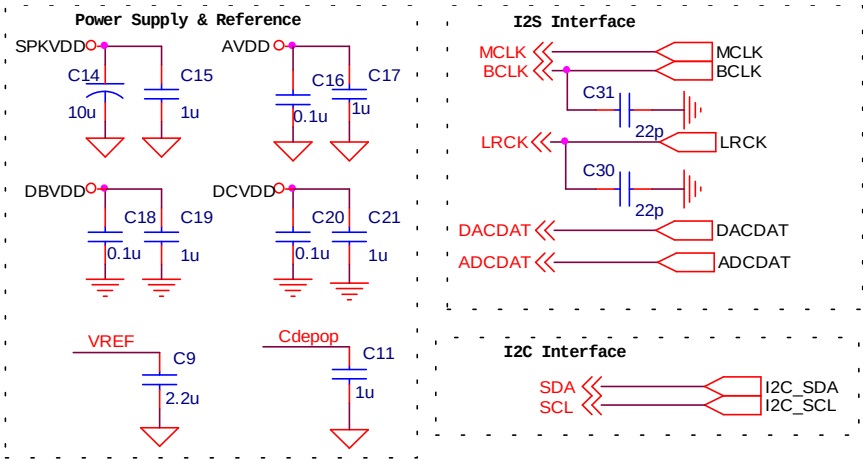
Figure 17. I²S/PCM Slave Mode Timing

Table 86. I²S/PCM Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10. Application Circuits





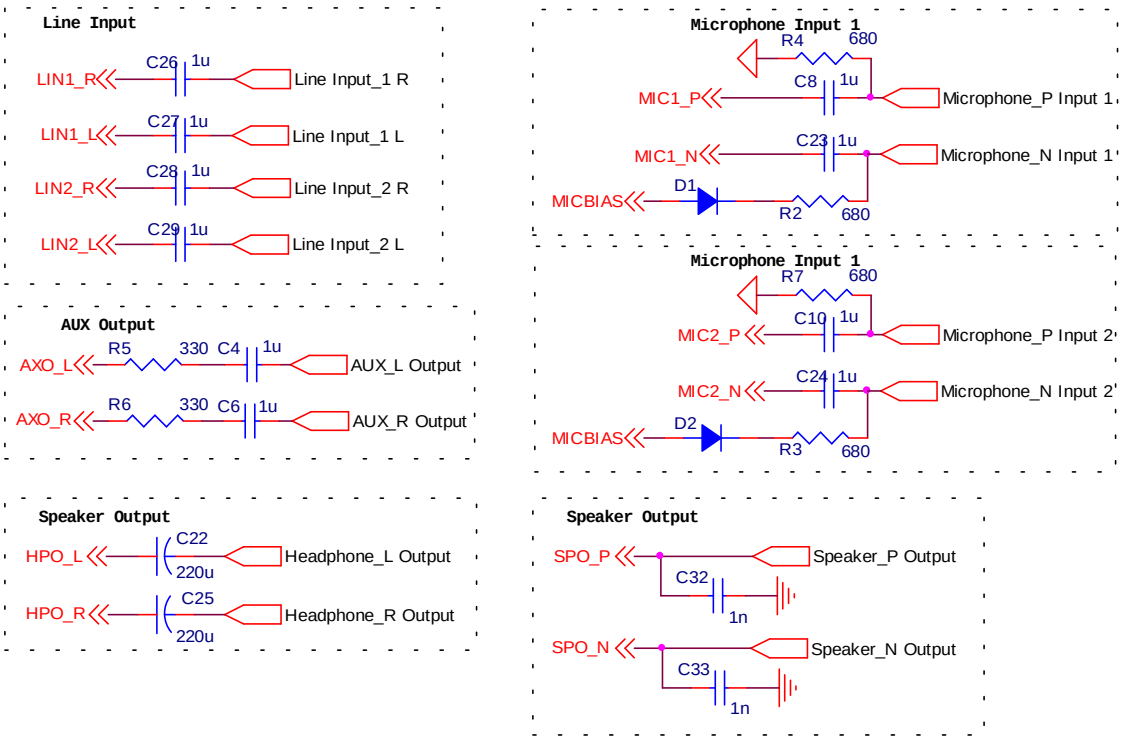
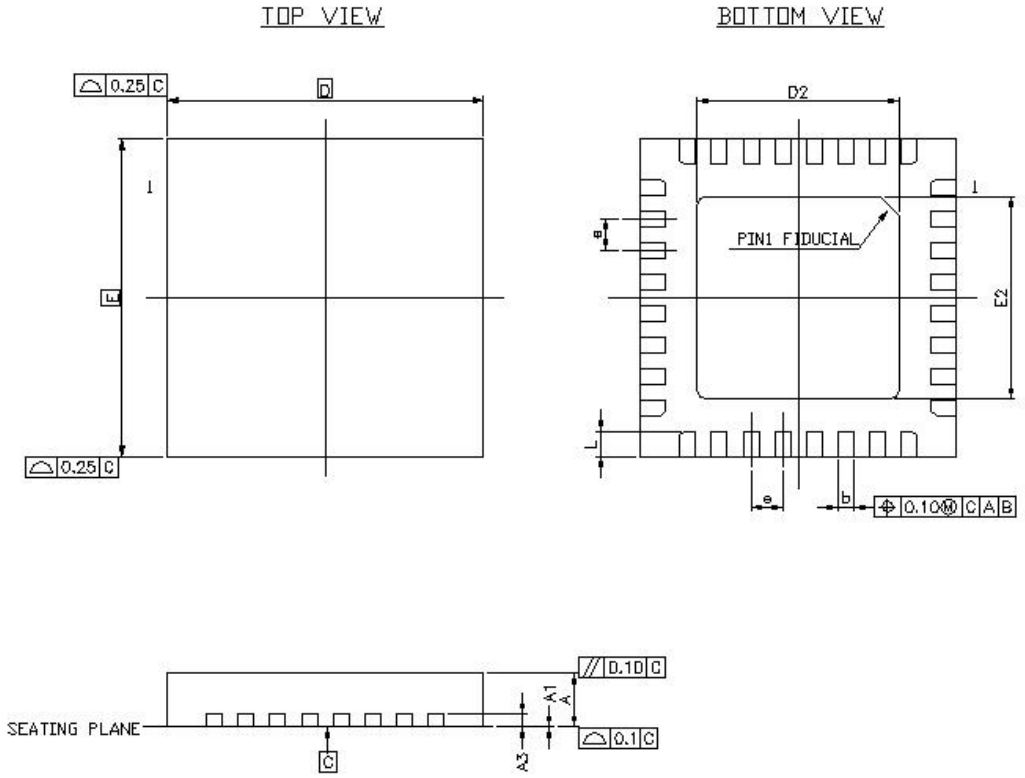


Figure 18. Application Circuit

11. Mechanical Dimensions

LFCSP32 (QFN-32, 5x5mm^2)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
c	—	—	0.6	—	—	0.024
D/E	5.00BSC			0.197BSC		
D_2/E_2	3.10	3.35	3.60	0.122	0.132	0.142
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

Figure 19. Package Dimension

12. Ordering Information

Table 87. Ordering Information

Part Number	Package	Status
ALC5633Q-GR	QFN-32 (5mmx5mm) Package	N/A