NOT FOR PUBLIC RELEASE

ALC5634

I²S AUDIO DAC + HEADPHONE AMPLIFIER

DATASHEET

Rev. 1.0
10 September 2009
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

DISCLAIMER

Realtek provides this document “as is”, without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5634 Audio DAC IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/09/10	First release.

Table of Contents

List of Tables

List of Figures

1. General Description

The ALC5634 is a highly-integrated I^2S/PCM interface audio DAC with multiple input/output ports, and is designed for multimedia handheld devices. It provides a Stereo Hi-Fi DAC for playback via the I^2S/PCM interface.

To reduce component count, the ALC5634 can connect to:

- LINEIN_L/R stereo Single-Ended analog inputs that can be configured to Differential analog input
- AUXIN_L/R stereo Single-Ended analog inputs that can be configured to Differential analog input
- LINE3_L/R stereo Single-Ended analog inputs
- Single-Ended stereo Headphone Output
- STEREO Bridge-Tied Load (BTL) LINE_OUT

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality.

The ALC5634 AVDD operates at supply voltages from 2.3V to 3.6V. DCVDD and DBVDD operate from 1.8 to 3.6V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10μA.

The ALC5634 is available in a 5x5mm 'Green' QFN-32 package, making it ideal for use in handheld portable systems.

2. Features

- Digital-to-Analog Converter with 100dB SNR, and –86dB THD+N at 3.3V
- Three analog stereo single-ended or one stereo differential input, LINEIN_L/R, AUXIN_L/R, and LINE3_L/R
- Stereo BTL (Bridge-Tied Load) LINE_OUT
- Supports playback soft-mute, digital volume, digital AVC
- Stereo headphone output with on-chip 45mW headphone driver (AVDD=3.3V, 16Ω load)
- Supports pop noise suppression with external capacitor
- Digital power supplies from 1.8V to 3.6V
- Analog power and headphone power supplied from 2.3V to 3.6V
- Power management and enhanced power saving
- Internal PLL can receive wide range of clock input
- Supports sampling rate 8KHz~192KHz
- Supports I^2C control interface
- Supports three programmable data interfaces
  - I^2S, left justified, or DSP
  - 16/20/24 bits word length
  - Master or Slave clock mode
- 32-pin QFN 5x5mm package for small footprint

3. System Applications

- Portable media player
- MP3 player
- Bluetooth A2DP (Advanced Audio Distribution Profile) headsets
- Portable Navigation Device (PND)
- Multimedia phone

4. Block Diagram

4.1. Function Block

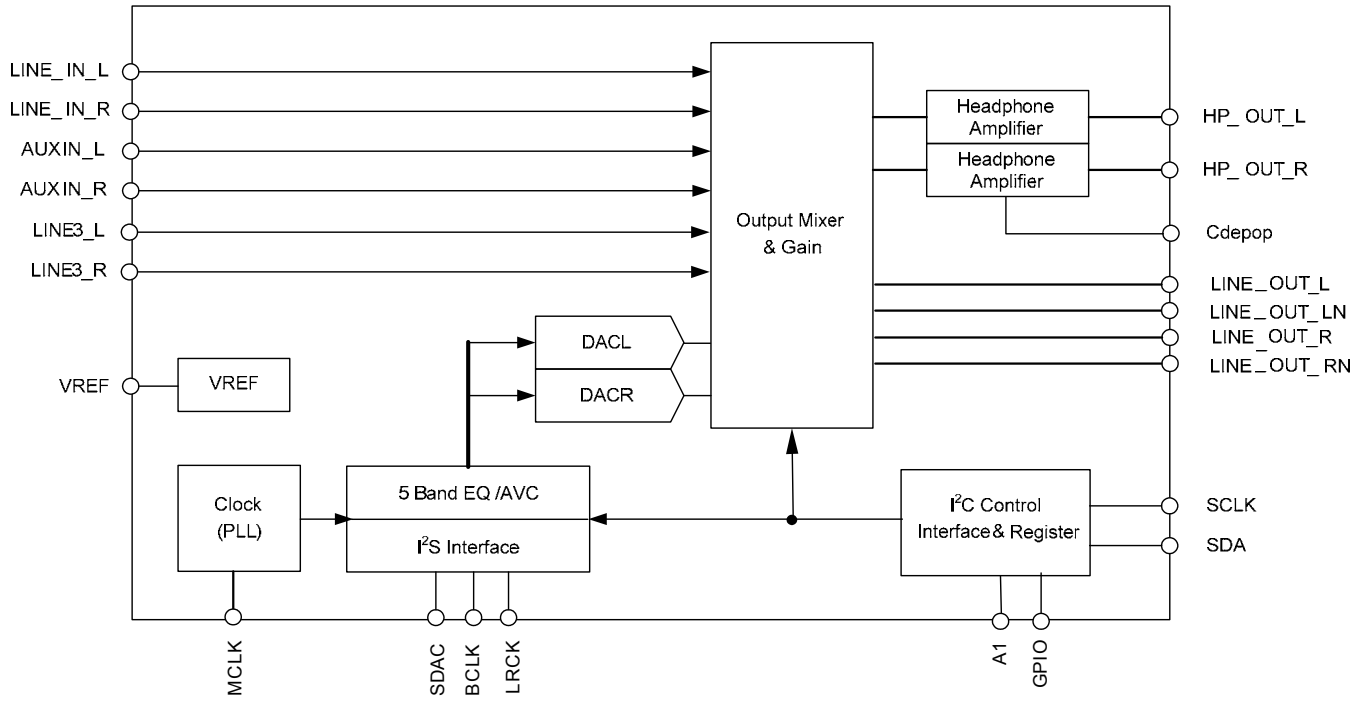


Figure 1. Block Diagram

4.2. Audio Mixer Path

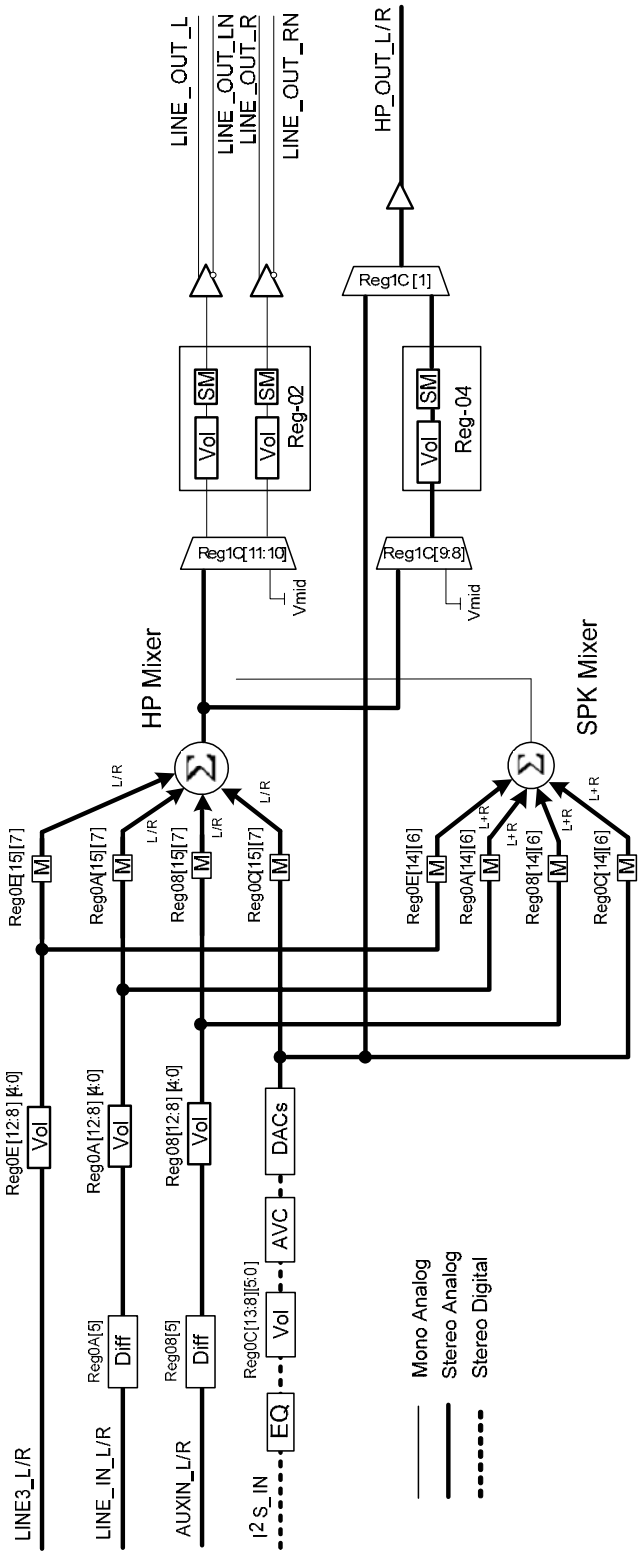


Figure 2. Audio Mixer Path

5. Pin Assignments

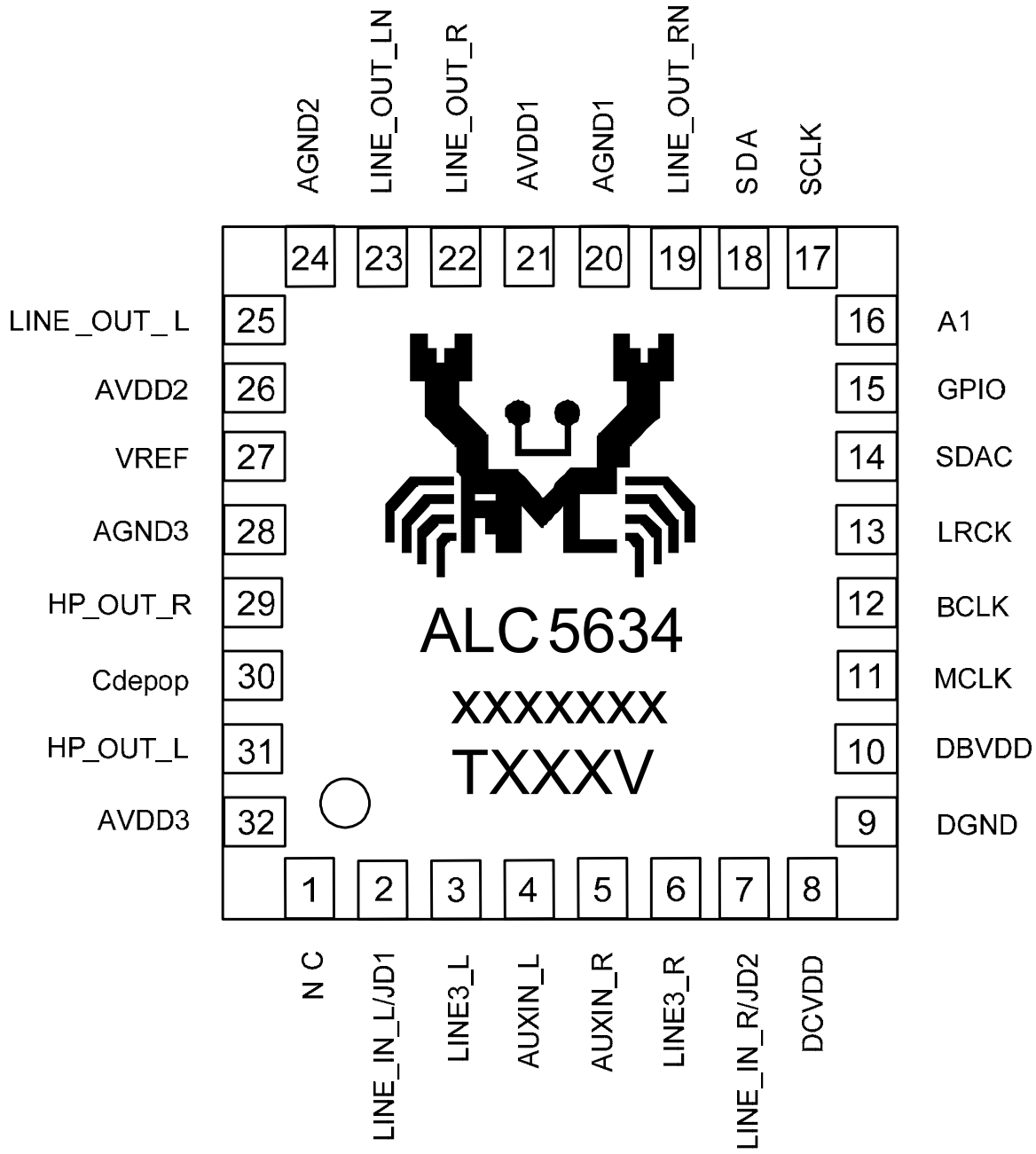


Figure 3. Pin Assignments

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3.

6. Pin Description

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin No.	Description	Characteristic Definition
MCLK	I	11	Main Clock Input	Schmitt trigger input
SCLK	I	17	I^2C: Clock Input	Schmitt trigger input
SDA	IO	18	I^2C: Data Input and Output	Schmitt trigger input/output
LRCK	IO	13	Digital Audio Input Frame Sync	Schmitt trigger input/output
BCLK	IO	12	Digital Audio Serial Clock	Schmitt trigger input/output
SDAC	I	14	Digital Audio Serial Data Input	Schmitt trigger input
GPIO	IO	15	General Purpose I/O	Schmitt trigger input/output
A1	I	16	I^2C Address A1; Directly Connect to GND or VDD	-

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
LINE_IN_L/JD1	I	2	Line Input Left Channel/Jack Detect_1	Analog input
LINE_IN_R/JD2	I	7	Line Input Right Channel/Jack Detect_2	Analog input
AUXIN_L	I	4	Aux Input Left Channel	Analog input
AUXIN_R	I	5	Aux Input Right Channel	Analog input
LINE3_L	I	3	LINE3 Input Left Channel	Analog input
LINE3_R	I	6	LINE3 Input Right Channel	Analog input
LINE_OUT_R	O	22	Line Out Right Channel	Line amplifier output
LINE_OUT_RN	O	19	Line Out Negative Right Channel	Line amplifier output
LINE_OUT_L	O	25	Line Out Left Channel	Line amplifier output
LINE_OUT_LN	O	23	Line Out Negative Left Channel	Line amplifier output
HP_OUT_R	O	29	Headphone Out Left Channel	Analog amplifier output
HP_OUT_L	O	31	Headphone Out Right Channel	Analog amplifier output

6.3. Filter/Reference/Test Pins

Table 3. Filter/Reference Pins

Name	Type	Pin No	Description	Characteristic Definition
VREF	O	27	Reference Voltage Output; Connect 4.7µf Capacitor to Analog GND	Capacitor to analog ground
Cdepop	O	30	Cdepop Capacitor; Connect 1µF Capacitor to Analog GND	Capacitor to analog ground

6.4. Power & Ground Pins

Table 4. Power/Ground Pins

Name	Type	Pin No	Description	Characteristic Definition
DGND	P	9	Digital GND	Digital ground
DCVDD	P	8	Digital VDD	Digital power for core
DBVDD	P	10	Digital VDD	Digital power for I/O
AGND1	P	20	Analog Amplifier GND	Analog ground
AGND2	P	24	Analog Amplifier GND	Analog ground
AVDD1	P	21	Analog Amplifier VDD	Analog power
AVDD2	P	26	Analog Amplifier VDD	Analog power
AGND3	P	28	Analog GND	Analog ground
AVDD3	P	32	Analog VDD	Analog power
DGND	P	Exposed Pad	Digital GND; must be connected to System DGND	Digital ground

Note1: DBVDD ≥ DCVDD, AVDD1=AVDD2=AVDD3 ≥ DCVDD.

Note2: All VDD individually connected to 1µF Capacitor to system GND is required.

6.5. Not Connected

Table 5. Not Connected Pins

Name	Type	Pin No	Description	Characteristic Definition
NC	-	1	Not Connected	-

7. Functional Description

7.1. Power

The ALC5634 has many power blocks. The power supply limit conditions are DBVDD ≥ DCVDD and AVDD1=AVDD2=AVDD3 ≥ DCVDD. To prevent pop noise, we suggest you to power on DCVDD before powering on AVDD.

7.2. Reset

There are two type of reset operation: Power-On-Reset (POR) and Register reset.

Table 6. Reset Operation

Reset Type	Trigger Condition	Codec Response
POR	Monitor Digital Power Supply Voltage Reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write Reg00	Reset all registers to default values.

7.2.1. Power-On Reset (POR)

When power is on, DCVDD passes through the V_{POR} band of the ALC5634 (V_{PORH}~V_{PORL}). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 7. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: V_{POR_OFF} must be below V_{POR_ON}.

7.3. Clocking

The ALC5634 audio system clock can be selected from an external MCLK or an internal PLL. No matter which is used, the ALC5634 requires 256/384*Fs to provide audio SYSCLK.

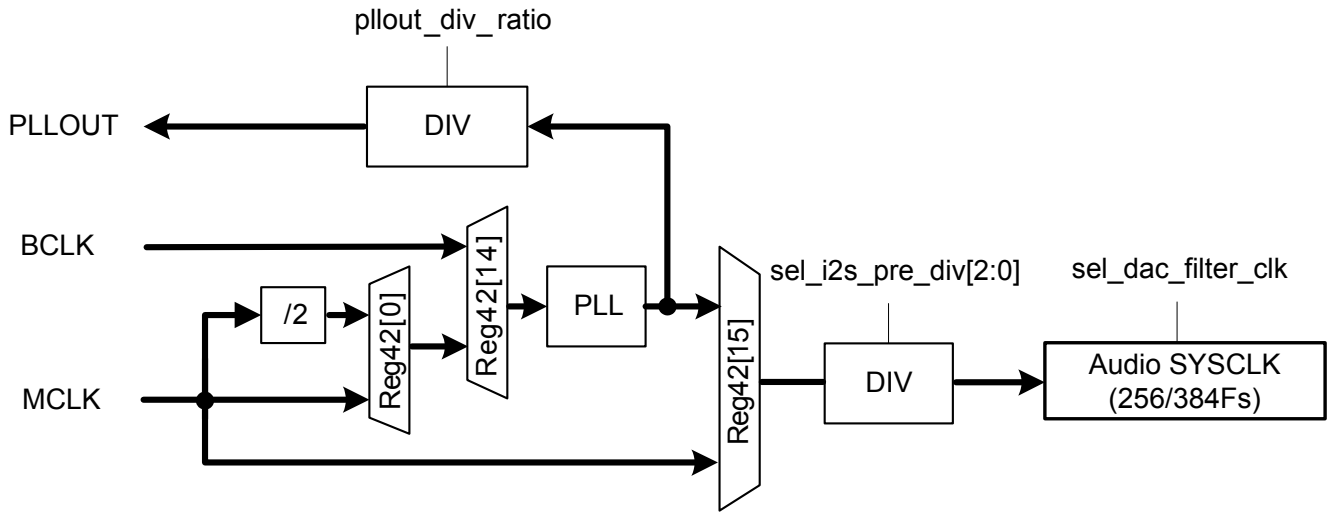


Figure 4. Audio SYSCLK

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz (64Fs of 32KHz) to 40MHz. Typical choices are 2.048MHz, 4.096MHz, and 13MHz. The source of the PLL can be set to MCLK or BCLK by setting sel_pll_sour (Reg42[14]). Firmware can setup a PLL to output the desired frequency as the system clock.

The PLL transmit formula is: F_{OUT} = (MCLK*(N+2)) / ((M+2)*(K+2)) (Typical K=2)

Table 8. PLL Clock Setting Table for 48K (Unit: MHz)

MCLK	M Code	N Code	Fvco	K Code	Fout
2.048	0	94	98.304	2	24.576
3.6864	1	78	98.304	2	24.576
4.096	0	46	98.304	2	24.576
12	14	129	98.25	2	24.5625
13	14	119	98.3125	2	24.57812
15.36	3	30	98.304	2	24.576
16	5	41	98.28571	2	24.57143
19.2	15	85	98.25882	2	24.5647
19.68	0	8	98.4	2	24.6

Table 9. PLL Clock Setting Table for 44.1K (Unit: MHz)

MCLK	M Code	N Code	Fvco	K Code	Fout
2.048	0	86	90.112	2	22.528
3.6864	0	47	90.3168	2	22.5792
4.096	9	241	90.48436	2	22.62109
12	15	126	90.35294	2	22.58824
13	15	116	90.23529	2	22.55882
15.36	15	98	90.35294	2	22.58824
16	12	77	90.28571	2	22.57143
19.2	15	78	90.35294	2	22.58824
19.68	15	76	90.29647	2	22.57412

7.4. I²C Control Interface

I²C is a 2-wire half-duplex serial communication interface, supporting only slave mode. The host must support MCLK during register access.

7.4.1. Addressing Setting

(MSB)			BIT				(LSB)
0	0	1	1	0	0	A1	RW

Note: A1 must be directly connected to VCC or GND.

7.4.2. Complete Data Transfer

Data Transfer over I²C Control Interface

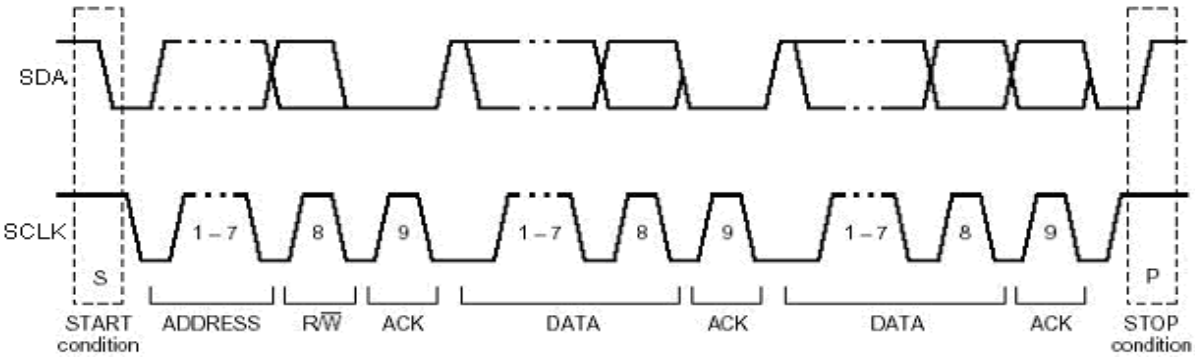


Figure 5. Data Transfer Over I²C Control Interface

Write WORD Protocol

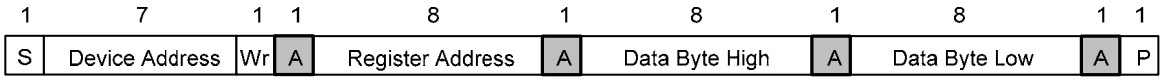
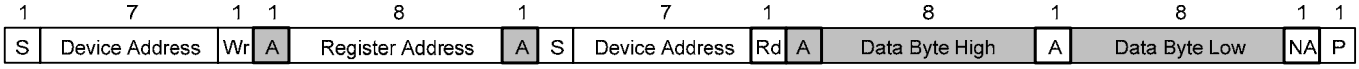


Figure 6. Write WORD Protocol

Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

Figure 7. Read WORD Protocol

7.4.3. Odd-Addressed Register Access

The ALC5634 will return '0000h' when odd-addressed and unimplemented registers are read.

7.5. Digital Data Interface

7.5.1. I²S/PCM Interface

The Digital to Analog Converter (DAC) serial data is input via the SDAC pin. The serial data is shifted in on the rising edge of BCLK (ctrl_i2s_bclk_polarity=0'b) or the falling edge (ctrl_i2s_bclk_polarity=1'b). The Left/Right Clock (LRCK) signal is the frame sync signal. Left/Right data can be swapped by en_dac_lrck_swap.

The ALC5634 I²S/PCM interface can be configured as Master mode or Slave mode. In Master mode (sel_i2s_mode=0'b), BCLK and LRCK are configured as output. In Slave mode (sel_i2s_mode=1'b), BCLK and LRCK are configured as input. The MCLK provides BCLK synchronized clock externally as Stereo System Clock.

The ALC5634 supports three independent I²S/PCM interfaces for Stereo Audio data formats:

- PCM/DSP mode
- Left justified mode
- I²S mode

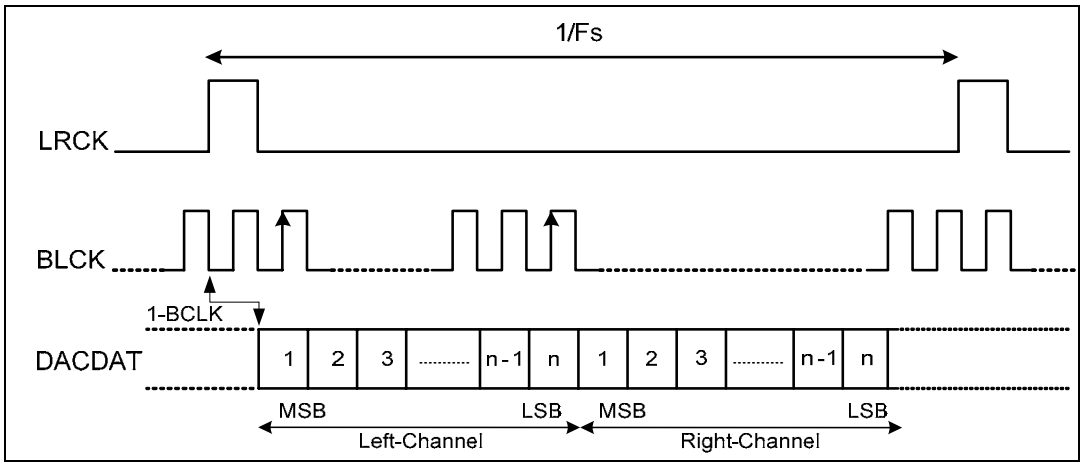


Figure 8. PCM Stereo Data Mode A Format-1 (sel_i2s_data_format=10'b, ctrl_i2s_bclk_polarity=0'b)

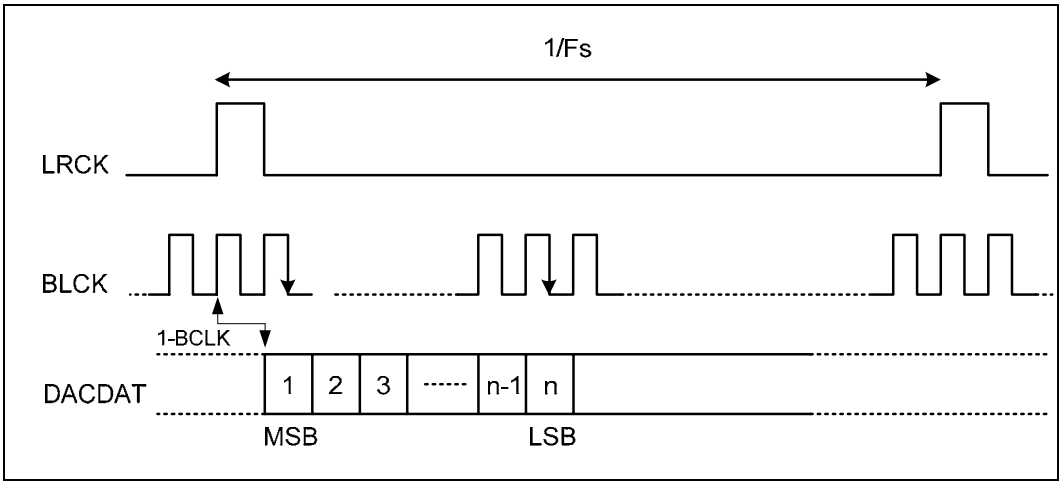


Figure 9. PCM Stereo Data Mode A Format-2 (sel_i2s_data_format=10'b, ctrl_i2s_bclk_polarity=1'b)

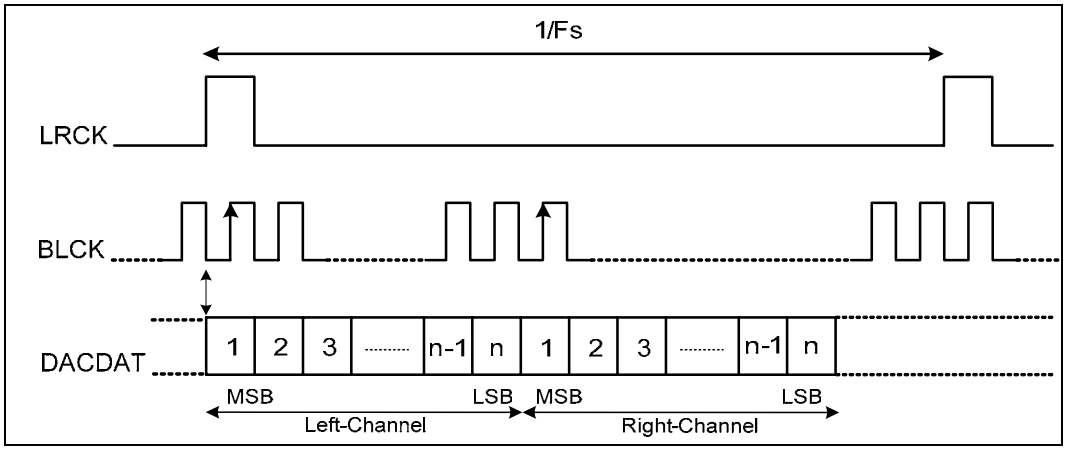


Figure 10. PCM Stereo Data Mode B Format (sel_i2s_data_format=11'b, ctrl_i2s_bclk_polarity=0'b)

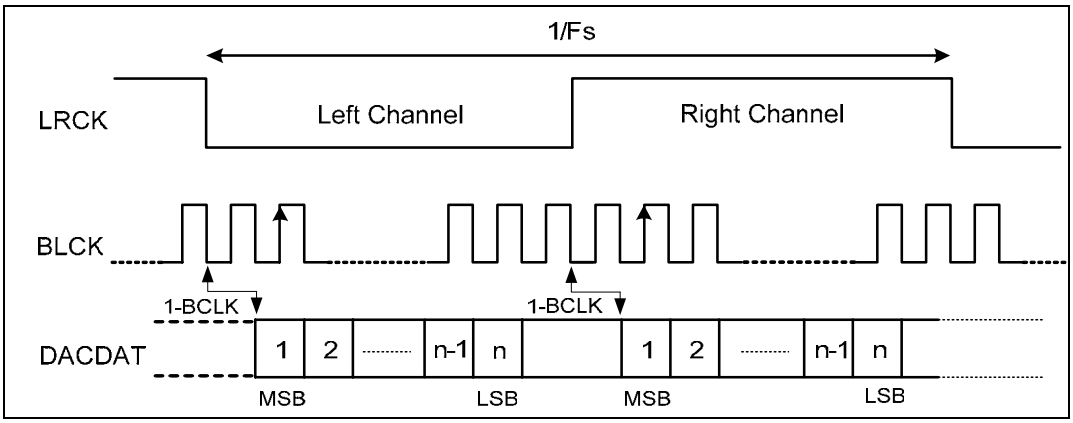


Figure 11. I²S Data Format (sel_i2s_data_format=00'b)

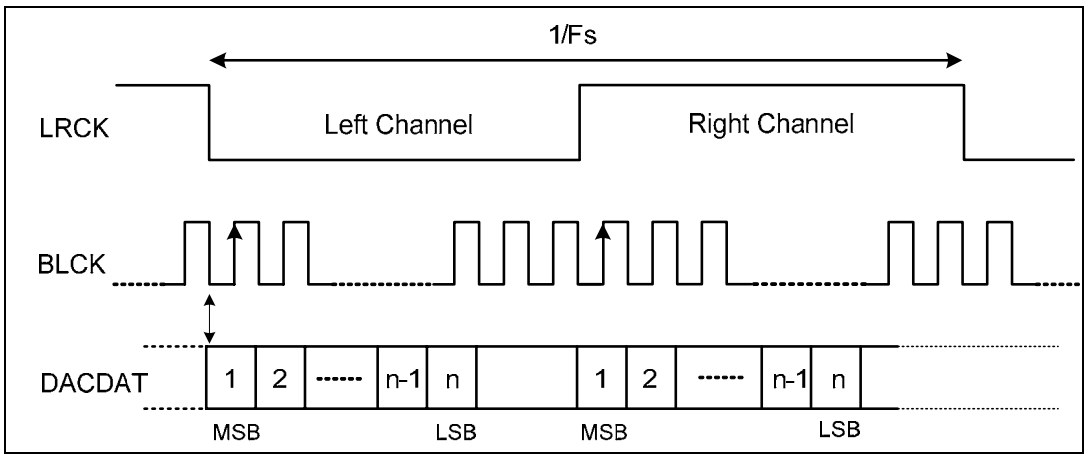


Figure 12. Left-Justified Data Format (sel_i2s_data_format=01'b, ctrl_i2s_bclk_polarity=0'b)

7.6. Analog Signal Path

7.6.1. Line Input

LINE_IN_L and LINE_IN_R provide 2-channel stereo single-ended inputs that can be mixed into any analog output mixer. In addition, LINE_IN_L and LINE_IN_R can be configured as mono channel differential input by en_li_diff, which can only output to the HP mixer.

- LINE_IN_L/R volume and mute are controlled by Reg0A
- sel_li_l_vol and sel_li_r_vol can be used to power down LINE_IN volume control
- LINE_IN_L is pin shared with JD1 and can be configured by sel_jd_source
- LINE_IN_R is pin shared with JD2 and can be configured by sel_jd_source

7.6.2. Auxiliary Input

AUXIN_L and AUXIN_R provide 2-channel stereo single-ended input that can be mixed into any analog output mixer. In addition, AUXIN_L and AUXIN_R can be configured as mono channel differential input by en_auxi_diff, which can only output to the HP mixer.

- AUXIN_L/R volume and mute are controlled by Reg08
- sel_auxi_l_vol and sel_auxi_r_vol can be used to power down AUXIN_L/R volume control

7.6.3. LINE3 Input

LINE3_L and LINE3_R provide 2-channel stereo single-ended input that can be mixed into any analog output mixer.

- LINE3_L/R volume and mute are controlled by Reg0E
- sel_li3_l_vol and sel_li3_r_vol can be used to power down LINE3_L/R volume control

7.6.4. Line Output

LINE_OUT provides two-channel differential output and can be configured to dual single-ended output.

The LINE_OUT source is selected in sel_lio_vol_in as below:

- No Input (V_{MID})
- Headphone mixer
- Speaker mixer

The LINE_OUT volume and mute are controlled by Reg02. pow_liol_vol and pow_lior_vol can be used to power down LINE_OUT.

LINE_OUT supports ‘Soft Volume Delay Mute’ and ‘Zero-Crossing Detect’ functions which can be enabled by en_lio_l_dezero, en_lio_l_softvol, en_lio_r_dezero, and en_lio_r_softvol.

7.6.5. Headphone Output

HP_OUT_L/R provides 2-channel single-ended output. The source of HP_OUT_L/R can be selected from sel_hp_l_in & sel_hp_r_in as below.

- V_{MID}
- Headphone mixer

The HP_OUT_L/R volume and mute are controlled by Reg04, and pow_hp_l_vol and pow_hp_r_vol can be used to power down the HP output volume.

HP_OUT supports 'Soft Volume Delay Mute' and 'Zero-Crossing Detect' functions which can be enabled by en_hp_l_dezero, en_hp_l_softvol, en_hp_r_dezero, and en_hp_r_softvol.

HP_OUT_L/R source can be selected from DAC Stereo output (en_dac_hp) for high quality performance playback.

7.6.6. Stereo DAC

The stereo DAC can be configured to different sample rates by driving 256Fs/384Fs into audio SYSCLK, and individually set by sel_i2s_bclk_ms.

sel_dac_l_vol & sel_dac_r_vol can be used to control the DAC output volume.

7.6.7. Headphone Mixer

The headphone (HP) mixer is used to drive stereo output, including HP_OUT_L/R, LINE_OUT_L/LN, and LINE_OUT_R/RN.

The following signals can be mixed into the headphone mixer:

- LINE_IN_L/R (controlled by Reg0A)
- AUXIN_L/R (controlled by Reg08)
- LINE3_L/R (controlled by Reg0E)
- Stereo DAC output (controlled by Reg0C)

When the LINE_OUT source is from the HP mixer, LINE_OUT_L/LN can be configured to stereo single-ended or mono differential output by setting lineout_source. The headphone mixer can be powered down by setting pow_hp_l_vol & pow_hp_r_vol.

7.6.8. Speaker Mixer

The speaker (SPK) mixer is used to drive LINE_OUT and HP_OUT. The stereo output (HP_OUT_L/R) of the SPK mixer has the same signal on both channels.

The following signals can be mixed into the speaker mixer:

- LINE_IN_L/R (controlled by Reg0A)
- AUXIN_L/R (controlled by Reg08)
- LINE3_L/R (controlled by Reg0E)
- Stereo DAC output (controlled by Reg0C)

Note: The speaker mixer can be powered down by setting pow_mix_spk.

7.7. Power Management

The ALC5634 supports detailed Power Management control registers within Reg3A, 3C, and 3E. Each particular block will be active only when individual bits of Reg3A, 3C, and 3E are set to 'Enable'.

7.8. GPIO and Jack Detect (JD) Function

7.8.1. GPIO Interface

The ALC5634 supports one GPIO that can be configured as Input/Output by sel_gpio_io. When GPIO is configured as Input, the status will be indicated in status_gpio_in. When GPIO is configured as Output, sel_gpio_o_logic is used to drive GPIO to High (1'b) or Low (0'b), and the status can be read in status_gpio_in.

GPIO input polarity can be changed by setting sel_polarity_gpio, and setting Reg48 in order to generate the interrupt (IRQ).

The ALC5634 supports Jack Detect (JD1/JD2/GPIO) to switch ON/OFF the Analog Output (Headphone Out and Line Out) and Mute (V_{MID}). JD1 and JD2 can be pin-shared from LINE_IN_L/R, and are used to enable specified Analog Output configured in the Reg5A Jack Detect Control Register.

In addition, GPIO can be configured to PLLOUT or IRQ_Output by setting Reg4A.

7.8.2. Interrupt

Independent of GPIOs, some Internal Event Signals (over-temperature or over-current) are handled the same as GPIO input, and can be treated as Interrupt sources. The application of an Internal Event Signal is the same as GPIO.

7.9. Headphone Depop

The ALC5634 provides a headphone depop mechanism in order to eliminate the pop noise of headphone out. An external 1µF capacitor is required to connect Cdepop and AGND in this application. See the separate ALC5634 Application Notes for details.

7.10. AVC Control

The Automatic Volume Control (AVC) function dynamically adjusts the input signal quantized by the DAC to an expected sound level by setting THmax and THmin.

When the average level of input signal quantized by the DAC is higher than THmax, the AVC will decrease the selected analog gain to attenuate the quantized Pulse Code Modulation (PCM) signal to a lower amplitude than THmax. When the average level of input signal quantized by DAC is lower than THmin, the AVC will increase the selected analog gain to amplify the input signal. The quantized PCM signal is then set to a higher amplitude than THmin. The quantized PCM has an average level between THmin and THmax.

In order to avoid outputting a strong amplified signal when the gain detector input level is transiting from a very small signal to a normal signal, the AVC block will limit the selected analog gain to unit gain (=0dB) when the input level of the gain detector is lower than THnonact.

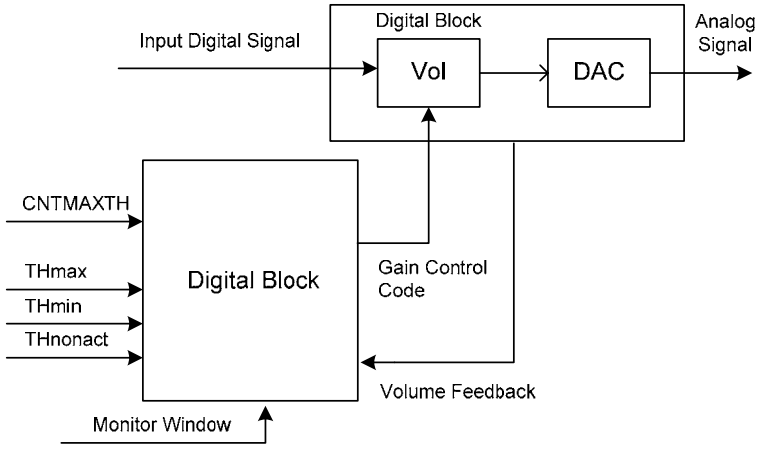


Figure 13. AVC Block of DAC Module

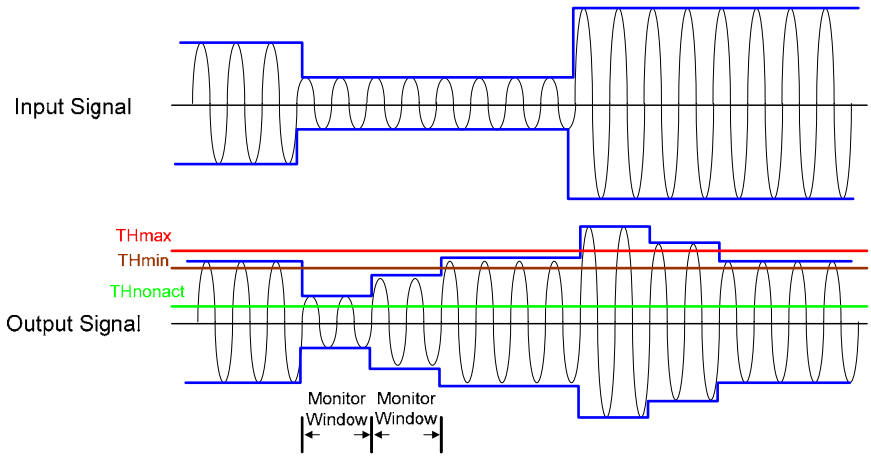


Figure 14. AVC Behavior

7.11. Zero Cross

When Zero-Cross detect is enabled, the ALC5634 will change each output volume or mute only if the signal swing crosses the zero point. This function can avoid pop noise when volume is changed or muted.

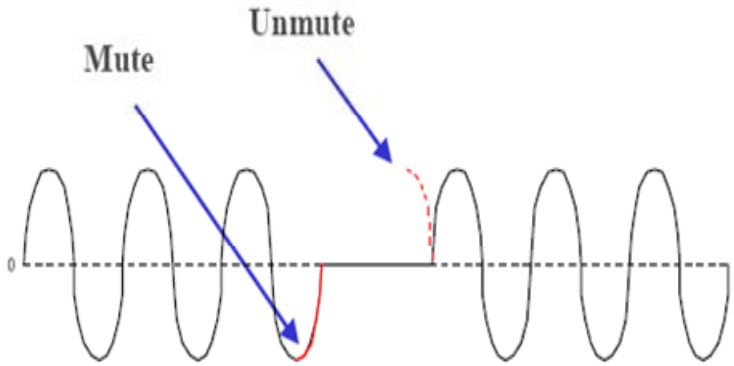


Figure 15. Zero Cross Disabled when Output Muted

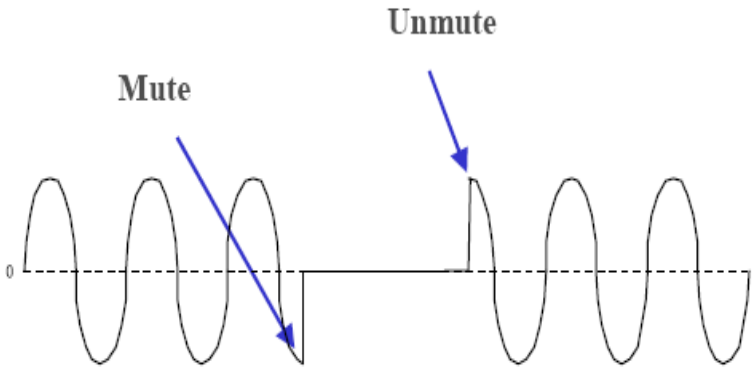


Figure 16. Zero Cross Enabled when Output Muted

8. Register Descriptions

8.1. Reg-02h: Line Output Volume

Default: 8080’h

Table 10. MX02 Line Output Volume

Name	Bits	RW	Default	Description
mute_lio_l	15	RW	1’h	Mute Line Left Output 0: On 1: Mute (-∞ dB)
Reserved	14:13	R	0’h	Reserved
sel_lio_l_vol	12:8	RW	00’h	Line Left Output Volume (LIOL[4:0]) in 1.5dB Steps
mute_lio_r	7	RW	1’h	Mute Line Right Output 0: On 1: Mute (-∞ dB)
Reserved	6:5	R	0’h	Reserved
sel_lio_r_vol	4:0	RW	00’h	Line Right Output Volume (LIOR[4:0]) in 1.5dB Steps *Note: For LIOL/LIOR: 00h: 0dB attenuation.* *1Fh: 46.5dB attenuation.*

8.2. Reg-04h: Headphone Output Volume

Default: C080’h

Table 11. MX04 Headphone Output Volume

Name	Bits	RW	Default	Description
mute_hp_l	15	RW	1’h	Mute Left Headphone Amp Control 0: On 1: Mute Left Channel (-∞ dB)
Reserved	14:13	RW	01’h	Reserved
sel_hp_l_vol	12:8	RW	00’h	Headphone Output Left Volume (HPL[4:0]) in 1.5dB Steps
mute_hp_r	7	RW	1’h	Mute Right Headphone Amp Control 0: On 1: Mute Left Channel (-∞ dB)
Reserved	6:5	R	0’h	Reserved
sel_hp_r_vol	4:0	RW	00’h	Headphone Output Right Volume (HPR[4:0]) in 1.5dB Steps *Note: For HPR/HPL: 00h: 0dB attenuation.* *1Fh: 46.5dB attenuation.*

8.3. Reg-08: Auxiliary Input Volume

Default: C8C8'h

Table 12. MX08 Auxiliary Input Volume

Name	Bits	RW	Default	Description
mute_auxil2hp	15	RW	1'h	Mute AUXIN Left Volume Output to Headphone Left Mixer Control 0: On 1: Mute
mute_auxil2spk	14	RW	1'h	Mute AUXIN Left Volume Output to Speaker Mixer Control 0: On 1: Mute
Reserved	13	R	0'h	Reserved
sel_auxi_l_vol	12:8	RW	08'h	AUXIN Left Volume (AUXLV [4:0]) in 1.5dB Steps
mute_auxir2hp	7	RW	1'h	Mute AUXIN Right Volume Output to Headphone Right Mixer Control* 0: On 1: Mute
mute_auxir2spk	6	RW	1'h	Mute AUXIN Right Volume Output to Speaker Mixer Control* 0: On 1: Mute
en_auxi_diff	5	RW	0'h	AUXIN Differential Input Control 0: Disable 1: Enable. Only output to HP right mixer
sel_auxi_r_vol	4:0	RW	8'h	AUXIN Right Volume (AUXIRV [4:0]) in 1.5dB Steps* *Note: For AUXIRV/AUXI LV: 00h: +12dB gain.* *08h: 0dB attenuation.* *1Fh: 34.5dB attenuation.*

Note: '' indicates no function when Reg-08[5] = 1'b.*

8.4. Reg-0A: Line Input Volume

Default: C8C8'h

Table 13. MX0A Line Input Volume

Name	Bits	RW	Default	Description
mute_lil2hp	15	RW	1'h	Mute Left Volume Output to Headphone Left Mixer Control 0: On 1: Mute
mute_lil2spk	14	RW	1'h	Mute Left Volume Output to Speaker Mixer Control 0: On 1: Mute
Reserved	13	R	0'h	Reserved
sel_li_l_vol	12:8	RW	08'h	Line-In Left Volume (NLV[4:0]) in 1.5dB Steps
mute_lir2hp	7	RW	1'h	Mute Right Volume Output to Headphone Right Mixer Control* 0: On 1: Mute
mute_lir2spk	6	RW	1'h	Mute Right Volume Output to Speaker Mixer Control* 0: On 1: Mute

Name	Bits	RW	Default	Description
en_li_diff	5	RW	0'h	Line-In Differential Input Control 0: Disable 1: Enable. Only output to HP left mixer
sel_li_r_vol	4:0	RW	08'h	Line-In Right Volume (NRV[4:0]) in 1.5dB Steps* *Note: For NRV/NLV: 00h: +12dB gain.* *08h: 0dB attenuation.* *1Fh: 34.5dB attenuation.*

Note: '' indicates no function when Reg-0A[5] = 1'b.*

8.5. Reg-0C: Stereo DAC Digital Volume

Default: D0D0'h

Table 14. MX0C Stereo DAC Digital Volume

Name	Bits	RW	Default	Description
mute_dacl2hp	15	RW	1'h	Mute DAC Left Channel Digital Volume Output to Headphone Left Mixer Control 0: On 1: Mute (-∞ dB)
mute_dacl2spk	14	RW	1'h	Mute DAC Left Channel Digital Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞ dB)
set_dac_l_vol	13:8	RW	10'h	DAC Left Channel Digital Volume (PLV[5:0]) in 0.75dB Steps
mute_dacr2hp	7	RW	1'h	Mute DAC Right Channel Digital Volume Output to Headphone Right Mixer Control 0: On 1: Mute (-∞ dB)
mute_dacr2spk	6	RW	1'h	Mute DAC Right Channel Digital Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞ dB)
Sel_dac_r_vol	5:0	RW	10'h	DAC Right Channel Digital Volume (PRV[5:0]) in 0.75dB Steps *Note: For PRV/PLV: 00h: +12dB gain.* *10h: 0dB attenuation.* *3Fh: 35.25.5dB attenuation.*

8.6. Reg-0E: LINE3 Volume

Default: C8C8'h

Table 15. MX0E LINE3 Volume

Name	Bits	RW	Default	Description
mute_li3l2hp	15	RW	1'b	Mute LINE3 Left Volume Output to Headphone Left Mixer Control 0: On 1: Mute
mute_li3l2spk	14	RW	1'b	Mute LINE3 Left Volume Output to Speaker Mixer Control 0: On 1: Mute
reserved	13	R	0'h	Reserved
sel_li3_l_vol	12:8	RW	08'h	LINE_IN3 Left Volume (NL3V[4:0]) in 1.5dB Steps
mute_li3r2hp	7	RW	1'b	Mute LINE3 Right Volume Output to Headphone Right Mixer Control 0: On 1: Mute
mute_li3r2spk	6	RW	1'b	Mute LINE3 right Volume Output to Speaker Mixer Control 0: On 1: Mute
reserved	5	R	0'h	Reserved
sel_li3_r_vol	4:0	RW	08'h	LINE_IN3 Right Volume (NR3V[4:0]) in 1.5dB Steps

For NL3V/NR3V: 00h: +12dB gain
08h: 0dB attenuation
1Fh: 34.5dB attenuation

8.7. Reg-16h: Soft Delay Volume Control Time

Default: 0009'h

Table 16. MX16 Soft Delay Volume Control Time

Name	Bits	RW	Default	Description
Reserved	15:4	R	0'h	Reserved
sel_sync_softvol	3:0	RW	1001'b	Soft Volume Change Delay Time (Default=1001b) 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved

Note: SVSYNC=1/Fs, Step: -1.5dBFS.

8.8. Reg-1Ch: Output Mixer Control

Default: 8000’h

Table 17. MX1C Output Mixer Control

Name	Bits	RW	Default	Description
Reserved	15:12	R	8’h	Reserved This register must be set to 08’h
sel_lio_vol_in	11:10	RW	00’h	Line Output Volume Source Select 00: VMID (No input) 01: HP Mixer 10: Speaker mixer (diff out) 11: Reserved
sel_hp_l_in	9	RW	0’h	HPL Volume Output Source Select 0: VMID (No input) 1: HP Left Mixer
sel_hp_r_in	8	RW	0’h	HPR Volume Output Source Select 0: VMID (No input) 1: HP Right Mixer
Reserved	7:2	R	0’b	Reserved
en_dac_hp	1	RW	0’b	DAC Direct Output to HP Amplifier Control 0: Normal 1: Enable direct output
Reserved	0	R	0’b	Reserved

8.9. Reg-34h: Stereo Audio Serial Data Port Control

Default: 8000'h

Table 18. MX34 Stereo Audio Serial Data Port Control

Name	Bits	RW	Default	Description
sel_i2s_mode	15	RW	1'h	Main Serial Data Port Mode Selection 0: Master 1: Slave
Reserved	14:8	R	0'h	Reserved
ctrl_i2s_bclk_polarity	7	RW	0'h	Stereo I^{2}S BCLK Polarity Control 0: Normal 1: Invert
Reserved	6:5	R	0'h	Reserved
en_dac_lrck_swap	4	RW	0'h	DAC Data L/R Swap 0: DAC data appear at left phase of LRCK 1: DAC data appear at right phase of LRCK *Note: Supports I^{2}S and PCM.*
sel_i2s_data_len	3:2	RW	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
sel_i2s_data_format	1:0	RW	0'h	Stereo PCM Data Format Selection 00: I^{2}S format 01: Left justified 10: PCM Mode A (LRCK One Plus at Master Mode) 11: PCM Mode B (LRCK One Plus at Master Mode)

8.10. Reg-38h: Stereo DAC Clock Control

Default: 2000'h

Table 19. MX38 Stereo DAC Clock Control

Name	Bits	RW	Default	Description
sel_i2s_pre_div	15:13	RW	1'h	I^{2}S Pre-Divider 000b: ÷1 001b: ÷2 010b: ÷4 011b: ÷8 100b: ÷16 101b: ÷32 Others: Reserved
sel_i2s_bclk_ms	12	RW	0'b	Master Mode Clock Relative to BCLK and LRCK 0b: 32bits (64FS) 1b: 16bits (32FS)
Reserved	11:3	R	0'h	Reserved
sel_dac_filter_clk	2	RW	0'b	Stereo DAC Filter Clock Select 0b: 256Fs 1b: 384Fs
Reserved	1:0	R	0'h	Reserved

8.11. Reg-3Ah: Power Management Addition 1

Default: 0000'h

Table 20. MX3A Power Management Addition 1

Name	Bits	RW	Default	Description
en_main_i2s	15	RW	0'h	I^2S Digital Interface Enable 0: Disable 1: Enable
pow_zcd	14	RW	0'h	All Zero Cross Detect Power Down (Includes Digital) 0: Disable 1: Enable
Reserved	13:9	R	0'h	Reserved
pow_softgen	8	RW	0'b	Power on Softgen 1: Power on 0: Power down *Note: When pow_softgen =1, whether HP and AUXAmp can be driven depends on the level on Cdepop (depends on depop mode selection)*
Reserved	7:6	R	0'h	Reserved
en_hp_out_amp	5	RW	0'h	1: Enable HP Output buffer for normal loading (used to drive High Impedance) 0: Disable (DEPOP mode) See Table 21 for details.
en_hp_enhance_amp	4	RW	0'h	1: Enable HP Enhance Output buffer 0: Disable (DEPOP mode or normal loading mode) See Table 21 for details.
Reserved	3:0	R	0'h	Reserved

The following table describes Bit 4 & Bit 5:

Table 21. Headphone Drive Ability Selection

en_hp_out_amp	en_hp_enhance_amp	Description
0'b	0'b	HP Output Off
0'b	1'b	Not Used
1'b	0'b	HP Output for High-Impedance Loading (>Kohm)
1'b	1'b	HP Output for Low-Impedance Loading (<Kohm)

8.12. Reg-3Ch: Power Management Addition 2

Default: 0000'h

Table 22. MX3C Power Management Addition 2

Name	Bits	RW	Default	Description
pow_lo	15	RW	0'b	0: Disable 1: Enable line output
Reserved	14	RW	0'h	Reserved
pow_vref	13	RW	0'h	0: Disable 1: Enable VREF for all analog circuits (passes control to Vref pin)
pow_pll	12	RW	0'h	0: Disable 1: Enable PLL
pow_thermal	11	RW	0'h	0: Disable 1: Enable thermal shutdown (temp sensor)
pow_dac_ref	10	RW	0'h	0: Disable 1: Enable DAC reference circuit (Vref+/Vref-)
pow_dac_l	9	RW	0'h	0: Disable 1: Enable left STEREO DAC and its filter clock
pow_dac_r	8	RW	0'h	0: Disable 1: Enable right STEREO DAC and its filter clock
pow_dacl2mixer_direct	7	RW	0'h	0: Disable 1: Enable left DAC to mixer and direct path power
pow_dacr2mixer_direct	6	RW	0'h	0: Disable 1: Enable Right DAC to mixer and direct path power
pow_mix_hp_l	5	RW	0'h	0: Disable 1: Enable left headphone mixer
pow_mix_hp_r	4	RW	0'h	0: Disable 1: Enable right headphone mixer
pow_mix_spk	3	RW	0'h	0: Disable 1: Enable Speaker mixer
Reserved	2:0	R	0'h	Reserved

8.13. Reg-3Eh: Power Management Addition 3

Default: 0000'h

Table 23. MX3E Power Management Addition 3

Name	Bits	RW	Default	Description
pow_main_bias	15	RW	0'h	0: Disable 1: Enable Main bias of analog circuit
Reserved	14:13	R	0'h	Reserved
pow_liol_vol	12	RW	0'h	0: Disable 1: Enable LINE_OUT left channel volume output
pow_lior_vol	11	RW	0'b	0: Disable 1: Enable LINE_OUT right channel volume output
pow_hp_l_vol	10	RW	0'h	0: Disable 1: Enable HP_OUT_L Volume control & HP_L Amplifier
pow_hp_r_vol	9	RW	0'h	0: Disable 1: Enable HP_OUT_R Volume control & HP_R Amplifier
Reserved	8	RW	0'b	Reserved (Must be set to 0'b)
pow_li_l_vol	7	RW	0'h	0: Disable 1: Enable LINE_IN Left Volume control
pow_li_r_vol	6	RW	0'h	0: Disable 1: Enable LINE_IN Right Volume control
pow_auxin_l_vol	5	RW	0'h	0: Disable 1: Enable AUXIN Left Volume control
pow_auxin_r_vol	4	RW	0'h	0: Disable 1: Enable AUXIN Right Volume control
pow_li3_l_vol	3	RW	0'b	0: Disable 1: Enable LINE_IN3 Left Volume control
pow_li3_r_vol	2	RW	0'b	0: Disable 1: Enable LINE_IN3 Right Volume control
Reserved	3:0	R	0'h	Reserved

8.14. Reg-40h: General Purpose Control

Default: 1B00'h

Table 24. MX40 General Purpose Control

Name	Bits	RW	Default	Description
Reserved	15:9	R	0D'h	Reserved
en_dac_hpf	8	RW	1'h	STEREO DAC High-Pass Filter 0: Disable 1: Enable
Reserved	7:0	R	0'h	Reserved

8.15. Reg-42h: Global Clock Control

Default: 0000'h

Table 25. MX42 Global Clock Control

Name	Bits	RW	Default	Description
sel_sysclk	15	RW	0'h	Clock Source MUX Control 0: MCLK 1: PLL
sel_pll_sour	14	RW	0'h	PLL Source Select 0: From MCLK 1: From BIT_CLK
se_btlb_lo	13	RW	0'b	Single End & BTL of Line Output Selection 0: Differential Mode 1: Single-End Mode
Reserved	12:3	R	0'h	Reserved
sel_pllout_div_ratio	2:1	RW	0'b	PLL Output Division Ratio PLL Output to GPIO Divider 00: ÷1 01: ÷2 10: ÷4 11: ÷8
sel_pll_pre_div	0	RW	0'b	PLL Pre-Divider 0b: ÷1 1b: ÷2

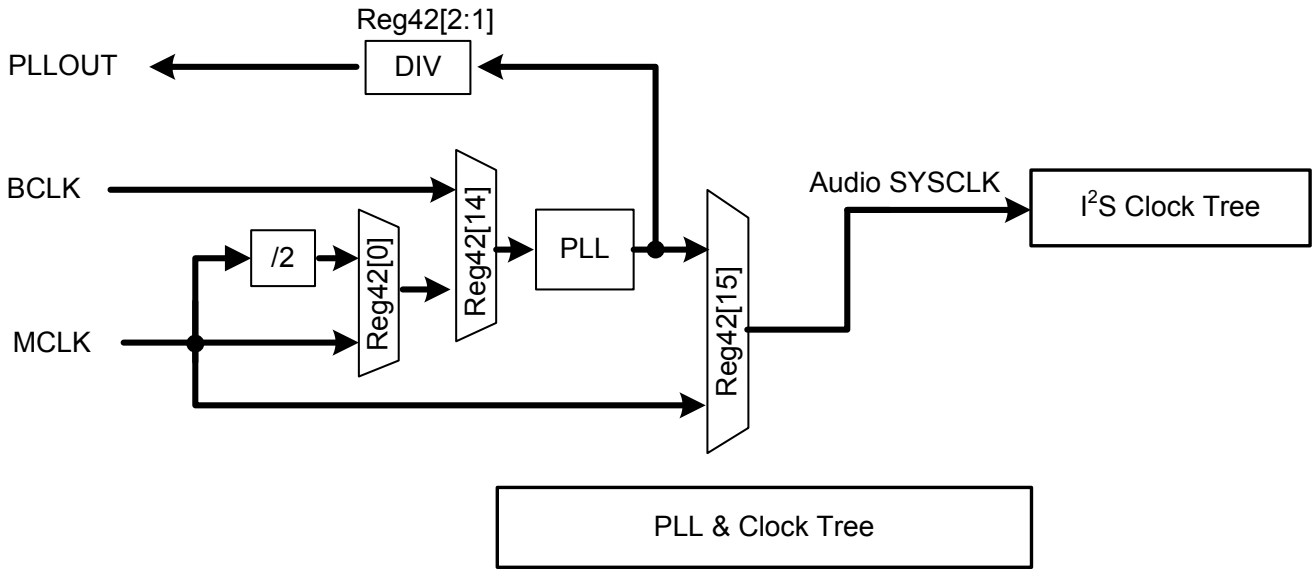


Figure 17. Global Clock Control

8.16. Reg-44h: PLL M/N Code Control

Default: 0000'h

Table 26. MX44 PLL M/N Code Control

Name	Bits	RW	Default	Description
sel_pll_n_code	15:8	RW	00'h	N[7:0] Code for Analog PLL 00000000: Div 2 00000001: Div 3 …… 11111111: Div 257
sel_pll_m_bypass	7	RW	0'h	Bypass PLL M 0b: No bypass 1b: Bypass
sel_pll_k_code	6:4	RW	0'h	K[2:0] Code for Analog PLL 000: Div 2 001: Div 3 …….. 111: Div 9
sel_pll_m_code	3:0	RW	0'h	M[3:0] Code for Analog PLL 0000: Div 2 0001: Div 3 …… 1111: Div 17

8.17. Reg-48h: Internal Status and IRQ Control

Default: 0000'h

Table 27. MX48 Internal Status and IRQ Control

Name	Bits	RW	Default	Description
en_irq_over_curr	15	RW	0'h	IRQ Output Source Configuration of Over-Current Status 0: Bypass 1: Normal
en_irq_over_temp	14	RW	0'h	IRQ Output Source Configuration of Over-Temperature Status 0: Bypass 1: Normal
en_irq_jd_conf	13	RW	0'h	IRQ Output Source Configuration of Jack Detection Status 0: Bypass 1: Normal
Reserved	12:6	R	0'h	Reserved
sel_polarity_over_temp	5	RW	0'h	Over-Temperature Sensor Status Polarity 0: Normal 1: Output Invert
status_over_temp	4	R	0'h	Over-Temperature Sensor Status Read: Return status of each status pin
Reserved	3:0	R	0'h	Reserved

8.18. Reg-4Ah: GPIO Control

Default: 0000’h

Table 28. MX4A GPIO Control

Name	Bits	RW	Default	Description
sel_gpio_o_conf	15:14	RW	0’h	GPIO Output Pin Select 00b: Logic Output (GPIO_out_logic) 01b: IRQ 10b: Reserved 11b: PLLOUT
Reserved	13:4	R	0’h	Reserved
sel_gpio_io	3	RW	0’h	GPIO Pin Configuration 0: Output 1: Input
sel_gpio_o_logic	2	RW	0’h	GPIO Output Pin Control 0: Drive Low 1: Drive High
sel_polarity_gpio	1	RW	0’h	GPIO Pin Polarity 0: Normal 1: Output Invert
status_gpio_in	0	R	0’h	GPIO Pin Status Read: Return status of each GPIO pin

8.19. Reg-5Ah: Jack Detect Control

Default: 0004’h

Table 29. MX5A Jack Detect Control

Name	Bits	RW	Default	Description
SEL_JD_SOURCE	15:14	RW	0’h	Jack Detect Select 00: OFF 01: GPIO 10: JD1 and enable Line in Left Ch. pin share 11: JD2 and enable Line in Right Ch. pin share
en_jd_vref	13	RW	0’b	Enable Jack Detect Trigger Vref 0: Disable 1: Enable
polarity_jd_tri_vref	12	RW	0’b	Selected Jack Detect Polarity Trigger Vref 0: Low trigger 1: High trigger
en_jd_hpout	11	RW	0’h	Enable Jack Detect Trigger HPOUT 0: Disable 1: Enable
polarity_jd_tri_hpout	10	RW	0’h	Select Jack Detect Polarity Trigger HPOUT 0: Low trigger 1: High trigger

Reg5A [15:14]	lineinl_pin _sharing	lineinr_pin _sharing	Enable ZCD (Power & Enable) for Mute
00'b	0'b	0'b	FALSE
01'b	0'b	0'b	TRUE
10'b	1'b	0'b	TRUE
11'b	0'b	1'b	TRUE

Name	Bits	RW	Default	Description
en_jd_lineoutl	9	RW	0'h	Enable Jack Detect Trigger LINE_OUT_L/LN 0: Disable 1: Enable
polarity_jd_tri_lineout	8	RW	0'h	Select Jack Detect Polarity Trigger LINE_OUT_L/LN 0: Low trigger 1: High trigger
en_jd_lineoutr	7	RW	0'b	Enable Jack Detect Trigger LINE_OUT_R/RN 0: Disable 1: Enable
polarity_jd_tri_lineoutr	6	RW	0'b	Select Jack Detect Polarity Trigger LINE_OUT_R/RN 0: Low trigger 1: High trigger
Reserved	5:3	R	0'b	Reserved
status_jd_internal	2	R	0'h	Jack Detect Status Read: Return status of Jack Detect Select output
Reserved	1:0	R	0'b	Reserved

8.20. Reg-5Ch: MISC1 Control

Default: 0000'h

Table 30. MX5C MISC1 Control

Name	Bits	RW	Default	Description
en_lio_l_dezero	15	RW	0'h	Line Output Left Volume Zero Cross Detector Control (Line Output Left Volume Zero Cross Detector when Reg1C[15:14]=01'b) 0: Disable 1: Enable
en_lio_l_softvol	14	RW	0'h	Line Output Left Soft Volume Change Enable (Line Output Left Soft Volume Change Enable when Reg1C[15:14]=01'b) 0: Disable 1: Enable
en_lio_r_dezero	13	RW	0'h	Line Output Right Zero Cross Detector 0: Disable 1: Enable
en_lio_r_softvol	12	RW	0'h	Line Output Right Soft Volume Change Enable 0: Disable 1: Enable
en_hp_l_dezero	11	RW	0'h	HP Out Left Zero Cross Detector Control 0: Disable 1: Enable
en_hp_l_softvol	10	RW	0'h	HP Out Left Soft Volume Change Control 0: Disable 1: Enable
en_hp_r_dezero	9	RW	0'h	HP Out Right Zero Cross Detector Control 0: Disable 1: Enable
en_hp_r_softvol	8	RW	0'h	HP Out Right Soft Volume Control 0: Disable 1: Enable
Reserved	7:4	R	0'h	Reserved
en_dac_zc	3	RW	0'b	Enable DAC Digital Volume Zero Crossing Detect 0: Disable 1: Enable
en_dac_soft_vol	2	RW	0'b	Enable DAC Digital Soft Volume 0: Disable 1: Enable
Reserved	1:0	R	0'h	Reserved

Note: When zero cross detector is enabled, change mute volume only on zero crossing or after timeout.

8.21. Reg-5Eh: MISC2 Control

Default: 0000’h

Table 31. MX5E MISC2 Control

Name	Bits	RW	Default	Description
en_vref_fastb	15	RW	0’b	Enable Fast Vref (This Bit must be Disabled in Normal Use) 0: Enable fast Vref 1: Disable fast Vref
en_thermal_shutdown	14	RW	0’b	Thermal Shut Down Enable 0: Disable 1: Enable
Reserved	13:10	R	0’h	Reserved
en_dp2_hp	9	RW	0’b	Enable De-Pop Mode 2 of HP_Out 0: Disable 1: Enable
en_dp1_hp	8	RW	0’h	Enable De-Pop Mode 1 of HP_Out 0: Disable 1: Enable
en_smt_hp_l	7	RW	0’b	Enable HP_L Mute-Unmute Depop 0: Disable 1: Enable
en_smt_hp_r	6	RW	0’b	Enable HP_R Mute-Unmute Depop 0: Disable 1: Enable
smt_trig	5	RW	0’b	Enable Mute-Unmute Depop 0: Disable 1: Enable
Reserved	4	R	0’b	Reserved
mute_dac_l	3	RW	0’h	Mute Main DAC Left Input 0: On 1: Mute (-∞ dB)
mute_dac_r	2	RW	0’h	Mute Main DAC Right Input 0: On 1: Mute (-∞ dB)
Reserved	1:0	R	0’h	Reserved

8.22. Reg-66h: EQ Control

Default: 0000'h

Table 32. MX66 EQ Control

Name	Bits	RW	Default	Description
eq_all_en	15	RW	0'b	EQ Block Control 0b: Disable 1b: Enable
eq_hpf_mode	14	RW	0'b	EQ High-Pass Shelving Filter Mode Control 0b: High-pass shelving filter 1b: -20dB/decade (HPF)
Reserved	13	R	0'h	Reserved
eq_hpf_status	12	R	0'b	EQ High-Pass Filter (HPF) Status 0: Normal 1: Overflow This bit is set if an overflow has occurred. Write 1 to clear it.
eq_bpf3_status	11	R	0'b	EQ Band-3 (BP3) Status 0: Normal 1: Overflow This bit is set if an overflow has occurred. Write 1 to clear it.
eq_bpf2_status	10	R	0'b	EQ Band-2 (BP2) Status 0: Normal 1: Overflow This bit is set if an overflow has occurred. Write 1 to clear it.
eq_bpf1_status	9	R	0'b	EQ Band-1 (BP1) Status 0: Normal 1: Overflow This bit is set if an overflow has occurred. Write 1 to clear it.
eq_lpf_status	8	R	0'b	EQ Low-Pass Filter (LPF) Status 0: Normal 1: Overflow This bit is set if an overflow has occurred. Write 1 to clear it.
eq_para_update	7	RW	0'b	EQ Parameter Update Control 0b: No action 1b: Update parameter
Reserved	6:5	R	0'h	Reserved
eq_hpf_en	4	RW	0'b	EQ High-Pass Filter (HPF) Control 0: Disable (bypass) and reset 1: Enable
eq_bpf3_en	3	RW	0'b	EQ Band-3 (BP3) Control 0: Disable and reset 1: Enable
eq_bpf2_en	2	RW	0'b	EQ Band-2 (BP2) Control 0: Disable and reset 1: Enable
eq_bpf1_en	1	RW	0'b	EQ Band-1 (BP1) Control 0: Disable and reset 1: Enable
eq_lpf_en	0	RW	0'b	EQ Low-Pass Filter (LPF) Control 0: Disable and reset 1: Enable

8.23. Reg-68h: AVC Control

Default: 1009’h

Table 33. MX68 AVC Control

Name	Bits	RW	Default	Description
EN_AVC	15	RW	0’b	AVC Enable (Default: 00b) 0: Disable AVC 1: Enable AVC to control Digital gain
sel_avc_ref_ch	14	RW	0’b	AVC Reference Channel Selection 0: Left Channel 1: Right Channel
sel_nonact_action	13	RW	0’b	Gain Action of Non-active Region 0: Keep previous Gain 1: Unit Gain
Reserved	12:5	R	80’h	Reserved
sel_monitor_window	4:0	RW	09’h	Monitor Window Control (Unit: 2^(n+1) Samples) (Default: 01011b) 00000b: 2^(1) samples 00001b: 2^(2) samples 00010b: 2^(3) samples …… 10000b: 2^(17) samples Others: Reserved (Maximum=1000000000000000=2^17)

8.24. Reg-6Ah: Private Register Index

Default: 0000’h

Table 34. MX6A Private Register Index

Name	Bits	RW	Default	Description
Reserved	15:7	R	0’h	Reserved
private_reg_index	6:0	RW	0’h	Private Register Index

8.25. Reg-6Ch: Private Register Data

Default: 0000’h

Table 35. MX6C Private Register Data

Name	Bits	RW	Default	Description
private_reg_data	15:0	RW	0’h	Private Register Data Port

8.26. Private-00h: EQ Band-0 Coefficient (LP0: a1)

Default: 0000h

Table 36. PR00h: EQ Band-0 Coefficient (LP0: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 formats (The range is from -4~3.99; the a1 should be in -2~1.99)

Note: For low-pass filter for Bass control – LP0 has filter coefficient a1 and gain Ho must be set (see Table 37).

8.27. Private-01h: EQ Band-0 Gain (LP0: Ho)

Default: 0000h

Table 37. PR01h: EQ Band-0 Gain (LP0: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the Ho should be in -4~3.99)

8.28. Private-02h: EQ Band-1 Coefficient (BP1: a1)

Default: 0000h

Table 38. PR02h: EQ Band-1 Coefficient (BP1: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a1 should be in -2~1.99)

8.29. Private-03h: EQ Band-1 Coefficient (BP1: a2)

Default: 0000h

Table 39. PR03h: EQ Band-1 Coefficient (BP1: a2)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a1 should be in -2~1.99)

8.30. Private-04h: EQ Band-1 Gain (BP1: Ho)

Default: 0000h

Table 40. PR04h: EQ Band-1 Gain (BP1: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the Ho should be in -4~3.99)

8.31. Private-05h: EQ Band-2 Coefficient (BP2: a1)

Default: 0000h

Table 41. PR05h: EQ Band-2 Coefficient (BP2: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a1 should be in -2~1.99)

8.32. Private-06h: EQ Band-2 Coefficient (BP2: a2)

Default: 0000h

Table 42. PR06h: EQ Band-2 Coefficient (BP2: a2)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a2 should be in -2~1.99)

8.33. Private-07h: EQ Band-2 Gain (BP2: Ho)

Default: 0000h

Table 43. PR07h: EQ Band-2 Gain (BP2: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the Ho should be in -4~3.99)

8.34. Private-08h: EQ Band-3 Coefficient (BP3: a1)

Default: 0000h

Table 44. PR08h: EQ Band-3 Coefficient (BP3: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a1 should be in -2~1.99)

8.35. Private-09h: EQ Band-3 Coefficient (BP3: a2)

Default: 0000h

Table 45. PR09h: EQ Band-3 Coefficient (BP3: a2)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a2 should be in -2~1.99)

8.36. Private-0Ah: EQ Band-3 Gain (BP3: Ho)

Default: 0000h

Table 46. PR0Ah: EQ Band-3 Gain (BP3: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the Ho should be in -4~3.99)

8.37. Private-0Bh: EQ Band-4 Coefficient (HPF: a1)

Default: 0000h

Table 47. PR0Bh: EQ Band-4 Coefficient (HPF: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the a1 should be in -2~1.99)

8.38. Private-0Ch: EQ Band-4 Gain (HPF: Ho)

Default: 0000h

Table 48. PR0Ch: EQ Band-4 Gain (HPF: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from -4~3.99; the Ho should be in -2~1.99)

8.39. Private-11h: EQ Input Volume Control

Default: 0000h

Table 49. PR11h: EQ Input Volume Control

Bit	Type	Function
15:2	-	Reserved
1:0	RW	7-Bit Volume Unsigned Ratio EQIn-VOL-LR 00b: 0dB 01b: -6dB 10b: -12dB 11b: -18dB

8.40. Private-12h: EQ Output Volume Control

Default: 0001h

Table 50. PR12h: EQ Output Volume Control

Bit	Type	Function
15:3	-	Reserved
2:0	RW	7-Bit Volume Unsigned Ratio EQOut-VOL-LR 000b: -3dB 001b: 0dB 010b: 3dB 011b: 6dB 100b: 9dB 101b: 12dB 110b: 15dB 111b: 18dB

8.41. Private-21h: Auto Volume Control Register 1

Default: 2000’h

Table 51. PR21 Auto Volume Control Register 1

Name	Bits	RW	Default	Description
Reserved	15	R	0’h	Reserved
sel_avc_thmax	14:0	RW	2000’h	The Maximum PCM Absolute Level After AVC, Thmax (=0~2^15-1)

8.42. Private-22h: Auto Volume Control Register 2

Default: 0800’h

Table 52. PR22 Auto Volume Control Register 2

Name	Bits	RW	Default	Description
Reserved	15	R	0’h	Reserved
sel_avc_thmin	14:0	RW	0800’h	The Minimum PCM Absolute Level After AVC, Thmin (=0~2^15-1)

8.43. Private-23h: Auto Volume Control Register 3

Default: 0060’h

Table 53. PR23 Auto Volume Control Register 3

Name	Bits	RW	Default	Description
Reserved	15	R	0’h	Reserved
sel_avc_thnonact	14:0	RW	0060’h	Non-Active PCM Absolute Level AVC. Will Keep Analog Unit Gain, Thnonact (= 0~2^15-1)

8.44. Private-24h: Auto Volume Control Register 4

Default: 00FF’h

Table 54. PR24 Auto Volume Control Register 4

Name	Bits	RW	Default	Description
sel_avc_cntminth	15:0	RW	00FF’h	CNTMAXTH1. Controls the Sensitivity to Increased Gain (Unit: 2^1). This value should be less than CNTMAXTH2 (Max=1111111111111110=2^17-2)

8.45. Private-25h: Auto Volume Control Register 5

Default: 0100’h

Table 55. PR25 Auto Volume Control Register 5

Name	Bits	RW	Default	Description
sel_avc_cntmaxth	15:0	RW	0100’h	CNTMAXTH2. Controls the Sensitivity to Increased Gain (Unit: 2^1). This value should be less than Monitor Window (Optimal is 1/2 Monitor Window) (Max=1111111111111110=2^17-2)

8.46. Private-39h: Digital Internal Register

Default: 8800’h

Table 56. PR39 Digital Internal Register

Name	Bits	RW	Default	Description
sel_pad_drive	15	RW	1’h	Pad Drive Capability 0b: 5mA 1b: 11mA
Reserved	8:0	R	0800’h	Reserved

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 57. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DCVDD	-0.3	-	3.63	V
Digital Power for IO and PLL	DBVDD	-0.3	-	3.63	V
Analog and HP Amplifier Power	AVDD1/2/3	-0.3	-	3.63	V
Ambient Operating Temperature	Ta	-20	-	+85	°C
Storage Temperature	Ts	-40	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 58. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Digital IO Buffer	DBVDD	1.8	3.3	3.6	V
Digital Core	DCVDD	1.8	3.3	3.6	V
Analog	AVDD1/2/3	2.3	3.3	3.6	V

Note: 1μF Capacitor must be connected from AVDD to AGND, DBVDD to DGND, and DCVDD to DGND. It should be placed as close as possible to the ALC5634.

9.1.3. Static Characteristics

DBVDD= 3.3V, $T_{ambient}$=25°C, with 25pF external load.

Table 59. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DBVDD +0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.33*DBVDD	V
High Level Input Voltage	V_{IH}	0.66*DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9*DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1*DBVDD	V
Low Level Input Voltage (JD2)	V_{IL}	-	-	0.33*AVDD3	V
High Level Input Voltage(JD2)	V_{IH}	0.66*AVDD3	-	-	V

9.2. Analog Performance Characteristics

Standard Test Conditions

- $T_{ambient}$=25°C, DBVDD=DCVDD=AVDD=3.3V, 1kHz Input Sine Wave; Sampling Frequency=48kHz; 0dB=1Vrms, 10KΩ/50pF load; Test Bench Characterization BW: 10Hz~22kHz, 0dB Attenuation.

Table 60. Analog Performance Characteristics

Parameter	Minimum	Typical	Maximum	Units
Full Scale Input Voltage				
LINE_IN/AUXIN/LINE3 Inputs (Gain=0dB)	-	1.0	-	Vrms
Full Scale Output Voltage				
DAC Outputs	-	1.0	-	Vrms
Headphone Outputs	-	1.0	-	Vrms
Line Outputs	-	1.0	-	Vrms
S/N (A Weighted)				
DAC	-	100	-	dB FSA
Headphone Amplifier Output (RL=32Ω, PO=20mW)	-	100	-	dB FSA
THD+N				
DAC	-	-90	-	dB FS
Headphone Amplifier Output (RL=32Ω, PO=20mW)	-	-85	-	dB FS
Speaker Power Supply Rejection (217Hz)				
SE	-	55	-	dB
BTL	-	70	-	dB
Amplifier Gain Step	-	1.5	-	dB
Crosstalk (DAC to HP_OUT)	-	-95	-	dB
HP Amplifier Quiescent Current (RL=32Ω @ 3.3V)	-	600	-	µA
HP Amplifier Output Power (RL=16Ω)	25	45	-	mW
Quiescent Power Supply Current (DAC to Headphone With 16ohm Load) AVDD=DCVDD=DBVDD=3.3V	-	8	-	mA
Digital Power Supply Current (Power Down Mode) DCVDD=DBVDD=3.3V (Include POR Circuit)	-	3	-	µA
Analog Power Supply Current (Power Down Mode) AVDD=3.3V	-	-	1	µA
VREF Output Voltage	-	0.5	-	AVDD
VREF Rising Time at Fast Mode (C=4.7µF)	-	-	50	ms

9.3. AC Timing Characteristics

9.3.1. I²C Control Interface

Table 61. I²C Control Interface Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Clock Pulse Duration	$t_{w(9)}$	1.3	-	-	µs
Clock Pulse Duration	$t_{w(10)}$	600	-	-	ns
Clock Frequency	f	0	-	400K	Hz
Re-Start Setup Time	$t_{su(6)}$	600	-	-	ns
Start Hold Time	$t_{h(5)}$	600	-	-	ns
Data Setup Time	$t_{su(7)}$	100	-	-	ns
Data Hold Time	$t_{h(6)}$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su(8)}$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

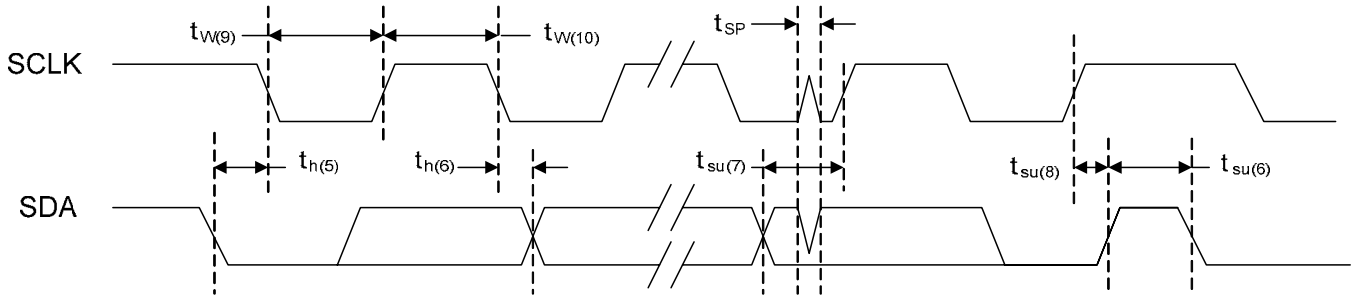


Figure 18. I²C Control Interface Waveform

9.3.2. I²S/PCM Interface Master Mode

Table 62. I²S/PCM Master Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

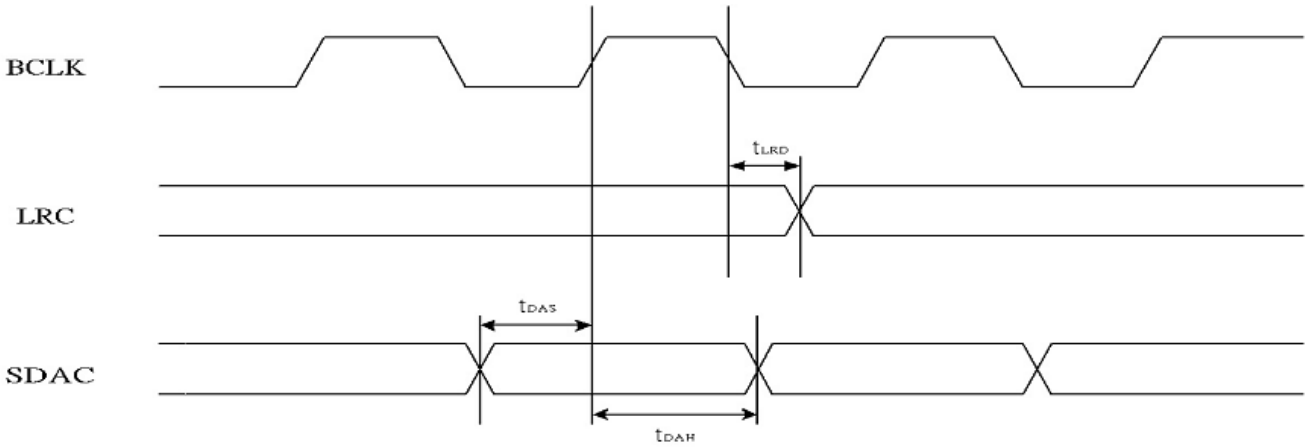


Figure 19. I²S/PCM Master Mode Waveform

9.3.3. I²S/PCM Interface Slave Mode

Table 63. I²S/PCM Slave Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

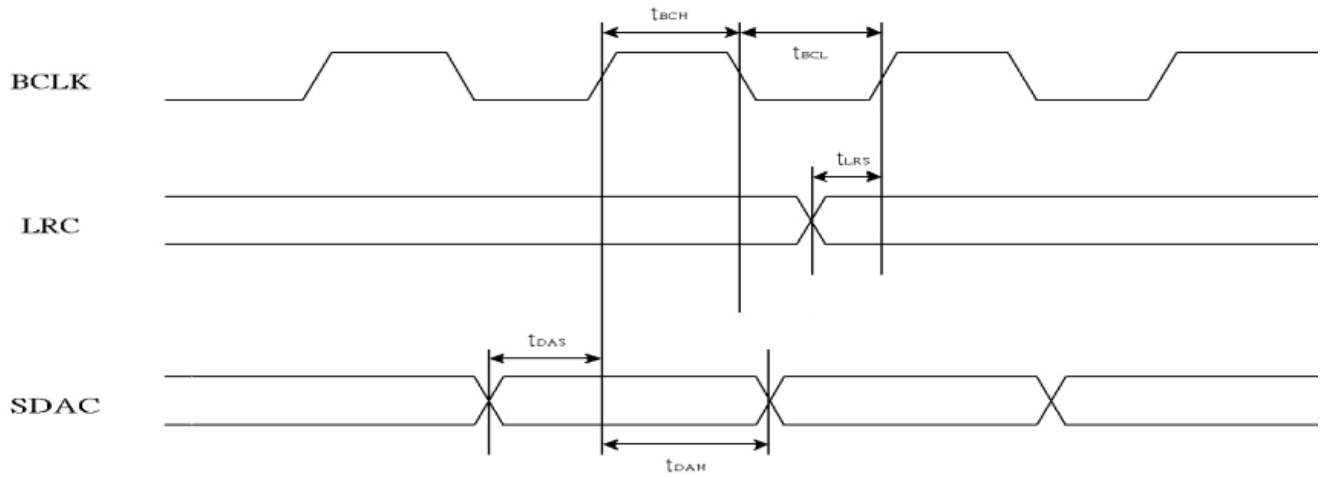
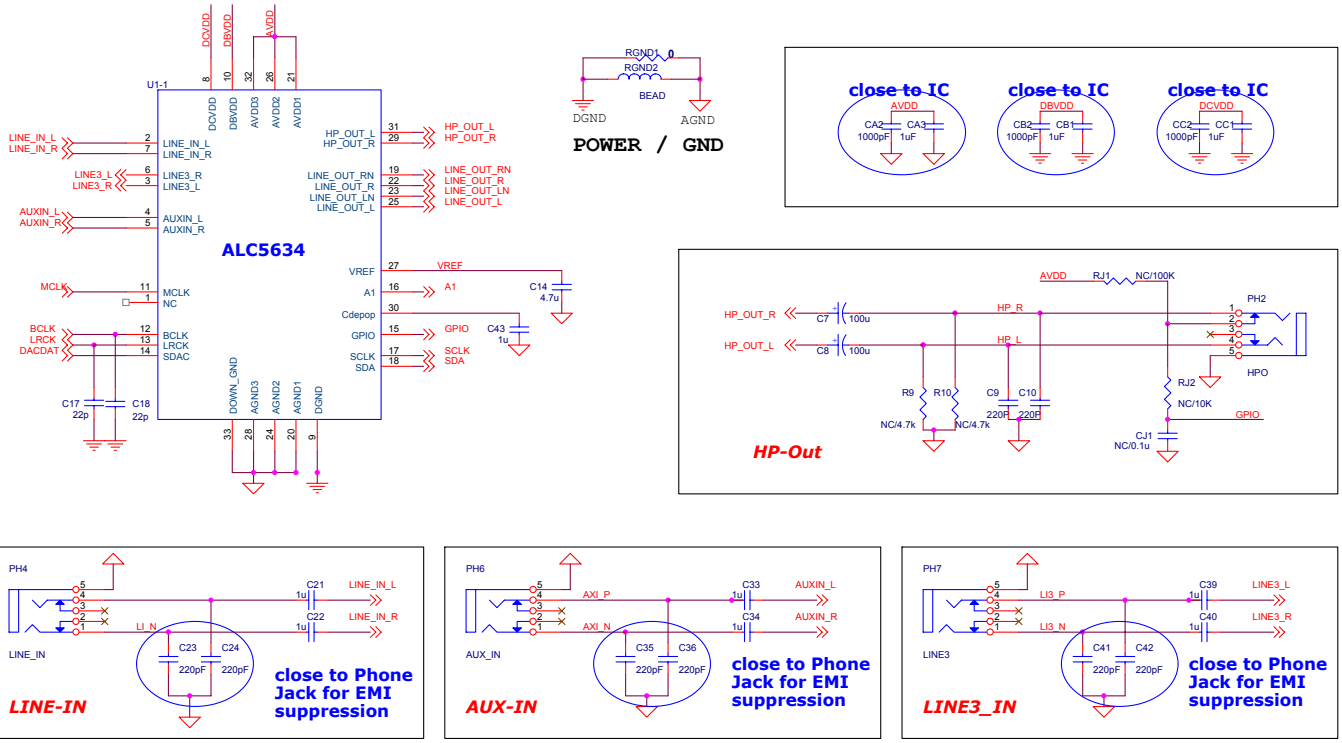


Figure 20. I²S/PCM Slave Mode Waveform

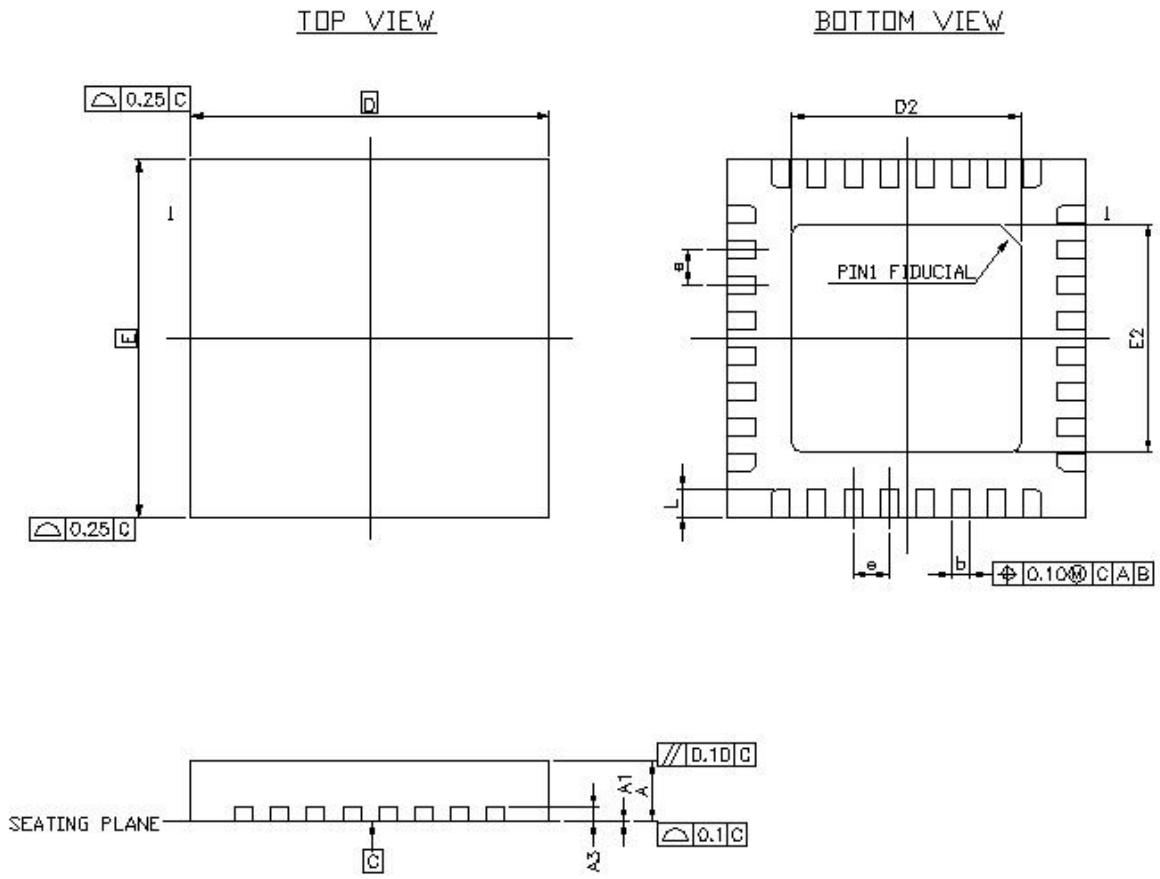
10. Application Circuits

Application circuits are for design reference only. System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, Realtek should confirm modifications of application circuits.



11. Mechanical Dimensions

QFN-32 Package; 5x5mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
c	-	-	0.6	-	-	0.024
D/E	5.00BSC			0.197BSC		
D_2/E_2	3.10	3.35	3.60	0.122	0.132	0.142
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Ordering Information

Table 64. Ordering Information

Part Number	Package	Status
ALC5634-GR	QFN-32 in 'Green' Package (Tray)	MP
ALC5634-GRT	QFN-32 in 'Green' Package (Tape & Reel)	MP

Note: See page 6 for package and version identification.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com