ALC655

SIX CHANNEL AC'97 2.3 AUDIO CODEC

DATASHEET

Rev. 1.10
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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC850 Audio CODEC chip.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.30	2003/03/19	Preliminary version release.
0.40	2003/04/04	1.Update application circuit for automatic jack sensing function. 2.Add a FRONT-MIC2 for stereo microphone input for front panel application. (Ver.D or later)
1.00	2003/07/10	Just change Version from 0.4 to 1.0 for official release.
1.01	2003/11/20	Correct dimension typing error in section 11.
1.10	2005/03/15	Add pb-free package & version identification on page 3 & 38

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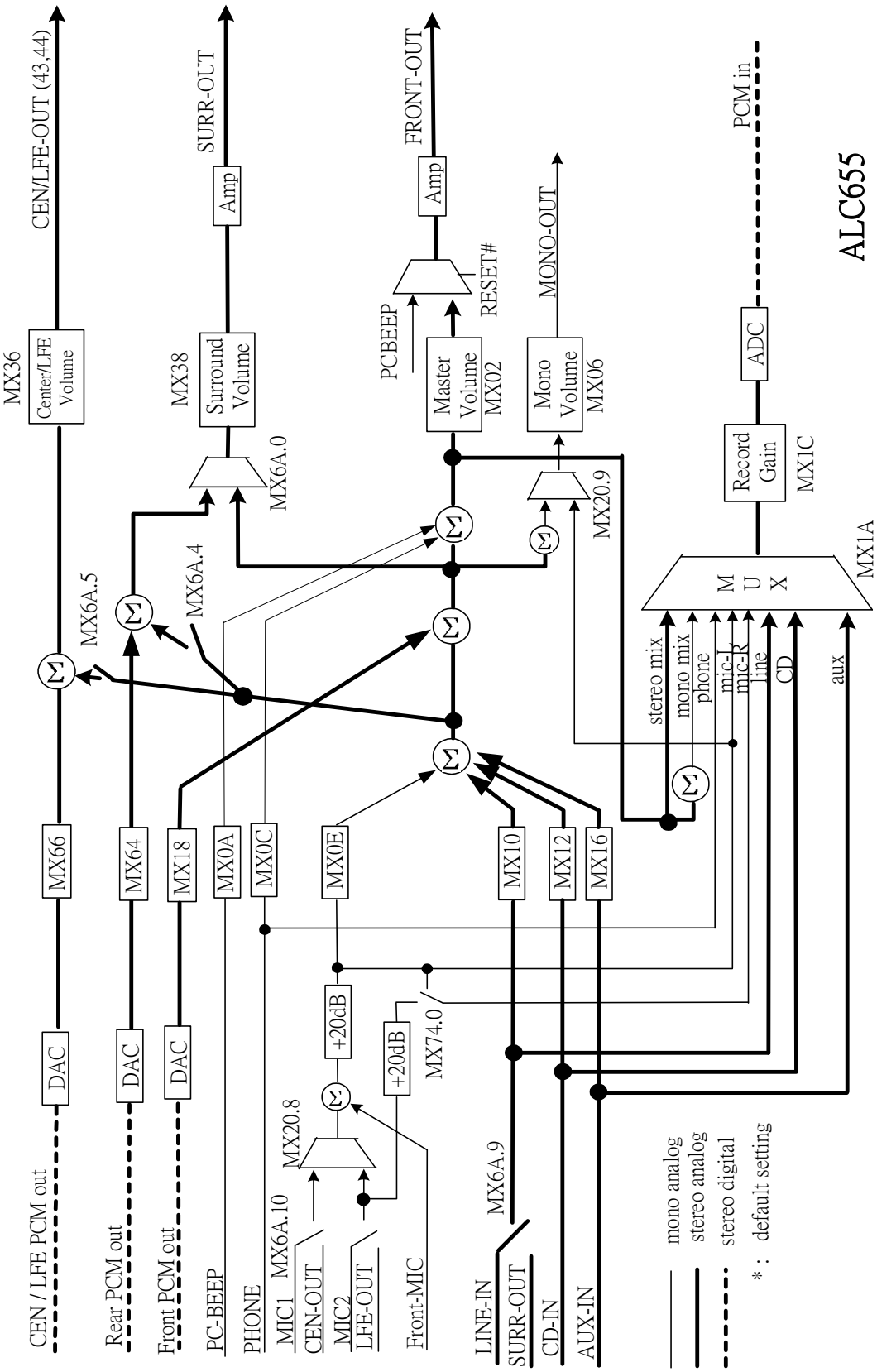
1. Features

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate
- ***Compliant with AC'97 2.3 specifications***
  -Front-Out, Surround-Out, MIC-In and LINE-In Jack Sensing
  -14.318MHz-→24.576MHz PLL to save crystal
  -12.288MHz BITCLK input can be consumed
  -Integrated PCBEEP generator to save buzzer
  -Interrupt capability
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP, PHONE-IN
- Two software selectable MIC inputs
- A dedicated Front-MIC input for front panel applications (software selectable)
- Boost preamplifier for MIC input
- LINE Input shared with surround output; MIC input shared with Center and LFE output
- Both Front-out and Surround-Out built-in 50mW/20Ω amplifier
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features
- **Stereo MIC record for AEC/BF application**
- Supports **Power Off CD** function
- Adjustable VREFOUT control
- Supports double sampling rate (96KHz) of DVD audio playback
- Support 48KHz of S/PDIF output is compliant with AC'97 rev2.3 specification
- Support 32K/44.1K/48KHz of S/PDIF input
- Power support: Digital: 3.3V; Analog: 3.3V/5V
- Standard 48-Pin LQFP Package
- **EAX™ 1.0&2.0 compatible**
- **Direct Sound 3D™ compatible**
- **A3D™ compatible**
- **I3DL2 compatible**
- **HRTF 3D Positional Audio**
- **Sensaura™ 3D Enhancement** (optional)
- **10 Bands of Software EQualizer**
- **Voice Cancellation and Key Shifting in Kara OK mode**
- **AVRack® Media Player**
- **Configuration Panel to improve Experience of User**

2. General Description

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bit volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M→24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/ Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

3. Block Diagram



4. Pin Assignments

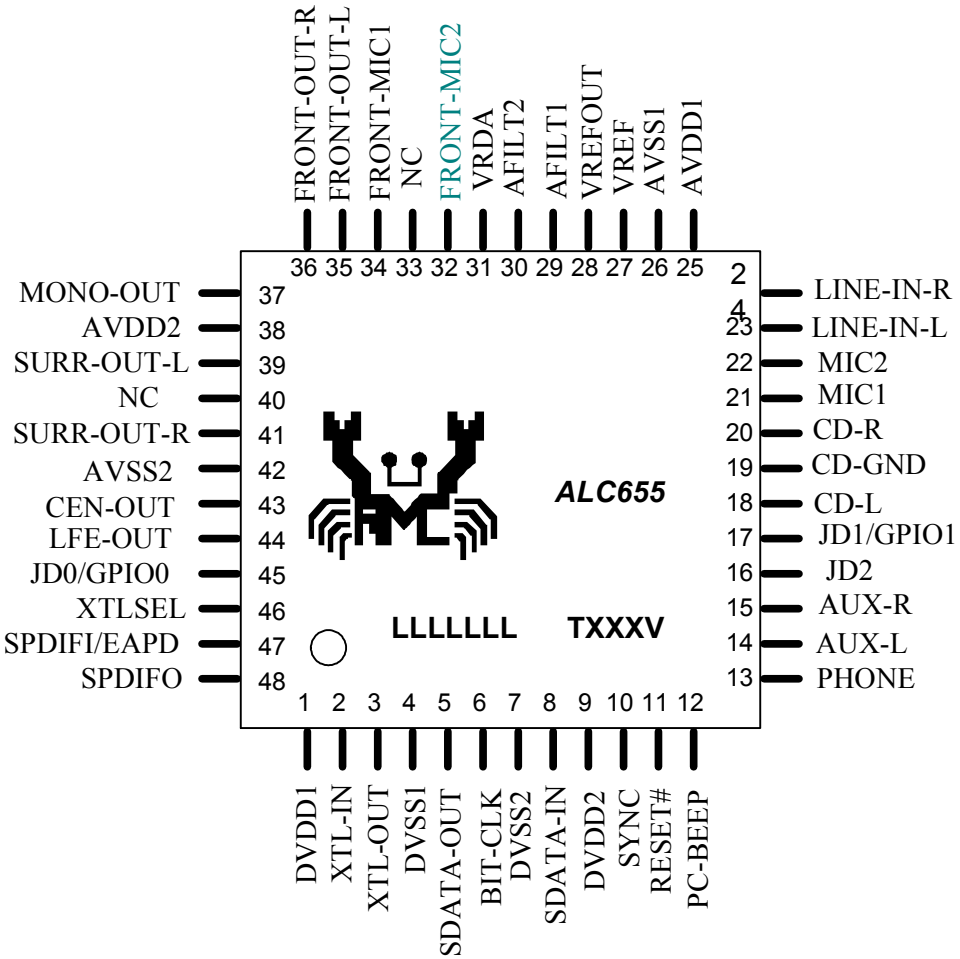


Figure 1. Pin Assignments

4.1 Lead (Pb)-Free Package and Version Identification

Lead (Pb)-free package is indicated by an “L” in the location marked “T” in Figure 1. The version number is shown in the location marked “V”.

5. Pin Description

5.1 Digital I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
XTL-IN	I	2	Crystal input pad (24.576Mhz)	Crystal input pad
XTL-OUT	O	3	Crystal output pad	Crystal output pad
SDATA-OUT	I	5	Serial TDM AC'97 output	CMOS input
BIT-CLK	IO	6	Bit clock output (12.288Mhz)	CMOS input/output, Vt=0.35Vdd, internal pulled low by a 100K resistor.
SDATA-IN	O	8	Serial TDM AC'97 input	CMOS output, internal pulled low by a 100K resistor.
SYNC	I	10	Sample Sync (48Khz)	CMOS input
RESET#	I	11	AC'97 master H/W reset	CMOS input
JD1/GPIO1	I / O	17	Jack Detect 1 / General Purpose I/O 1	Internally pulled high to AVDD by a 100K resistor
JD2	I	16	Jack Detect 2	Internally pulled high to AVDD by a 100K resistor
JD0/GPIO0	I/O	45	Jack Detect 0 / General Purpose I/O 0	Internally pulled high to AVDD by a 100K resistor
XTLSEL	I	46	Crystal Selection	Internally pulled high
SPDIFI / EAPD	I/O	47	S/PDIF input / External Amplifier power down control	Digital input / output
SPDIFO	O	48	S/PDIF output	Digital output
				TOTAL: 13 Pins

XTLSEL=floating, bypass 14.318MHz→24.576MHz digital PLL. The clock source is 24.576MHz crystal or external clock.
XTLSEL=pull low, select 14.318MHz→24.576MHz digital PLL

5.2 Analog I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1Vrms)
PHONE	I	13	Speaker phone input	Analog input (1Vrms)
AUX-L	I	14	AUX Left channel	Analog input (1Vrms)
AUX-R	I	15	AUX Right channel	Analog input (1Vrms)
CD-L	I	18	CD audio Left channel	Analog input (1Vrms)
CD-GND	I	19	CD audio analog GND	Analog input (1Vrms)
CD-R	I	20	CD audio Right channel	Analog input (1Vrms)
MIC1	I / O	21	First Mic in / CEN-OUT	Analog input (1Vrms) / Analog output (1Vrms)
MIC2	I / O	22	Secondary Mic in / CEN-OUT	Analog input (1Vrms) / Analog output (1Vrms)
LINE-L	I / O	23	Line-In Left channel / S-OUT-L	Analog input (1Vrms) / Analog output (1Vrms)
LINE-R	I / O	24	Line-In Right channel/ S-OUT-R	Analog input (1Vrms) / Analog output (1Vrms)
Front-MIC1	I	34	Dedicated MIC Input 1	Analog input (1Vrms) for front panel MIC input
Front-MIC2	I	32	Dedicated MIC Input 1 (Supported by D version or later)	Analog input (1Vrms) for front panel MIC input
LINE-OUT-L	O	35	Line-Out Left channel	Analog output (1Vrms)
LINE-OUT-R	O	36	Line-Out Right channel	Analog output (1Vrms)
MONO-OUT	O	37	Speaker Phone output	Analog output (1Vrms)
S-OUT-L	O	39	Surround Out Left channel	Analog output (1Vrms)
S-OUT-R	O	41	Surround Out Right channel	Analog output (1Vrms)
CEN-OUT	O	43	Center Out channel	Analog output (1Vrms)
LFE-OUT	O	44	Low Frequency Effect Out channel	Analog output (1Vrms)
				TOTAL: 20 Pins

5.3 Filter/Reference

Name	Type	Pin No	Description	Characteristic Definition
VREF	O	27	Reference voltage	Analog output. +4.7uf and 0.1uf cap to AVSS
VREFOUT	O	28	Ref. voltage out with 5mA drive	Analog output (2.5V/4.0V)
AFILT1	O	29	ADC anti-aliasing filter capacitor	1nf cap to AVSS
AFILT2	O	30	ADC anti-aliasing filter capacitor	1nf cap to AVSS
VRDA	O	31	Vref for DAC	1uf cap to AVSS
NC		33,40	Not connected	
				TOTAL: 7 Pins

5.4 Power/Ground

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD (5.0V)	The minimum value is 3.0V The maximum value is 5.5V
AVDD2	I	38	Analog VDD (5.0V)	The minimum value is 3.0V The maximum value is 5.5V
AVSS1	I	26	Analog GND	
AVSS2	I	42	Analog GND	
DVDD1	I	1	Digital VDD (3.3V)	The minimum value is 3.0V (DVdd-0.3) The maximum value is 3.6V (DVdd+0.3)
DVDD2	I	9	Digital VDD (3.3V)	The minimum value is 3.0V (DVdd-0.3) The maximum value is 3.6V (DVdd+0.3)
DVSS1	I	4	Digital GND	
DVSS2	I	7	Digital GND	
				TOTAL: 8 Pins

6. Registers

6.1 Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0.

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	Mute**	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono-Out Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	F7	F6	F5	F4	F3	F2	F1	F0	PB3	PB2	PB1	PB0	X	8000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	X	X	X	X	X	X	MIX	MS	LBK	X	X	X	X	X	X	X	0000h
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	X	X	X	X	X	X	X	PG3	PG2	PG1	PG0	0000h
26h	Power Down Ctrl/Status	EAPD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	0	0	X	X	REV1	REV0	0	LDAC	SDAC	CDAC	X	X	X	SPDIF	X	VRA	09C4h
2Ah	Extended Audio Status	X	X	PRK	PRJ	PRI	SPCV	X	LDAC	SDAC	CDAC	SPSA1	SPSA0	X	SPDIF	X	VRA	0040h
2Ch	PCM front Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
2Eh	PCM Surr. Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
30h	PCM LFE. Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
32h	PCM Input Sample Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
36h	Center/LFE Volume	Mute	X	X	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	X	X	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surround Volume	Mute	X	X	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	X	X	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	S/PDIF Ctl	V	0	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h
64h	Surr. DAC Volume	Mute	X	X	LSD4	LSD3	LSD2	LSD1	LSD0	X	X	X	RSD4	RSD3	RSD2	RSD1	RSD0	0808h
66h	CEN/LFE DAC Volume	Mute	X	X	LD4	LD3	LD2	LD1	LD0	X	X	X	CD4	CD3	CD2	CD1	CD0	0808h
6Ah	Multi-channel Ctl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
7Ah	Extension Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	60A2h
7Ch	Vendor ID1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	414Ch
7Eh	Vendor ID2	0	1	0	0	0	1	1	1	0	1	1	0	0	0	0	0	4760h

X: reserved bit

*: MX36 is the master volume control of CENTER/LFE output.
MX38 is the master volume control of surround output.

6.1.1 MX00 Reset

Default: 0000H

Writing any value to this register will start a register reset, and causes all of the registers to revert to their default values. Reading this register returns the ID code of the specific part.

Bit	Type	Function
15:10	-	**Reserved**
9	R	Read as 0 (Does not support 20-bit ADC)
8	R	Read as 0 (Does not support 18-bit ADC)
7	R	Read as 0 (Does not support 20-bit DAC)
6	R	Read as 0 (Does not support 18-bit DAC)
5	R	Read as 0 (No Loudness support)
4	R	Read as 0 (No True Line Level output support)
3	R	Read as 0 (No simulated stereo for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	Read as 0 (No Modem Line support)
0	R	Read as 0 (No Dedicated Mic PCM input channel)

❶ Writing any data into this register will reset all mixer registers to their default value. The written data is ignored.

6.1.2 MX02 (Front) Master Volume

Default: 8000H

These registers control the volume level of Front-Out. Each step on the left and right channels correspond to 1.5dB in increase/decrease in volume.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**Master Left Volume** (ML[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**Master Right Volume** (MR[4:0]) in 1.5 dB steps

❶ For MR/ML, 00h 0 dB
1Fh 46.5 dB attenuation

6.1.3 MX06 MONO_OUT Volume

Default: 8000H

Register 06H controls the mono volume output. Mono output is the same data sent on all output channels. Each step in bits 0:4 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5	-	**Reserved**
4:0	R/W	**Mono Master Volume** (MM[4:0]) in 1.5 dB steps

❶ For MM, 00h 0 dB attenuation
1Fh 46.5 dB attenuation

6.1.4 MX0A PC BEEP Volume

Default: 0000H

This register controls the input volume for the PC beep signal. Each step in bits 4:1 correspond to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC655, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the Front-Out. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)

14:13		**Reserved**
12:5	R/W	**Internal PCBEEP Frequency, F[7:0]** The internal PCBEEP frequency is the result of dividing the 48KHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48KHz/(255*4)=47Hz. The highest tone is 48KHz/(1*4)=12KHz. A value of 00h in F[7:0] disables internal PCBEEP generator and allows external PCBEEP input.
4:1	R/W	**PC Beep Volume** (PBV[3:0]) in 3 dB steps
0		**Reserved**

❶ For PB, 00h 0 dB attenuation
0Fh 45 dB attenuation

6.1.5 MX0C PHONE Volume

Default: 8008H

Register 0CH controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5	-	**Reserved**
4:0	R/W	**Phone Volume** (PV[4:0]) in 1.5 dB steps

❶ For PV, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.6 MX0E MIC Volume

Default: 8008H

Register 0EH controls the microphone input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Each step in bit 6 corresponds to a magnification of 20dB increase in volume.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:7	-	**Reserved**
6	R/W	**20 dB Boost Control** 0: Normal 1: 20 dB boost
5	-	**Reserved**
4:0	R/W	**Mic Volume** (MV[4:0]) in 1.5 dB steps

❶ For MV, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.7 MX10 LINE_IN Volume

Default: 8808H

Register 10H controls the LINE_IN input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**Line-In Left Volume** (NL[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**Line-In Right Volume** (NR[4:0]) in 1.5 dB steps

❶ For NL/NR, 00h +12 dB Gain
08h 0dB gain

1Fh -34.5dB Gain

6.1.8 MX12 CD Volume

Default: 8808H

Register 12H controls the CD input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

it	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**CD Left Volume** (CL[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**CD Right Volume** (CR[4:0]) in 1.5 dB steps

❶ For CL/CR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.9 MX16 AUX Volume

Default: 8808H

Register 16H controls the auxiliary input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**AUX Left Volume** (AL[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**AUX Right Volume** (AR[4:0]) in 1.5 dB steps

❶ For AL/AR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.10 MX18 PCM_OUT Volume

Default: 8808H

Register 18H controls the PCM_OUT output volume of **front DAC**. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**PCM Left Volume** (PL[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**PCM Right Volume** (PR[4:0]) in 1.5 dB steps

❶ For PL/PR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.11 MX1A Record Select

Default: 0000H

Register 1AH controls the record input volume. Each step in bits 2:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 7 levels of volume, from 000 to 111. Each step in bits 10:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 7 levels of volume, from 000 to 111.

Bit	Type	Function
15:11	-	**Reserved**
10:8	R/W	**Left Record Source Select** (LRS[2:0])
7:3	-	**Reserved**
2:0	R/W	**Right Record Source Select** (RRS[2:0])

❶ For LRS

0	MIC
1	CD LEFT
2	Muted
3	AUX LEFT
4	LINE LEFT
5	STEREO MIXER OUTPUT LEFT
6	MONO MIXER OUTPUT
7	PHONE

❷ For RRS

0	MIC
1	CD RIGHT
2	Muted
3	AUX RIGHT
4	LINE RIGHT
5	STEREO MIXER OUTPUT RIGHT
6	MONO MIXER OUTPUT
7	PHONE

6.1.12 MX1C Record Gain
Default: 8000H

Register 1CH controls the record gain. Each step in bits 3:0 correspond to 1.5dB in increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 correspond to 1.5dB in increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:12	-	**Reserved**
11:8	R/W	**Left Record Gain Select** (LRG[3:0]) in 1.5 dB steps
7:4	-	**Reserved**
3:0	R/W	**Right Record Gain Select** (RRG[3:0]) in 1.5 dB steps

❶ For LRG/RRG,

0Fh	+22.5dB
00h	0 dB (No Gain)

6.1.13 MX20 General Purpose Register
Default: 0000H

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 9 allows selection of mono output. Bit 8 controls the mic selector. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

Bit	Type	Function
15:12	-	**Reserved**, Read as 0
11:10	R	**DRSS[1:0], Double Rate Slot Select** 01: PCM(n+1) data is on Slots 7/8 **(Default)** 00,10,11: Reserved
9	R/W	**Mono Output Select** 0: MIX 1: MIC
8	R/W	**Mic Select** MIC select 0: MIC 1+(Front-MIC) 1: MIC2+ (Front-MIC)
7	R/W	**AD to DA Loop-Back Control** 0: Disable 1: Enable

6:0	-	**Reserved**

❶ Bit 7 enables ADC to front DAC loop-back.

6.1.14 MX24 Audio interrupt and Paging

Default: 0000h

Bit	Type	Function
15		**Interrupt Status, I4** 0: Interrupt is clear. 1: Interrupt was generated Interrupt event and status are clear by writing a 1 to this bit. The status will change regardless of interrupt enable (I0).
14	R	**Interrupt Cause, I3** Reserved, read as 0
13	R	**Interrupt Cause, I2** I2=0: Sense value in page ID-01h MX6A.[12:8] has not changed. 1: Sense cycle completed or new sense value in page ID-01h MX6A.[12:8] is available. This bit reflects the cause of the **first** interrupt event generated. Software should read it after interrupt status (I4) has been confirmed as interrupting. I2 will be zero when I4 is cleared.
12	R/W	**Sense Cycle, I1** 0: Sense cycle not in progress 1: Sense cycle start Writing a '1' to this bit causes a sense cycle start. If a sense cycle is in progress, writing a '0' to this bit will abort the sense cycle. Whether the data in the sense result register (page ID-01h MX6A) is valid or not is determined by the IV bit in MX6A, Page ID-1h.
11	R/W	**Interrupt Enable, I0** 0: Interrupt is masked, interrupt status (I4) will not be shown in bit 0 in Slot 12 in SDATA-IN. 1: Interrupt is un-masked, interrupt status (I4) will be shown in bit 0 in Slot 12 in SDATA-IN. In ALC655, this bit controls the interrupt of sense cycle.
10:4	NA	Reserved, read as 0
3:0	R/W	**Page Selector, PG[3:0]** 0000b: Vendor Specific 0001b: Page ID 01 (AC'97 2.3 Discovery Descriptor Definition) Others: Reserved. This register is used to select a descriptor of 16 word pages between registers MX60 to MX6F. Value of 0 is used to select vendor specific space to maintain compatibility with AC'97 2.2 vendor specific register. Once PG[3:0] is not 0000b and 0001b, ALC655 will return zero data for ACLINK mixer read command.

6.1.15 MX26 Powerdown Control/Status

Default: 0000H

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status; a "1" indicating that the subsection is "ready." Ready is defined as the subsection's ability to perform in its nominal state.

When the AC-Link "CODEC Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this powerdown control /status register to determine exactly which subsections, if any are ready.

Bit	Type	Function
15	R/W	PR7 **External Amplifier Power Down** (EAPD) 0: EAPD output low (enable external amplifier) 1: EAPD output high (shut down external amplifier)
14	-	**Reserved**
13	R/W	PR5 0: Normal 1: Disable internal clock usage (BCLK still be output for modem CODEC)
12	R/W	PR4 0: Normal 1: Power down AC-Link
11	R/W	PR3 0: Normal 1: Power down Mixer (Vref off)
10	R/W	PR2 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	PR1 0: Normal 1: Power down PCM DAC (front DAC)
8	R/W	PR0 0: Normal 1: Power down PCM ADC and input MUX
7:4	-	**Reserved**, Read as 0
3	R	**Vref Status** 1: Vref is up to normal level 0: Not yet
2	R	**Analog Mixer Status** 1: Ready 0: Not yet
1	R	**DAC Status** 1: Ready 0: Not yet
0	R	**ADC Status** 1: Ready 0: Not yet

True table for power down mode:

	CDAC	SDAC *	LDAC	ADC	DAC	Mixer	Vref	ACLINK	Int CLK	EAPD
PR0=1				PD						
PR1=1					PD					
PR2=1						PD				
PR3=1	PD	PD	PD	PD	PD	PD	PD			
PR4=1	PD	PD	PD	PD	PD			PD		
PR5=1	PD	PD	PD	PD	PD				PD	
PR7=1										High
PRI=1	PD									
PRJ=1		PD								
PRK=1			PD							

PD: Power down Blank: Don't care High: output high

* SDAC= Surround DAC, LDAC= LFE DAC, CDAC= Center DAC.
PRI: Center DAC power down control bit defined in MX2A.11
PRJ: Surround DAC power down control bit defined in MX2A.12
PRK: LFE DAC power down control bit defined in MX2A.13

6.1.16 MX28 Extended Audio ID

Default: 09C6H

The Extended Audio ID register is a read only register used to communicate information to the digital controller.

Bit	Type	Function
15:14	R	**ID[1:0]**. Always read as 0
13:12	-	**Reserved**, Read as 0
11:10	R	**REV** [1:0]=10 to indicate that the ALC655 is AC'97 rev2.3 compliant
9	R	**AMAP,** Read as 0.
8	R	**LDAC**, Read as 1 (LFE DAC is supported, according to AC'97 rev2.3)
7	R	**SDAC**, Read as 1 (Surround DAC is supported, according to AC'97 rev2.3)
6	R	**CDAC**, Read as 1 (Center DAC is supported, according to AC'97 rev2.3)
5:3	-	**Reserved**, Read as 0
2	R	**SPDIF**, Read as 1 (S/PDIF output is supported)
1	R	**DRA**, Read as 1 (Double Rate Audio is supported)
0	R	**VRA**, Read as 0 (Variable Rate Audio is not supported)

6.1.17 MX2A Extended Audio Status and Control Register

Default: 05F0H

This register contains two active bits for powerdown and status of the surrounding DACs. Bits 1 & 2 are read/write bits which are used to enable or disable DRA and SPDIF respectively. Bits 4 & 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bits 6, 7 & 8 are read only bits which tell the controller when the Center, Surround and LFE DACs are ready to receive data. Bit 10 is a read only bit which tells the controller if the S/PDIF configuration is valid. Bits 11, 12 & 13 are read/write bits which are used to powerdown the Center, Surround and LFE DACs respectively.

Bit	Type	Function
15	R/W	**VCFG, Validity Configuration of S/PDIF Output** Combined with MX3A.15 to decide validity control in S/PDIF output signal.
14	-	**Reserved.**
13	R/W	**Power Down LFE DAC**. (PRK) 0: Normal 1: Power down LFE DAC
12	R/W	**Power Down Surround DAC**. (PRJ) 0: Normal 1: Power down Surround DAC
11	R/W	**Power Down Center DAC**. (PRI) 0: Normal 1: Power down Center DAC
10	R	**SPCV** (S/PDIF Configuration Valid) 0: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is not valid 1: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is valid
9	-	**Reserved**
8	R	**LFE DAC Status** (LDAC). 0: Not yet 1: Ready
7	R	**Surround DAC Status** (SDAC). 0: Not yet 1: Ready
6	R	**Center DAC Status** (CDAC). 0: Not yet 1: Ready
5:4	R/W	**SPSA**[1:0] (S/PDIF Slot Assignment) 00: S/PDIF source data assigned to AC-LINK slot3/4 01: S/PDIF source data assigned to AC-LINK slot7/8 10: S/PDIF source data assigned to AC-LINK slot6/9 11: S/PDIF source data assigned to AC-LINK slot10/11 (default)
3	-	Reserved
2	R/W	**SPDIF Enable**. 1: Enable 0: Disable (Hi-Z)
1	R/W	**DRA Enable**. 1: Enable 0: Disable ‡
0	-	Reserved.

❶**SPCV** is a read only bit that indicates whether the current S/PDIF-Out configuration is supported or not. If the configuration is supported, SPCV is set as 1 by H/W. So driver can

check this bit to determine the status of the S/PDIF transmitter system. SPCV is always operating, independent of the SPDIF enable bit (MX2A.2). The S/PDIF output is active if MX2A.2 is set in spite of SPCV. Once S/PDIF output is enabled but SPCV is invalid (SPCV=0), channel status is still output, but the output data bits will be all zero. ***The condition to allow S/PDIF output is SPDIF(MX2A.2)=1 & SPACV=1, otherwise the S/PDIF output will be all zero when MX2A.2=1 and SPACV=0 (invalid)***.

❷Only front DACs supports 96KHz sample rate when DRA=1. MX2A.1 just selects clock source for front DACs. ***Software must mute surround DACs and CEN/LFE DACs.***

6.1.18 MX2C PCM Front/Center Output Sample Rate

Default: BB80H

Bit	Type	Function
15:0	R	Read as BB80h. (ALC655 supports 48KHz sample rate.)

6.1.19 MX2E PCM Surround Output Sample Rate

Default: BB80H

Bit	Type	Function
15:0	R	Read as BB80h. (ALC655 supports 48KHz sample rate.)

6.1.20 MX30 PCM LFE Output Sample Rate

Default: BB80H

Bit	Type	Function
15:0	R	Read as BB80h. (ALC655 supports 48KHz sample rate.)

6.1.21 MX32 PCM Input Sample Rate

Default: BB80H

Bit	Type	Function
15:0	R	Read as BB80h. (ALC655 supports 48KHz sample rate.)

6.1.22 MX36 LFE/Center Master Volume

Default: 8080H

Bit	Type	Function
15	R/W	**LFE Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**LFE Master Volume** (LFE[4:0]) in 1.5 dB steps
7	R/W	**Center Mute Control** 0: Normal 1: Mute (-∞ dB)
6:5	-	**Reserved**
4:0	R/W	**Center Master Volume** (CNT[4:0]) in 1.5 dB steps

❶ For LFE/CEN, 00h 0dB
1Fh 46.5dB attenuation

6.1.23 MX38 Surround Master Volume

Default: 8080H

Bit	Type	Function

15	R/W	**Left Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**Surround Master Left Volume** (LSR[4:0]) in 1.5 dB steps
7	R/W	**Right Mute Control** 0: Normal 1: Mute (-∞ dB)
6:5	-	**Reserved**
4:0	R/W	**Surround Master Right Volume** (RSR[4:0]) in 1.5 dB steps

❶ For LSR/RSR, 00h 0dB
1Fh -46.5dB attenuation

6.1.24 MX3A S/PDIF Output Channel Status and Control

Default: 2000H

Bit	Type	Function
15	R/W	**Validity Control** (control V bit in Sub-Frame) 0: The V bit (valid flag) in sub-frame depends on whether or not the S/PDIF data is under-run 1: The V bit in sub-frame is always send as 1 to indicate the invalid data is not suitable for receiver
14	R	**DRS** (Double Rate S/PDIF) The ALC655 does not support double rate S/PDIF, this bit is always 0.
13:12	R/W	**SPSR** [1:0] (S/PDIF Sample Rate) 10: Sample rate set to 48KHz. Fs[**0:3**]=0100 (default) 00,01,11: Reserved
11	R/W	**LEVEL** (Generation Level)
10:4	R/W	**CC** [6:0] (Category Code)
3	R/W	**PRE** (Preemphasis) 0: None 1: Filter preemphasis is 50/15 µsec
2	R/W	**COPY** (Copyright) 0: Asserted 1: Not asserted
1	R/W	/**AUDIO** (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	**PRO** (Professional or Consumer format) 0: Consumer format 1: Professional format ALC655 supports consumer channel status format, this bit is always 0

❶To ensure the control and status information started up correctly at the beginning of S/PDIF transmission, MX3A.[14:0] should only be written to when S/PDIF transmitter is disabled (MX2A.2=0).

❷If validity control is set (MX3A.15=1), those data bits (bit 8 ~ bit 27) should be forced to 0 to get better compatibility with mini disc.

6.2 Vendor Defined Registers (Page ID-00h)

These registers are available to Realtek and Realtek customers for specialized functions.

6.2.1 MX60 S/PDIF Input Channel Status [15:0]

Default: 0000h

The data in MX60 are captured from channel status [15:0] of S/PDIF-IN signal.

Bit	Type	Function
15	R	LEVEL (Generation Level)
14:8	R	CC[6:0] (Category Code)
7:6	R	Mode[1:0]
5:3	R	PRE[2:0] (Pre-Emphasis)
2	R	COPY (Copyright) 0: asserted 1: Not asserted
1	R	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	PRO (Professional or Consumer format) 0: consumer format 1: professional format

6.2.2 MX62 S/PDIF Input Channel Status [29:15]

Default: 0000h

The data in MX62 are captured from channel status [29:16] of S/PDIF-IN signal.

Bit	Type	Function
15	R	"V" bit in sub-frame of SPDIFI 0: Data X and Y are valid 1: At least one of data X and Y is invalid This bit is real-time updated, and it is meaning when S/PDIF-IN is locked
14	R	S/PDIF-IN Input Signal Locked by hardware 0: Unlocked 1: Locked
13:12	R	Ca[1:0] (Clock Accuracy)
11:8	R	Fs[3:0]. (Sample Frequency in channel status) 0000: 44.1KHz 0010: 48 KHz 0011: 32 KHz Others: Reserved
7:4	R	Cn[3:0] (Channel Number)
3:0	R	Sn[3:0] (Source Number)

❶The bits [13:0] are captured from channel status [29:16] of SPDIFI.

❷The consumer channel status of SPDIFI (bit0~bit31):

0	1	2	3	4	5	6	7
PRO	/AUDIO	COPY	PRE0	PRE1	PRE2	Mode0	Mode1
8	9	10	11	12	13	14	15
CC0	CC1	CC2	CC3	CC4	CC5	CC6	LEVEL
16	17	18	19	20	21	22	23
Sn0	Sn1	Sn2	Sn3	Cn0	Cn1	Cn2	Cn3
24	25	26	27	28	29	30	31
Fs0	Fs1	Fs2	Fs3	Ca0	Ca1	0	0

❸The data from SPDIF input is forced to 0 once the SPDIF input signal is unlocked. Software must check this 'LOCK' bit before dealing with SPDIF input operations.

6.2.3 MX64 Surround DAC Volume

Default: 0808H

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**Surround DAC Left** Volume (SDL[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**Surround DAC Right Volume** (SDR[4:0]) in 1.5 dB steps

❶ For SDL/SDR, 00h +12 dB gain
08h 0dB
1Fh -34.5dB attenuation

❷ The default value is 0808H (unmuted).

6.2.4 MX66 Center/LFE DAC Volume

Default: 0808H

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**LFE DAC Volume** (LD[4:0]) in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**Center DAC Volume** (CD[4:0]) in 1.5 dB steps

❶ For LD/CD, 00h +12 dB gain
08h 0dB
1Fh -34.5dB attenuation

❷ The default value is 0808H (unmuted).

6.2.5 MX6A Data Flow Control

Default: 0000h

This register is used to control various parts of the ALC655 multi-channel functions.

Bit	Type	Function
15	RW	**SPDIF Input Enable** 0: Disable **(Default)** 1: Enable
14	R/W	**SPDIF-In Monitoring Control** 0: Disable, SPDIFI data is not added into PCM data to DAC. (Default) 1: Enable, MSB 16-bit of SPDIFI data will be added into PCM data to DAC ***if*** SPDIFI is locked.
13:12	R/W	**S/PDIF Output Source** 00: S/PDIF output data is from ACLINK (default) 01: S/PDIF output data is from ADC 10: Directly bypass S/PDIF-In signal to S/PDIF-Out 11: Reserved.
11	R/W	**PCM Data to AC-LINK** 0: PCM Data are from ADC (default) 1: PCM Data are from SPDIF input.
10	R/W	**MIC1 & MIC2 / CENTER & LFE Output Control** 0: pin-21 is MIC1, pin-22 is MIC2 (default) 1: pin-21 is CENTER-Out, pin-22 is LFE-Out.
9	R/W	**Line-In / Surround Output Control** 0: pin-23 and pin-24 are analog input (Line-In). (default) 1: pin-23 and pin-24 are duplicated output of surround channel (Surround-Out)
8:6	-	Reserved
5	R/W	**Analog Input Pass to Center/LFE Control**

		0: off 1: on
4	R/W	**Analog Input Pass to Surround Control** 0: off 1: on
3:1	-	Reserved
0	R/W	**Surround Output Source.** 0: S-OUT is the real surround output. (default) 1: S-OUT is the duplicated output of LINE-OUT

6.3 Discovery Descriptor (Page ID-01h)

These registers are defined in AC'97 2.3 for sensing and analog plug&play functions.

6.3.1 MX62 PCI Sub System ID

Default: FFFFh

Bit	Type	Function
15:0	R/W	**PCI Sub System Vendor ID** This register can be written once only after power on, and **is not affected by AC97 cold reset**. System manufacture's BIOS can set its own sub-system ID. The default value FFFFh means this register is implemented and data is not set by BIOS.

6.3.2 MX64 PCI Sub Vendor ID

Default: FFFFh

Bit	Type	Function
15:0	R/W	**PCI Vendor ID** This register can be written once only after power on, and **is not affected by AC97 cold reset**. System manufacture's BIOS can set its own sub-vendor ID. The default value FFFFh means this register is implemented and data is not set by BIOS.

6.3.3 MX66 Sense Function Select

Default: 0000h

Bit	Type	Function
15:5		Reserved
4:1	R/W	**Function Code bits, FC[3:0]** These bits specify the type of audio function described in page ID-01h MX66, MX68 and MX6A. 0h: FRONT OUT 1h: SURROUND OUT 5h: MIC1 In 6h: MIC2 In 7h: LINE In Others: Not supported
0	R/W	**Tip or Ring Selection, T/R** This bit sets which jack conductor the sense value is measured from. It is combined with FC[3:0]. 0: Tip (Left channel) 1: Ring (Right channel)

6.3.4 MX68 Sense Function Information

Default: 02F1h

Bit	Type	Function

15:5	-	Reserved
4	R/W	**Information Valid bit, IV** 0: After a sense cycle is completed indicates that **no** information is provided on the sensing method 1: After a sense cycle is completed indicates that information is provided on the sensing method Clearing this bit by writing "1", writing "0" to this bit has no effect.
3:1	NA	Reserved
0	R	**Function Information Present, FIP** This bit is set to a '0' indicates that the G[4:0], INV, DL[4:0] and ST[2:0] bits are ***not*** supported.

6.3.5 MX6A Sense Detail

Default: 0000h

Bit	Type	Function
15:13	-	Reserved
12:8	R	**Sense bits, S[4:0]** (Default value depends on sensed result after Cold Reset) For output devices: 02h: Not specificed or unknown 05h: Powered speaker 06h: Earphone or passive speaker Other: Not supported For input deices: 12h: Not specified or unknown 13h: Mono Microphone 15h: Stereo Line-In Other: Not supported This field reports the type of output/input peripheral plugged in the jack after sensing.
7:0	R	Always read as 0.

6.4 Extension Registers

6.4.1 MX78 GPIO(JD) Interrupt Control & Status

Default: 0000h

Bit	Type	Function
15	R/W	**GPIO Statue Indication in SDATA_IN** 0:The status of GPIO0(JD0)/GPIO1(JD1)/JD2 and its valid tag are not indicated in SDATA_IN. 1: The status of GPIO0(JD0)/GPIO1(JD1)/JD2 and its valid tag are indicated in SDATA_IN
14	R/W	**JD2 interrupt Enable** 0: Disable 1: Enable. A low to high transaction will trigger the interrupt in bit0 in SDATA_IN's slot-12.
13	R/W	**GPIO1(JD1) interrupt Enable** (when GPIO1/JD1 is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the interrupt in bit0 in SDATA_IN's slot-12.
12	R/W	**GPIO0(JD0) interrupt Enable** (when GPIO0/JD0 is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the interrupt in bit0 in SDATA_IN's slot-12.
11:10	NA	Reserved
9	R/W	**GPIO1Primitiveness Control** 0: Set GPIO1(JD1) as input pin. 1: Set GPIO1(JD1) as output pin.
8	R/W	**GPIO0 Primitiveness Control** 0: Set GPIO0(JD0) as input pin. 1: Set GPIO0(JD0) as output pin.
7	NA	Reserved
6	R/W	**JD2 Interrupt Status (JD2_IS)** 0: No JD2 interrupt. 1: JD2 interrupt. JD2_IS= (MX78.14==1) & (JD2 transition).

		Write 1 to clear this status bit.
5	R/W	**GPIO1/JD1 Interrupt Status (JD1_IS)**. (When GPIO1 is used as input) 0: No JD1 interrupt. 1: JD1 interrupt. JD1_IS= (MX78.13==1)&(MX78.9==0) & (JD1 transition). Write 1 to clear this status bit.
4	R/W	**GPIO0/JD0 Interrupt Status (JD0_IS)**. (When GPIO0 is used as input) 0: No JD0 interrupt. 1: JD0 interrupt. JD0_IS= (MX78.12==1)&(MX78.8==0) & (JD0 transition) Write 1 to clear this status bit.
3	NA	Reserved
2	R	**JD2 Input Status** 0: JD2 is driven low by external device (input). 1: JD2 is driven high by external device (input).
1	R/W	**GPIO1(JD1) Input/Output Status** 0: GPIO1 is driven low by/to external device. 1: GPIO1 is driven high by/to external device.
0	R/W	**GPIO0(JD0) Input/Output Status** 0: GPIO0 is driven low by/to external device. 1: GPIO0 is driven high by/to external device.

❶GPINT in bit0 of SDATA_IN's slot-12 = **(MX78.4 | MX78.5 | MX78.6) | (MX24.15&MX24.11)**

❷When GPIO1/0 is used as input pin, its status will be also reflected in bit2/1 of SDIN's slot-12. Once GPIO1/0 is used as output pin, the bit2/1 of SDATA_IN's slot-12 is always 0.
The GPIOx is internally pulled high by a weak resistor. (Weak resistor is about 50K ~ 100K ohm)

6.4.2 MX7A Miscellaneous Control

Default: 60A2H

This register is used for three types of information. Bit 0 is a read/write bit which enables/disables the S/PDIF input receiver. Bit 1 is used to switch pin 47, which is duplexed due for pin-count reduction, between EAPD and S/PDIF modes. Bit 2 is used to select the clock source for the ALC655.

Bit	Type	Function
15	~~R~~	**Clock Source Selection (XTLSEL)** 0: Disable 14.318M→24.576M digital PLL. (Default if XTSEL is floating) 1: Enable 14.318M→24.576M digital PLL. (Default if XTLSEL is pull low)
14:13	-	Reserved
12	R/W	**Vrefout Disable** 0: Vrefout is driven by the internal reference (Default) 1: Vrefout is in high-Z mode. Software must set this bit to disable Vrefout output before MX6A.10 is set (MIC1 and MIC2 are shared as Center and LFE output).
11	R/W	**Independent Left/Right Mute Control for MX02** 0: Disable, only bit15 is a mute bit for left and right channel (Default) 1: Enable, bit15 mute left channel, bit7 mute right channel.
10:4	-	Reserved
3	R/W	**JD2 Control Surround-Out, Center-Out and LFE-Out** 0: Disable. (Default) 1: Enable, when (MX7A.3=1 & MX78.2=1), Surr-Out and CEN/LFE-Out are muted.
2	R/W	**JD1 Control Surround-Out, Center-Out and LFE-Out** 0: Disable. (Default) 1: Enable, when (MX7A.2=1 & MX78.1=1 & MX78.9=0), Surr-Out and CEN/LFE-Out are muted.
1	R/W	**Pin-47 Function Selection** 0: EAPD 1: SPDIF Input (Default)
0	R/W	**JD0 Control Surround-Out, Center-Out and LFE-Out** 0: Disable. (Default) 1: Enable, when (MX7A.0=1 & MX78.0=1 & MX78.8=0), Surr-Out and CEN/LFE-Out are muted. (Internal MX36.15, MX36.7, MX38.15 and MX38.7 are all set to 1.)

		This function should be implement by digital designer.

6.4.4 MX7C VENDOR ID1

Default: 414CH

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC655. The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4760h, which is the third of the Microsoft ID code.

Bit	Type	Function
15:0	R	**Vendor ID-** "AL"

6.4.5 MX7E VENDOR ID2

Default: 4760H

Bit	Type	Function
15:8	R	**Vendor ID-** "G"
7:4	R	**Chip ID-** 0110b (ALC655)
3:0	R	**Version number-** 0000b.

7. Electrical Characteristics

7.1.1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital	DVDD	3.0	3.3	3.6	V
Analog	AVDD	3.5	5.0	5.5	V
Operating Ambient Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts			+125	°C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				

7.1.2 Threshold Hold Voltage

Dvdd= 3.3V±5%, $T_{ambient}$=25^{0}C, with 50pF external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage range	V_{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage (SYNC,SDATA_OUT,RESET#)	V_{IL}	-	0.7	0.35Dvdd	V
Low level input voltage (XTAL_IN,BIT_CLK)	V_{IL}	-	1.0	0.35Dvdd	V
Low level input voltage (Other digital pins)	V_{IL}	-	1.2	0.35Dvdd	V
High level input voltage (SYNC,SDATA_OUT,RESET#)	V_{IH}	0.4DVdd	1.7	-	V
High level input voltage (XTAL_IN,BIT_CLK)	V_{IH}	0.4DVdd	2.2	-	V
High level input voltage (Other digital pins)	V_{IH}	0.4DVdd	1.7	-	V
High level output voltage	V_{OH}	0.9DVdd		-	V
Low level output voltage	V_{OL}	-	-	0.1DVdd	V
Input leakage current	-	-10	-	10	µA
Output leakage current (Hi-Z)	-	-10	-	10	µA
Output buffer drive current	-	-	5	-	mA
Internal pull up resistance	-	30k	50k	100k	Ω

7.1.3 Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		+- 0.20		dB
DAC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		+- 0.20		dB

7.1.4 S/PDIF output Characteristics

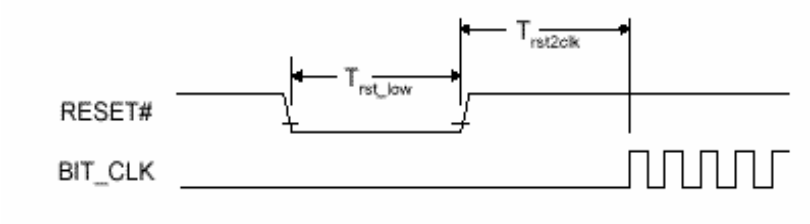
Dvdd= 3.3V, $T_{ambient}$=25^{0}C, with 75Ω external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
High level output voltage	V_{OH}	3.0	3.3		V
Low level output voltage	V_{OL}	-	0	0.5	V

7.2 AC Timing Characteristics

7.2.1 Cold Reset

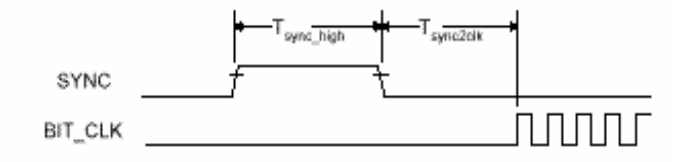
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK Startup delay	$T_{rst2clk}$	162.8	-	-	ns



Cold reset timing diagram

7.2.2 Warm Reset

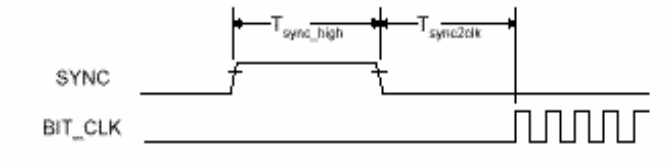
Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK Startup delay	$T_{sync2clk}$	162.8	-	-	ns



Warm reset timing diagram

7.2.3 AC-Link Clocks

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Note 1: Worse case duty cycle restricted to 45/55.					



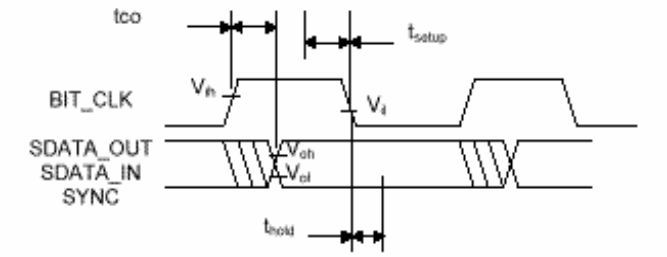
BIT_CLK and SYNC timing diagram

7.2.4 Data Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. Note 2: 50pF external load					

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output.					

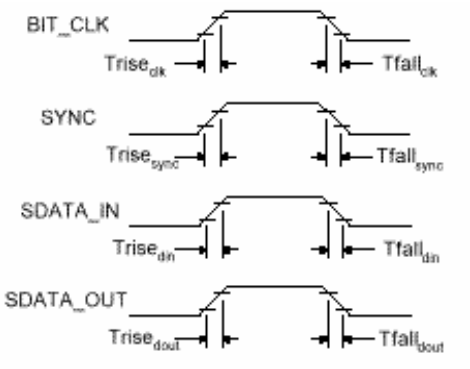
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.					



Data Output and Input timing diagram

7.2.5 Signal Rise and Fall Timing

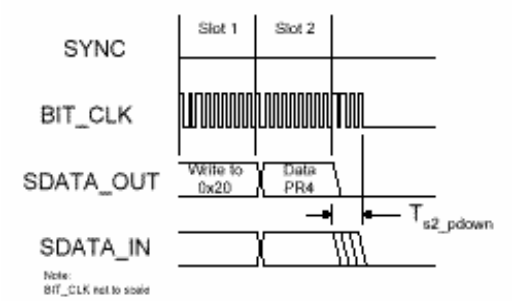
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time	$Trise_{clk}$	-	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	-	-	6	ns
SYNC rise time	$Trise_{sync}$	-	-	6	ns
SYNC fall time	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	-	-	6	ns
Note 1: 75pF external load (50 pF in AC'97 rev2.1) Note 2: rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3: fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					



Signal Rise and Fall timing diagram

7.2.6 AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

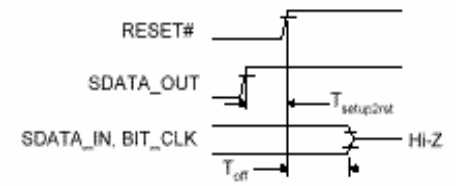


AC-Link low power mode timing diagram

7.2.7 ATE Test Mode

To meet AC'97 rev2.3 specifications, EAPD, SPDIFO, BIT_CLK and SDATA_IN should be floating in test mode.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns



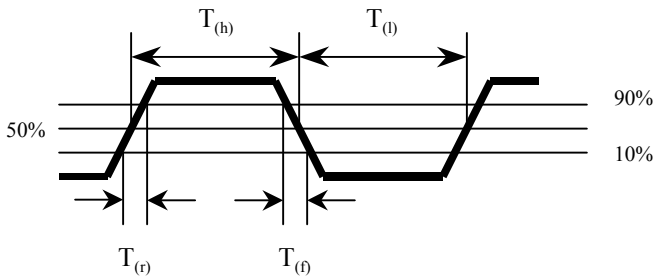
ATE test mode timing diagram

7.2.8 AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

7.2.9 SPDIF Output

SPDIF_OUT	Minimum	Typical	Maximum	Units
Rise time/fall time	0		10	%
Duty cycle	45		55	%



Notes:
Rise time = 100 * $T_{(r)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Fall time = 100 * $T_{(f)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Duty cycle = 100 * $T_{(h)}$/ ($T_{(l)}$+ $T_{(h)}$)%

8. Analog Performance Characteristics

Standard test conditions: $T_{ambient}=25^0C$, Dvdd=3.3V ±5%,Avdd=5.0V±5%
1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
10KΩ/50pF load; Test bench Characterization BW: 10Hz~22KHz
0dB attenuation; tone and 3D disabled

Parameter	Minimum	Typical	Maximum	Units
Full scale input voltage: Line inputs (Mixers)	-	1.6	-	
Line inputs (A/D)	-	1.0	-	Vrms
Mic input (0 dB)	-	1.6	-	
Mic input (20 dB boost)	-	0.16	-	
Full scale output voltage				
FRONT-OUT / SURROUND-OUT	-	1.25	-	Vrms
CEN/LFE-OUT	-	1.25	-	Vrms
Analog to Analog S/N: CD to LINE-OUT	-	90	-	dB
Other to LINE-OUT	-	90	-	
Analog frequency response	10	-	22,000	Hz
S/N (A-weighted): D/A	-	86	-	dB
A/D	-	86	-	
Total Harmonic Distortion: D/A	-	-70	-	dB
A/D	-	-75	-	
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-75	-	-	dB
Out-of-Band Rejection	-	-65	-	dB
Group delay	-	-	1	ms
Power Supply Rejection	-	-65	-	dB
MIC Boost Gain	6		30	dB
Master Volume (FRONT/SURR/CEN/LFE): 32 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-46.5	dB
Master Volume (MONO-OUT): 32 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-46.5	dB
PC Beep Volume 16 steps:				
Step Size	-	3.0	-	dB
Attenuation Control Range	0	-	-45	dB
Analog Mixer Volume 32 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	-34.5	-	+12	dB
Record Gain 16 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	0	-	+22.5	dB
Input impedance (gain = 0dB, mixer = off)				
LINE-IN, CD-IN, AUX-IN, MIC1 / MIC2	-	64	-	KΩ
PCBEEP, PHONE	-	16	-	KΩ

cont…

Output Impedance FRONT-OUT / SURROUND-OUT CEN/LFE-OUT MONO-OUT	 - - -	 5 200 500	 - - -	 Ω Ω Ω
Amplifier Maximum Output Power @20Ω load	-	-	50	mW
Power Supply Current VA=5.0V VD=3.3V	 - - -	 50 15	 - -	 mA mA
Power Down Current VA=5.0V VD=3.3V	 - -	 - -	 1000 700	 uA uA
Vrefout/Vrefout2/Vrefout3	-	2.50	4.0	V
Vrefout Drive Current	-	5	-	mA

9. Design Suggestions

9.1 Clocking

The clock source is decided by XTLSEL latched from pin-46 after **power-on reset.** The clock source of different configuration is listed below:

Configuration	**Operation & ID0**		
Pin-46(XTLSEL)	**ID0**	**BIT-CLK**	**Clock source**
NC	0 (Primary)	Output 12.288MHz	Crystal or ext. 24.576MHz is attached at XTL-IN
Low	0 (Primary)	Output 12.288MHz	Crystal or ext. 14.318MHz is attached at XTL-IN
NC	0 (Primary)	Input	*12.288M input at BIT-CLK*❶

*Low: Pulled low by a 0 ohm resistor. NC: Not connect or pulled high.
*Pin-46is internally pulled high by a weak resistor.

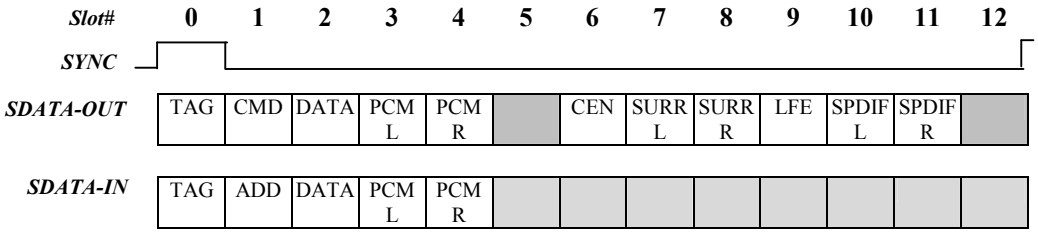
❶According to AC'97 ver 2.3, the primary mode while RESET# is asserted, if a clock is present at BIT-CLK pin for at least 5 cycles before RESET# is de-asserted, ALC655 is a consumer of BITCLK. ALC655 should use external 12.288MHz BITCLK as its clock source.

9.2 AC-Link

When the ALC655 receives serial data from the AC97 controller, it samples SDATA_OUT on the falling edge of BIT_CLK. When the ALC655 sends serial data to the AC97 controller, it starts to drive SDATA_IN on the rising edge of BIT_CLK.

The ALC655 will return any uninstalled bits or registers with 0 for read operations. The ALC655 also stuffs the unimplemented slot or bit with 0 in SDATA_IN. Note that AC-LINK is MSB-justified.

Refer to "Audio CODEC '97 Component Specification Revision 2.3." for details.



Default ALC655 Slot Arrangement – CODEC ID = 00 **(ALC655 supports only primary mode)**

9.3 Reset

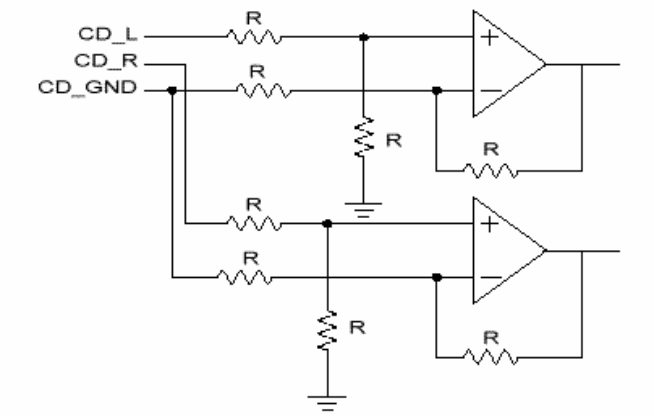
There are 3 types of reset operations: Cold, Warm and Register.

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to its default value.
Register	Write register indexed 00h	Reset all registers to its default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA_OUT low during the period of RESET# assertion to guarantee that the ALC655 has reset successfully.

9.4 CD Input

It is important to pay attention to differential CD input. Below is an example of differential CD input.



Example of differential CD input

9.5 Odd Addressed Register Access

The ALC655 will return “0000h” when odd-addressed and unimplemented registers are read.

9.6 Power-down Mode

It is important to pay special attention to the power down control register (index 26h), especially PR4 (powerdown AC-link).

9.7 Test Mode

To provide compatibility with AC’97 rev2.2, the ALC655 will float its digital output pins in both ATE and Vendor-Specific test modes. Please refer to AC’97 rev2.2 section 9.2 for a detailed description of the test modes.

9.7.1 ATE In Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode, the ALC655 will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

9.7.2 Vendor Specific Test Mode

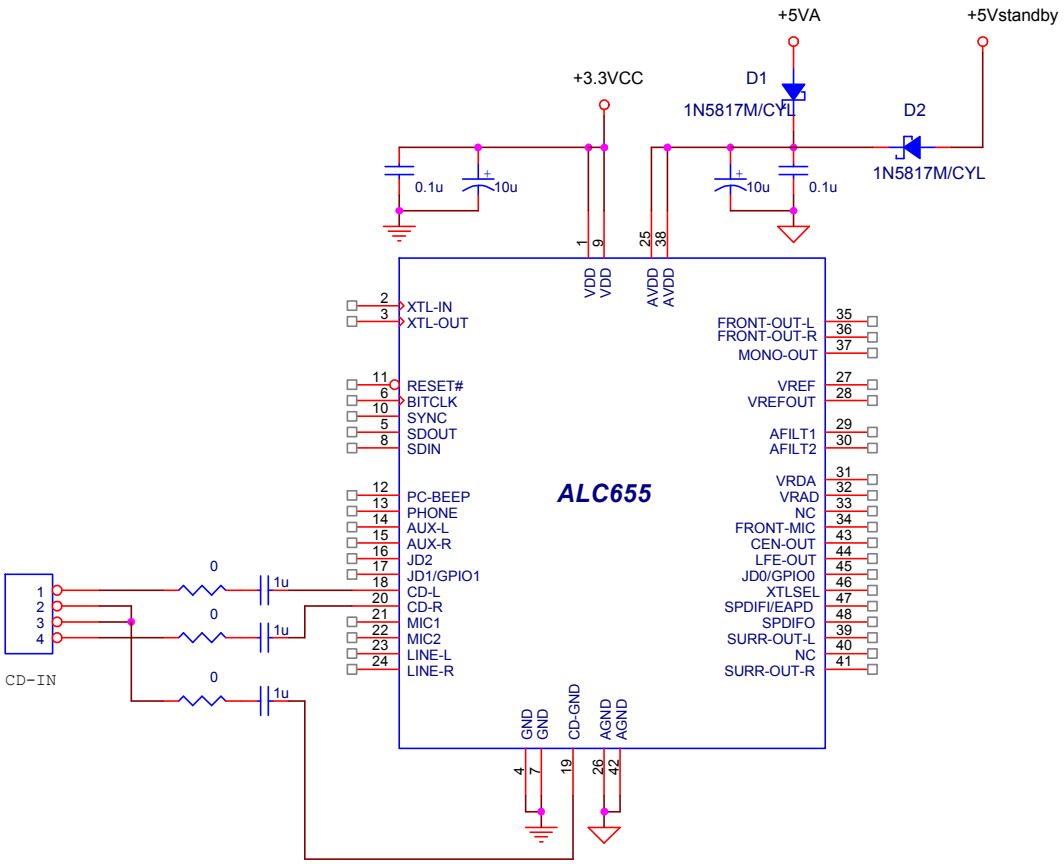
The Vendor Specific Test mode is no longer supported.

9.8 POWER OFF CD Function

The 'POWER OFF CD' function describes a state after the system has been shut down (digital power is off) and a +5V analog power is supplied, the ALC655 will turn on the CD-IN op and output amplifier. It is possible to design a system which will save op-amp circuitry and bypass CD output directly to the speaker.

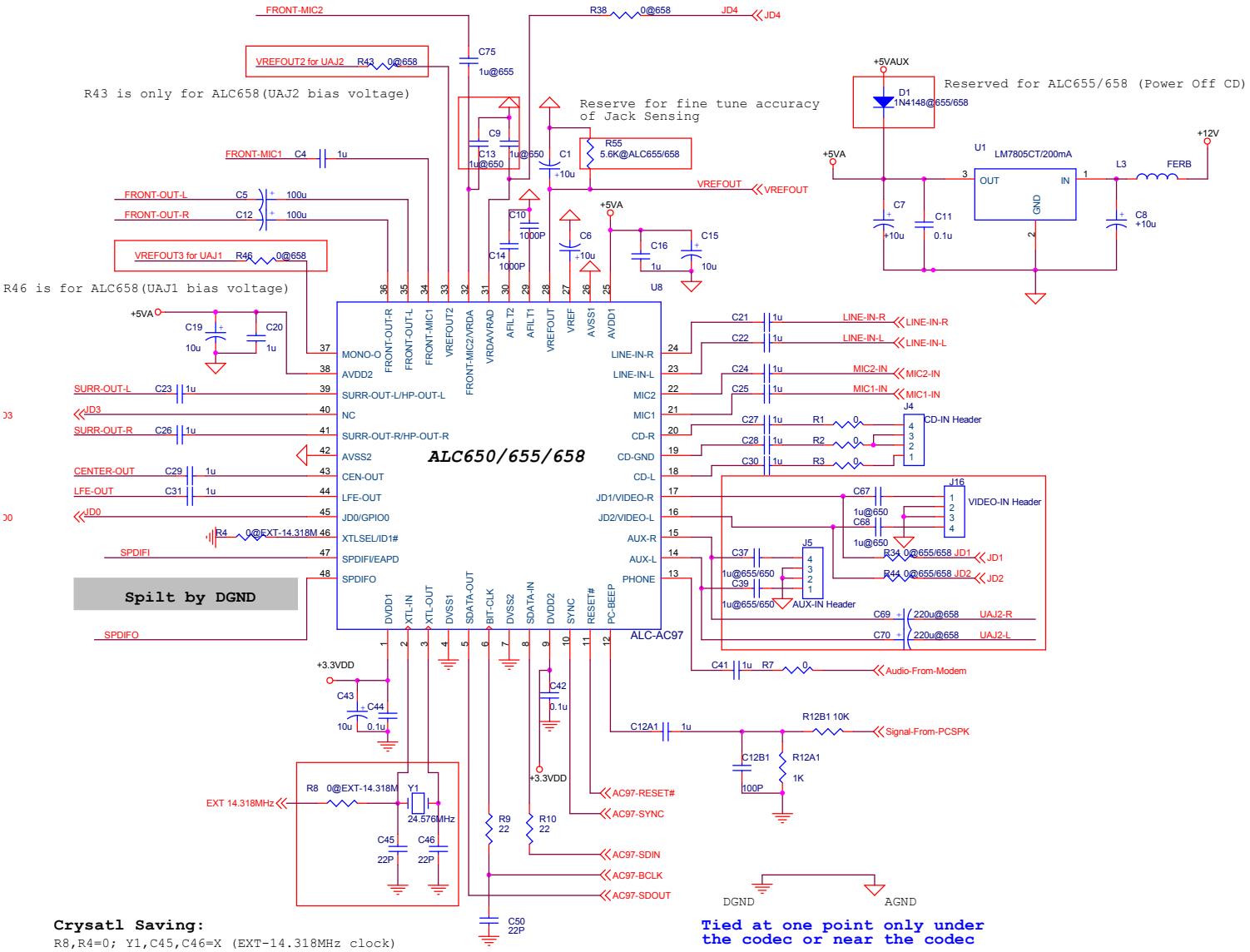
The figure below indicates the system application circuitry to support the 'POWER OFF CD' function. The operation mode is defined by +3.3VCC and +5VA analog power **without VAUX** is required for ALC20x series codec.

+3.3VCC	+5VA	+5Vstandby	Operation Mode
No (0)	No (0)	No (0)	Shut Down
No (0)	Yes (1)	-	Power Off CD
No (0)	-	Yes (1)	Power Off CD
Yes (1)	No (0)	No (0)	Digital on, Analog is off
Yes (1)	Yes (1)	-	Normal



10. Application Circuits

The application circuit is for design reference only. System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications of application circuits have to be confirmed by Realtek.



	ALC655	ALC658	ALC650
C67	x	x	1u
C68	x	x	1u
R34	0	0	x
R44	0	0	x
C37	1u	x	1u
C39	1u	x	1u
C69	x	100u	x
C70	x	100u	x
C13	x	x	1u
C9	x	x	1u
C75	1u	1u	x
R46	x	0	x
R43	x	0	x

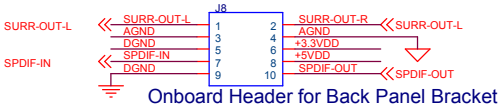
Arrangement of Jack Detection Pin:(ALC655)

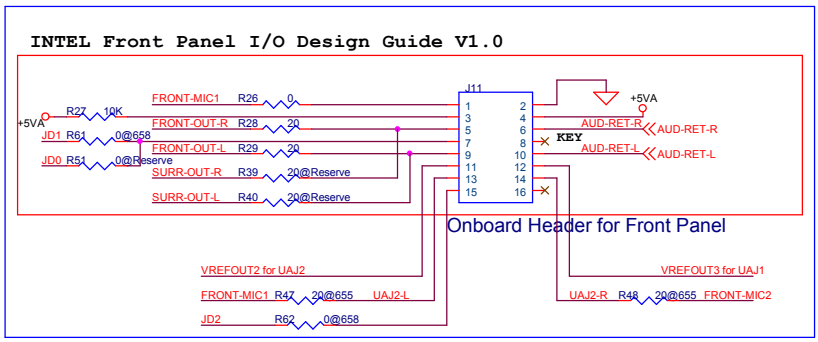
JD0 for MIC-IN
JD1 for FRONT-OUT
JD2 for LINE-IN

Arrangement of Jack Detection Pin:(ALC658)

JD0 for MIC-IN
JD1 for UAJ1(Front-Pannel)
JD2 for UAJ2 (Front-Pannel)
JD3 for FRONT-OUT
JD4 for LINE-IN

Compatible Filter Connection with ALC655

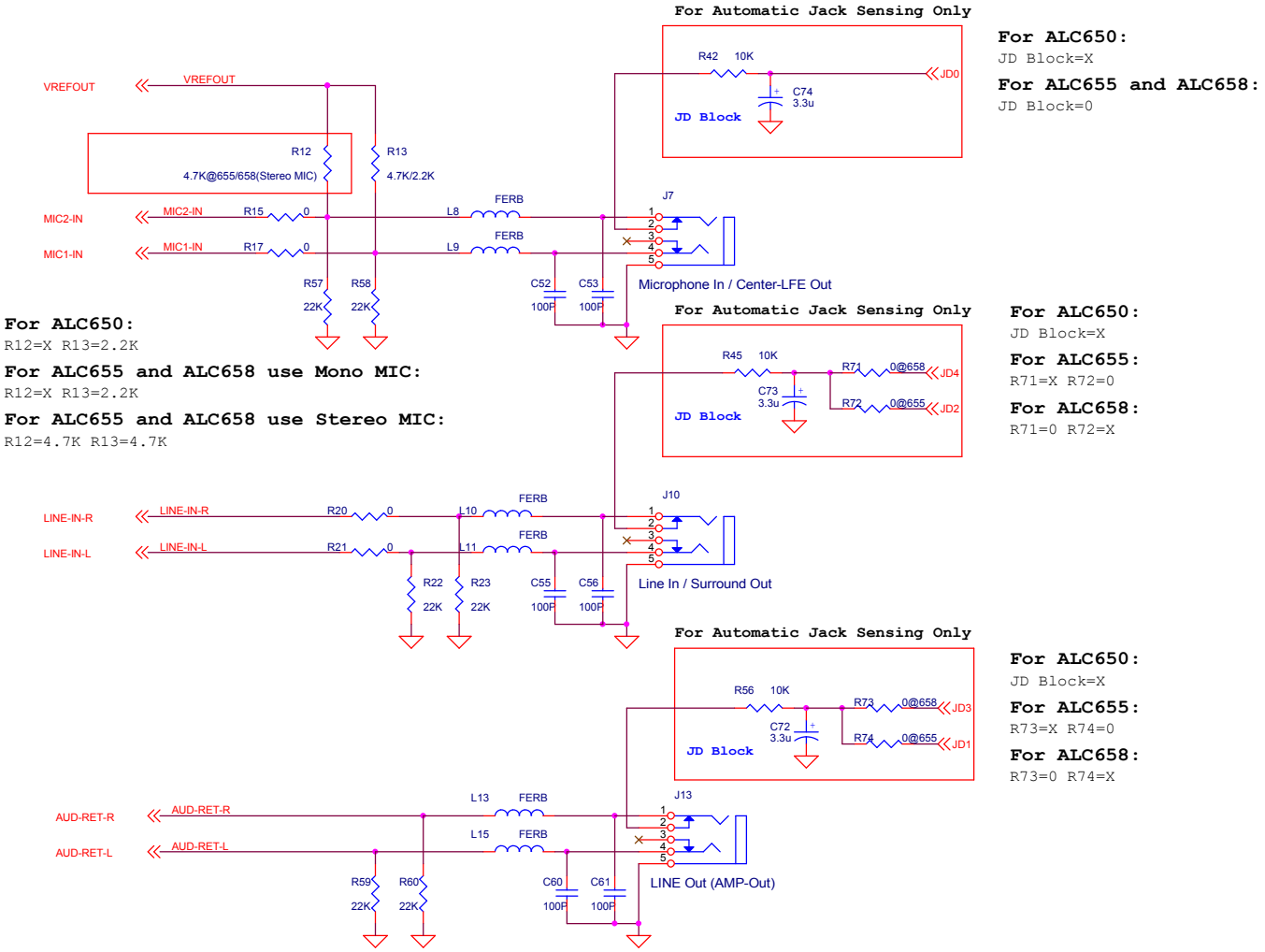




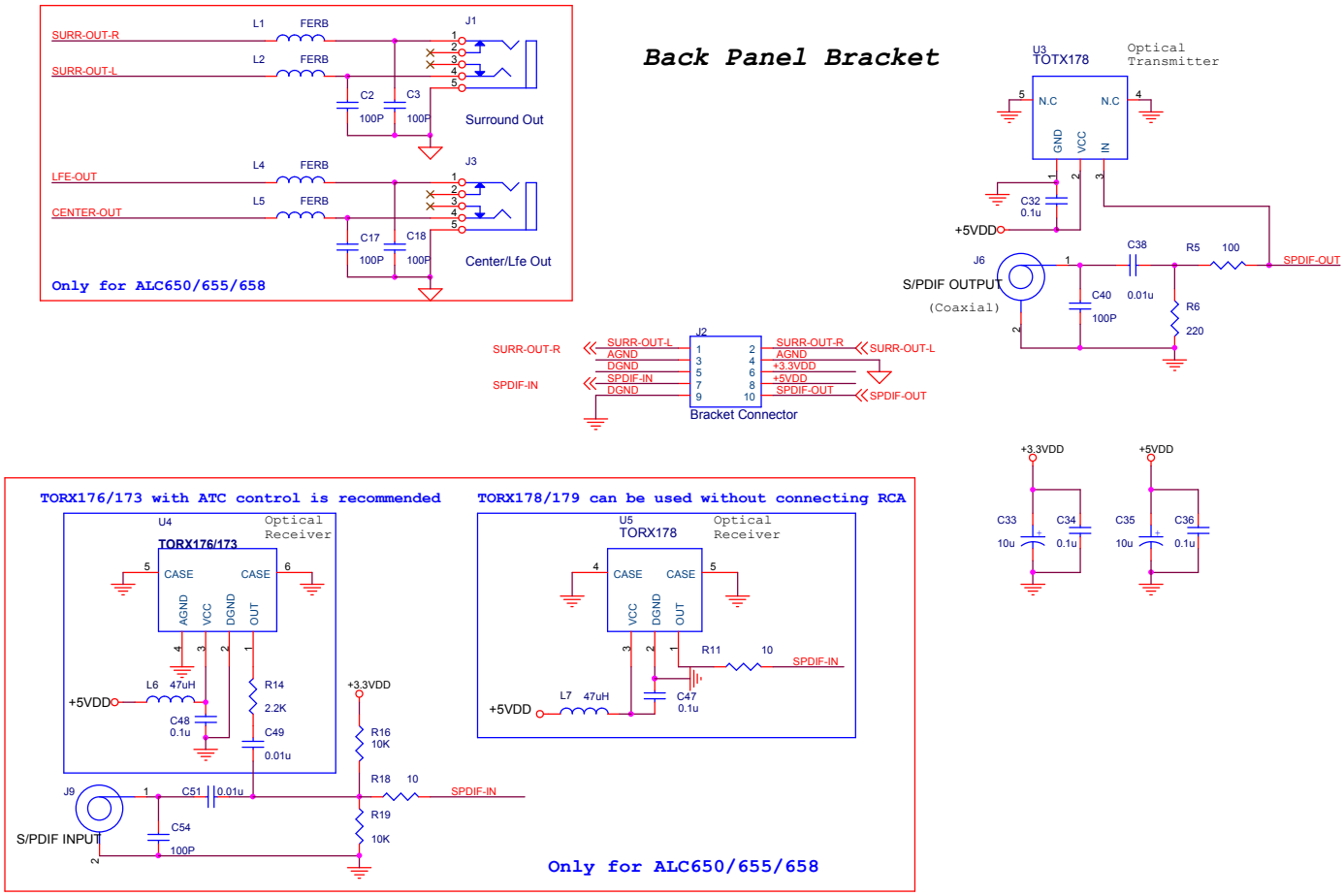
REALTEK Front Panel I/O for UAJ

	R26	R61	R62	R51	R47	R48
ALC655/658/650(with Intel Front Pannel)	0	x	x	x	x	x
ALC658(with Realtek Front Pannel - UAJ function)	x	0	0	x	x	x

Onboard Headers for Back Panel Bracket and Front Panel

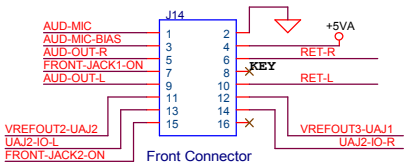


Analog I/O Connection

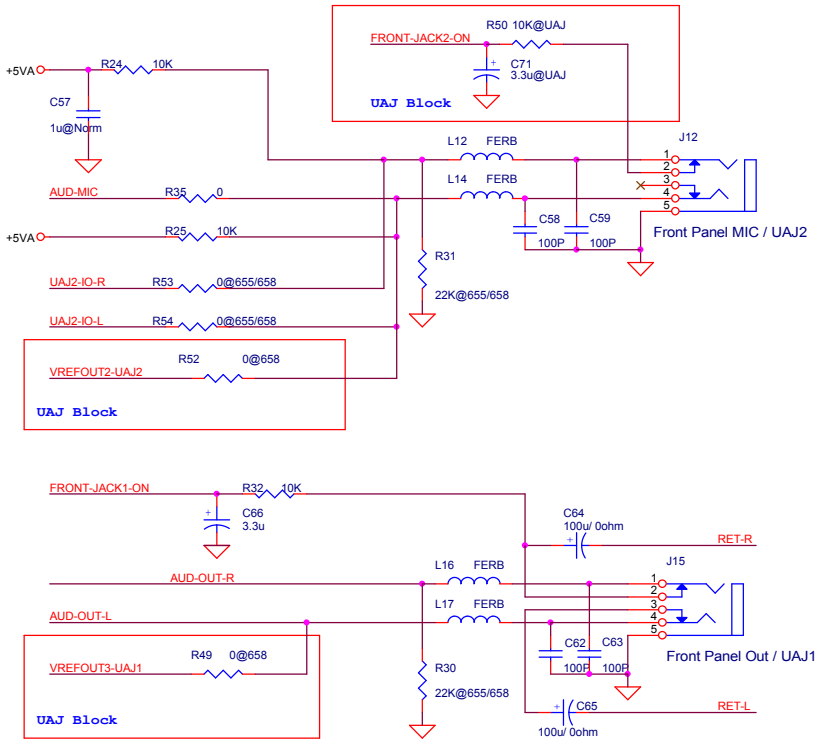


Back Panel Bracket for Surround/CEN/LFE outputs and S/PDIF I/O

Front Panel Module



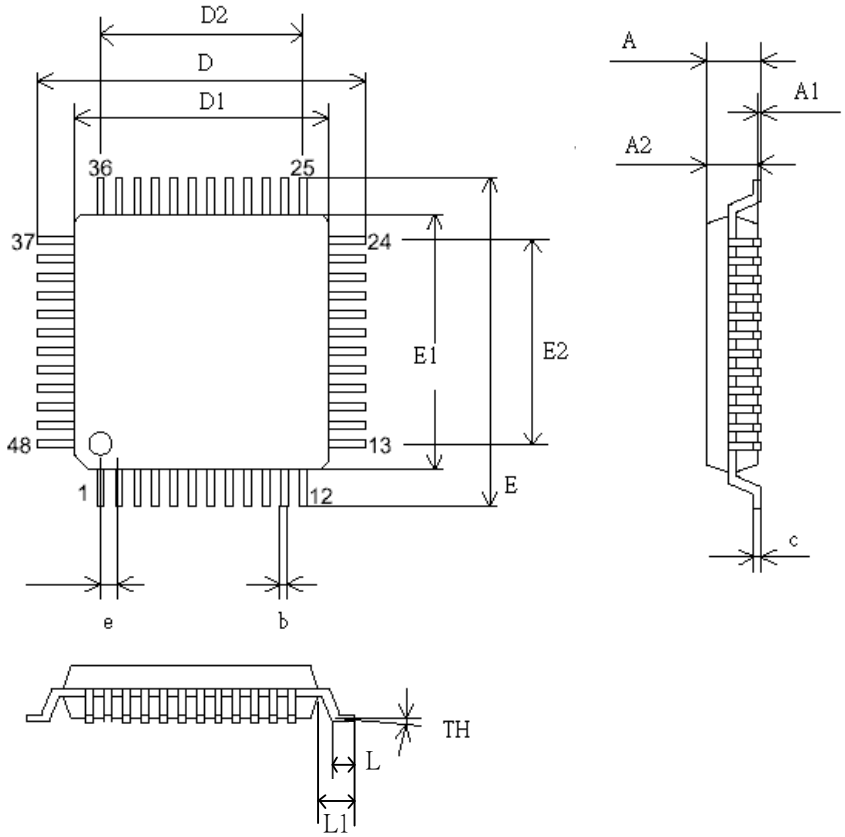
1~10 pin connector: INTEL Front Panel I/O Design Guide V1.0
11~16 pin: REALTEK Front Panel I/O for UAJ



	R64	R65	R32	R66	R30	R31	R24	R57	R35	R25	R53	R54	UAJ Block
ALC655/658/650(with Intel Front Pannel)	0	0	X	X	X	X	4.7K	1u	0	X	X	X	X
ALC658(with Realtek Front Pannel - UAJ function)	0	0	10K	3.3u	22K	22K	X	X	X	X	0	0	ON

Front Panel Connection

11. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
C	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0197 BSC		
TH	0^o	3.5^o	7^o	0^o	3.5^o	7^o
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

Ordering Information

Table 1. Ordering Information

Part Number	Package	Status
ALC655	Standard product. LQFP-48	
ALC655-LF	ALC655 with Lead (Pb)-Free LQFP-48 package	

Note: See page 3 for lead (Pb)-free package and version identification.

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