

120Watts

AEO/ALO40

High Efficiency



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Special Features

- 2.3" x 0.9" Industry Standard 8th brick outline
- Baseplate or Openframe construction
- Low Ripple and Noise
- Regulation to zero load
- High Capacitive Load start-up
- Fixed Switching Frequency
- Industry Standard features: Input UVLO with hysteresis, Enable, OVP, OCP, OTP, Output VoltageTrim, Differential Remote Sense
- Meets Basic Insulation

Environmental

Operating ambient temperature: -40°C to +85°C
 Storage temperature: -55°C to +125°C
 MTBF: > 1 million hours

Safety

UL, cUL 60950 Recognized
 TUV EN60950 Licensed

Total Power: 120 Watts
 Input Voltages: 48V
 No. of Outputs: Single

Electrical Specs

Input

Input Range 36 to 75 VDC
 Input Surge 100V /100ms
 Efficiency¹ 3.3V @ 91% (typical)

Output

Line / Load Regulation < 0.1% V_O (typical)
 Load Current Up to 40A for $V_O \leq 1.8V$
 Ripple and Noise² 40mV_{PK-PK} at 1.8V_O (typical)
 Transient Response 2% typical deviation
 50% to 75% step load
 20ms settling time (typical)
 Over Voltage Protection 130% V_O Typ (autorecovery)
 Over Current Protection 120% $I_{O,max}$ Typ (autorecovery)
 Over Temperature Protection 110°C average PCB temperature (autorecovery)
 Switching Frequency Fixed Frequency
 Isolation Voltage 1500Vdc

Control

Output Voltage Trim $\pm 10\% V_O$
 Enable TTL compatible
 (Positive or Negative Logic)

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Ordering Information

Input Voltage	Output Voltage	Output Current	Efficiency ¹	Model Number
36V to 75V	12.0V	10A	92.0%	A(X)O10B48 (N) - (6)(S)
36V to 75V	5.0V	20A	93.0%	A(X)O20A48 (N) - (6)(S)
36V to 75V	3.3V	30A	91.0%	A(X)O30F48 (N) - (6)(S)
36V to 75V	2.5V	35A	90.0%	A(X)O35G48 (N) - (6)
36V to 75V	1.8V	40A	89.5%	A(X)O40Y48 (N) - (6)
36V to 75V	1.5V	40A	88.0%	A(X)O40M48 (N) - (6)
36V to 75V	1.2V	40A	86.0%	A(X)O40K48 (N) - (6)

OPTIONS:

(X) : "L" = Open Frame / Low Profile

"E" = Baseplate Construction

(N) : "N" = designates Negative Logic Enable (default is Positive Enable with no suffix "N" required)

(6) : "-6" = 3.7mm nominal pin length (default is 5mm nominal pin length with no suffix "-6" required)

(S) : "-S" = Surface Mount Termination (default is Through Hole Termination with no suffix "-S" required)

Pin Assignment

Single Output

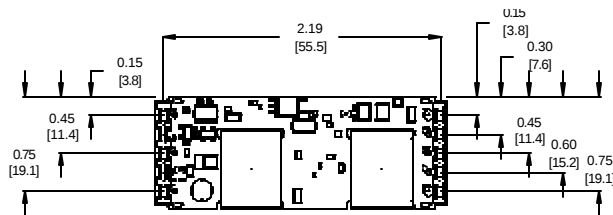
1. +Vin
2. Enable (On/Off)
3. -Vin
4. -V_{OUT}
5. -Sense
6. Trim
7. +Sense
8. +V_{OUT}

Notes:

1. Efficiency measurements are typical values taken at full load, nominal line and T_A = 25°C.
2. 20 MHz bandwidth. External 10 uF tant. capacitor in parallel with 1 uF ceramic capacitor placed across the output and secondary return ground.
3. All specifications are typical at nominal line, full load and T_A = 25°C unless otherwise noted.
4. All specifications subject to change without notice.
5. Mechanical drawings are for reference only. Dimensions are in inches [mm]. Pin placement tolerance ± 0.005 [0.127]. Mechanical Tolerance ± 0.02 [0.5], recommended surface mount pads (min: 0.080 x 0.112 [2.03 x 2.84] / max: 0.092 x 0.124 [2.34 x 3.15]); through hole pin diameter (Pins 4&8) Ø = 0.062 [1.57], others Ø = 0.04 [1.0] (6X).
6. Technical Reference Notes should be consulted for detailed information.
7. Warranty: 1yr.

* Astec reserves the right to make changes to the information contained herein without notice and assumes no liability as a result of its use and application. (REV D: AUGUST 25, 2005)

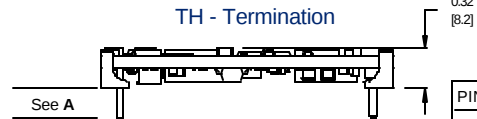
ALO - OPENFRAME



SMT - Termination



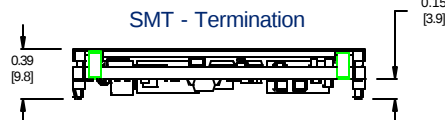
TH - Termination



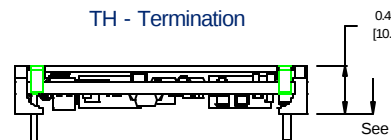
AEO - BASEPLATE



SMT - Termination



TH - Termination



PIN LENGTH	A
Std Pin Length:	0.189 [4.8] MIN 0.205 [5.2] MAX
"-6" Option:	0.137 [3.5] MIN 0.152 [3.9] MAX

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Astec Industry Standard