

100 Watts

ALQ20-Dual

Total Power: 100 Watts
 Input Voltages: 48V
 No. of Outputs: Dual

High Efficiency



Special Features

- Industry standard Dual O/p 1/4 Brick Footprint
- Open Frame Construction
- Low Ripple and Noise¹ < 30mV_{PK-PK}
- Regulation to zero load
- High Capacitive Load start-up
- Fixed Frequency Switching for EMI predictability
- Industry Standard features: OVP, OCP, OTP, Input UVLO, Enable, Trim
- Input Under Voltage Lockout with hysteresis
- Output Voltage Adjustability
- Meets Basic Insulation

Environmental

Operating Ambient Temperature -40°C to +85°C
 Storage temperature: -55°C to +125°C
 MTBF: > 1 Million Hrs

Safety

UL, cUL 60950 Recognized (Pending)
 TUV EN60950 Licensed (Pending)

Electrical Specs

Input

Input Range	36 to 75 VDC
Input Surge	100V /100ms
Efficiency ²	3.3V/1.5V @ 90% 3.3V/1.2V @ 90%

Output

Line / Load Regulation	< 1% Vo
Load Current	20A max per channel
Noise/Ripple ¹	30mV _{PK-PK} typical
Transient Response	40mV typical deviation (50% to 75% Step Load) < 300μs settling time (typ)
Over Voltage Protection	130% Vo Typ (latching)
Over Current Protection	130% I _{O,max} Typ (autorecovery)
Over Temperature Protection	115°C average PCB temperature (autorecovery)
Switching Frequency	410kHz (typ)
Isolation Voltage	1500Vdc

Control

Voltage Adjust	±10% V _{O,NOM}
Enable	TTL compatible (Positive or Negative options)

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ALQ20 - DUAL

Ordering Information

Input Volatge	Output Voltage		Output Current		Efficiency ²	Model Number
	Vo1	Vo2	Io1	Io2		
36V to 75V	3.3V	1.5V	20A	20A	90%	ALQ20FM48(N) - (6)
36V to 75V	3.3V	1.2V	20A	20A	90%	ALQ20FK48(N) - (6)
36V to 75V	3.3V	1.2V	15A	15A	90%	ALQ15FK48(N) - (6)

OPTIONS:

Enable Function "N" = Negative Logic Enable (default is Positive Logic Enable - no suffix "N")
 Pin Length "-6" = 3.7mm nominal pin length (default is 5mm nominal - no suffix "6")

Pin Assignment

Dual Output

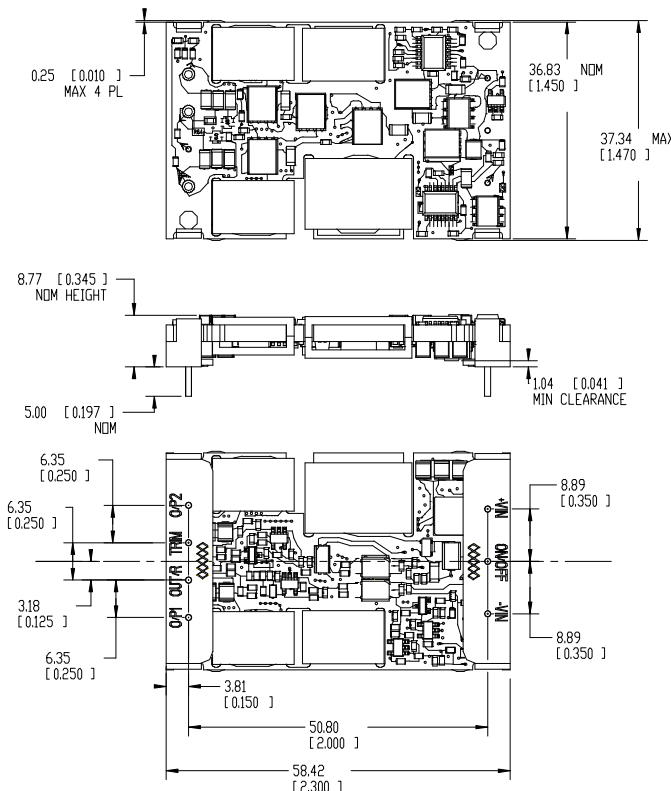
1. +Vin
2. Enable (On/Off)
3. -Vin
4. +V_{O2}
5. Secondary Return/Ground
6. Trim
7. +V_{O1}

Notes:

1. 20 MHz bandwidth. External 10 uF tant. capacitor in parallel with 1 uF ceramic capacitor placed output and secondary return ground.
2. Efficiency measurements taken at full load - balanced output load current, nominal line and T_A = 25°C.
3. All specifications are typical at nominal line, full load and T_A = 25°C unless otherwise noted.
4. All specifications subject to change without notice. Mechanical drawings are for reference only
5. Technical Reference Notes should be consulted for detailed information when available
6. Warranty 1yr.

This is a Preliminary Data Sheet. Astec reserves the right to make changes to the information contained herein without notice and assumes no liability as a result of its use and application.
 (REV A: APRIL12, 2004)

Mechanical Outline



Dimensions are in inches [millimeters]
 Pin placement tolerance ± 0.005 [0.127]
 Mechanical Tolerance ± 0.02 [0.5]

Astec Industry Standard