

ALi M3328C DVB-S Solution

DB-M3328c-02V02

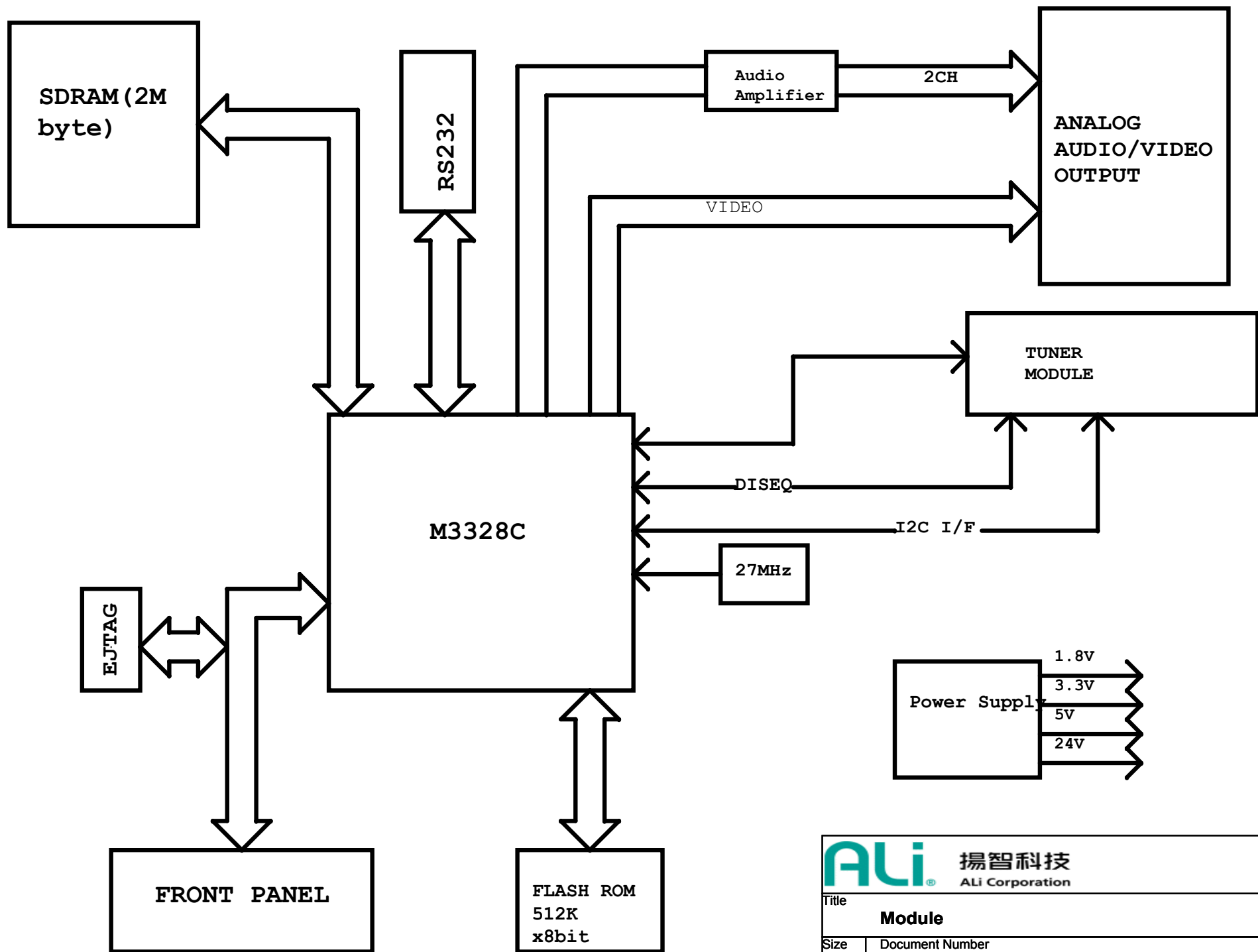
Change List:

ITEM	Change	DATE	BY
1	Created DB-M3328C-02V02	2005-06-10	qinhe
2	Changed some GPIO of panel.	2005-06-20	Tom
3	Changed DiSEqC Control Circuit	2005-06-20	Tom
4	Add a FLASH as 39LV040	2005-07-6	Tom

GPIO MAPPING:

Number	USAGE	USAGE DETAIL	NOTE
GPIO0	F_LOCK	PANEL LOCK LED(0:LIGHT)	
GPIO2	F_KEY2	PANEL KEY DETECT 2	NEED PULL HIGH
GPIO3	F_KEY1	PANEL KEY DETECT 1	NEED PULL HIGH
GPIO4	F_CLOCK	PANEL CLOCK	
GPIO5	F_DATA	PANEL DATA	
GPIO8	F_COM1	PANEL COM1	NEED PULL HIGH
GPIO9	F_COM2	PANEL COM2	NEED PULL HIGH
GPIO17	F_COM3	PANEL COM3	NEED PULL HIGH
GPIO18	LNB_CUT	LNB POWER CUT(1: OFF)	

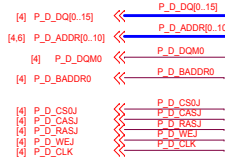
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Title COVER		
Size A	Document Number M3328C CB	Rev 1.0
Date: Thursday, January 05, 2006		
Sheet 1 of 8		



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Title Module		
Size A	Document Number M3328C CB	Rev 1.0
Date:	Thursday, January 05, 2006	Sheet 2 of 8

SDRAM I/F

[4] P_D_DQ[0..15]	← P_D_DQ[0..15]
[4:6] P_D_ADDR[0..10]	← P_D_ADDR[0..10]
[4] P_D_DQM0	← P_D_DQM0
[4] P_D_BADDR0	← P_D_BADDR0
P_D_CS0J	← P_D_CS0J
P_D_CASJ	← P_D_CASJ
P_D_RASJ	← P_D_RASJ
P_D_WEJ	← P_D_WEJ
P_D_CLK	← P_D_CLK



FLASH I/F

[4]	ROM_AD[0..18]	←←	ROM_AD[0..18]
[4]	ROM_DA[0..7]	←←	ROM_DA[0..7]
[4,6]	ROM_OE _J	←←	ROM_OE _J
[4]	ROM_WE _J	←←	ROM_WE _J



EJTAG I/F

		TRSTJ
[4]	TRSTJ	TDI
[4]	TDI	TDO
[4]	TDO	TMS
[4]	TMS	TCK
[4]	TCK	



RESET CIRCUIT

5VDC

R3 330R

D1 1N4148

TCS 100uF/16V

R6 1K

Q1 2N3906

R7 1K

D2 3.3V(ZENER Diode)

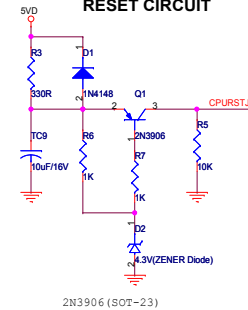
R5 10K

CPURSTJ

2N3906 (SOT-23)

Pinout diagram for 2N3906 (SOT-23):

3	C
PNP	
1	B
2	E



Front Panel I/F

Option
See the front panel
circuit

VDD33

5VDD

TP15 TP16 TP17 TP18 TP19

TP20 TP21 TP22 TP23

TP TP TP TP

R10 R11 R12 R13 R14

R9

33R

BC18

BC19

0.1uF

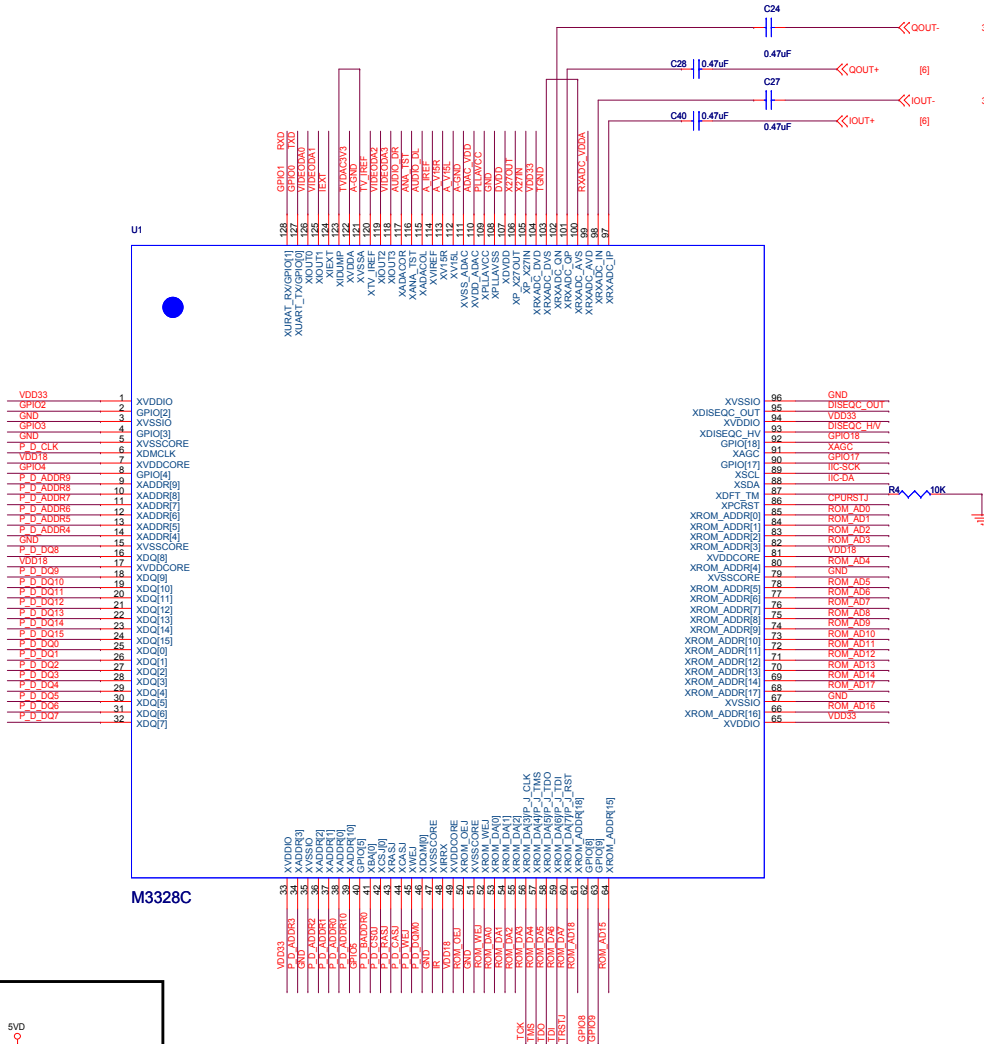
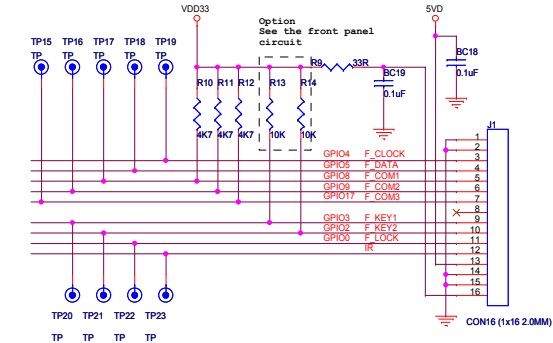
0.1uF

J1

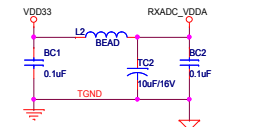
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

GPIO4 F CLOCK
GPIO5 F DATA
GPIO8 F COM1
GPIO9 F COM2
GPIO17 F COM3
GPIO3 F KEY1
GPIO2 F KEY2
GPIO0 F LOCK
GPIO0 IR

CON16 (1x16 2.0MM)

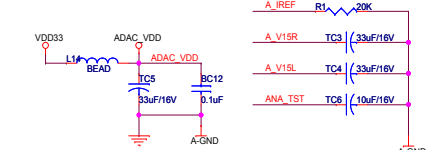
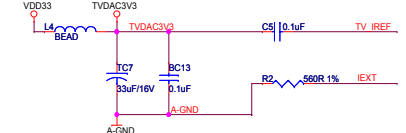


QPSK-ADC



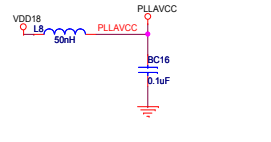
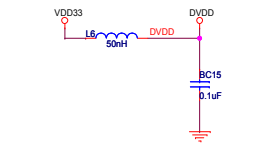
Audio-DAC

The diagram illustrates the Audio-DAC circuit. It features a voltage divider network connected to VDD33 and ADAC_VDD. The divider consists of a 20K resistor (R1) and a 33uF118V capacitor (TC3) in series. The output of this divider is connected to the ADAC_VDD pin. The ADAC_VDD pin is also connected to a 33uF118V capacitor (TC5) to ground. The output of the DAC is connected to a 33uF118V capacitor (TC4) to ground. The output of the DAC is also connected to a 10uF118V capacitor (TST) to ground. The output of the DAC is connected to the A_IREF pin. The output of the DAC is also connected to the A_V15R pin. The output of the DAC is also connected to the A_V15L pin. The output of the DAC is also connected to the ANA_TST pin. The output of the DAC is connected to the A_GND pin.

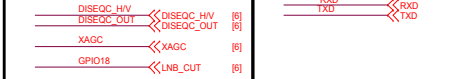
[illegible]

PLL

The diagram shows a PLL circuit. A 1.6 ohm resistor and a 50nH inductor are connected in series between VDD33 and DVDD. A 0.1uF capacitor is connected from DVDD to ground.



TUNER I/F		PERIPHERAL	
		IIC-SCK	IIC-SCK [6]
		IIC-DA	IIC-DA [6]
DISEQC_HV	DISEQC_HV [6]	RXD	RXD [4]
DISEQC_OUT	DISEQC_OUT [6]	TXD	TXD [4]
XAGC	XAGC [6]		
GPIO18	LNB_CUT [6]		



IIC-SCK	≡	IIC-SCK	[6]
IIC-DA		IIC-DA	[6]
RXD	≡	RXD	[4]
TXD		TXD	[4]



Crystal

X27OUT

R8

1M

Y1

27MHz

C8

27pF

X27IN

C7

27pF

AV I/F

AUDIO_DR

AUDIO_DL

AUDIO_0R

AUDIO_0L

5

15

VIDEO0A0

VIDEO0A1

VIDEO0A2

VIDEO0A3

VIDEO0A0

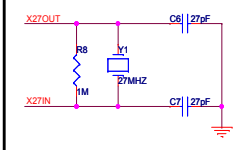
VIDEO0A1

VIDEO0A2

VIDEO0A3

5

15



AUDIO_DR
AUDIO_DL

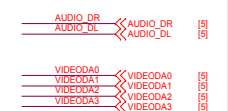
AUDIO_DR
AUDIO_DL

[5]
[5]

VIDEODATA0
VIDEODATA1
VIDEODATA2
VIDEODATA3

VIDEODATA0
VIDEODATA1
VIDEODATA2
VIDEODATA3

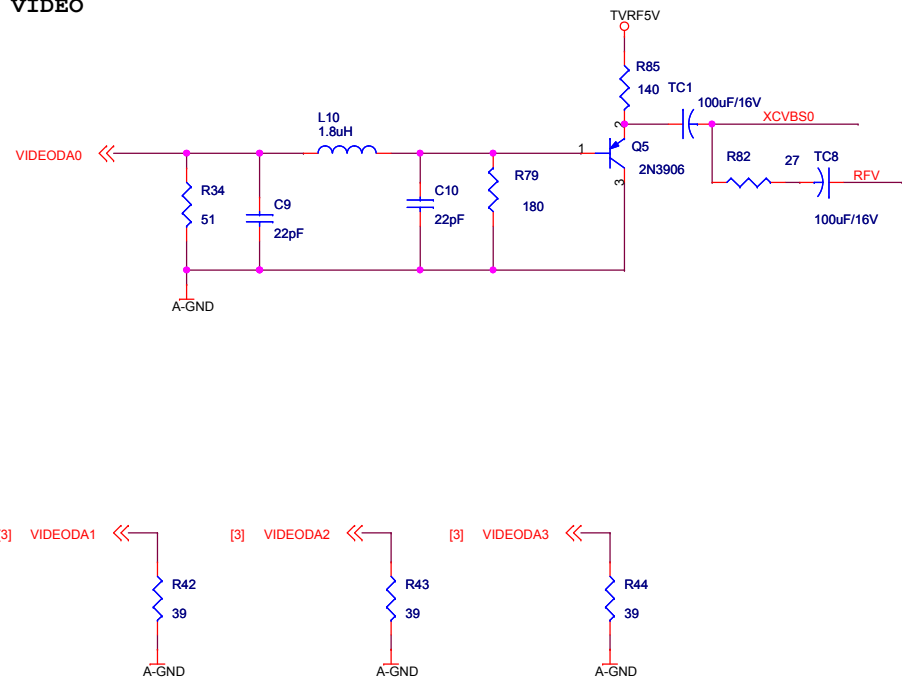
[5]
[5]
[5]
[5]



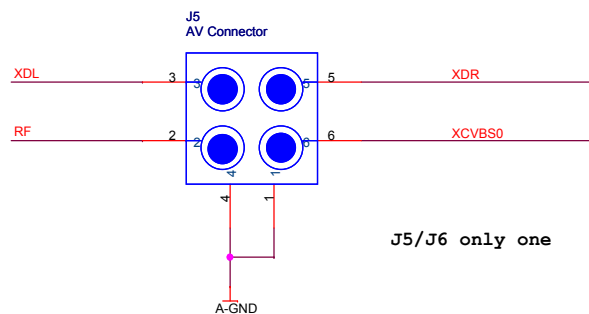
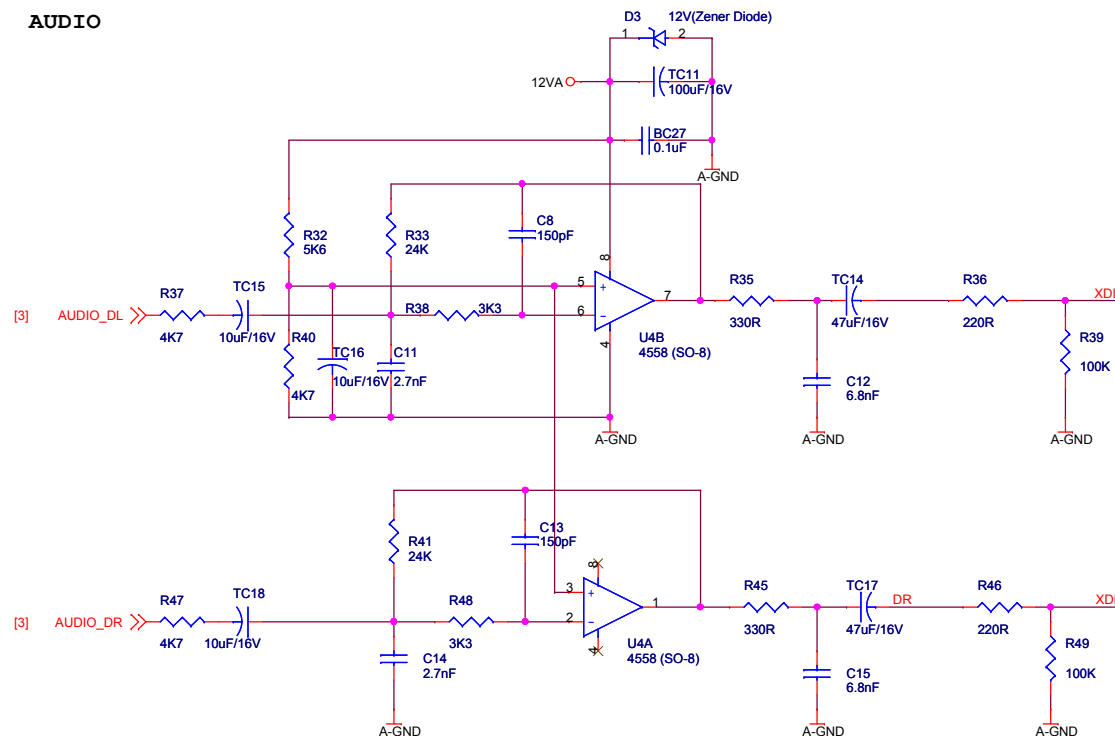
[3] ROM_DA[0..7] << ROM_DA[0..7]
 [3] ROM_AD[0..18] << ROM_AD[0..18]
 [3,6] ROM_OEJ << ROM_OEJ
 [3] ROM_WEJ << ROM_WEJ



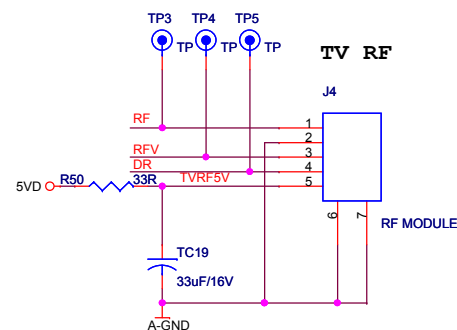
VIDEO



AUDIO



J5/J6 only one



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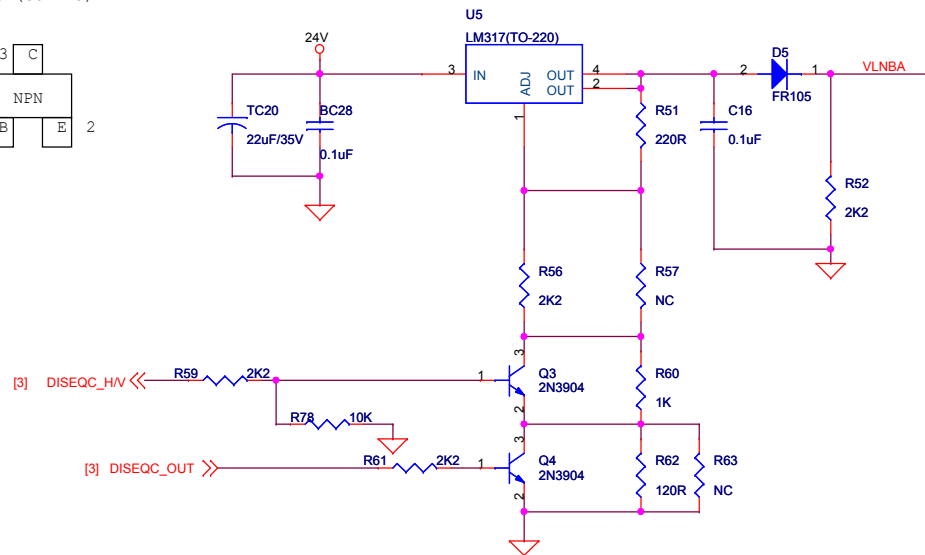
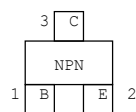
Title
AUDIO/VIDEO

Size B Document Number
M3328C CB

Rev
1.0

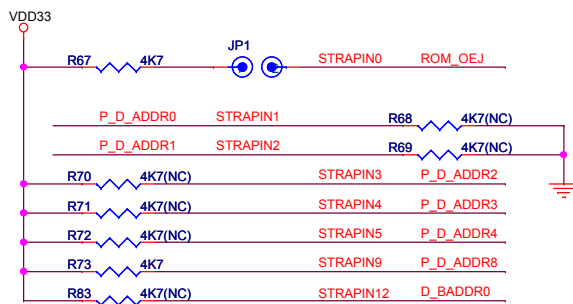
Date: Thursday, January 05, 2006 Sheet 5 of 8

2N3904 (SOT-23)



M3328c Hardware Config

P_D_ADDR[0..10] << P_D_ADDR[0..10] [3,4]
D_BADDR0 >> D_BADDR0 [4]
ROM_OEJ << ROM_OEJ [3,4]



1. CPU_PROBE_EN
STRAPIN[0]: ROM_OEJ
0: Disable (DEFAULT)
1: Enable

2. CPU_PLL_M
STRAPIN[3:1]: P_D_ADDR[2..0]
011: 216M (DEFAULT)
100: 180M
101: 154M

3. MEM_PLL_M
STRAPIN[6:4]: P_D_ADDR[5..3]
000: 135M (DEFAULT)
001: 120M
010: 98M
011: 108M

4. CHIP_MODE
STRAPIN[11:9]: [P_D_ADDR10:8]
000: Mode0 (Flash muxed 8-bit MODE) (DEFAULT)
001: Mode1 (Flash and GPIO muxed MODE)

5. CRYSTAL_SELECT
STRAPIN[12]: [P_D_BADDR0]
0: 27MHz (DEFAULT)
1: 13.5MHz

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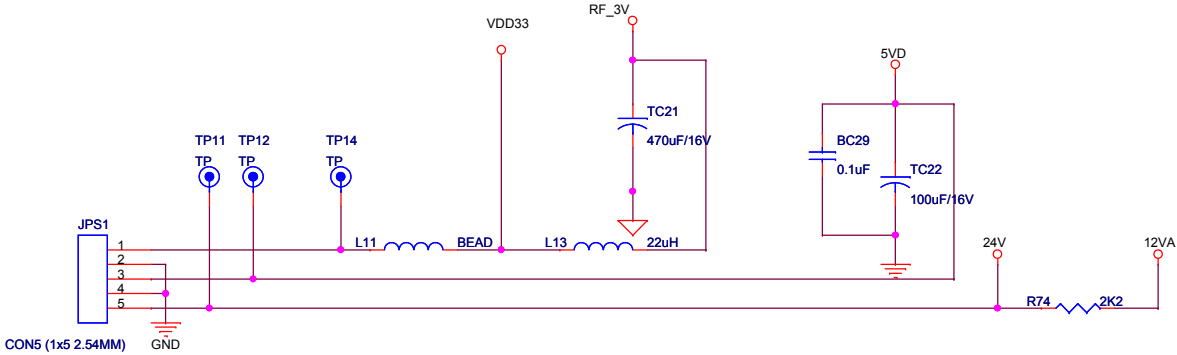
Title
TUNER

Size B Document Number
M3328C CB

Rev
1.0

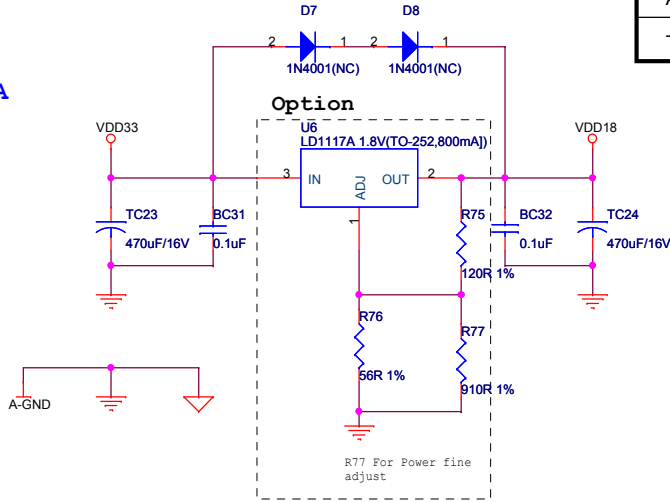
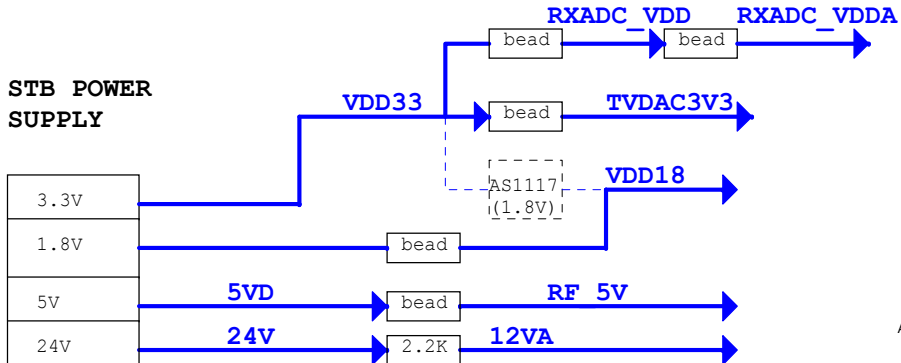
Date: Thursday, January 05, 2006 Sheet 6 of 8

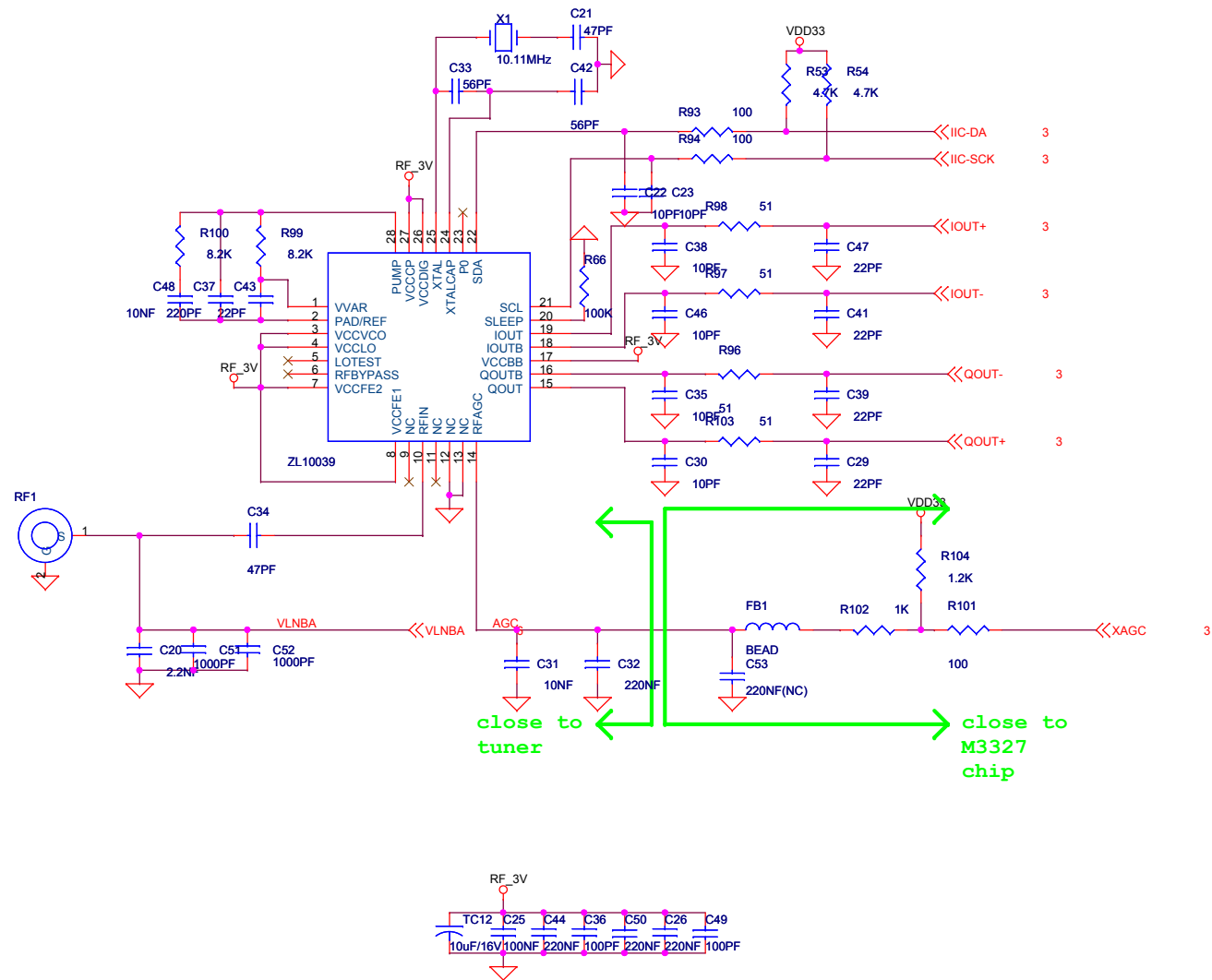
System Board Power Connector



VDD33	M3328C IO PART 3.3V
TVDAC3V3	M3328C VIDEO DAC 3.3V
RXADC_VDD	M3328C QPSK DIGITAL 3.3V
RXADC_VDDA	M3328C QPSK ANALOG 3.3V
VDD18	M3328C CORE 1.8V
5VD	DIGITAL 5V
RF_5V	TUNER POWER 5V
12VA	Audio OP POWER 12V
24V	LNB POWER 24V

GND	Digital GND
A-GND	ANALOG GND
TGND	TUNER RF GND





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Title		
ZL10039		
Size	Document Number	Rev
B	M3327 SB	1.0
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Sheet 8 of 8		