晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	**AM-240320LTNQW00H**
APPROVED BY	
DATE	

☐ **Approved For Specifications**
☑ **Approved For Specifications & Sample**

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2006/4/04	-	New Release	Jason
2006/4/7	9	Modify LED back light specifications	Jason
2006/4/7	13	Modify Block Diagram	Jason
2006/4/7	15	Modify Interface specifications	Jason
2006/4/7	48	Modify Outline Dimension	Jason
2006/5/2	-	Revised all T.B.D data.	Jason

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1. Features

LCD 2.4 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments. The LCD adopts one backlight with High brightness 4-lamps white LED.

(1) Construction: 2.4" a-Si color TFT-LCD with White LED Backlight and FPC.
(2) LCD : 2.1 Amorphous-TFT 2.4 inch display, transmissive, Normally white type, 12 o'clock.
2.2 240(RGB)X320 dots Matrix,1/320 Duty.
2.3 LCD controller is HX8312A.
2.4 Real 262K colors display:
Red-5bit, Green-6bit, Blue-5bit (MPU8/16 mode)
Red-6bit, Green-6bit, Blue-6bit (MPU9/18 mode)

(3) 16-bit high speed bus interface and high speed RAM-write function.
(4) Direct data display with display RAM.
LCD Internal RAM capacity: 172,800bytes.
(5) MPU interface: 8/16/18 bit parallel and16/18–bit Serial Bus Interface Timing.
(6) RGB interface: 16/18-bit RGB Interface Circuit Input.

2. Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 43.6 (W) x 85.5(H) x 4.34 (TMax.)	mm
Main LCD	Pixel pitch	0.153 (W) x 0.153(H)	mm
	Active area	36.72 (W) x 48.96 (H)	mm
	Viewing area(T/P)	39.9 (W) x 51.95 (H)	mm
Weight		Approx. 11.0	g

*1. This specification is about External shape on shipment from AMPIRE.

3. Absolute max. ratings and environment

3.1. Absolute max ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power Supply for Logic	VDD – GND	-0.3	+4.0	V	
Power Input Voltage	Vci	-0.3	+4.6	V	
Power Supply for LED backlight	LED A – LED K	-0.5	+3.6	V	
Input voltage	VIN	-0.5	VDD+0.5	V	

3.2. Environment

Item	Specifications	Remarks
Storage temperature	Max. +70°C Min. –30°C	Note 1: Non-condensing
Operating temperature	Max. +60°C Min. -20°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4. Electrical specifications

4.1. Electrical characteristics of LCD

(V_{DD}=2.8V, Ta=25 °C)

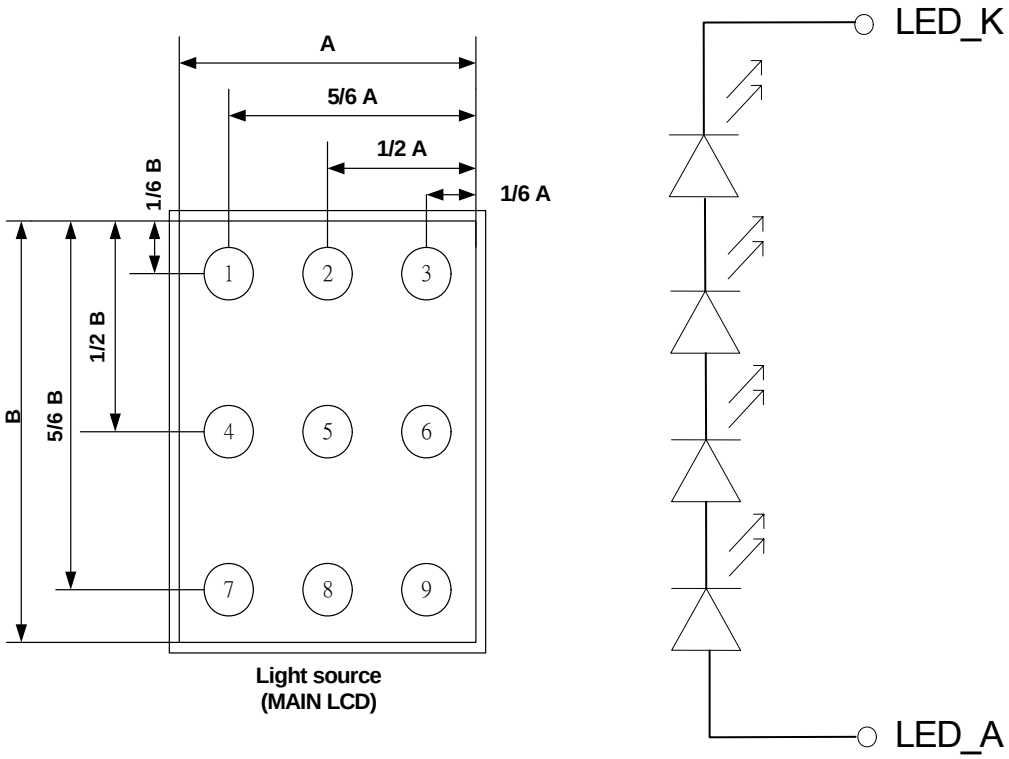
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.2	2.8	3.3	V
Power input voltage	Vci		2.5	-	3.3	V
High-level input voltage	V_{IHC}		$0.8V_{DD}$		V_{DD}	V
Low-level input voltage	V_{ILC}		0		$0.2V_{DD}$	V
Consumption current of VDD	I_{DD}		-	2.5	4	mA
Consumption current of LED	I_F	V_F=12.8V	-	20	-	mA

※ 1. 1/320 duty

4.2. LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =20mA	12.3	12.8	13.8	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	4-chip serial	-	20	-	mA
Power Consumption	P_{BL}	I_f =20mA	-	256	276	mW
Uniformity (with L/G)	-	I_f=20mA	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	12.8V 20mA	3200	-	-	cd/m^2
Luminous color	White					
Chip connection	4 chip serial connection					

LCM measure position:



*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5. Optical characteristics

5.1. Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

LED backlight transmissive module:

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	-	10	20	ms	θ =0°, φ =0° (Note 2)
	Tf	25°C	-	20	30		
Contrast ratio	CR	25°C	150	250	-	-	θ =0°, φ =0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	-	4.7	-	%	
Visual angle range front and rear	θ	25°C	(θ f) 15 (θ b) 35			De-gree	φ 1= 0°, φ = 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θ l)45 (θ r) 45			De-gree	φ 1= 0°, φ =90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			190	220	-	Cd/ m2	I_F=80mA, Full White pattern

5.2. CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

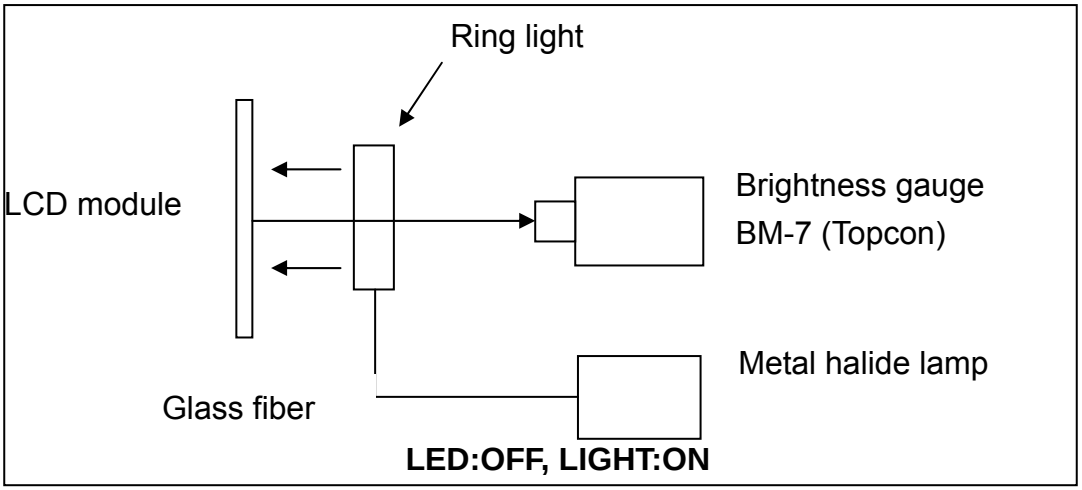
Main LCD: (1/320 Duty Ta = 25°C)

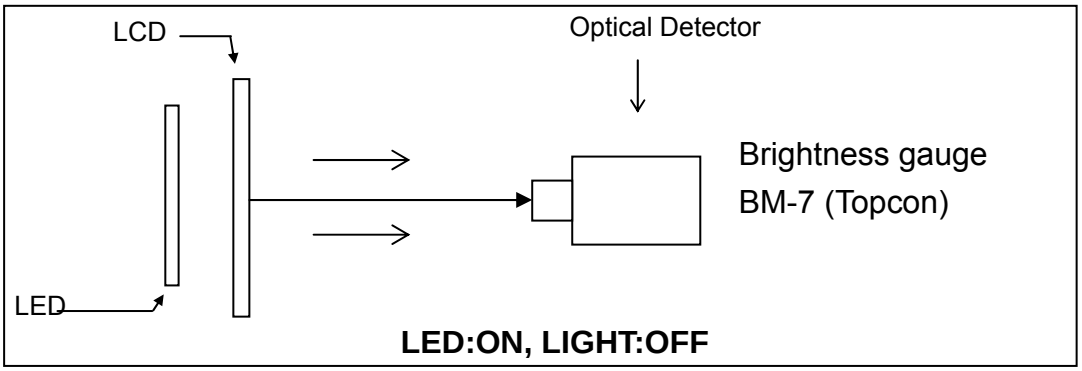
Item	Symbol	Transmissive			Conditions
		Min.	Std.	Max.	
Red	x	0.603	0.633	0.663	θ =0° , φ =0°
	y	0.299	0.329	0.359	
Green	x	0.264	0.294	0.324	θ =0° , φ =0°
	y	0.546	0.576	0.606	
Blue	x	0.103	0.133	0.163	θ =0° , φ =0°
	y	0.092	0.122	0.152	
White	x	0.278	0.308	0.338	θ =0° , φ =0°
	y	0.316	0.346	0.376	

Light source

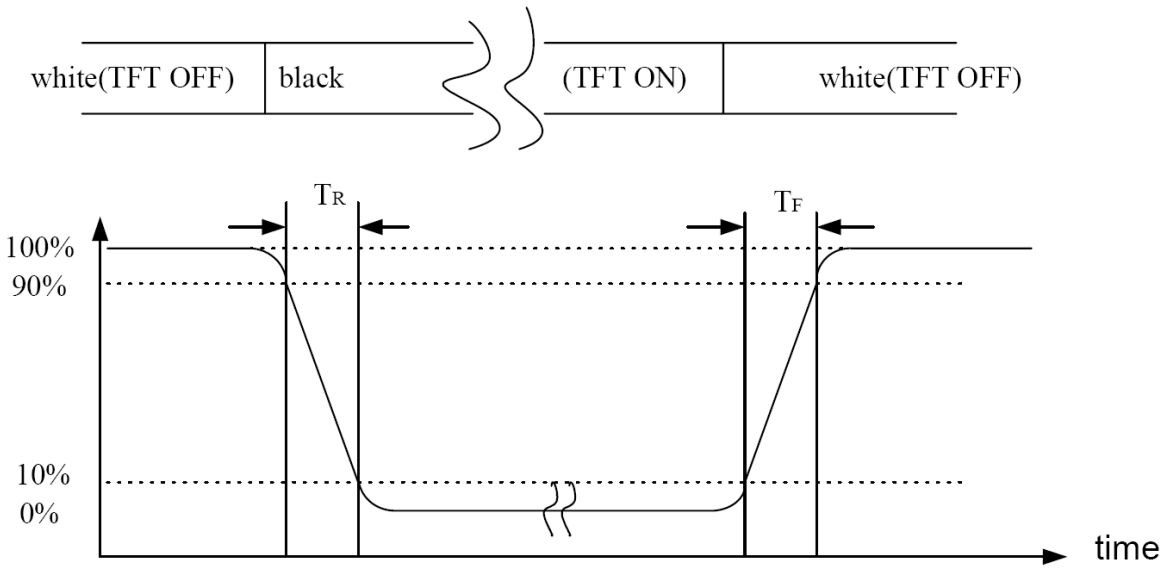
Item	Symbol	Value			Conditions
		Min.	Std.	Max.	
Light source	x	0.28	0.315	0.34	θ =0° , φ =0°
	y	0.28	0.305	0.34	
LED brightness		3200	-	-	Unit: cd/m^2 (I_F=80mA)

NOTE 1: Optical characteristic measurement system

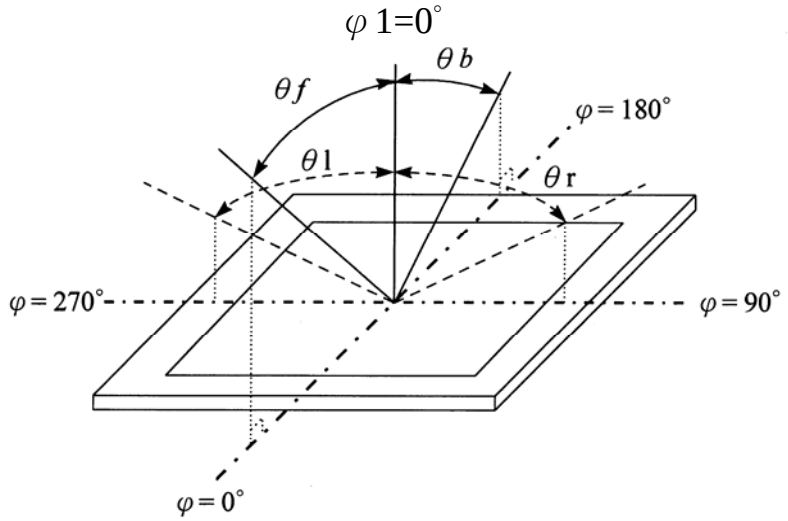




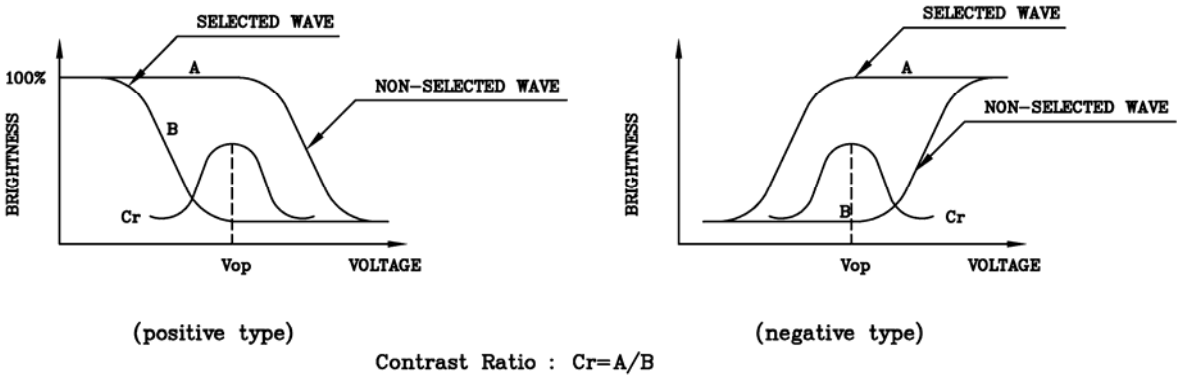
NOTE 2: Definition of Response Time : Sum of TR and TF



NOTE 3: φ 、θ definition

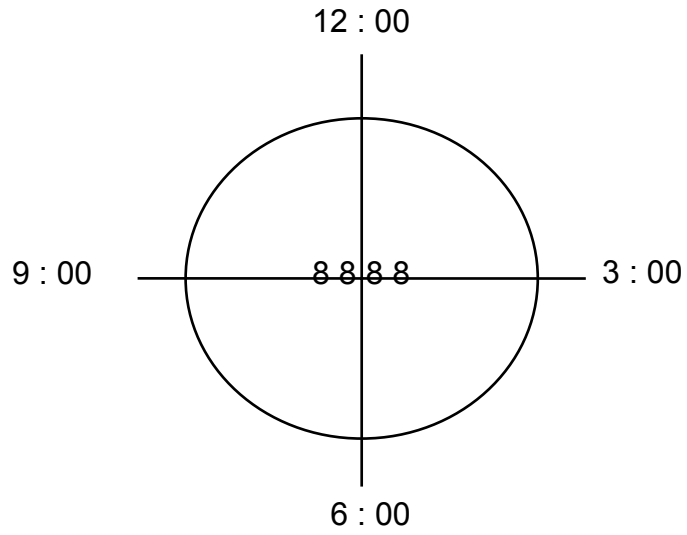


NOTE 4: Contrast definition



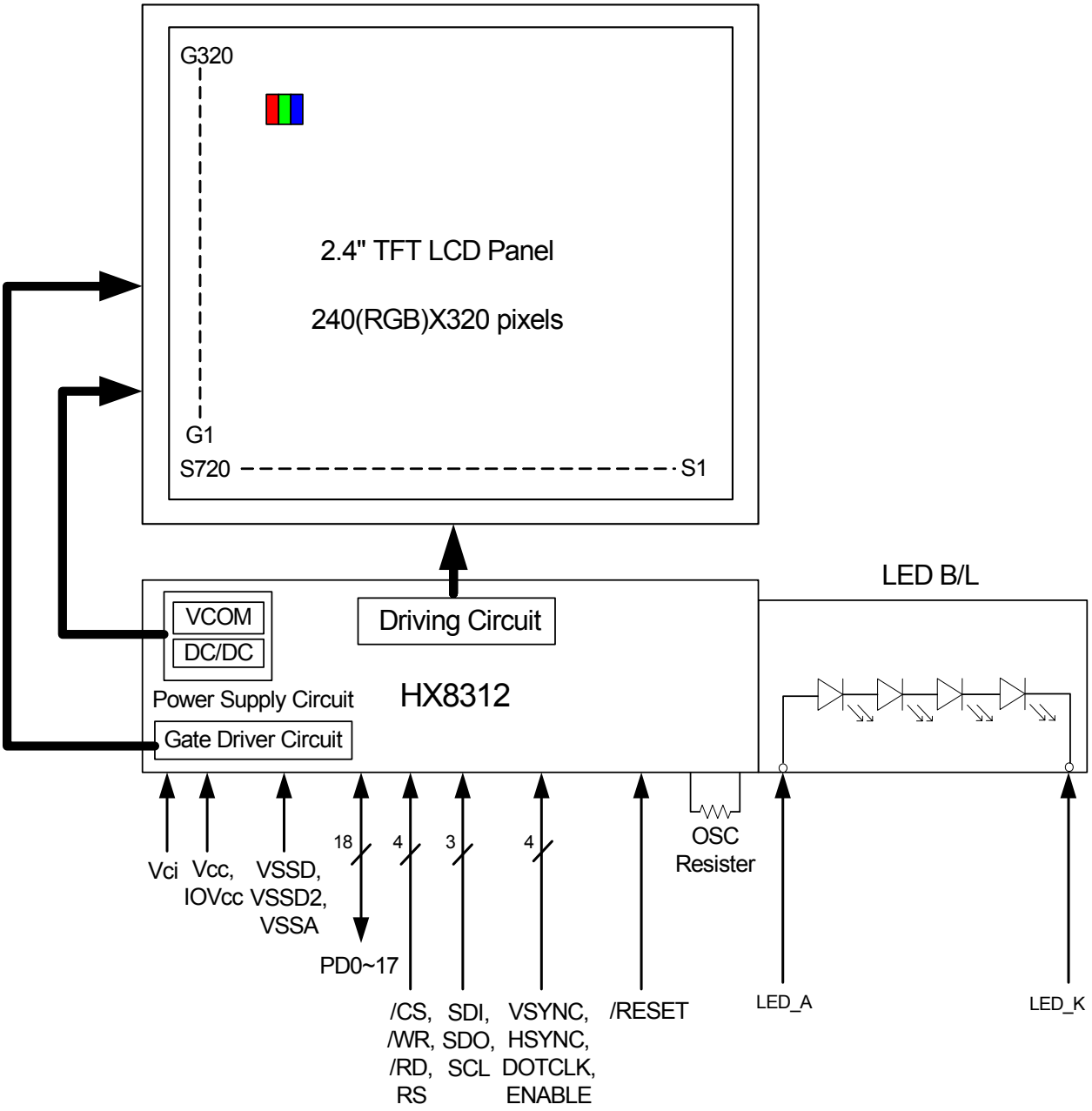
Contrast Ratio : Cr=A/B

NOTE 5: Visual angle direction priority



6. Block Diagram

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display mode: Normally white
Display composition: 240 x RGB x 320 pixels
LCD Driver : HX8312
Back light: White LED x 4 (I_F=20mA)



7. Interface specifications

Pin No.	Terminal	Functions
1	ENABLE	A data ENABLE signal in RGB I/F mode.
2	DOTCLK	Dot clock signal in RGB I/F mode.
3	HSYNC	Frame synchronizing signal in RGB I/F mode.
4	VSYNC	Frame synchronizing signal in RGB I/F mode.
5	/CS	Chip select signal.
6	SCL	Serial bus interface clock input pin.
7	SDI	Serial bus interface data input pin.
8	RS	Command/display Data Selection.
9	/WR	Write enable signal.
10	/RD	Read enable signal.
11	/RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.
12	PD0	18-bits Interface Circuit
13	PD1	
14	PD2	
15	PD3	
16	PD4	
17	PD5	
18	PD6	
19	PD7	
20	PD8	
21	PD9	
22	PD10	
23	PD11	
24	PD12	
25	PD13	
26	PD14	
27	PD15	
28	PD16	
29	PD17	

(To be continue)

30	VDD	Power supply for the internal logic circuit. (VCC=2.2~3.3V)
31	VCI	Power supply for Step-up circuit. (VCi=2.5~3.3V)
32	VCI	
33	NC	NC
34	NC	
35	NC	
36	NC	
37	NC	
38	BWS2	Selection the RGB interface mode. L:18-bit, H: 16-bit
39	BWS1	Selection the Serial bus interface mode. L:18-bit, H: 16-bit
40	GND	GND-terminal
41	NC	NC
42	NC	
43	NC	
44	NC	
45	GND	GND-terminal
46	SDO	Serial bus interface data output pin.
47	NC	NC
48	NC	
49	NC	
50	GND	GND-terminal
51	GND	

Selection the System Interface mode

Interface type	for FPCB Circuit on JP1~JP3			for FPCB Circuit on Interface	
	PSX (JP1)	DTX2 (JP2)	BSW0 (JP3)	BSW1	BSW2
MPU1 (18Bit)	L	L	L	L	RGB Type
MPU4 (16Bit)	L	L	L	H	L:18 Bit H:16 Bit
MPU7 (8Bit)	L	H	H	H	
MPU8 (Serial 18Bit)	H	L	H	L	
MPU9 (Serial 16Bit)	H	L	H	H	

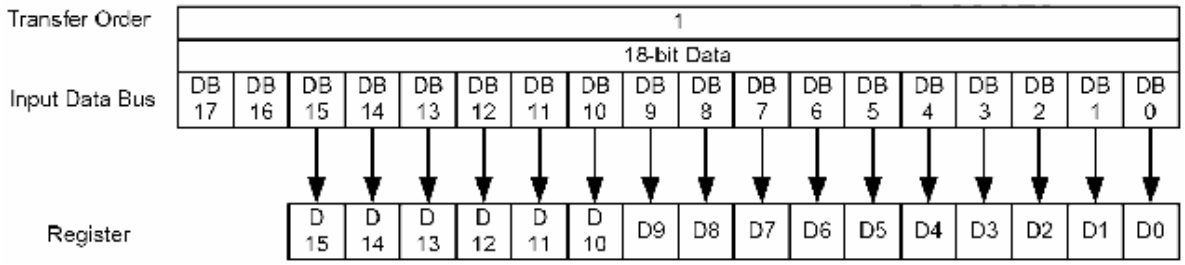
Jumper Default: JP[1:3]= “L”

8. System interface

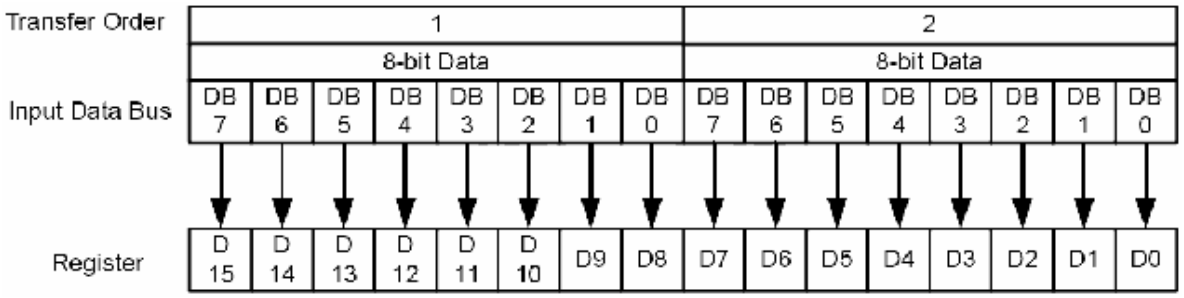
8.1. Relation between Register Command Data Format and Input Bus

The RS pin specifies whether the access is to the register command or to the display data RAM. The input data for register command is consist of 16 bits. The upper 8 bits (D15-8) are address and the lower 8 bits (D7-0) are data.

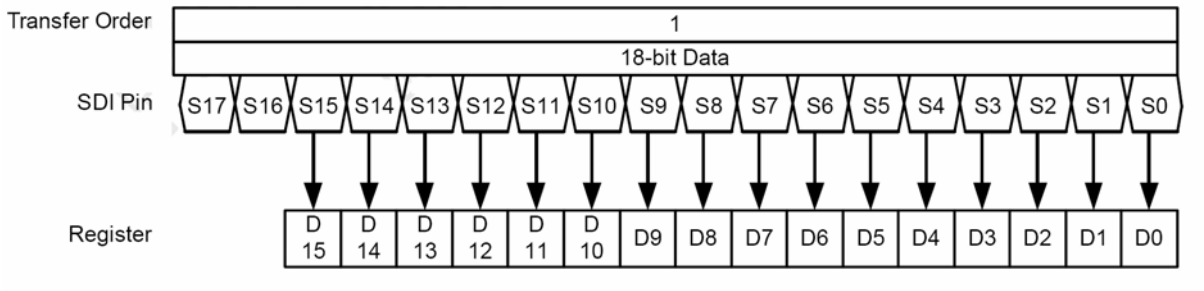
MPU1、4 Type



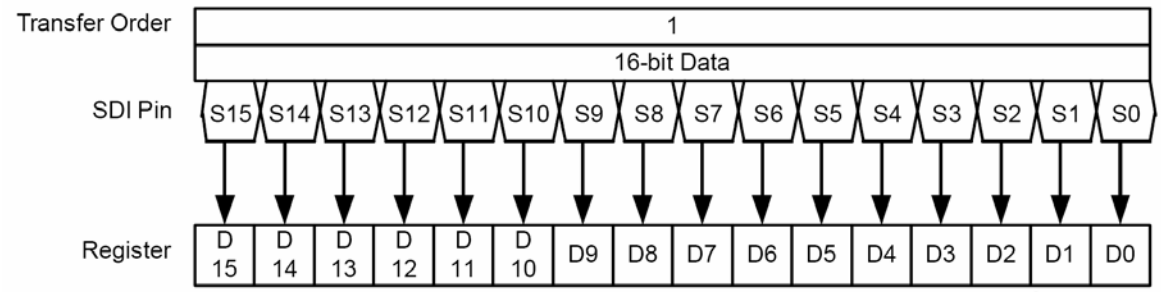
MPU7 Type



MPU8 Type

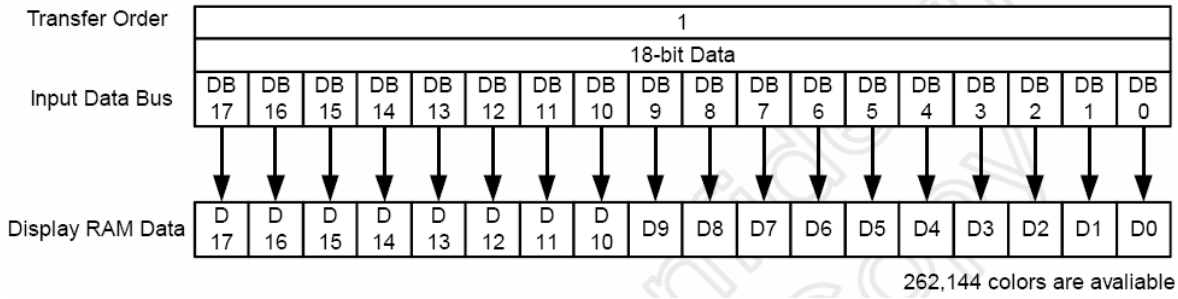


MPU9 Type



8.2. Relation between Display RAM Data Format and Input Bus in System Interface

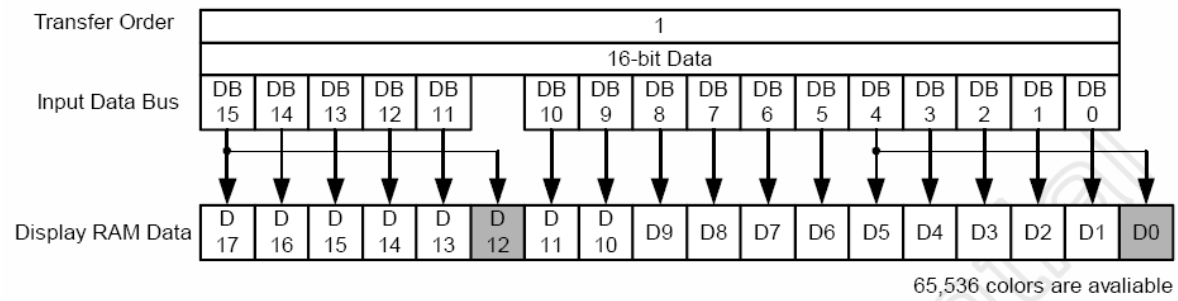
Data format for MPU1 Type



Data format for 18-bit Bus interface

Data format for MPU4 Type

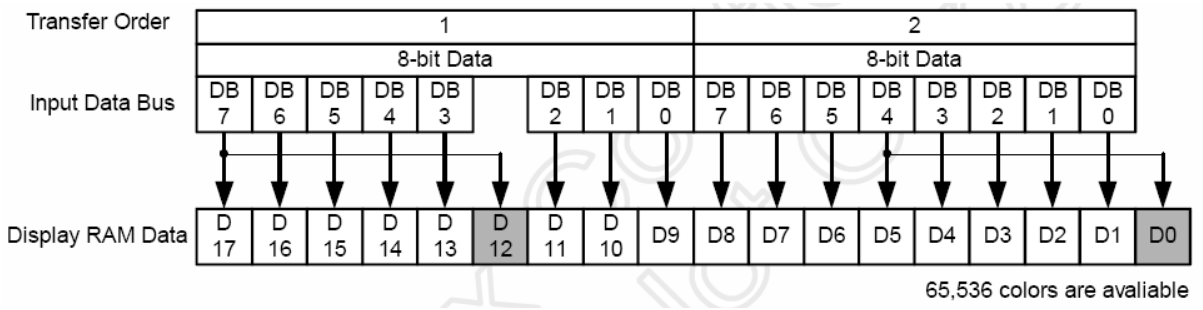
In the MPU4 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from DB15 and D0 of the display data RAM is compensated by the data from DB4 in the transfer.



Data format for 16-bit Bus interface

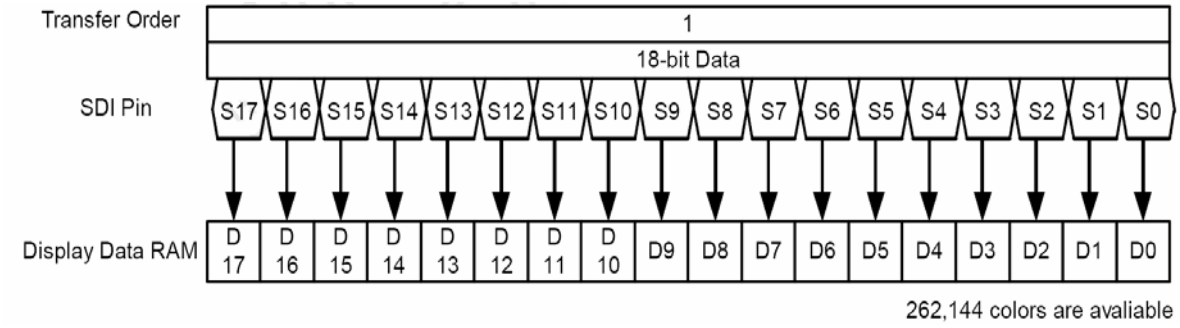
Data format for MPU8 Type

In the MPU7 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from DB7 in the first transfer and D0 of the display data RAM is compensated by the data from DB4 in the second transfer.



Data format for 8-bit Bus interface

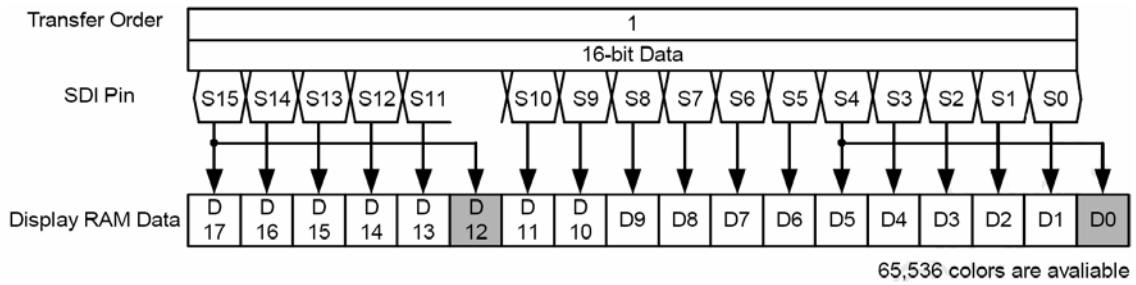
Data format for MPU8 Type



Data format for 18-bit serial interface

Data format for MPU9 Type

In the MPU9 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from S15 and D0 of the display data RAM is compensated by the data from S4 in the transfer.



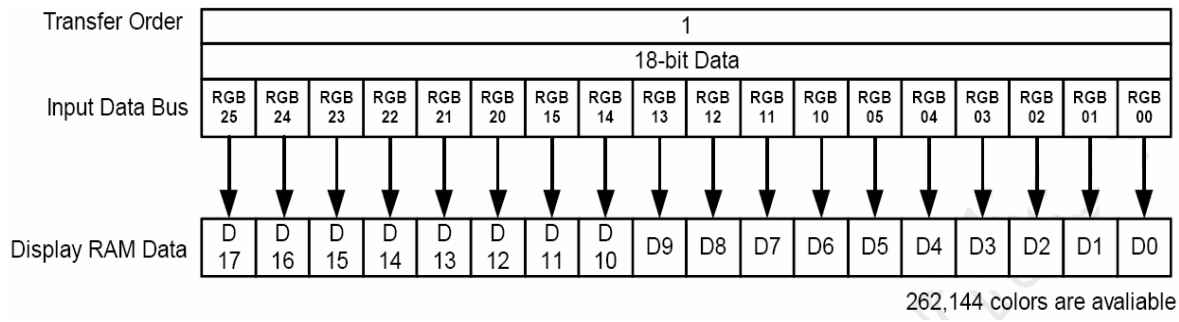
Data format for 16-bit serial interface

8.3. RGB interface

Relation between Display RAM Data Format and Input Bus

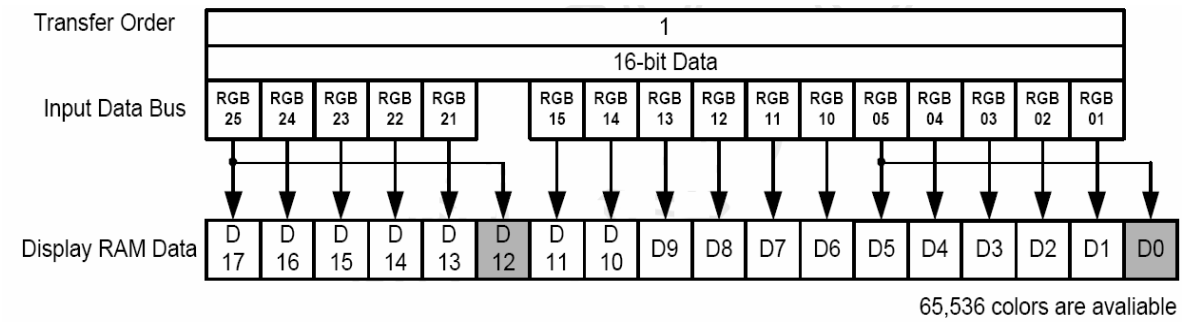
The following shows the relation between display RAM data allocation and input data bus in different RGB type input data format.

18 Bit Type



16 Bit Type

In the RGB2 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from RGB23 and RGB04 of the display data RAM is compensated by the data from DB4 in the transfer.



8.4. Display RAM Address

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---------	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
	17---------0			17---------0			17---------0			---------	17---------0			17---------0			17---------0			17---------0		
G1	0000h			0001h			0002h			---------	00ECh			00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			---------	01ECh			01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			---------	02ECh			02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			---------	03ECh			03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			---------	04ECh			04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			---------	05ECh			05EDh			05EEh			05EFh		
G7	0600h			0601h			0602h			---------	06ECh			06EDh			06EEh			06EFh		
G8	0700h			0701h			0702h			---------	07ECh			07EDh			07EEh			07EFh		
G9	0800h			0801h			0802h			---------	08ECh			08EDh			08EEh			08EFh		
G10	0900h			0901h			0902h			---------	09ECh			09EDh			09EEh			09EFh		
G11	0A00h			0A01h			0A02h			---------	0AECh			0AEDh			0AEEh			0AEFh		
G12	0B00h			0B01h			0B02h			---------	0BECh			0BEDh			0BEEh			0BEFh		
G13	0C00h			0C01h			0C02h			---------	0CECh			0CEDh			0CEEh			0CEFh		
G14	0D00h			0D01h			0D01h				0DECh			0DEDh			0DEEh			0DEFh		
G15	0E00h			0E01h			0E01h				0EECh			0EEDh			0EEEh			0EEFh		
⋮	⋮			⋮			⋮			---------	⋮			⋮			⋮			⋮		
G231	13600h			13601h			13602h			---------	136ECh			136EDh			136EEh			136EFh		
G232	13700h			13701h			13702h			---------	137ECh			137EDh			137EEh			137EFh		
G233	13800h			13801h			13802h			---------	138ECh			138EDh			138EEh			138EFh		
G234	13900h			13901h			13902h			---------	139ECh			139EDh			139EEh			139EFh		
G235	13A00h			13A01h			13A02h			---------	13AECh			13AEDh			13AEEh			13AEFh		
G236	13B00h			13B01h			13B02h			---------	13BECh			13BEDh			13BEEh			13BEFh		
G237	13C00h			13C01h			13C02h			---------	13CECh			13CEDh			13CEEh			13CEFh		
G238	13D00h			13D01h			13D02h			---------	13DECh			13DEDh			13DEEh			13DEFh		
G239	13E00h			13E01h			13E02h			---------	13EECh			13EEDh			13EEEh			13EEFh		
G240	13F00h			13F01h			13F02h			---------	13FECh			13FEDh			13FEEh			13FEFh		

Display RAM Address and Display Panel Position (X Size = 240, ADX = 0)

9. INSTRUCTION DESCRIPTIONS

9.1. Register Description (Driver IC: HX8312)

Register	Bit	Symbol	Function	Configuration
	Control register 1			
R0 (R00h) default "A0"h	D7	DISP1	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
	D6	DISP0	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
	D5	ADC	Specifies source output and display RAM address mapping .	Refer to 4.1 "Relation between the Display RAM Address and the Source Output Channel"
	D4	DTY	Specifies partial display mode.	"0" : Normal display mode. "1" : Partial display mode. Refer to "5. Partial Display Mode".
	D3	STBY	Specifies stand-by mode.	"0" : Normal operation. "1" : Stand-by mode.
	D2	COLOR	Specifies color mode.	"0" : 262,144 color mode. "1" : 8 color mode. Refer to "9 8-color Display Mode".
	D1	-	-	-
	D0	GSM	Gate scan selection in partial-off display areas.	"0" : Normal scan in non-display area "1" : Configures the scanning cycle in non-display area by the number of the R52 register.
	Control register 2			
R1 (R01h) default "00"h	D7	ADX	RAM X address increment direction after one write or read operation .	"0" : From X0 to X239 Refer to "4.2. Display RAM Access" "1" : From X239 to X0 *Note : ADX = "1" setting is prohibited when RGB interface circuit is in use.
	D6	ADR	RAM Y address increment direction after one write or read operation .	"0" : Y0 to Y319 Refer to "4.2. Display RAM Access" "1" : Y319 to Y0 *Note : ADR = "1" setting is prohibited when RGB interface circuit is in use.
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	LTS	Specifies setting period of calibration.	"0" : 1line period = tcal "1" : 1 line period = tcal x 2 Refer to "3.3 Internal Clock Mode".
	D0	OSCSTBY	Oscillation control.	"0" : Starts oscillation. "1" : Stops oscillation.
	RGB interface register 2			
R2 (R02h) default "00"h	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	VMODE	Vsync interface selection.	"0" : Normal Refer to "Table 9-1". "1" : Uses Vsync interface.
	D3	WNRGB	RGB interface writing mode selection.	"0" : Requires 1 frame data. "1" : Requires data only for the window area. Refer to "9.1.6 Restriction when using the RGB interface circuit".
	D2	RGBS	RGB interface writing mode selection.	"0" : Capture mode. Refer to "Table 9-1". "1" : Through mode.
	D1	DISPCK	Specifies display timing at RGB interface circuit.	"0" : Internally synchronized display mode by SYSCLK. "1" : Externally synchronized display mode by Vsync and Hsync. Refer to "Table 9-1".
	D0	NWRGB	RGB interface pin control.	"0" : Writes to the display data RAM via the system interface circuit. "1" : Writes to the display data RAM via the RGB interface circuit. Refer to "Table 9-1".

R3 (R03h) default "00"h	**Reset register 1**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	RES	Reset command for the HX8312A	"0" : Normal operation. "1" : Reset Operation.
R5 (R05h) default "00"h	**RAM access control register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	WAS	Specifies window area access mode.	"0" : Normal writing mode. "1" : Window area access mode. Refer to "4.3. Window Area Access Mode".
	D3	-		
	D2	AM	Specifies the address increment direction.	"0" : X address increment, then Y address increment. "1" : Y address increment, then X address increment, *Note: This setting is invalid when RGB interface circuit is in use. Refer to "4.2. Access to the Display Data RAM".
	D1	-	-	-
	D0	-	-	-
R6 (R06h) default "00"h	**Data reverse register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	REV	Reverse the source output data voltage	"0": Data "0000"h; Source output: V63 at VCOML "1": Data "0000"h; Source output V0 at VCOML
R13 (R0Dh) default "00"h	**Display size control register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	NSO1	Specify source output size.	Refer to "4.1 Relation between the Display RAM Address and the Source Output Channel".
	D1	NSO0		
	D0	-	-	-
R14 (R0Eh) default "00"h	**Partial non-display area color register 1**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	PSEL	Specifies the color of the partial non-display area	"0" : Displays the color specified in the R15 register. "1" : Displays the most significant bit of the display RAM data. Refer to "5.2 Display Color Selection and Gate Scan Method in Partial Non-Display Areas".

R15 (“0F“h) default “00“h	Partial non-display area color register 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	PGR	Specifies display data for pixel R.	"0" : Displays "0". "1" : Displays "1".
	D1	PGG	Specifies display data for pixel G.	"0" : Displays "0". "1" : Displays "1".
	D0	PGB	Specifies display data for pixel B.	"0" : Displays "0". "1" : Displays "1".
R16 (R10h) default “00“h	First display window area starting register 1 , 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P1SL8	Specify the starting line number of the first display window area.	Set within the range of "000"h - "13F"h.
R17 (R11h) default “00“h	D7	P1SL7		
	D6	P1SL6		
	D5	P1SL5		
	D4	P1SL4		
	D3	P1SL3		
	D2	P1SL2		
	D1	P1SL1		
	D0	P1SL0		
R18 (R12h) default “00“h	Second display window area starting register 1 , 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P2SL8	Specify the starting line number of the second display window area.	Set within the range of "000"h - "13F"h.
R19 (R13h) default “00“h	D7	P2SL7		
	D6	P2SL6		
	D5	P2SL5		
	D4	P2SL4		
	D3	P2SL3		
	D2	P2SL2		
	D1	P2SL1		
	D0	P2SL0		
R20 (R14h) default “00“h	First display window area display line number 1 , 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P1AW8	Specify the display line number of the first display window area.	Set within the range of "001"h - "140"h.
R21 (R15h) default “00“h	D7	P1AW7		
	D6	P1AW6		
	D5	P1AW5		
	D4	P1AW4		
	D3	P1AW3		
	D2	P1AW2		
	D1	P1AW1		
	D0	P1AW0		

R22 (R16h) default "00"h	**Second display window area display line number 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P2AW8	Specify the display line number of the second display window area.	Set within the range of 000"h - "13F"h.
R23 (R17h) default "00"h	D7	P2AW7		
	D6	P2AW6		
	D5	P2AW5		
	D4	P2AW4		
	D3	P2AW3		
	D2	P2AW2		
	D1	P2AW1		
	D0	P2AW0		
R24 (R18h) default "00"h	**Power Supply System Control Register 1**			
	D7	VR2ON	Controls the VR2 regulator.	"0" : VR2 regulator off. "1" : VR2 regulator on.
	D6	VR1ON	Controls the VR1 regulator.	"0" : VR1 regulator off. "1" : VR1 regulator on.
	D5	VCLON	Controls the step-up circuit 3 for VCL..	"0" : VCL step-up circuit off. "1" : VCL step-up circuit on.
	D4	VGON	Controls the step-up circuit 2.	"0" : Step-up circuit 2 off. "1" : Step up circuit 2 on.
	D3			
	D2	DDVDHON	Controls the step-up circuit 1 for DDVDH.	"0" : DDVDH step-up circuit off. "1" : DDVDH step-up circuit on.
	D1			
	D0	DCON	Controls the DC/DC converter.	"0" : DC/DC converter off. "1" : DC/DC converter on.
R25 (R19h) default "00"h	**Power Supply System Control Register 2**			
	D7	VR2SEL2	Specify the output voltage of the VR2 regulator.	-
	D6	VR2SEL1		
	D5	VR2SEL0		
	D4	VR1SEL2	Specify the output voltage of the VR1 regulator.	-
	D3	VR1SEL1		
	D2	VR1SEL0		
	D1	-	-	-
	D0	-	-	-
R26 (R1Ah) default "05"h	**Power Supply System Control Register 3**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	FS3	Specify the step-up circuit 2and 3 frequency	-
	D2	FS2		
	D1	FS1	Specify the step-up circuit 1 frequency	-
	D0	FS0		
R27 (R1Bh) default "0A"h	**Power Supply System Control Register 4**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	VSEL2	Specify the output voltage of the VS and VDH regulator.	-
	D2	VSEL1		
	D1	VSEL0		
	D0	RGON	Controls the VS and VDH regulator.	"0" : VS and VDH regulator off. "1" : VS and VDH regulator on.

R28 (R1Ch) **default "33"h**	**Power Supply System Control Register 5**			
	D7	-	-	-
	D6	SAP2	Source driver circuit operating current control	(SAP2, SAP1, SAP0) = "000": Halt (SAP2, SAP1, SAP0) = "001": 0.5(fixed) (SAP2, SAP1, SAP0) = "010": 0.75(fixed) (SAP2, SAP1, SAP0) = "011": 1.0(fixed) (SAP2, SAP1, SAP0) = "100": 1.25(fixed) (SAP2, SAP1, SAP0) = "101": 1.5(fixed) (SAP2, SAP1, SAP0) = "110": 1.5(fixed) (SAP2, SAP1, SAP0) = "111": Setting disable
	D5	SAP1		
	D4	SAP0		
	D3	-	-	-
	D2	AP2	Step-up circuit operating current control	(AP2, AP1, AP0) = "000": Halt (AP2, AP1, AP0) = "001": Setting disable (AP2, AP1, AP0) = "010": 0.5(fixed) (AP2, AP1, AP0) = "011": 0.75(fixed) (AP2, AP1, AP0) = "100": 1.0(fixed) (AP2, AP1, AP0) = "101": 1.25(fixed) (AP2, AP1, AP0) = "110": 1.5(fixed) (AP2, AP1, AP0) = "111": Setting disable
	D1	AP1		
	D0	AP0		
R29 (R1Dh) **default "03"h**	**Power Supply System Control Register 6**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	R/L	Specifies the gate scan direction.	-
	D2	SCN2	Specify gate scan mode.	(SCN2, SCN1, SCN0) = "XX0" : MODE5 (SCN2, SCN1, SCN0) = "011" : MODE2
	D1	SCN1		
	D0	SCN0		
R30 (R1Eh) **default "00"h**	**Power Supply System Control Register 8**			
	D7	VCOMEN	Specify the VCOM1 operation.	-
	D6			
	D5	VCOMFX		
	D4	VCOMHI		
	D3	XVCOMG	VCOML output control	"0": VCOML is setting by VDV and VCM bits "1": VCOML = VSSA
	D2	-	-	-
	D1	-	-	-
	D0	DDVDHXON	Specifies whether to use or not to use the extra step-up circuit 1 for DDVDH.	"0" : Doesn't use the extra step-up circuit 1. "1" : Uses the extra step-up circuit 1.
R31 (R1Fh) **default "00"h**	**Power Supply System Control Register 9**			
	D7	-	Specify the VCOM amplitude.	-
	D6	-		
	D5	-		
	D4	VDV4		
	D3	VDV3		
	D2	VDV2		
	D1	VDV1		
	D0	VDV0		
R32 (R20h) **default "00"h**	**Power Supply System Control Register 10**			
	D7	-	Specify the VCOMH voltage level	-
	D6	-		
	D5	-		
	D4	VCM4		
	D3	VCM3		
	D2	VCM2		
	D1	VCM1		
	D0	VCM0		

	ID code register 1			
R49 (R31h)	D7	MCOD3	Manufacturer code.	-
	D6	MCOD2		
	D5	MCOD1		
	D4	MCOD0		
default "10"h	D3	VCOD3	The version of this LSI.	Depends on the version of the product.
	D2	VCOD2		
	D1	VCOD1		
	D0	VCOD0		
	-	-	-	**ID code register 2**
R50 (R32h)	D7	DCOD7	Device code of this LSI.	-
	D6	DCOD6		
	D5	DCOD5		
	D4	DCOD4		
default "03"h	D3	DCOD3		
	D2	DCOD2		
	D1	DCOD1		
	D0	DCOD0		
	D7	**N line inversion register**		
R51 (R33h)	D6	NLINE6	Specify the number of lines for N line inversion.	Set within the range of "01"h - "78"h. Refer to "7 Gate Line Driving Function".
	D5	NLINE5		
	D4	NLINE4		
	D3	NLINE3		
default "01"h	D2	NLINE2		
	D1	NLINE1		
	D0	NLINE0		
	Partial gate register 1			
R52 (R34h)	D7	GSMLN7	Specify the gate scanning cycle of the non-display area	"00"h : Doesn't scan the partial non-display area. "01"h : Scans the partial non-display area every frame. "02"h : Scans the partial non-display area every two frames.
	D6	GSMLN6		
	D5	GSMLN5		
	D4	GSMLN4		
default "01"h	D3	GSMLN3		
	D2	GSMLN2		
	D1	GSMLN1		
	D0	GSMLN0		
	Partial gate register 2			
R53 (R35h)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	PNFRM	Configures the driving method of the partial non-display area.	"0" : The partial non-display area is driven as that in the partial display area. "1" : The partial non-display area is driven by the frame inversion.
	Gate scan selection register			
R55 (R37h)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	
default "00"h	D2	GSCAN2	Select the method of gate scanning.	-
	D1	GSCAN1		
	D0	GSCAN0		
	Gate output control register			
R59 (R3Bh)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	DISPTMG	Controls the gate output	"0" : Fix all gate outputs to VGL level. "1" : Gate scanning normal operation.

Gamma control register 12				
R154 (R9Ah) default “00“h	D7	-	Gamma adjustment register	-
	D6	-		
	D5	-		
	D4	ON14		
	D3	ON13		
	D2	ON12		
	D1	ON11		
	D0	ON10		
Extend mode register				
R157 (R9Dh) default “00“h	D7	-	-	-
	D6	-	-	-
	D5	MON_EN	Specify the V0 and V63 monitor function	“0”: V0 and V63 output monitor is disable. “1”: V0 and V63 output monitor is enable.
	D4	MON_SEL	V0 and V63 monitor selection	“0”: V0 outputs at DS1 pin. “1”: V63 outputs at DS1 pin
	D3	-	-	-
	D2	BPEN	Specify the Enable operation	“0”: Enable control is available. “1”: VBP/HBP control is enable
	D1	EPL	Specify the Enable polarity	“0”: High active “1”: Low active
	D0	MSBF	NWRGB (R2:D0)="1"	"0" : 18-bit x 1transfer (BWS2="L"). RGB interface type "0" : 16-bit x 1transfer (BWS2="H"). RGB interface type "1" : 6-bit x 3 transfer (BWS2=x). RGB interface type
			NWRGB (R2:D0)="0"	"0" : MPU5 mode A (use lower 6bits). MPU interface type "1" : MPU5 mode B (use upper 6bits). MPU interface type This bit is invalid in other modes.
Off mode register				
R192 (“C0“h) default “00“h	D7	OFFMOD	Specify the Off mode	“0”: Normal mode “1”: Off mode In off mode, only OFFMOD bit can be updated. Other register and the display RAM can not be updated. The display RAM data may not be retained in off mode, and need to rewrite after off mode canceling.
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	-	-	-

9.2. Set up Sequence

Power On Sequence

Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
VCC, VCI, IOVCC On										
R1	"xx" h	x	x	0	0	0	0	x	0	Start oscillation.
R0	"xx" h	x	x	x	x	0	x	0	x	Stand by mode cancel.
R3	"01" h	0	0	0	0	0	0	0	1	Software reset operation.
Wait for 10ms										
R3	"00" h	0	0	0	0	0	0	0	0	Software reset cancel.
R43	"0x" h	0	0	0	0	x	x	x	x	Oscillation frequency adjust.
R40	"xx" h	x	x	x	x	x	x	x	x	DCDCf setting.
R26	"0x" h	0	0	0	0	x	x	x	x	Step up circuit frequency setting.
R37	"0x" h	0	0	0	0	x	x	x	x	Step up circuit 2 factor setting.
R28	"3x" h	0	0	1	1	0	x	x	x	Set the step-up circuit operating current.
R30	"0x" h	0	0	0	0	x	0	0	1	Set extra CP1 available.
R25	"xx" h	x	x	x	x	x	x	0	0	Set the VR1, VR2 regulator to fit to LCD module.
R24	"C1" h	1	1	0	0	0	0	0	1	Set VR1 and VR2 regulator on.
Wait for 10ms										
R24	"E1" h	1	1	1	0	0	0	0	1	VCL turn on.
R24	"F1" h	1	1	1	1	0	1	0	1	VGH / VGL turn on.
Wait for 60ms										
R24	"F5" h	1	1	1	1	0	1	0	1	DDVDH turn on.
Wait for 60ms										
R27	"0x" h	0	0	0	0	x	x	x	1	VS / VDH set and VS / VDH turn on.
Wait for 10ms										
R32	"xx" h	0	0	0	x	x	x	x	x	Set VCOMH voltage.
R31	"xx" h	0	0	0	x	x	x	x	x	Set VCOM amplitude.
R30	"8x" h	1	0	0	0	x	0	0	1	VCOM start
Wait for 10ms										

Power Off Sequence

Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
R30	"0x" h	0	0	0	0	x	0	0	1	VCOM stop
R27	"0x" h	0	0	0	0	x	x	x	0	VS / VDH turn off.
R24	"C0" h	1	1	0	0	0	0	0	0	CP1, CP2, CP3 turn off.
Wait for 10ms										
R24	"00" h	0	0	0	0	0	0	0	0	VR1 / VR2 Off.
R28	"30" h	0	0	1	1	0	0	0	0	Step up circuit operating current stop.
VCC, VCI, IOVCC Off										

Display On Sequence

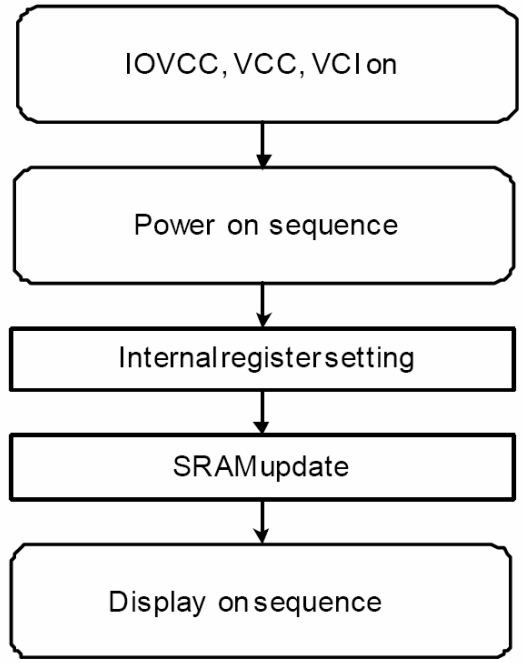
Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
R0	“xx” h	1	0	x	x	0	x	0	x	White display mode setting.
Wait for 2 frame scan										
R59	“00” h	0	0	0	0	0	0	0	0	Gate scan stop.

Display Off Sequence

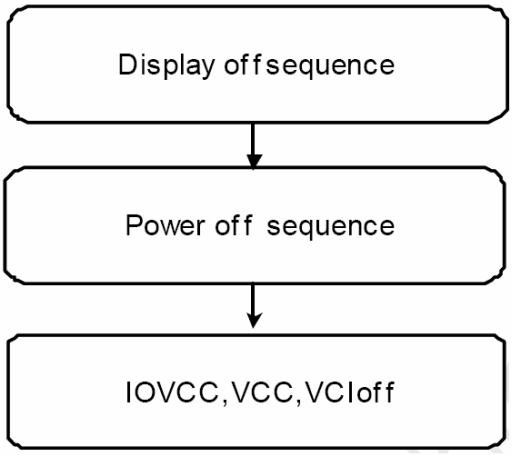
Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
R0	“xx” h	1	0	x	x	0	x	0	x	White display mode setting.
Wait for 2 frame scan										
R59	“00” h	0	0	0	0	0	0	0	0	Gate scan stop.

9.3. Operation Sequence

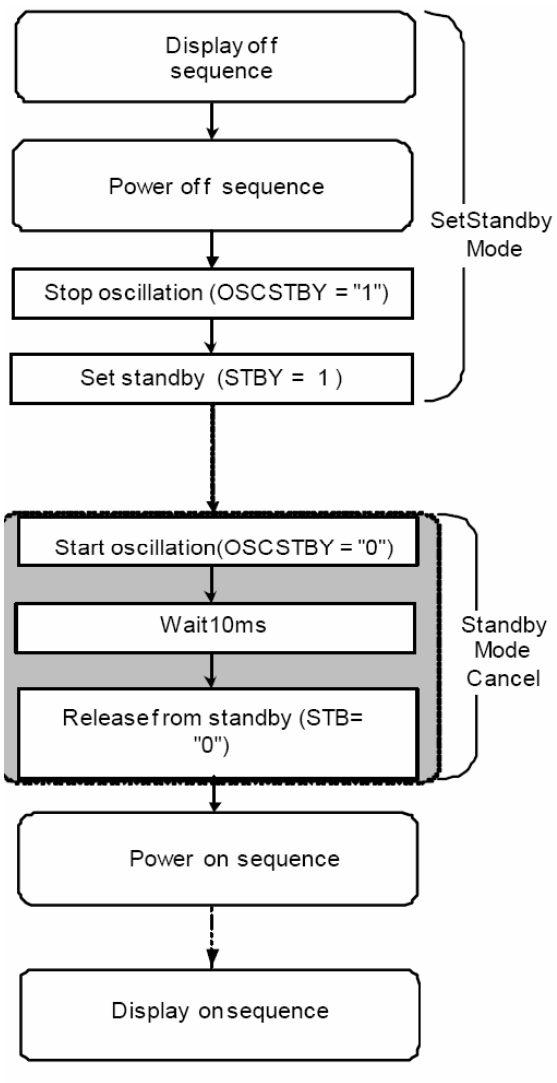
Norma Display On Sequence

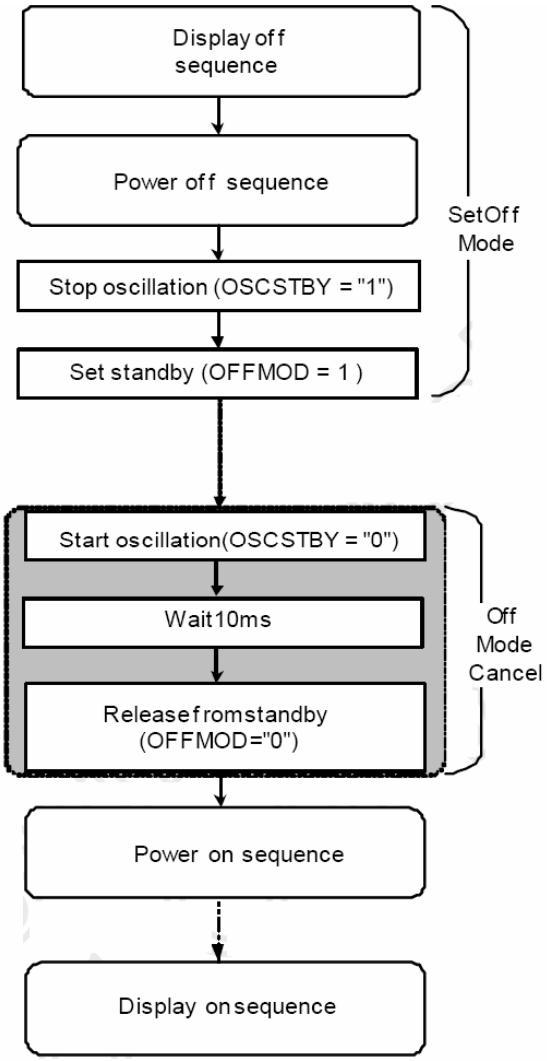


Norma Display Off Sequence



Standby Mode **Off Mode**


Display off sequence
Power off sequence
Stop oscillation (OSCSTBY = "1")
Set standby (STBY = 1)
Set Standby Mode
Start oscillation(OSCSTBY = "0")
Wait10ms
Release from standby (STB= "0")
Standby Mode Cancel
Power on sequence
Display on sequence


Display off sequence
Power off sequence
Stop oscillation (OSCSTBY = "1")
Set standby (OFFMOD = 1)
Set Off Mode
Start oscillation(OSCSTBY = "0")
Wait10ms
Release from standby (OFFMOD="0")
Off Mode Cancel
Power on sequence
Display on sequence

9.4. Initial Code (for TFT2.4 inch display and Driver IC 8312)

The reference setting of chip initial on

```
void Initial_HX8312 (void)
{
//============ Start Oscillation ============//
   HX8312_Reg(0x0001,0x0010);    //R01:Start oscillation
   HX8312_Reg(0x0000,0x00A0);    //R00:Standby mode cancel
   HX8312_Reg(0x0003,0x0001);    //R03:Software reset operation
   delay(10000);                  //delay 10ms
   HX8312_Reg(0x0003,0x0000);    //R03:Software reset operation cancel
   HX8312_Reg(0x002B,0x0004);    //R43:Oscillator frequency adjust setting
   HX8312_Reg(0x0059,0x0001);    //Test register setting enable
   HX8312_Reg(0x0060,0x0022);    //Test register setting
   HX8312_Reg(0x0059,0x0000);    //Test register setting disable
   HX8312_Reg(0x0028,0x0018);    //R40:DC/DC clock frequency adjust setting
   HX8312_Reg(0x001A,0x0005);    //R26:Step up circuit frequency adjust setting
   HX8312_Reg(0x0025,0x0005);    //R37:Step up factor in step up circuit 2 setting
   HX8312_Reg(0x0019,0x0000);    //R25:VR1 and VR2 regulator factor setting

//============ void Power_On_Set ============//
   HX8312_Reg(0x001C,0x0073);    //R28:Step up circuit operating current setting
   HX8312_Reg(0x0024,0x0074);    //R36:V18 and VCOM regulator current setting
   HX8312_Reg(0x001E,0x0001);    //R30:Extra step up circuit1 operation
   HX8312_Reg(0x0018,0x00C1);    //R24:VR1 and VR2 regulator on
   delay(10000);                  //delay 10ms
   HX8312_Reg(0x0018,0x00E1);    //R24:VCL trun on
   HX8312_Reg(0x0018,0x00F1);    //R24:VGH and VGL trun on
   delay(60000);                  //delay 60ms
   HX8312_Reg(0x0018,0x00F5);    //R24:DDVDH turn on
   delay(60000);                  //delay 60ms
   HX8312_Reg(0x001B,0x0009);    //R27:VS/VDH turn on and set
   delay(10000);                  //delay 10ms
   HX8312_Reg(0x001F,0x0011);    //R31:VCOM amplitude voltage setting
   HX8312_Reg(0x0020,0x000E);    //R32:VCOMH voltage setting
   HX8312_Reg(0x001E,0x0081);    //R30:VCOM operation start
   delay(10000);                  //delay 10ms
```

```
//============ Void Chip_Set ============//
   HX8312_Reg(0x009D,0x0000);
   HX8312_Reg(0x00C0,0x0000);
   HX8312_Reg(0x00C1,0x0000);    //R193:BGR bit='0'
   HX8312_Reg(0x000E,0x0000);
   HX8312_Reg(0x000F,0x0000);
   HX8312_Reg(0x0010,0x0000);
   HX8312_Reg(0x0011,0x0000);
   HX8312_Reg(0x0012,0x0000);
   HX8312_Reg(0x0013,0x0000);
   HX8312_Reg(0x0014,0x0000);
   HX8312_Reg(0x0015,0x0000);
   HX8312_Reg(0x0016,0x0000);
   HX8312_Reg(0x0017,0x0000);
   HX8312_Reg(0x0034,0x0001);
   HX8312_Reg(0x0035,0x0000);
   HX8312_Reg(0x004B,0x0000);
   HX8312_Reg(0x004C,0x0000);
   HX8312_Reg(0x004E,0x0000);
   HX8312_Reg(0x004F,0x0000);
   HX8312_Reg(0x0050,0x0000);
   HX8312_Reg(0x003C,0x0000);
   HX8312_Reg(0x003D,0x0000);
   HX8312_Reg(0x003E,0x0001);
   HX8312_Reg(0x003F,0x003F);
   HX8312_Reg(0x0040,0x0002);
   HX8312_Reg(0x0041,0x0002);
   HX8312_Reg(0x0042,0x0000);
   HX8312_Reg(0x0043,0x0000);
   HX8312_Reg(0x0044,0x0000);
   HX8312_Reg(0x0045,0x0000);
   HX8312_Reg(0x0046,0x00EF);
   HX8312_Reg(0x0047,0x0000);
   HX8312_Reg(0x0048,0x0000);
   HX8312_Reg(0x0049,0x0001);
   HX8312_Reg(0x004A,0x003F);
   HX8312_Reg(0x001D,0x0008);    //R29:Gate scan direction setting
   HX8312_Reg(0x0086,0x0000);
```

```
   HX8312_Reg(0x0087,0x0030);
   HX8312_Reg(0x0088,0x0002);
   HX8312_Reg(0x0089,0x0005);
   HX8312_Reg(0x008D,0x0001);    //R141:Register set-up mode for one line clock
number
   HX8312_Reg(0x008B,0x0030);    //R139:One line SYSCLK number in one-line
scan
   HX8312_Reg(0x0033,0x0001);    //R51:N line inversion setting
   HX8312_Reg(0x0037,0x0001);    //R55:Scanning method setting
   HX8312_Reg(0x0076,0x0000);

//============ void Gamma_Set ============//
   HX8312_Reg(0x008F,0x0010);
   HX8312_Reg(0x0090,0x0067);
   HX8312_Reg(0x0091,0x0007);
   HX8312_Reg(0x0092,0x0065);
   HX8312_Reg(0x0093,0x0007);
   HX8312_Reg(0x0094,0x0001);
   HX8312_Reg(0x0095,0x0076);
   HX8312_Reg(0x0096,0x0056);
   HX8312_Reg(0x0097,0x0000);
   HX8312_Reg(0x0098,0x0006);
   HX8312_Reg(0x0099,0x0003);
   HX8312_Reg(0x009A,0x0000);
//============ void Display_On ============//
   HX8312_Reg(0x003B,0x0001);
   delay(40000);                        //delay 40ms
   HX8312_Reg(0x0000,0x0020);
   }
```

The reference settings of stand by mode cancel

```
void Power_On_Set(void)
{
   HX8312_Reg(0x001C,0x0073);    //R28:Step up circuit operating current setting
   HX8312_Reg(0x0024,0x0074);    //R36:V18 and VCOM regulator current setting
   HX8312_Reg(0x001E,0x0001);    //R30:Extra step up circuit1 operation
   HX8312_Reg(0x0018,0x00C1);    //R24:VR1 and VR2 regulator on
   delay(10000);                 //delay 10ms
   HX8312_Reg(0x0018,0x00E1);    //R24:VCL trun on
   HX8312_Reg(0x0018,0x00F1);    //R24:VGH and VGL trun on
   delay(60000);                 //delay 60ms
   HX8312_Reg(0x0018,0x00F5);    //R24:DDVDH turn on
   delay(60000);                 //delay 60ms
   HX8312_Reg(0x001B,0x0009);    //R27:VS/VDH turn on and set
   delay(10000);                 //delay 10ms
   HX8312_Reg(0x001F,0x0011);    //R31:VCOM amplitude voltage setting
   HX8312_Reg(0x0020,0x000E);    //R32:VCOMH voltage setting
   HX8312_Reg(0x001E,0x0081);    //R30:VCOM operation start
   delay(10000);                  //delay 10ms
}

void Into_Standby(void)
{
//============ void Display_Off ============//
   HX8312_Reg(0x0000,0x00A0);
   delay(40000);                 //delay 40ms
   HX8312_Reg(0x003B,0x0000);
//============ void Power_Off ============//
   HX8312_Reg(0x001E,0x0001);    //VCOM off
   HX8312_Reg(0x001B,0x0008);    //VS/VDH power off
   HX8312_Reg(0x001C,0x0000);    //setup up circuit operating current off
   HX8312_Reg(0x0024,0x0000);    //V18 nad VCOM regulator current off
   HX8312_Reg(0x0018,0x0000);
//============ Into standby mode ============//
   HX8312_Reg(0x0001,0x0011);    //Internal oscillator stop
   HX8312_Reg(0x0000,0x0028);    //Into standby mode
```

```
}
void Cancel_Standby(void)
{
//============ Standby mdoe cancel ============//
   HX8312_Reg(0x0000,0x00A0);    //R00:Standby mode cancel
   HX8312_Reg(0x0001,0x0010);    //R01:Start oscillation
   delay(10000);                 //delay 10ms
   Power_On_Set();
//============ void Display_On ============//
   HX8312_Reg(0x003B,0x0001);
   delay(40000);                 //delay 40ms
   HX8312_Reg(0x0000,0x0020);
}

void Into_Standby(void)
{
//============ void Display_Off ============//
   HX8312_Reg(0x0000,0x00A0);
   delay(40000);                 //delay 40ms
   HX8312_Reg(0x003B,0x0000);
//============ void Power_Off ============//
   HX8312_Reg(0x001E,0x0001);    //VCOM off
   HX8312_Reg(0x001B,0x0008);    //VS/VDH power off
   HX8312_Reg(0x001C,0x0000);    //setup up circuit operating current off
   HX8312_Reg(0x0024,0x0000);    //V18 nad VCOM regulator current off
   HX8312_Reg(0x0018,0x0000);
//============ Into standby mode ============//
   HX8312_Reg(0x0001,0x0011);    //Internal oscillator stop
   HX8312_Reg(0x0000,0x0028);    //Into standby mode
}
```

10. Timing Characteristics

10.1 Read / Write Characteristics (8080-series MPU)

Please refer to HX8312A specification

<<Normal Write Mode(HWM=0),IoVcc=1.65V-2.4V>>

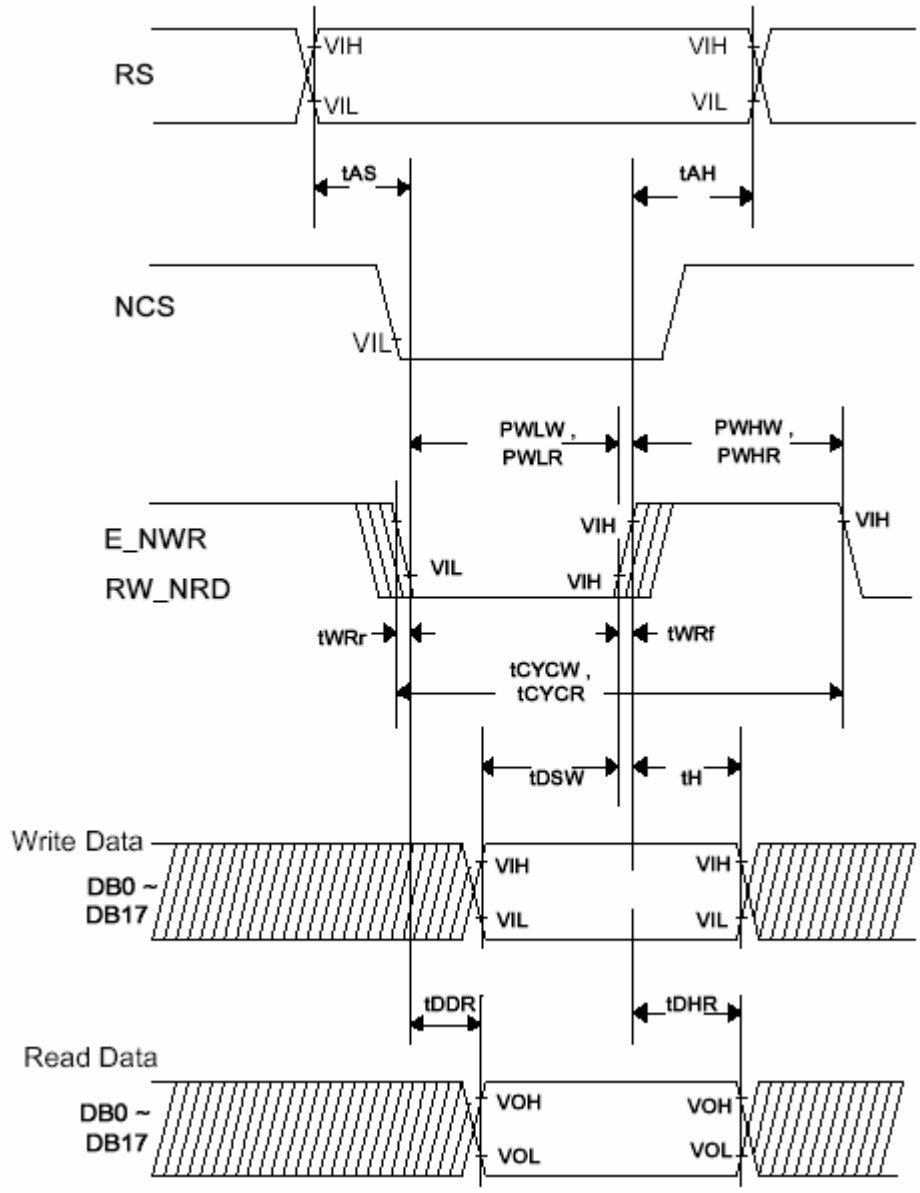
Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	125	-	-
	Read	t_{CYCR}	ns	300	-	-
Write low-level pulse width		PW_{LW}	ns	40	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-
Write high-level pulse width		PW_{HW}	ns	70	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-
Write/Read rise/fall time		t_{WRr},t_{WRf}	ns	-	-	25
Set up time	(RS to NCS,E_NWR)	t_{AS}	ns	5	-	-
RS hold time	(NCS,NWR to RS)	t_{AH}	ns	5	-	-
Write data set up time		t_{DSW}	ns	20	-	-
Write data hold time		t_H	ns	15	-	-
Read data delay time		t_{DDR}	ns	-	-	100
Read data hold time		t_{DHR}	ns	5	-	-

<<Normal Write Mode(HWM=0),IoVcc=2.4V-3.3V>>

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	200	-	-
	Read	t_{CYCR}	ns	300	-	-
Write low-level pulse width		PW_{LW}	ns	40	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-
Write high-level pulse width		PW_{HW}	ns	70	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-
Write/Read rise/fall time		t_{WRr},t_{WRf}	ns	-	-	25
Set up time	(RS to NCS,E_NWR)	t_{AS}	ns	5	-	-
RS hold time	(NCS,NWR to RS)	t_{AH}	ns	5	-	-
Write data set up time		t_{DSW}	ns	20	-	-
Write data hold time		t_H	ns	15	-	-
Read data delay time		t_{DDR}	ns	-	-	100
Read data hold time		t_{DHR}	ns	5	-	-

Reset Timing Characteristics

Item	Symbol	Unit	Min	Typ	Max
Reset"low"level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	us	-	-	10



80-System Bus Timing

Note 1) PWEL is specified during the overlap period. (SC*="Low", WR* or RD*="Low")

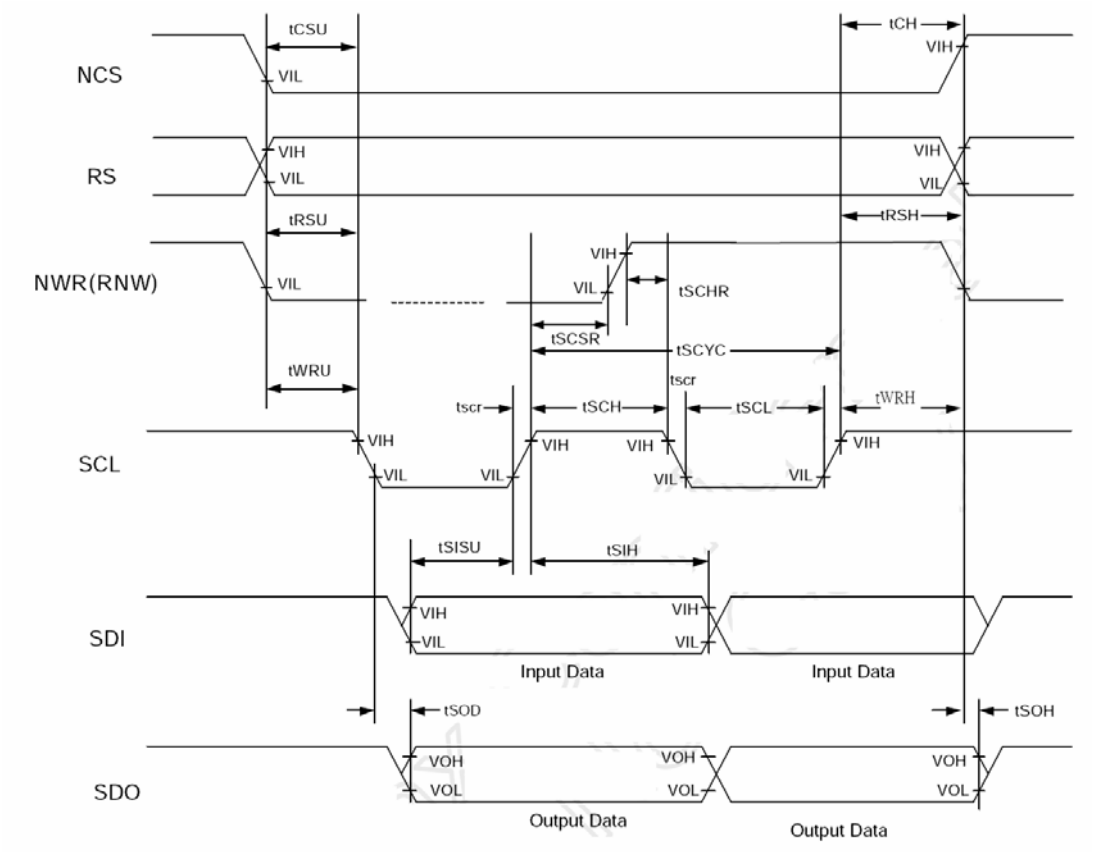
Note 2) When using 16-bit bus interface, parallel data can be transferred through DB17-10 pin and DB8-1 and DB0 must be fixed to "Vcc" or "GND".

10.2 RGB Interface Timing Characteristics

IoVcc=2.4V-3.3V

Item		Symbol	Unit	Min	Typ	Max
Serial clock cycle time	Write	t_{SCYC}	ns	100	-	-
	Read	t_{SCYC}	ns	200	-	-
Serial clock high – level pulse width	Write	t_{SCH}	Ns	40	-	-
	Read	t_{SCH}	ns	150	-	-
Serial clock low – level pulse width	Write	t_{SCL}	ns	40	-	-
	Read	t_{SCL}	ns	150	-	-
Serial clock rise / fall time		t_{SCR}, t_{SCF}	ns	-	-	-
Chip select (NCS) set up time		T_{CSU}	ns	20	-	-
Chip select (NCS) hold time		T_{CH}	ns	60	-	-
RS set up time		T_{RSU}	ns	10	-	-
RS hold time		T_{RSH}	ns	10	-	-
Read/write select (RNW) set up time		T_{WRU}	ns	10	-	-
Read/write select (RNW) hold time		T_{WRH}	ns	10	-	-
Read clock set up time		T_{SCSR}	ns	10	-	-
Read clock hold time		T_{SCHR}	ns	10	-	-
Serial input data set up time		T_{SISU}	ns	30	-	-
Serial input data hold time		T_{SIH}	ns	30	-	-
Serial output data delay time		T_{SOD}	Ns	-	-	100
Serial output data hold time		T_{SOH}	ns	5	-	-

Clock Synchronized Serial Data Transfer Interface Operation



10.3 RGB Interface Timing Characteristics

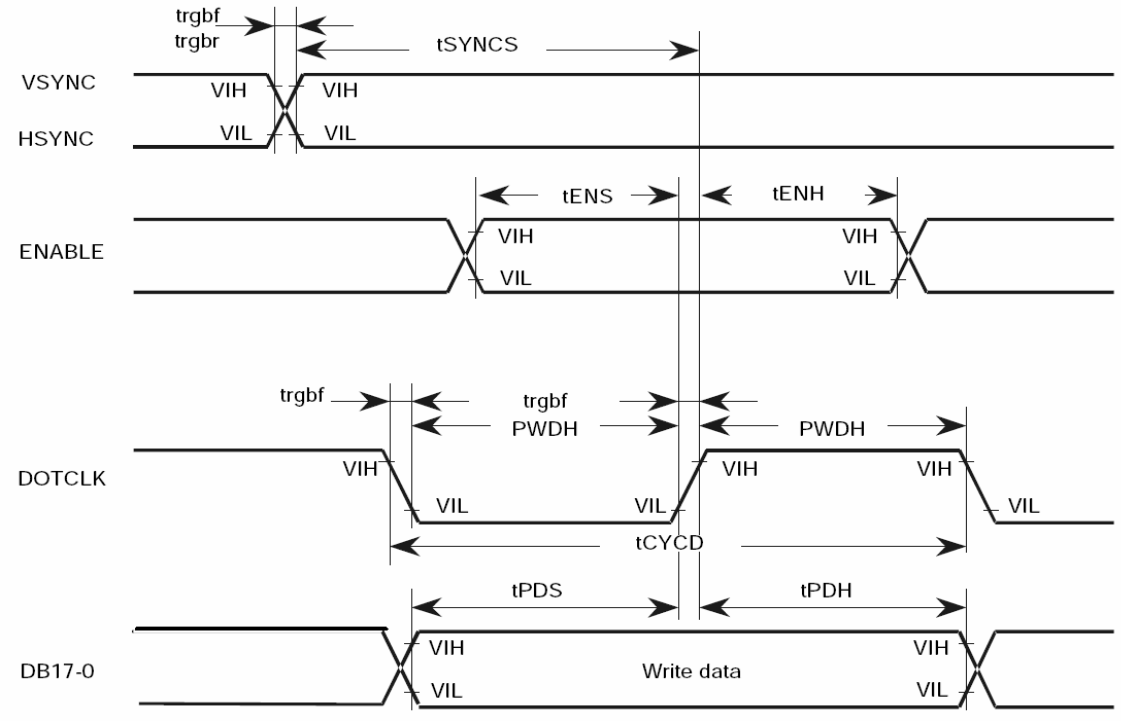
Normal Write Mode (IOVCC=1.65~2.4V) / (VCC = 2.4V~3.3V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC / HSYNC set up time	T_{SYNCS}	ns	10	-	-
ENABLE set up time	T_{ENS}	ns	10	-	-
ENABLE hold time	T_{ENH}	ns	10	-	-
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-
DOTCLK cycle time	T_{CYCD}	ns	200	-	-
DATA set up time	T_{PDS}	ns	20	-	-
DATA hold time	T_{PDH}	ns	20	-	-
DOTCLK , VSYNC , HSYNC rising and falling time	T_{rgbr}, t_{rgbf}	ns	-	-	25

Normal Write Mode (IOVCC=2.4~3.3V) / (VCC = 2.4V~3.3V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC / HSYNC set up time	T_{SYNCS}	ns	10	-	-
ENABLE set up time	T_{ENS}	ns	10	-	-
ENABLE hold time	T_{ENH}	ns	10	-	-
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-
DOTCLK cycle time	T_{CYCD}	ns	150	-	-
DATA set up time	T_{PDS}	ns	20	-	-
DATA hold time	T_{PDH}	ns	20	-	-
DOTCLK , VSYNC , HSYNC rising and falling time	T_{rgbr}, t_{rgbf}	ns	-	-	25

RGB Interface Operation



11 QUALITY AND RELIABILITY

11.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

11.2 SAMPLING PLAN

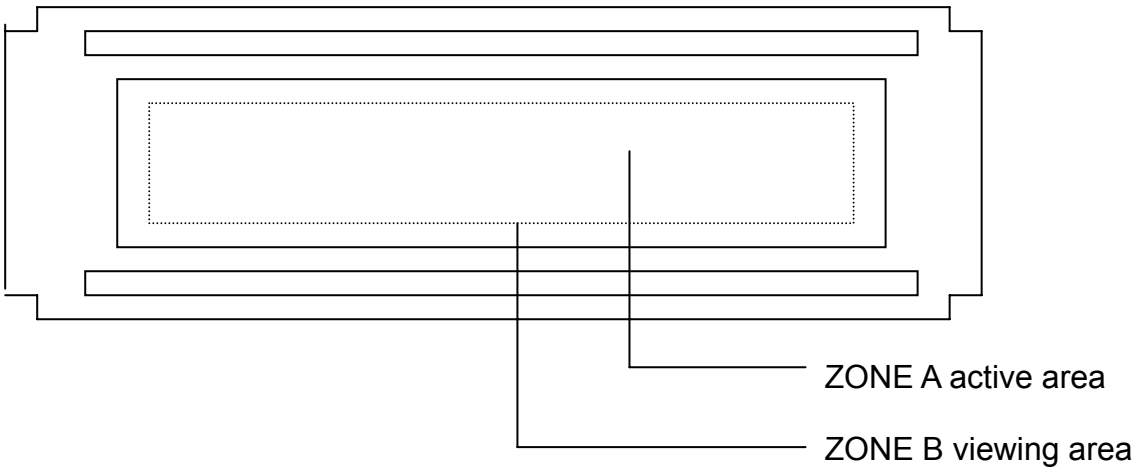
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

11.3 ACCEPTABLE QUALITY LEVEL

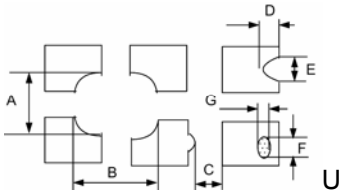
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

11.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



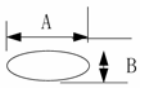
11.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don’t activate are rejectable.</td><td>Major</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>6</td><td>Black/White line (I)</td><td><table><tr><th>Length(mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>10 < L</td><td>0.03 < W ≤ 0.04</td><td>5</td></tr><tr><td>5.0 < L ≤10</td><td>0.04 < W ≤ 0.06</td><td>3</td></tr><tr><td>1.0 < L ≤ 5.0</td><td>0.06 < W ≤ 0.07</td><td>2</td></tr><tr><td>L ≤ 1.0</td><td>0.07 < W ≤ 0.09</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Black/White sport (II)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.30</td><td>Ignore</td></tr><tr><td>0.30 < D ≤ 0.50</td><td>5</td></tr><tr><td>0.50 < D ≤ 1.20</td><td>3</td></tr><tr><td>1.20 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>8</td><td>Black/White line (II)</td><td><table><tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>20 < L</td><td>0.05 < W ≤ 0.07</td><td>5</td></tr><tr><td>10 < L ≤ 20</td><td>0.07 < W ≤ 0.09</td><td>3</td></tr><tr><td>5.0 < L ≤ 10</td><td>0.09 < W ≤ 0.10</td><td>2</td></tr><tr><td>L ≤ 5.0</td><td>0.10 < W ≤ 0.15</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>9</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td></tr>
<tr><td>10</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there’re to two or more pinholes per dot</td><td>Minor</td></tr>
</table>

<table>
<tr><td>11</td><td>Blemish & Foreign matters

Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>12</td><td>Scratch on Polarizer

  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.03</td><td>Ignore</td><td>Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L ≤ 2.0</td><td>Ignore</td></tr><tr><td></td><td>L > 2.0</td><td>1</td></tr><tr><td>0.05<W≤0.08</td><td>L > 1.0</td><td>1</td></tr><tr><td></td><td>L ≤ 1.0</td><td>Ignore</td></tr><tr><td>0.08<W</td><td>Note (1)</td><td>Note(1)</td></tr></table>Note(1) Regard as a blemish</td><td>Minor</td></tr>
<tr><td>13</td><td>Bubble in polarizer</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.20</td><td>Ignore</td></tr><tr><td>0.20 < D ≤ 0.50</td><td>3</td></tr><tr><td>0.50 < D ≤ 0.80</td><td>2</td></tr><tr><td>0.80 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>14</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>15</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
<tr><td>16</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td></tr>
<tr><td>17</td><td>Parts mounting</td><td>1. Failure to mount parts
2. Parts not in the specifications are mounted
3. Polarity, for example, is reversed</td><td>Major
Major
Major</td></tr>
<tr><td>18</td><td>Parts alignment</td><td>1. LSI, IC lead width is more than 50% beyond pad outline.
2. Chip component is off center and more than 50% of the leads is off the pad outline.</td><td>Minor

Minor</td></tr>
<tr><td>19</td><td>Conductive foreign matter (Solder ball, Solder chips)</td><td>1. 0.45< φ ,N≧1
2. 0.30< φ ≤0.45 ,N≧1
φ :Average diameter of solder ball (unit: mm)
3. 0.50<L ,N≧1
L: Average length of solder chip (unit: mm)</td><td>Major
Minor

Minor</td></tr>
<tr><td>20</td><td>Faulty PCB correction</td><td>1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB.
2. Short circuited part is cut, and no resist coating has been performed.</td><td>Minor

Minor</td></tr>
</table>

11.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 70°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 USE PRECAUTIONS

12.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

1) To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between

0°C and 35°C and also the humidity under 60%.

2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk

occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

13 OUTLINE DIMENSION