AMP DISPLAY INC.

A Brighter Solution

SPECIFICATIONS

TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

AMP DISPLAY INC

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2009/3/30	--	New Release	Edward

1 Features

This single-display module is suitable for cell phone application. The Main-LCD adopts one backlight with High brightness 4-lamps white LED.

(1) Construction: 2.8” a-Si color TFT-LCD, White LED Backlight, and FPC.

(2) Main LCD : 2.1 Amorphous-TFT 2.8 inch display, transmissive, Normally white type, 12 o’clock.
2.2 240(RGB)X320 dots Matrix,1/320 Duty.
2.3 Narrow-contact ledge technique.
2.4 Main LCD Driver IC: ILI9320

(3) Low cross talk by frame rate modulation
(4) Direct data display with display RAM
(5) Partial display function: You can save power by limiting the display space.
(6) RGB interface: 18bits, series interface for power setting.
(7) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function
Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 50.2 (W) x 108.5 (H) .	mm
Main LCD	Pixel size	0.18 (W) x 0.18 (H)	mm
	Active area	43.2 (W) x 57.6 (H)	mm
	Number of Pixels	240(H)x320(V) pixels	mm
Weight		TBD	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VCC – GND	-0.3	+3.6	V	
Power voltage	LED A – LED K	-0.5	+16.0	V	Parallel
Input voltage	VIN	-0.5	VCC	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70°C Min. -20°C	Note 1: Non-condensing
Operating temperature	Max. +60°C Min. -10°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{CC}=3.0V, Ta=25°C)

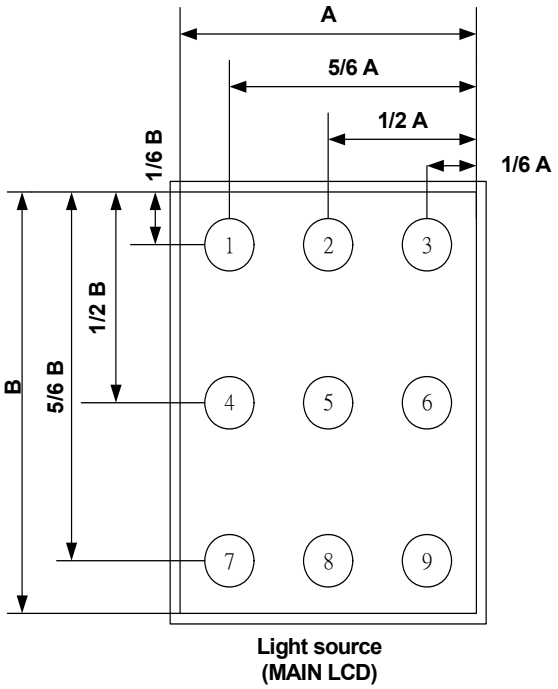
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{CC}		2.6	2.8	3.3	V
High-level input voltage	V_{IHC}		0.8V_{CC}		V_{CC}	V
Low-level input voltage	V_{ILC}		0		0.2V_{CC}	V
Consumption current of VDD	I_{CC}	LED OFF	-	12	-	mA

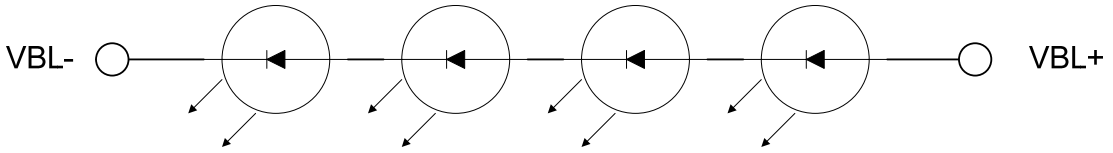
※ 1. 1/320 duty.

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =20mA	12.0	13.6	15.2	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	4-chip Serial	10	15	20	mA
Power Consumption	P_{BL}	I_f =20mA	-	272	-	mW
Uniformity (with L/G)	-	I_f=20mA	80%*1	-	-	
Bare LED Luminous intensity	I_f	I_f =20mA	3000	-	-	cd/m^2
Luminous color	White					
Chip connection	4 chip Serial connection					

Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

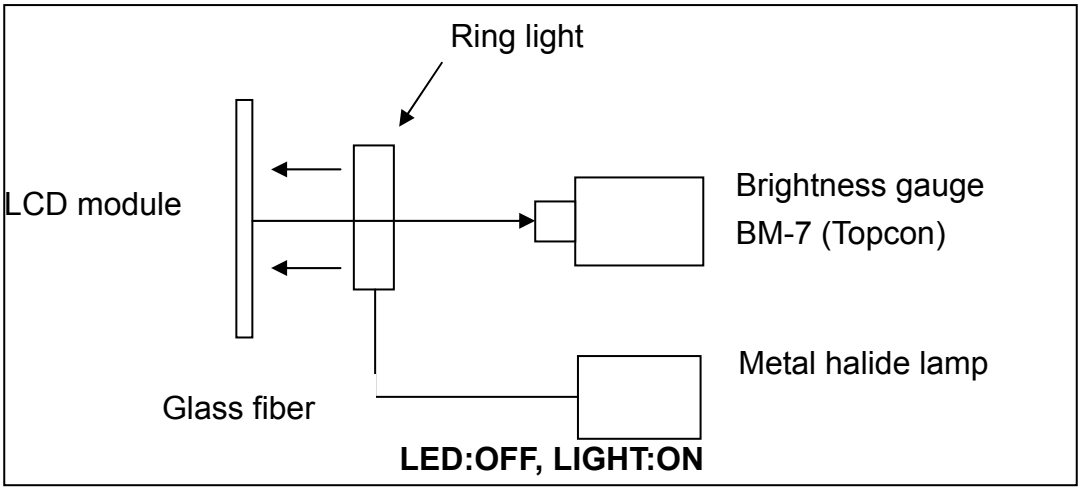
LED backlight transmissive module:

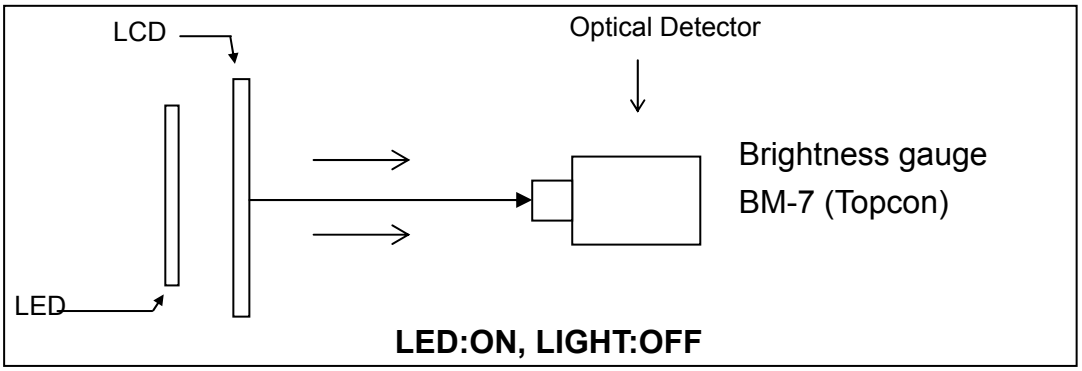
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	--	10	--	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	--	15	--		
Contrast ratio	CR	25°C	-	(250)	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	(5.7)	(6.0)	-	%	
Visual angle range front and rear	θ	25°C	(θf) 70 (θb) 50			De-gree	φ= 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 70 (θr) 70			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			225	250	--	Cd/m2	V_{LED}=3.2V, 20mA Full White pattern

5.2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

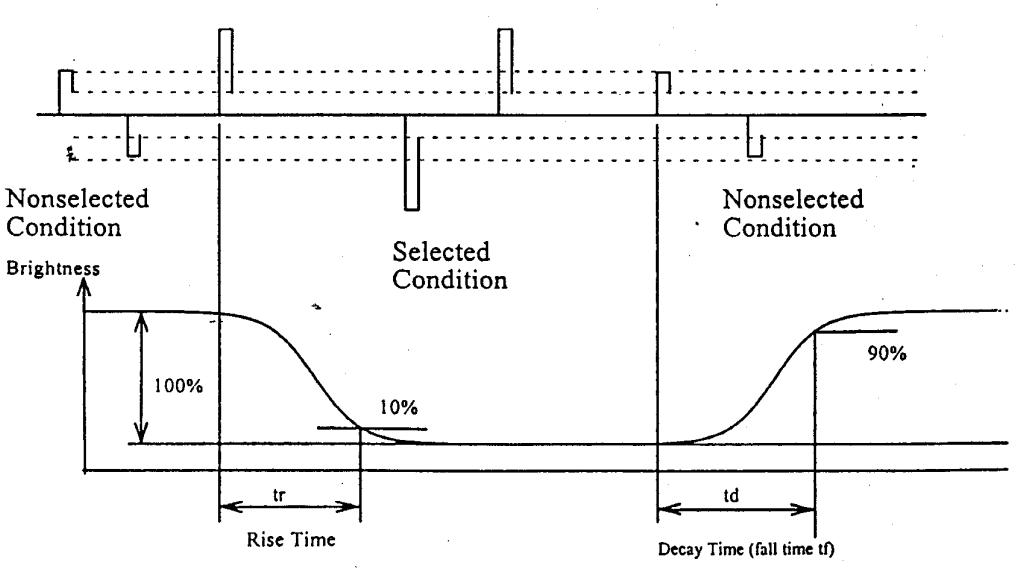
Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	--	0.6196	--	θ=0°, φ=0°
	Y	--	0.3423	--	
Green	X	--	0.3513	--	θ=0°, φ=0°
	Y	--	0.5635	--	
Blue	X	--	0.1456	--	θ=0°, φ=0°
	Y	--	0.0949	--	
White	X	--	0.3161	--	θ=0°, φ=0°
	Y	--	0.337	--	

NOTE 1: Optical characteristic measurement system

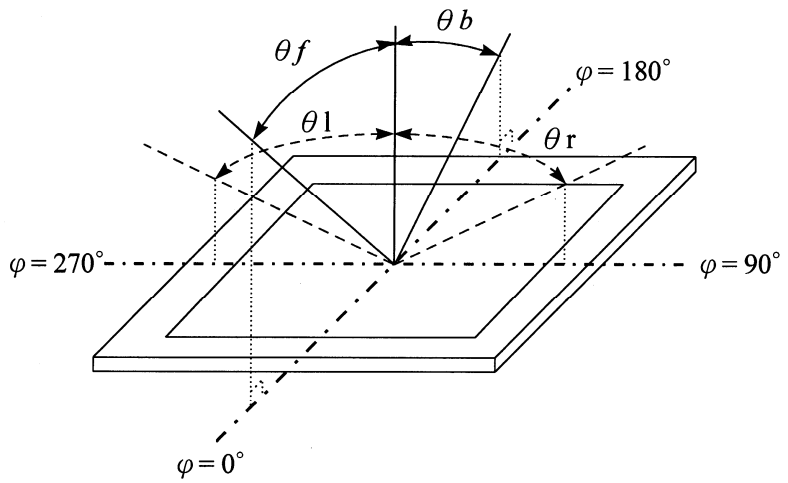




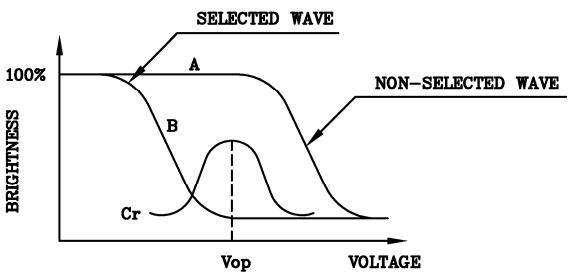
NOTE 2: Response tome definition



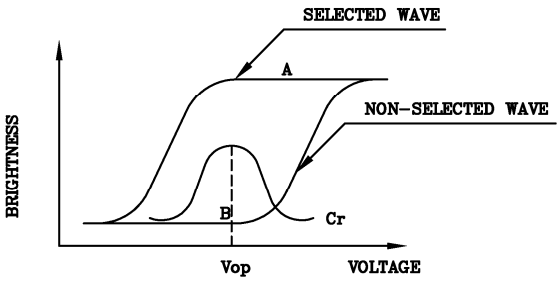
NOTE 3: φ、θ definition



NOTE 4: Contrast definition



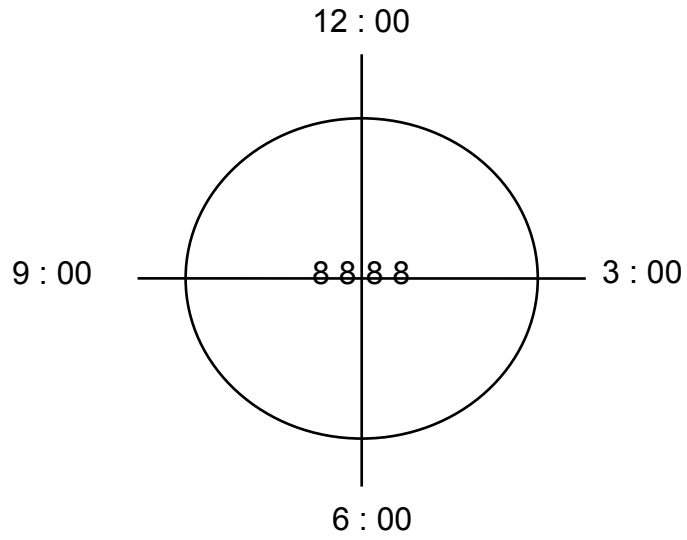
(positive type)



(negative type)

Contrast Ratio : Cr=A/B

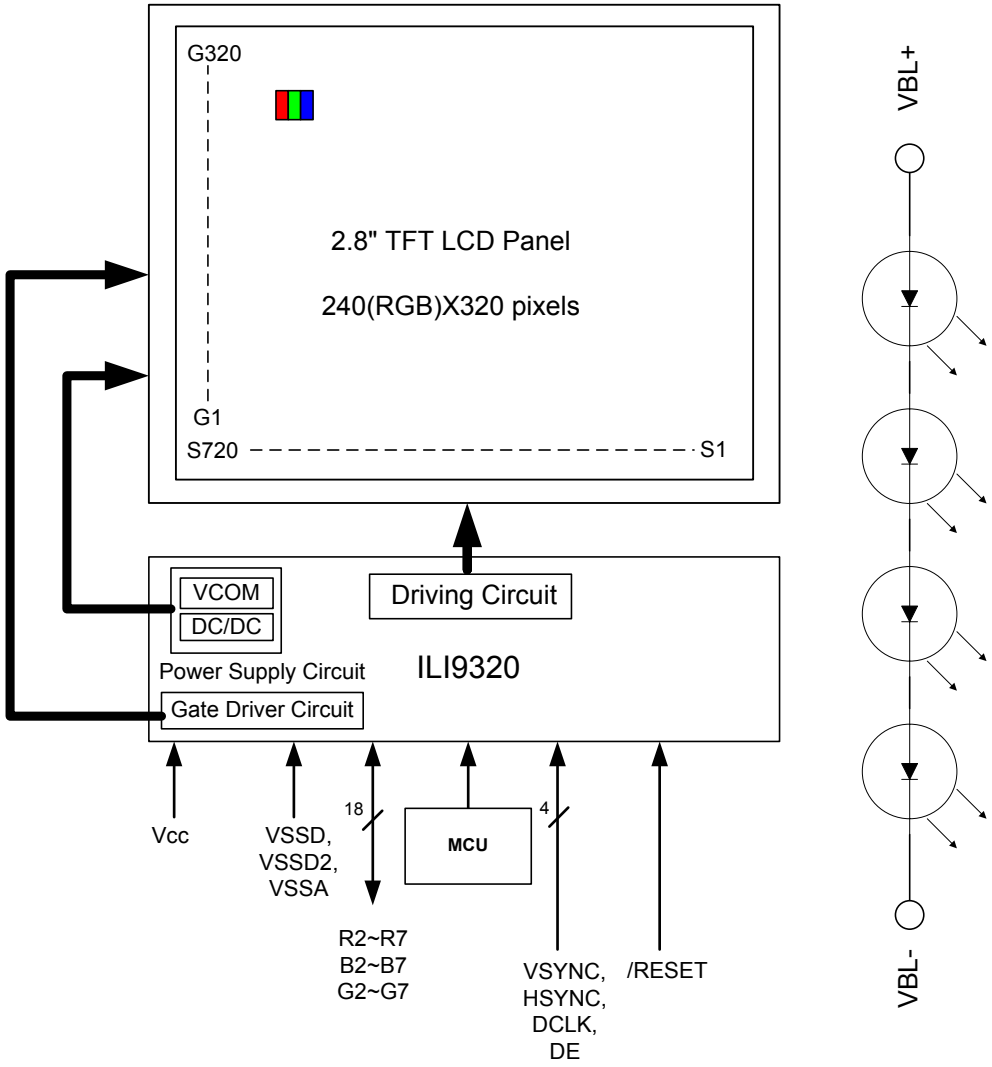
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format:	A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition:	240 x RGB x 320 dots
LCD Driver :	ILI9320
Back light:	White LED x 4 (I_{LED}=80mA)



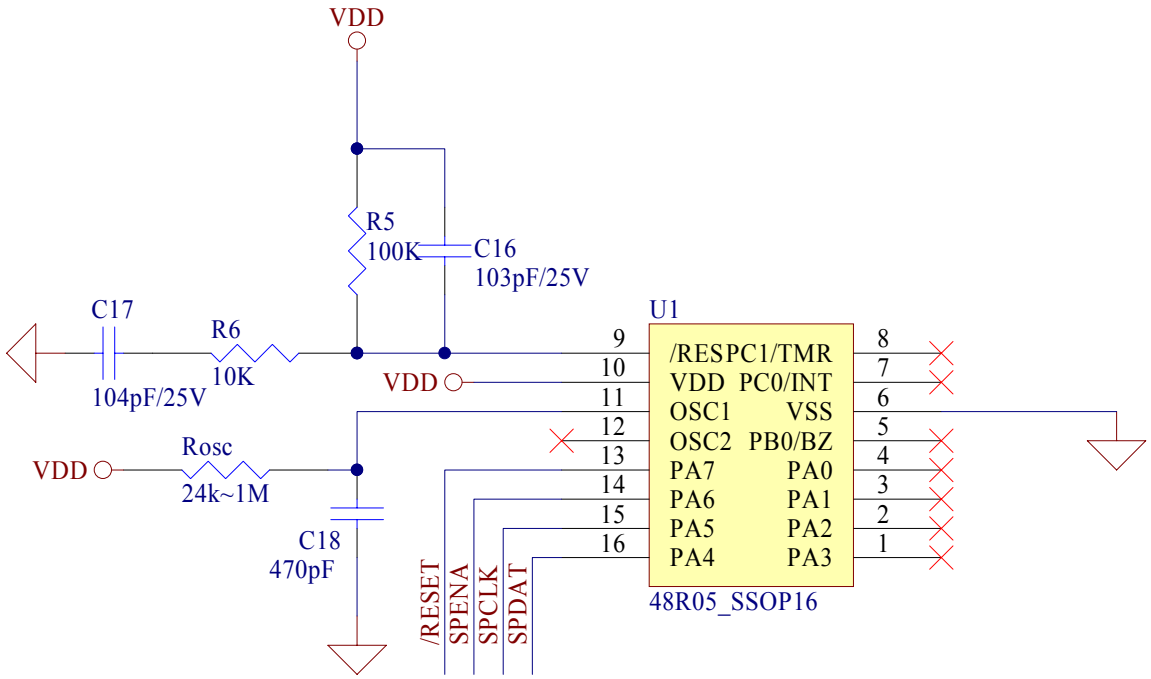
7. Electrical Specifications

7.1 TFT LCD Panel FPC Descriptions

No.	Symbol	I/O	Description	Remark
1.	VBL-	I	Backlight LED Cathode.	
2.	VBL-	I	Backlight LED Cathode.	
3.	VBL+	I	Backlight LED Anode.	
4.	VBL+	I	Backlight LED Anode.	
5.	NC	-	No connection.	
6.	/RESET		Hardware Reset	
7.	NC		Not Use	
8.	Y-	I	Touch Panel--Top electrode	
9.	X+	I	Touch Panel--Right electrode	
10.	Y+	I	Touch Panel--Bottom electrode	
11.	X-	I	Touch Panel--Left electrode	
12.	NC		Not Use	
13.	NC		Not Use	
14.	B2	I	Blue Data Bit 2	
15.	B3	I	Blue Data Bit 3	
16.	B4	I	Blue Data Bit 4	
17.	B5	I	Blue Data Bit 5	
18.	B6	I	Blue Data Bit 6	
19.	B7	I	Blue Data Bit 7	
20.	NC		Not Use	
21.	NC		Not Use	
22.	G2	I	Green Data Bit 2	
23.	G3	I	Green Data Bit 3	
24.	G4	I	Green Data Bit 4	
25.	G5	I	Green Data Bit 5	
26.	G6	I	Green Data Bit 6	
27.	G7	I	Green Data Bit 6	
28.	NC		Not Use	
29.	NC		Not Use	
30.	R2	I	Red Data Bit 2	
31.	R3	I	Red Data Bit 3	
32.	R4	I	Red Data Bit 4	
33.	R5	I	Red Data Bit 5	
34.	R6	I	Red Data Bit 6	
35.	R7	I	Red Data Bit 7	
36.	HSYNC	I	Horizontal Sync Input	
37.	VSYNC	I	Vertical Sync Input	
38.	DCLK	I	Dot Data Clock	

39.	NC		Not Use	
40.	NC		Not Use	
41.	VCC	I	Digital Power	
42.	VCC	I	Digital Power	
43.	SPENA	I	SPI Interface Data Enable Signal	Note1
44.	NC		Not Use	
45.	NC		Not Use	
46.	NC		Not Use	
47.	NC		Not Use	
48.	NC		Not Use	
49.	SPCLK	I	SPI Interface Data Clock	Note1
50.	SPDAT	I	SPI Interface Data	Note1
51.	NC		Not Use	
52.	DE	I	Data Enable Input	
53.	GND	I	Ground	
54.	GND	I	Ground	

Note1: The module is with a MCU 48R05. The MCU will send the initial code to ILI9320 when power ON. Please let these pins open.



7.2 Instruction List

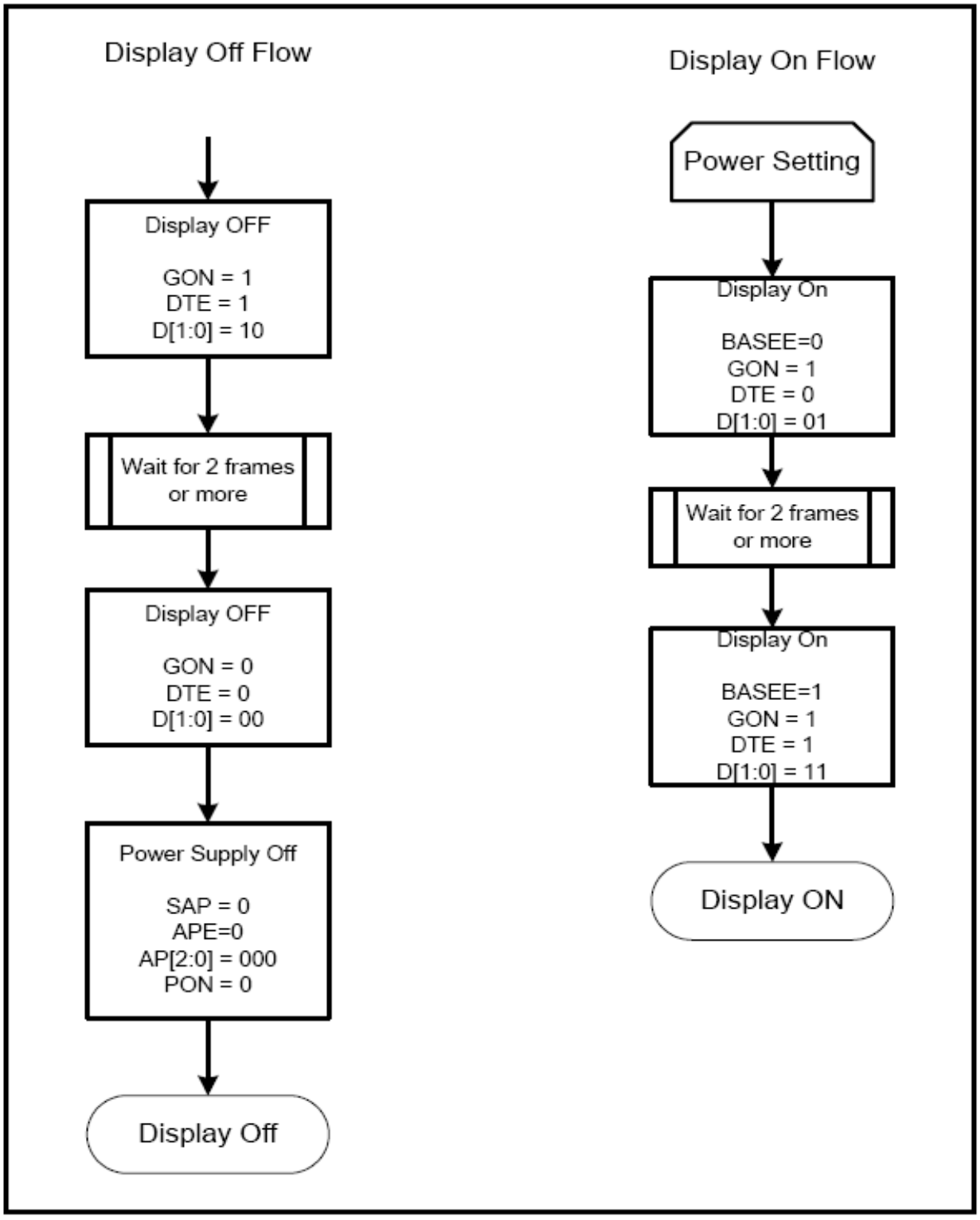
Main LCD Driver IC:ILI9320

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0
00h	Start Oscillation	W	1	-	-	-	-	-		-	-		-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV 1	RCV 0	0	0	RCH 1	RCH 0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTD E1	PTD E0	0	0	0	BAS EE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMA RKO E	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	ENC 2	ENC 1	ENC 0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP 8	FMP 7	FMP 6	FMP 5	FMP 4	FMP 3	FMP 2	FMP 1	FMP 0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSP L	0	DPL	EPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DST B	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCM R	0	0	0	PON	VRH 3	VRH 2	VRH 1	VRH 0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	EXT_ R	0	FR_S EL1	FR_S EL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1 [4]	VRP1 [3]	VRP1 [2]	VRP1 [1]	VRP1 [0]	0	0	0	VRP0 [4]	VRP0 [3]	VRP0 [2]	VRP0 [1]	VRP0 [0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]

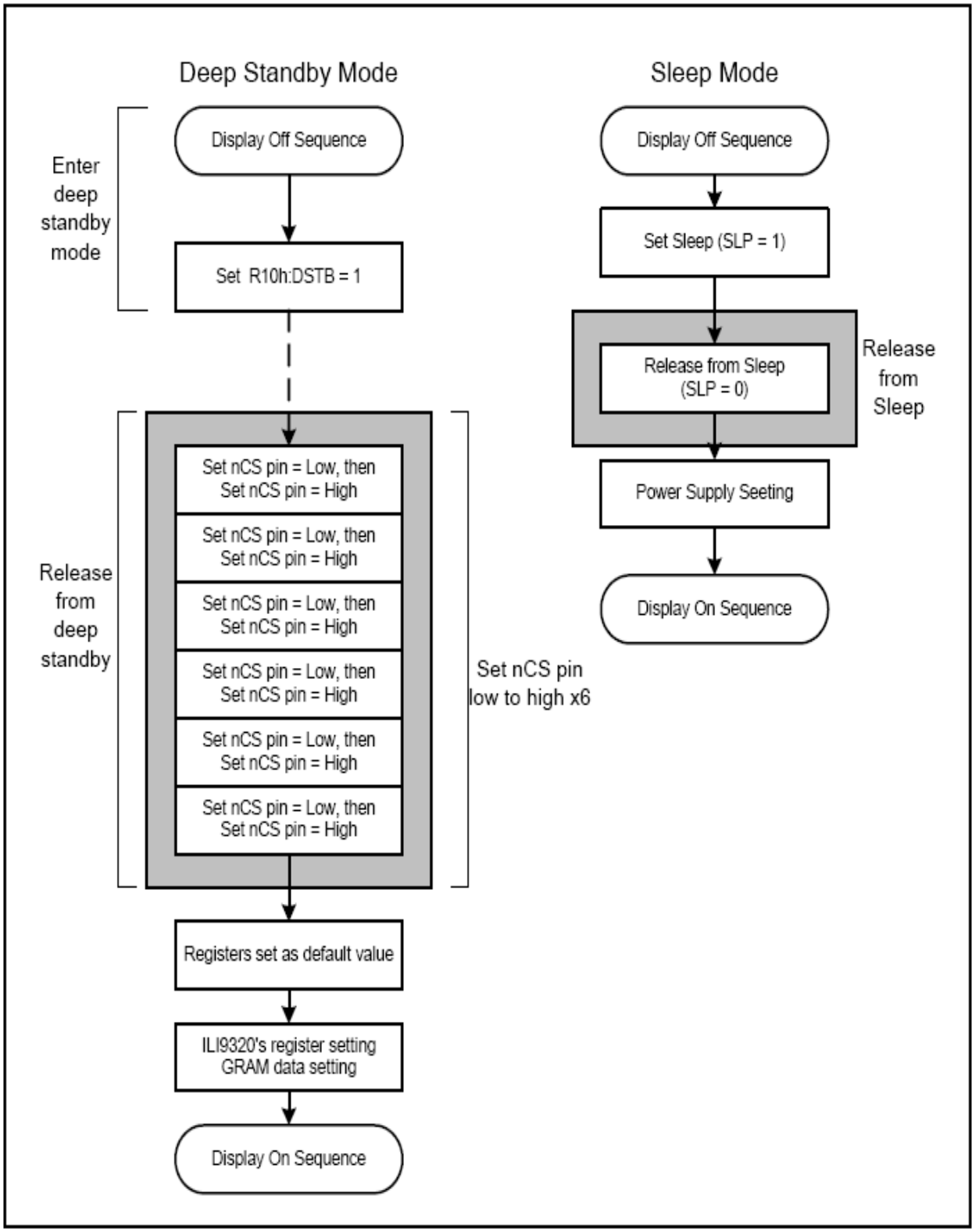
No.	Registers	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38h	Gamma Control 7	**W**	**1**	**0**	**0**	**0**	**0**	**0**	**KN3[2]**	**KN3[1]**	**KN3[0]**	**0**	**0**	**0**	**0**	**0**	**KN2[2]**	**KN2[1]**	**KN2[0]**
39h	Gamma Control 8	**W**	**1**	**0**	**0**	**0**	**0**	**0**	**KN5[2]**	**KN5[1]**	**KN5[0]**	**0**	**0**	**0**	**0**	**0**	**KN4[2]**	**KN4[1]**	**KN4[0]**
3Ch	Gamma Control 9	**W**	**1**	**0**	**0**	**0**	**0**	**0**	**RN1[2]**	**RN1[1]**	**RN1[0]**	**0**	**0**	**0**	**0**	**0**	**RN0[2]**	**RN0[1]**	**RN0[0]**
3Dh	Gamma Control 10	W	1	0	0	0	VRN 1[4]	VRN 1[3]	VRN 1[2]	VRN 1[1]	VRN 1[0]	0	0	0	VRN 0[4]	VRN 0[3]	VRN 0[2]	VRN 0[1]	VRN 0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA 08	PTSA 07	PTSA 06	PTSA 05	PTSA 04	PTSA 03	PTSA 02	PTSA 01	PTSA 00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA 08	PTEA 07	PTEA 06	PTEA 05	PTEA 04	PTEA 03	PTEA 02	PTEA 01	PTEA 00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA 18	PTSA 17	PTSA 16	PTSA 15	PTSA 14	PTSA 13	PTSA 12	PTSA 11	PTSA 10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA 18	PTEA 17	PTEA 16	PTEA 15	PTEA 14	PTEA 13	PTEA 12	PTEA 11	PTEA 10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI0 0	0	0	0	0	RTNI 3	RTNI 2	RTNI 1	RTNI 0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOW I2	NOW I1	NOW I0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI 2	MCPI 1	MCPI 0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE 1	DIVE 0	0	0	RTN E5	RTN E4	RTN E3	RTN E2	RTN E1	RTN E0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOW E3	NOW E2	NOW E1	NOW E0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCP E2	MCP E1	

8. Application

8.1 Display ON / OFF Sequence

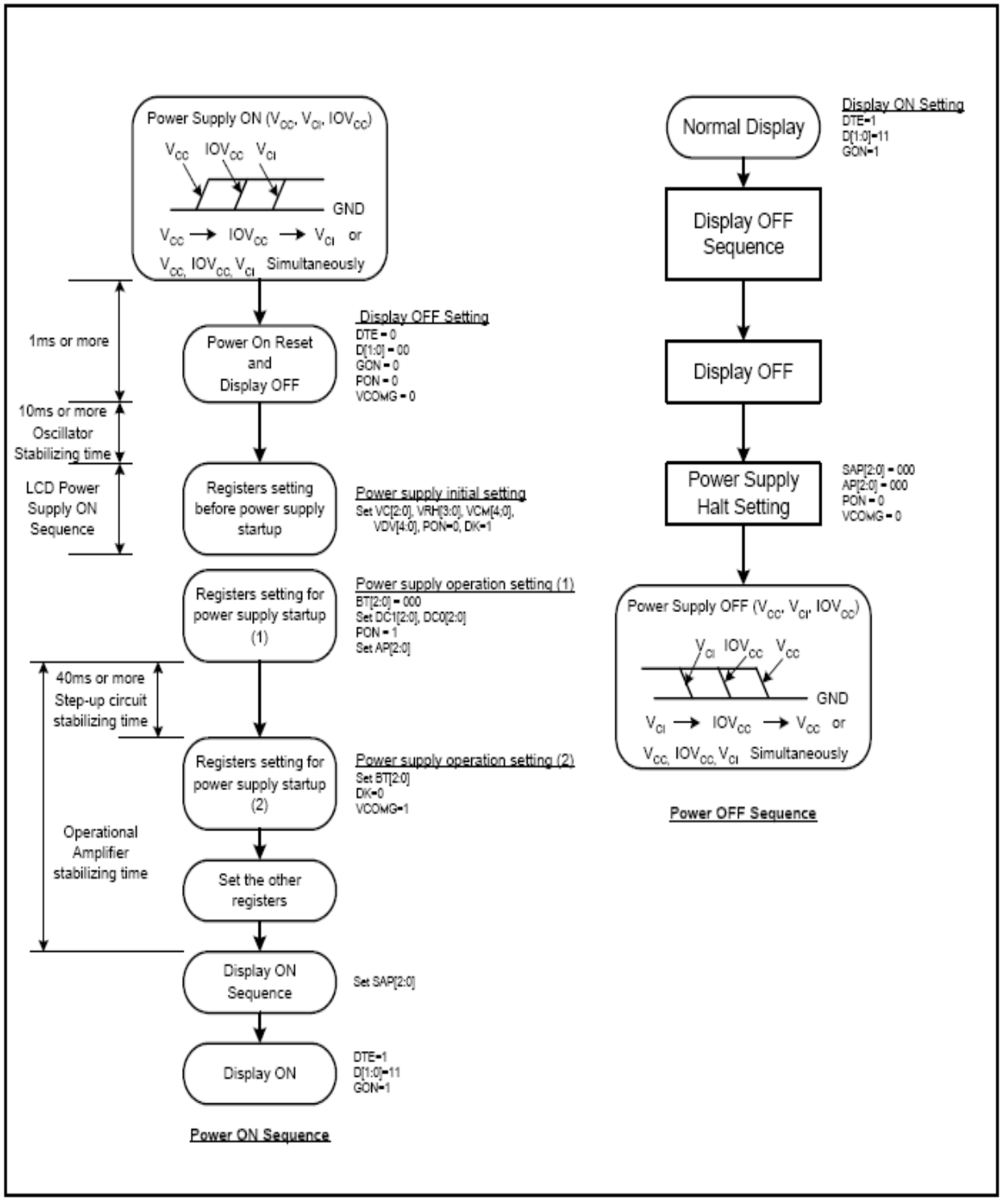


8.2 Deep Standby and Sleep Mode



8.3 Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.



9. Electrical Characteristics

9.1 Clock Characteristics

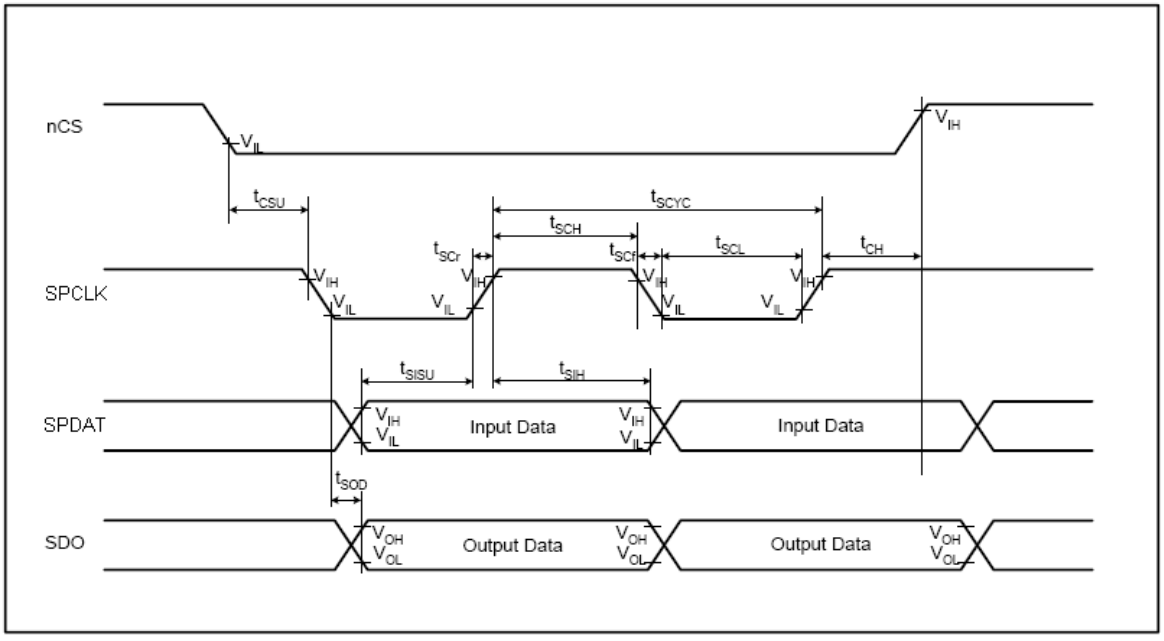
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	fcp	VCC = 2.4 ~ 3.3V	450	550	650	KHz
External Clock Duty	f_{Duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
RC oscillation clock	f_{osc}	Rf = 100KΩ, VCC = 2.8V	450	550	650	KHz

9.2 AC Characteristics (Serial Data Transfer Interface Timing Characteristics)

(IOVCC= 1.653.3V and VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	
	Read (transmitted)	t_{SCYC}	ns	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	



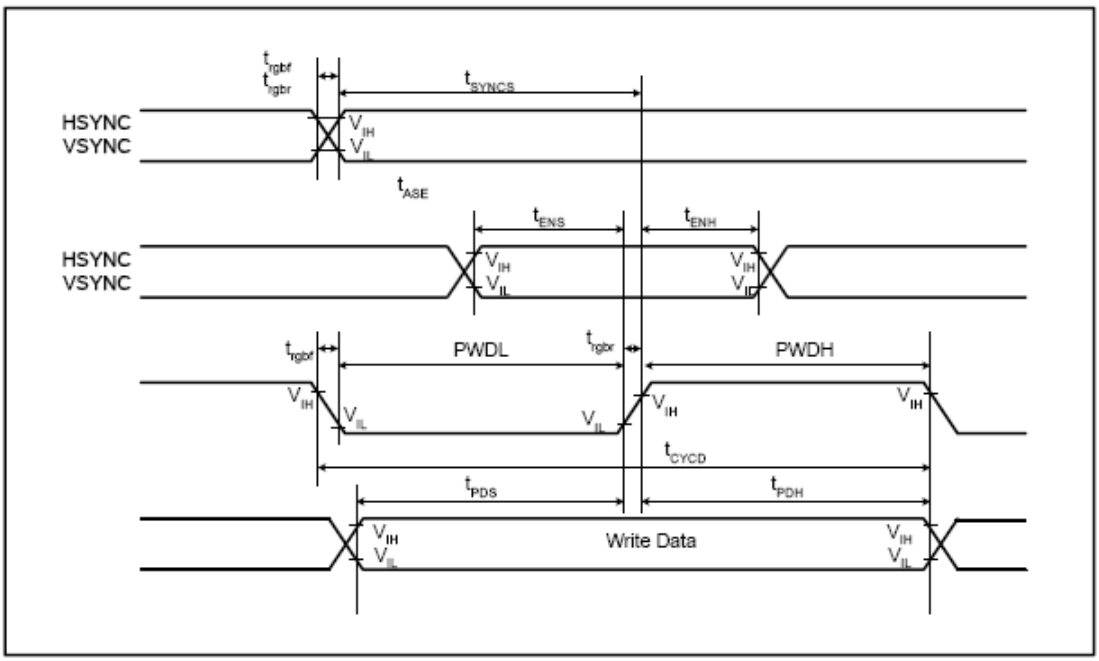
9.3 AC Characteristics (RGB Interface Timing Characteristics)

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-



10.QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

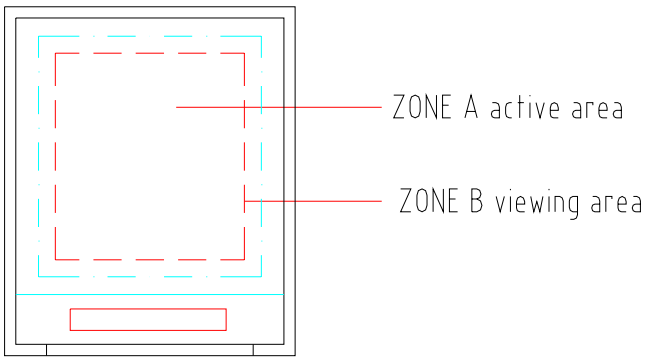
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

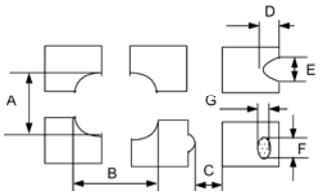
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



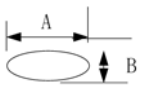
11.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defec</th><th>Accept able level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>2</td><td>Scratch,Dent of Plastic Mold</td><td>Serious one is not allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>3</td><td>Scratch on FPC</td><td>By limited sample</td><td>Major</td><td>0.65</td></tr>
<tr><td>4</td><td>Dot Defect</td><td><table><tr><th>Item</th><th>Number</th></tr><tr><td>Bright dot defect</td><td>N ≦ 0</td></tr><tr><td>Black dot defect</td><td>N ≦ 2</td></tr><tr><td>Total</td><td>N ≦ 2</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>5</td><td>Line Defect</td><td>None</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Uneven Brightness : Line Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>7</td><td>Uneven Brightness : Dot Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>8</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot</td><td>Minor</td><td>1.5</td></tr>
<tr><td>9</td><td>Scratch of Polarizer :Dot Shape s
Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.1
0.1 < D ≤ 0.3
0.3 < D</td><td>Ignore
3
0</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr>
<td>10</td>
<td>Scratch of Polarizer :

Line Shape

  </td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.05</td><td>L ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.1<W≤0.05</td><td>0.3 < L ≤ 2.0</td><td>N≦3.</td></tr>
<tr><td>0.1<W</td><td>-</td><td>See dot shape</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>11</td>
<td>Bubble in polarizer</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.30 < D ≤ 0.50</td><td>1</td></tr>
<tr><td>0.50 < D</td><td>0</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>12</td>
<td>Stains inclusion : Line shape</td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.04</td><td>Ignore</td><td>Not Allowed</td></tr>
<tr><td>0.04<W≤0.06</td><td>L ≤ 0.8</td><td>Not Allowed</td></tr>
<tr><td>0.06<W</td><td>-</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>13</td>
<td>Stains inclusion : dot shape</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.1</td><td>Not Allowed</td></tr>
<tr><td>0.1 < D ≤ 0.2</td><td>Not Allowed</td></tr>
<tr><td>0.25< D</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
</table>

11.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	60±3°C , t=72 hrs	
Low Temperature Operation	-10±3°C , t=72 hrs	
High Temperature Storage	70±3°C , t=72hrs	1,2
Low Temperature Storage	-20±3°C , t=72 hrs	1,2
Humidity Test	40°C , Humidity 90%, 72 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge ±5kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 USE PRECAUTIONS

12.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

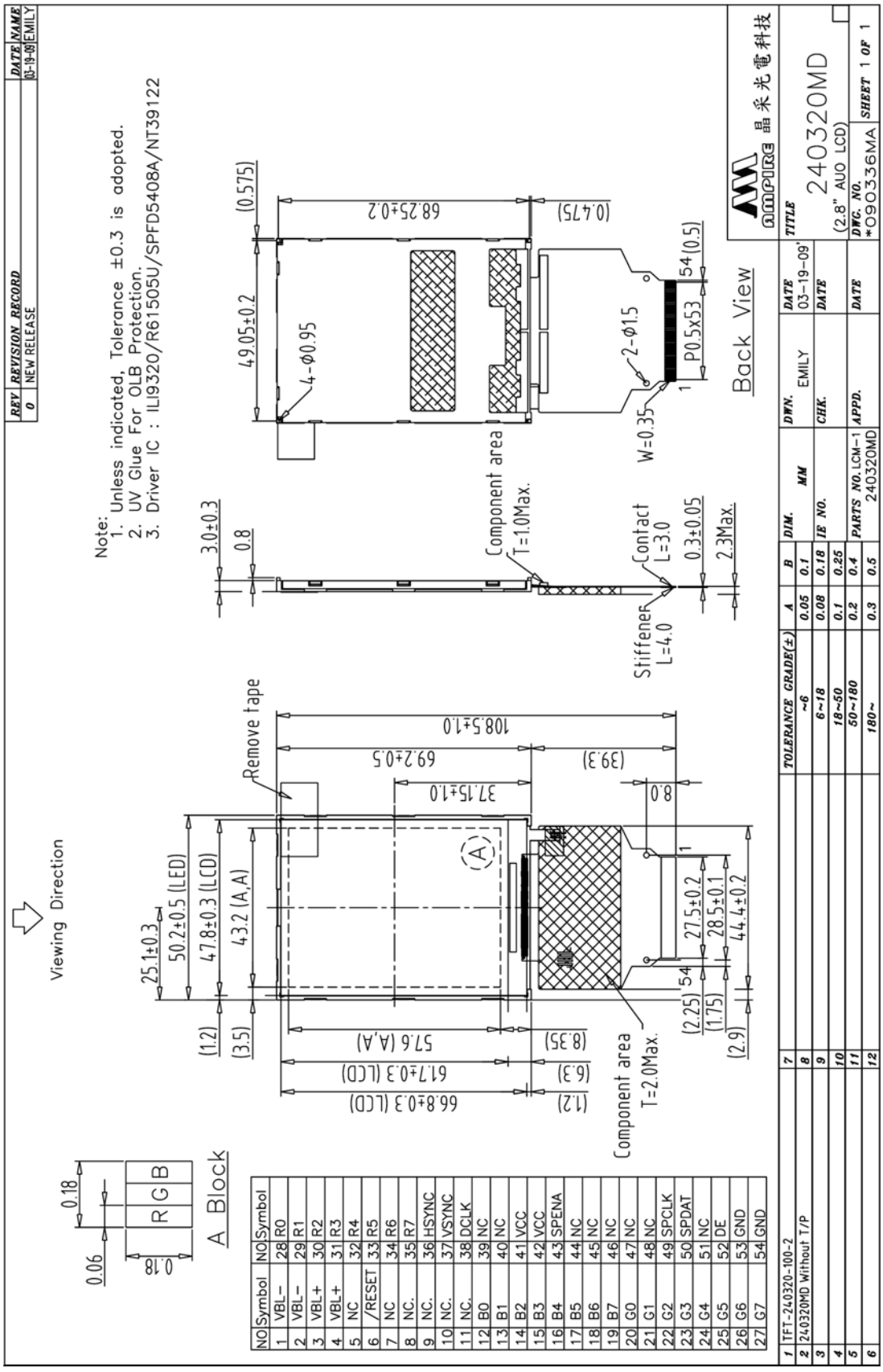
1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.

7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

13. MECHANIC DRAWING



NO	Symbol	NO	Symbol
1	VBL−	28	R0
2	VBL−	29	R1
3	VBL+	30	R2
4	VBL+	31	R3
5	NC	32	R4
6	/RESET	33	R5
7	NC	34	R6
8	NC.	35	R7
9	NC.	36	HSYNC
10	NC.	37	VSYNC
11	NC.	38	DCLK
12	B0	39	NC
13	B1	40	NC
14	B2	41	VCC
15	B3	42	VCC
16	B4	43	SPENA
17	B5	44	NC
18	B6	45	NC
19	B7	46	NC
20	G0	47	NC
21	G1	48	NC
22	G2	49	SPCLK
23	G3	50	SPDAT
24	G4	51	NC
25	G5	52	DE
26	G6	53	GND
27	G7	54	GND

TOLERANCE GRADE(±)	A	B
~6	0.05	0.1
6~18	0.08	0.18
18~50	0.1	0.25
50~180	0.2	0.4
180~	0.3	0.5

DIM. MM
IB NO.