Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

Revision Record

REV NO.	REV DATE	CONTENTS	Note
A	2015-07-01	NEW ISSUE	
B	2016-09-08	Remove the double-sided adhesive	
C	2018-01-10	Change P.6 pin41 and pin42	

Table of Contents

1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.
If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Information

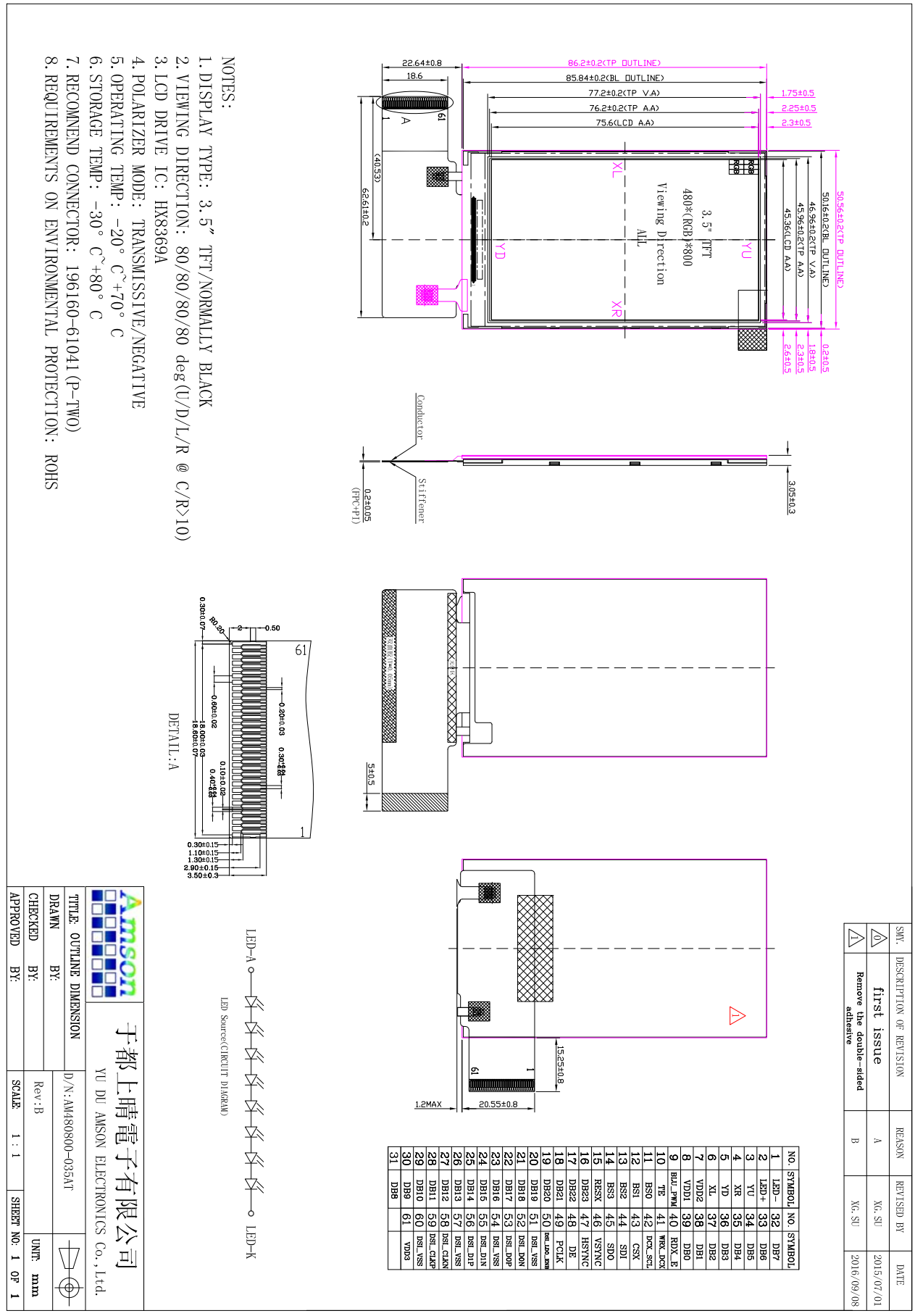
LCM

ITEM	STANDARD VALUES	UNITS
LCD type	3.5”TFT	--
Dot arrangement	480(RGB)×800	dots
Color filter array	RGB vertical stripe	--
Display mode	IPS / Transmission / Normally Black	-
Viewing Direction	80/80/80/80 deg(U/D/L/R @ C/R>10)	--
Driver IC	HX8369A	--
Module size	50.56(W)×86.20(H)×3.05(T)	mm
Active area	45.36(W)×75.60(H)	mm
Dot pitch	0.0945(W)×0.0945(H)	mm
Interface	8/ 9/16/18-bit i80-series system interface SPI + 16/18/24-bit RGB interface SPI + MIPI interface	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	8 White LED	--
Weight	TBD	g

RTP

ITEM	STANDARD VALUES	UNITS
RTP type	Film + Glass + FPC	--
Surface hardness	3H	--
Transmittance	≥80％	--
RTP size	50.56 (W)×86.20 (H)×1.2(T)	mm
Active area	45.96(W)×76.20 (H)	mm
Response Time	≤10ms	ms
Linearity	≤1.5%	%
Hitting Life	≥1000000times	Times
Insulation resistance	>20MΩ	MΩ
Operation force	≤120g	g
Resistance	X:300Ω ~ 900Ω Y:200Ω ~ 500Ω	Ω

3. External Dimensions



NO.	SYMBOL	NO.	SYMBOL
1	LED-	32	DB7
2	LED+	33	DB6
3	YU	34	DB5
4	XR	35	DB4
5	YD	36	DB3
6	XL	37	DB2
7	VDD2	38	DB1
8	VDD1	39	DB0
9	BKL_PWM	40	RDX_E
10	TE	41	WRX_DCX
11	BS0	42	DCX_SCL
12	BS1	43	CSX
13	BS2	44	SDI
14	BS3	45	SDO
15	RESX	46	VSYNC
16	DB23	47	HSYNC
17	DB22	48	DE
18	DB21	49	PCLK
19	DB20	50	DSI_LDO_EN
20	DB19	51	DSI_VSS
21	DB18	52	DSI_DON
22	DB17	53	DSI_DOP
23	DB16	54	DSI_VSS
24	DB15	55	DSI_DIN
25	DB14	56	DSI_DIP
26	DB13	57	DSI_VSS
27	DB12	58	DSI_CLKN
28	DB11	59	DSI_CLKP
29	DB10	60	DSI_VSS
30	DB9	61	VDD3
31	DB8		

4. Interface Description

PIN	PIN NAME	DESCRIPTION
1	LEDK	LED backlight (Cathode).
2	LEDA	LED backlight (Anode).
3	YU	Touch pin.
4	XR	
5	YD	
6	XL	
7	VDD2	A supply voltage to the analog circuit.
8	VDD1	A supply voltage to the I/O circuit.
9	BLU_PWM	Backlight on/off control pin. If use CABC function, the pin can Connect to external LED driver IC. Please refer to Brightness control block.
10	TE	Output a frame head pulse signal.
11	BS0	MPU interface mode selection signal. Must be connected to GND or VDD1.For the details, please refer to NOTE3
12	BS1	
13	BS2	
14	BS3	
15	RESX	Reset input pin, Active “L”.
16~39	DB[23:00]	Data bus. For the connection condition of the MPU & RGB Interface mode, please refer to NOTE3
40	RDX_E	DBI Type-A: 0: Read/Write disable, 1: Read / Write enable. DBI Type-B: a read signal and read data at the low level.
41	WRX_DCX	Writes strobe signal to write data when WRX is “Low” in MPU I/F. Data / Command Selection pin in 4-wire SPI I/F.
42	DCX_SCL	Display data / command selection in 80-series MPU I/F. A synchronous clock signal in SPI I/F.
43	CSX	Chip select input pin (“Low” enable) in MPU I/F and SPI I/F.
44	SDI	Serial input signal in SPI I/F.
45	SDO	Serial output signal in SPI I/F.
46	VSYNC	Vertical sync signal in RGB I/F.
47	HSYNC	Horizontal sync signal in RGB I/F.
48	DE	Data enable signal in RGB I/F mode
49	PCLK	Pixel clock signal in RGB I/F.
50	DSI_LDO_ENB	DSI I/F: Control signal of DSI_LDO. The default setting is Low. High: Disable the DSI_LDO. Low: Enable the DSI_LDO. It must be connected to VDD1 or GND. (latch type)
51	DSI_VSS	Ground.
52	DSI_D0P	MIPI-DSI Data differential signal input pins. (Data lane 0)
53	DSI_D0N	MIPI-DSI Data differential signal input pins. (Data lane 0)
54	DSI_VSS	Ground.
55	DSI_D1P	MIPI-DSI Data differential signal input pins. (Data lane 1)
56	DSI_D1N	MIPI-DSI Data differential signal input pins. (Data lane 1)

57	DSI_VSS	Ground.
58	DSI_CLKP	MIPI-DSI CLOCK differential signal input pins.
59	DSI_CLKN	MIPI-DSI CLOCK differential signal input pins.
60	DSI_VSS	Ground.
61	VDD3	A supply voltage to the logic circuit.

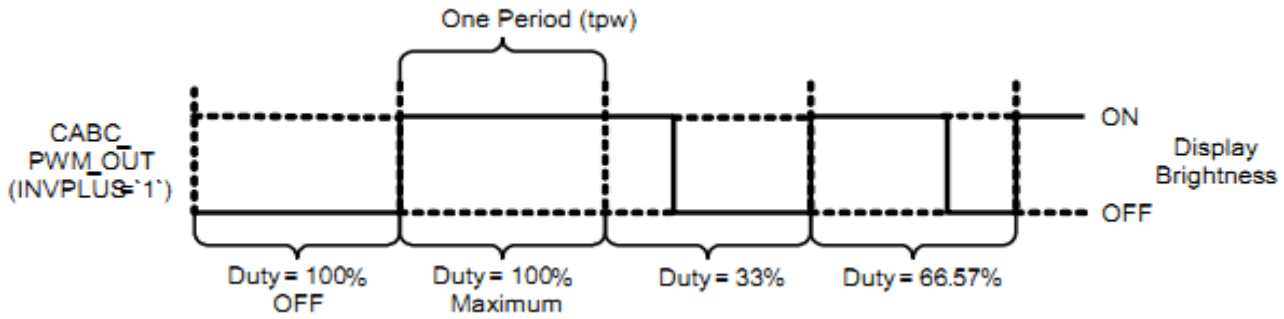
Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness .

There are resister bits, DBV [7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as (DBV [7:0])/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period=2.95 ms, and DBV [7:0] (R51h)='228DEC' and CABC duty is 74%. Then CABC_PWM_OUT duty=(228) / 255 x 74.42%º66.54%. Correspond to the CABC_PWM_OUT period=2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT

=0.99ms.



CABC_PWM_OUT output duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

CABC timing table

Note1: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Note2: The pulse width range by setting CABC related registers is locate between 0.0333ms to 8.33ms.

When Architecture II module is used (BL='0') with the example below, the

CABC_PWM_OUT is always output low and the DBV [7:0] (R51h) will be read a value as 169DEC ((169)/255º 66.27%).

NOTE3:

BS3	BS2	BS1	BS0	MPU interface mode	DB pins	Display mode
0	0	0	0	DBI TYPE-A 8-bit (CLK-E)	DB23-DB8: Unused, DB7-DB0: Data	Type 1
0	0	0	1	DBI TYPE-A 9-bit (CLK-E)	DB23-DB9:Unused, DB8-DB0: Data	Type 1
0	0	1	0	DBI TYPE-A 16-bit (CLK-E)	DB23-DB16: Unused, DB15-DB0: Data	Type 1
0	0	1	1	DBI TYPE-A 18-bit (CLK-E)	DB23-DB18: Unused, DB17-DB0: Data	Type 1
0	1	0	0	DBI TYPE-B 8-bit	DB23-DB8: Unused DB7-DB0: Data	Type 1
0	1	0	1	DBI TYPE-B 9-bit	DB23-DB9:Unused, DB8-DB0: Data	Type 1
0	1	1	0	DBI TYPE-B 16-bit	DB23-DB16: Unused, DB15-DB0: Data	Type 1
0	1	1	1	DBI TYPE-B 18-bit	DB23-DB18: Unused, DB17-DB0: Data	Type 1
1	0	0	0	DSI (Command mode)	DSI_CLKP, DSI_CLKN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N	Type 1
1	0	0	1	3-wire serial + MDDI interface (note 1)	MDDI _STBP, MDDI _STBN, MDDI _D0P, MDDI _D0N, MDDI _D1P, MDDI _D1N,	-
1	0	1	0	DBI TYPE-B 24-bit	DB23-DB0: Data	Type 1
1	1	0	0	DSI (Video mode)	DSI_CLKP, DSI_CLKN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N	Type 3
1	1	0	1	DPI/DBI TYPE-C Option 1	SDI/SDO, DB23-DB0	Type 3
1	1	1	0	DPI/DBI TYPE-C Option 2	SDI/SDO, DB23-DB0	Type 3
1	1	1	1	DPI/DBI TYPE-C Option 3	SDI/SDO, DB23-DB0	Type 3

5. Absolute Maximum Ratings

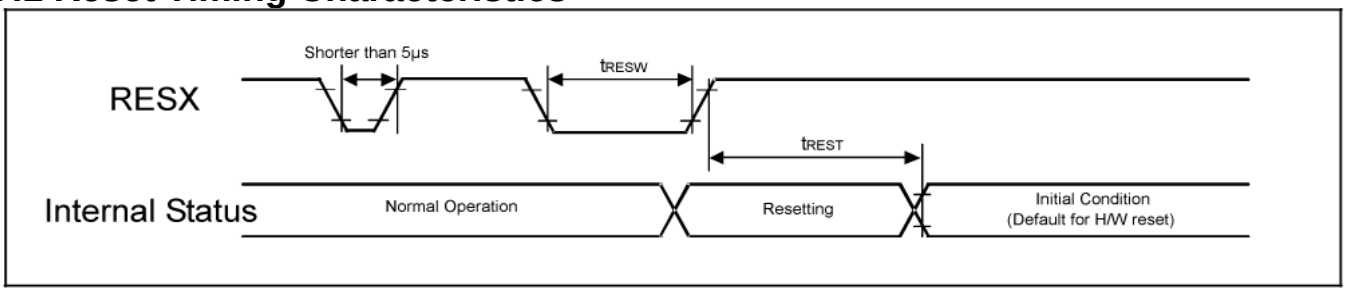
Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	VDD1	-0.3	3.6	V
Analog Supply Voltage	VDD2,3	-0.3	5.5	V
Input Voltage	Vin	-0.3	VDD1+0.3	V
Operating Temperature	TOP	-20	70	°C
Storage Temperature	TST	-30	80	°C
Storage Humidity	HD	20	90	%RH

6. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic Supply Voltage	VDD1	1.65	1.8/2.8	3.3	V	-
Analog Supply Voltage	VDD2,3	2.3	2.8	3.3	V	-
Input High Voltage	V_{IH}	0.7VDD1	-	IVDD1	V	-
Input Low Voltage	V_{IL}	GND	-	0.3VDD1	V	-
Output High Voltage	V_{OH}	0.8VDD1	-	VDD1	V	-
Output Low Voltage	V_{OL}	GND	-	0.2VDD1	V	-
I/O Leak Current	ILI	-1	-	1	uA	-

7. Timing Characteristics

7.1 Reset Timing Characteristics

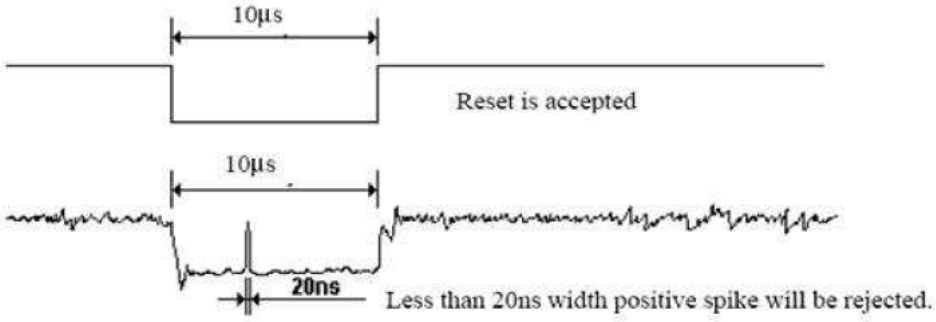


Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

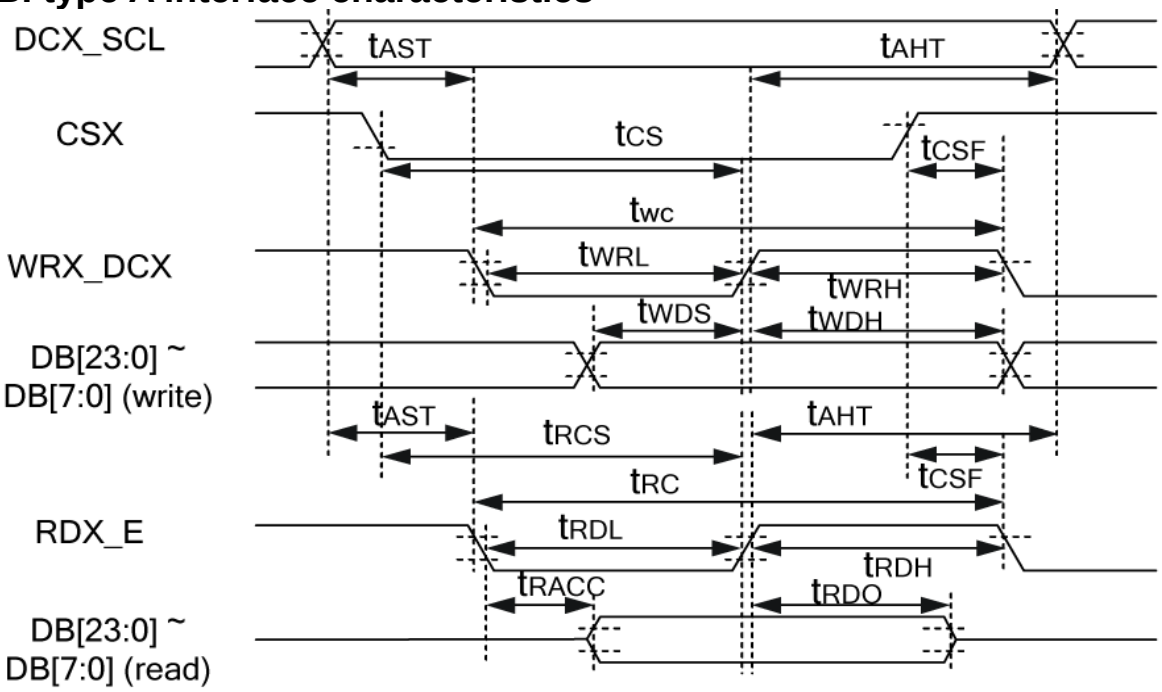
(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.2 i80-System Interface Timing Characteristics

7.2.1 DBI type A interface characteristics

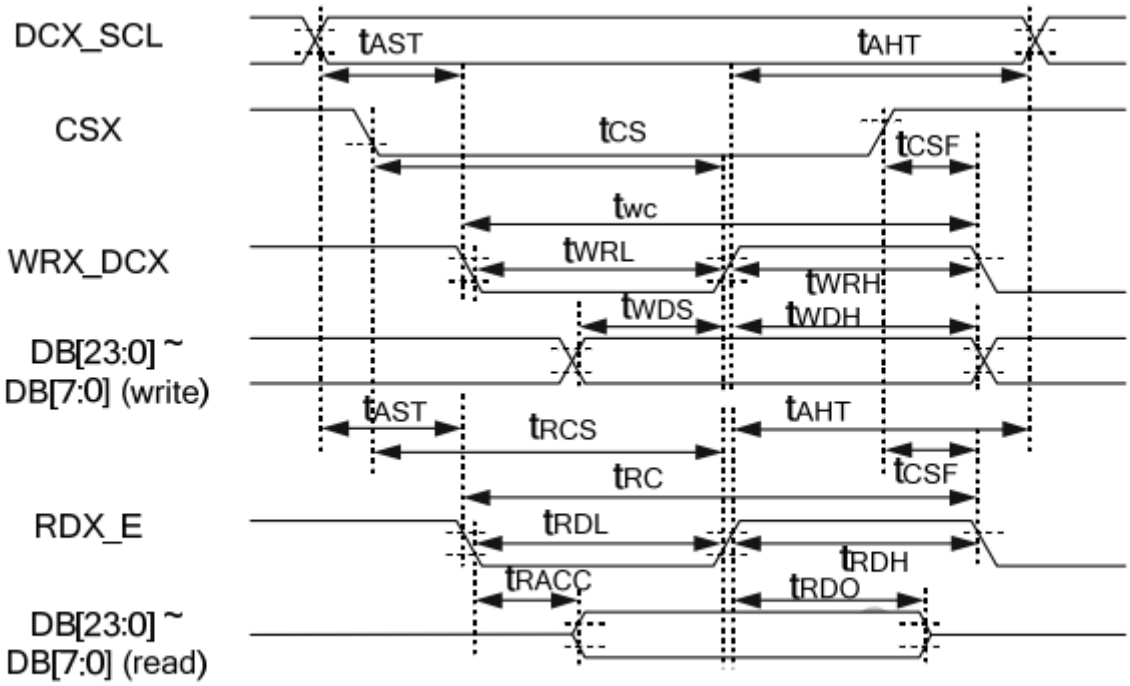


(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX_SCL	t_{AST}	Address setup time	10	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
CSX	t_{CS}	Chip select setup time (Write)	20	-	ns	-
	t_{RCS}	Chip select setup time (Read ID)	45	-		
	t_{RCSFM}	Chip Select setup time (Read FM)	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	20	-		
WRX_DCX	t_{WC}	Write cycle (write register)	100	790	ns	-
	t_{WC}	Write cycle (write GRAM@SLPOUT)	33	790		
	t_{WC}	Write cycle (write GRAM@SLPIN)	100	790		
	t_{WRH}	Control pulse “H” duration	15	630		
	t_{WRL}	Control pulse “L” duration	15	160		
RDX_E	t_{RC}	Read cycle (read register)	100	790	ns	-
	t_{RC}	Read cycle (GRAM)	350	790		
	t_{RDH}	Control pulse “H” duration	30	630		
	t_{RDL}	Control pulse “L” duration	20	160		
DB23-DB0	t_{WDS}	Data setup time	15	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{WDH}	Data hold time	25	-		
	t_{RACC}	Read access time	10	-		
	t_{RDO}	Output disable time	10	-		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

7.2.2 DBI type B interface characteristics



DBI Type B interface characteristics

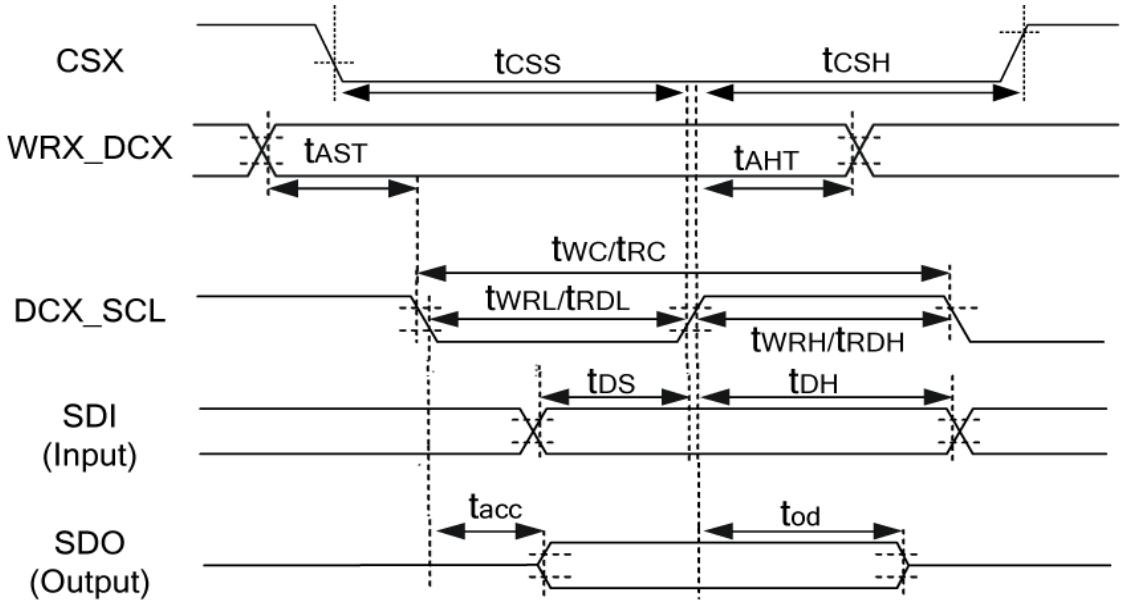
(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX_SCL	tAST tAHT	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
CSX	tCS tRCS tRCSFM tCSF	Chip select setup time (Write) Chip select setup time (Read ID) Chip Select setup time (Read FM) Chip select wait time (Write/Read)	20 45 355 20	- - - -	ns	-
WRX_DCX	twc twc twc tWRH tWRL	Write cycle (write register) Write cycle (write GRAM@SLPOUT) Write cycle (write GRAM@SLPIN) Control pulse "H" duration Control pulse "L" duration	100 33 100 15 15	790 790 790 630 160	ns	-
RDX_E	tRC tRC tRDH tRDL	Read cycle (read register) Read cycle (GRAM) Control pulse "H" duration Control pulse "L" duration	100 350 30 20	790 790 630 160	ns	-
DB23-DB0	tWDS tWDH tRACC tRDO	Data setup time Data hold time Read access time Output disable time	15 25 10 10	- - - -	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

DBI Type B interface characteristics

7.3 Display Serial Interface Timing Characteristics

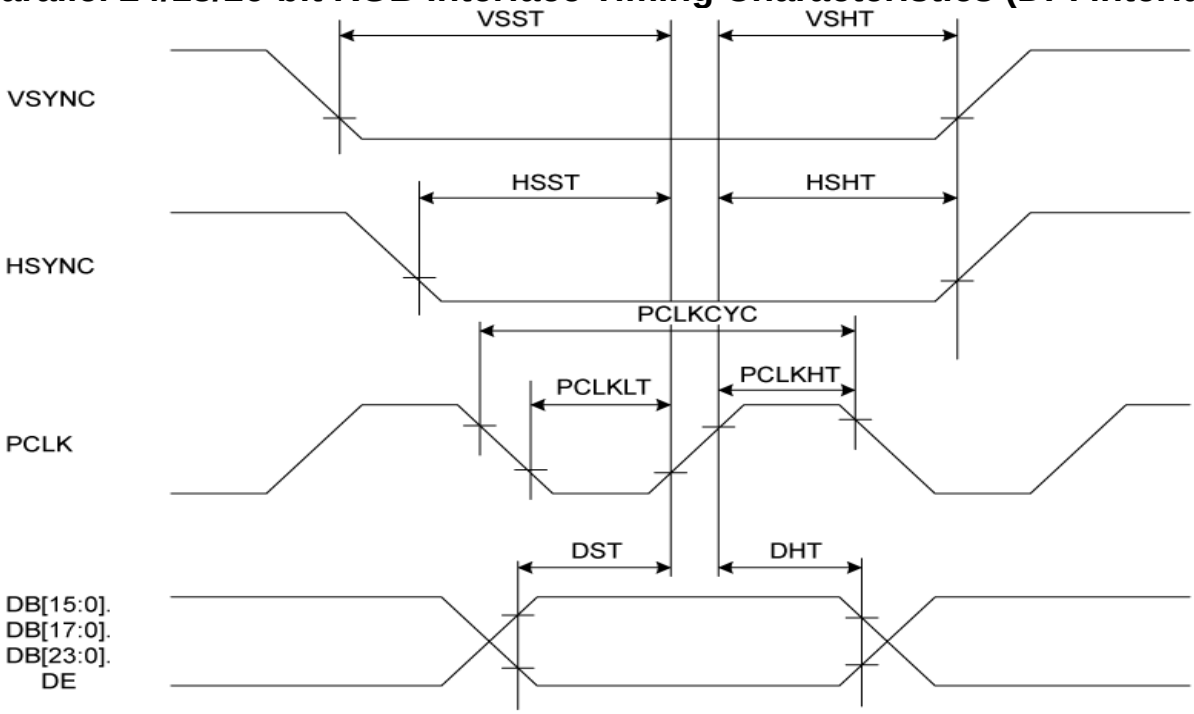


(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A = 25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS} t_{CSH}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
WRX_DCX	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
DCX_SCL (Write)	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 40 40	- - -	ns	-
DCX_SCL (Read)	t_{RC} t_{RDH} t_{RDL}	Read cycle Control pulse “H” duration Control pulse “L” duration	150 60 60	- - -	ns	-
SDI/SDO (Input)	t_{DS} t_{DT}	Data setup time Data hold time	30 30	- -	ns	For maximum C_L=30pF For minimum C_L=8pF
SDI/SDO (Output)	t_{RACC} t_{OD}	Read access time Output disable time	10 10	- 50	ns	

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

7.4 Parallel 24/18/16-bit RGB Interface Timing Characteristics (DPI interface)

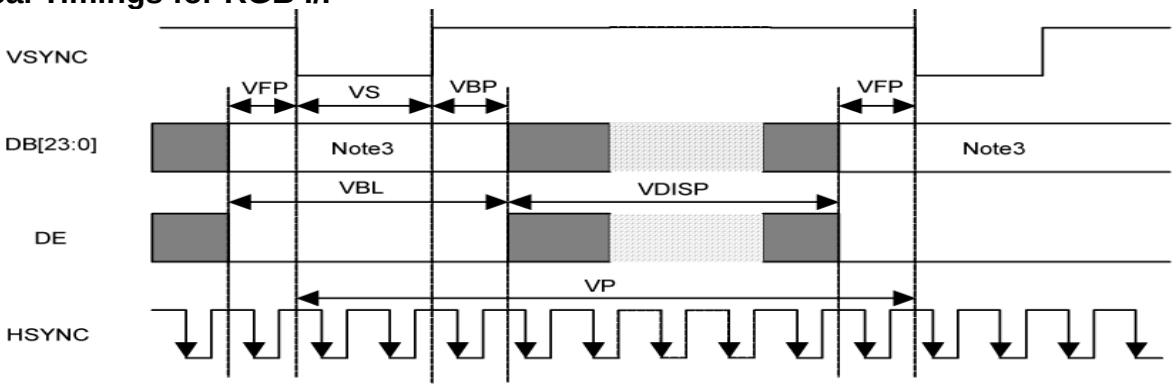


Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	5	-	-	ns
Vertical sync. hold time	VSHT	-	5	-	-	ns
Horizontal sync. setup time	HSST	-	5	-	-	ns
Horizontal sync. hold time	HSHT	-	5	-	-	ns
Pixel clock cycle when RGB I/F is running	PCLKCYC	VRR(5) = Min . 50 Hz Max. 70 Hz	31(3)	-	49.2(4)	ns
Pixel clock low time	PCLKLT	-	5	-	-	ns
Pixel clock high time	PCLKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) 32.2 MHz
(4) 20.3 MHz
(5) VRR : Vertical Refresh Rate, equal to VSYNC frequency.

Vertical Timings for RGB I/F

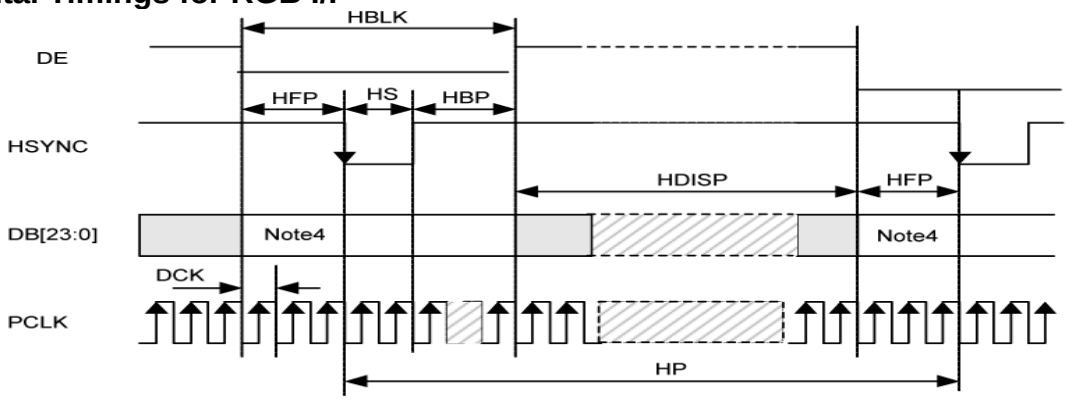


Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for highstate.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) The VS and VBP pulse width are related to ASG/GIP STV and CKV timing. The STV and CKV must be set at corresponding position for LCD normal display. Also refer to setion 6.2.66 SETGIP.

Horizontal Timings for RGB I/F



Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note 3	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency When RGB I/F is running	DCK	VRR = Min. 50 Hz – Max. 70 Hz	20.3	-	32.2	MHz
			31	-	49.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) HP is multiples of eight DCK.
(4)Data lines can be set to "High" or "Low" during blanking time – Don't care.

7.5 MDDI electrical Characteristics

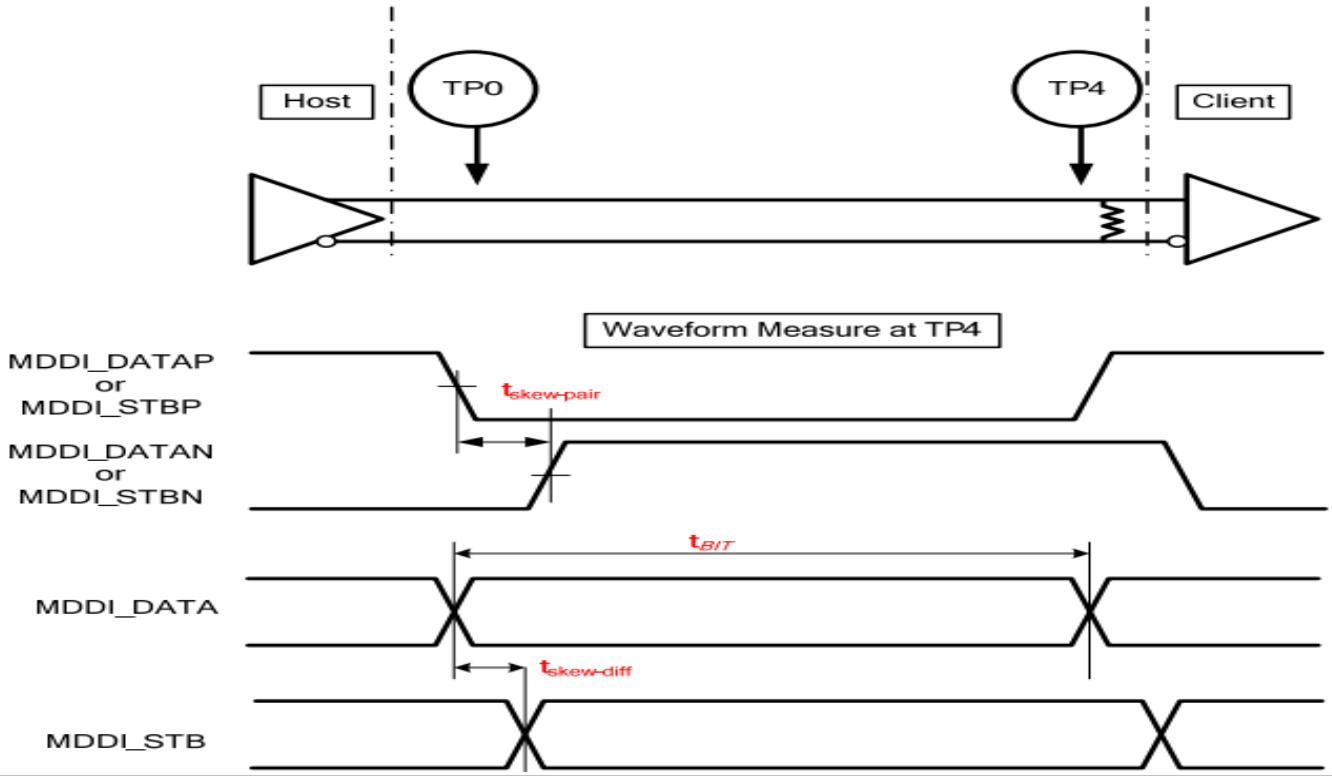
7.5.1 DC Characteristics

DC characteristic:

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.	-	0	50	mV
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as a logic-zero level.	-50	0	-	-
V_{IT+_hib}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.	-	100	125	mV
V_{IT-_hib}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as a logic-zero level.	75	100	-	mV
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0. 5	-	1.2	V

7.5.2 AC Characteristics

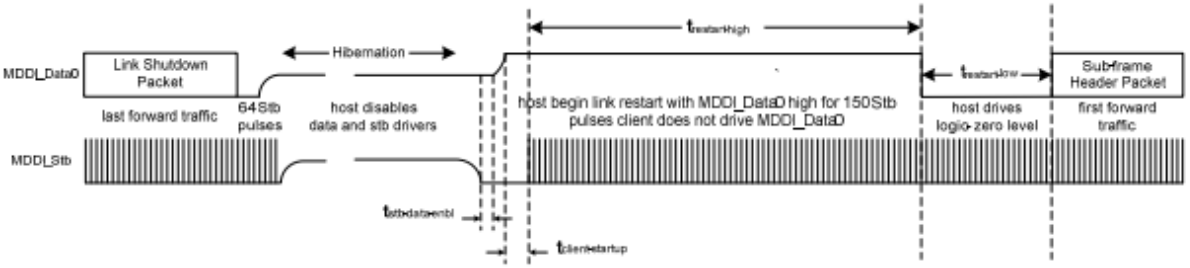
AC characteristic:



Parameter	Description	Min.	Typ.	Max.	Unit
$1/t_{BIT}$	MDDI operate speed	50	350	400	Mbps
$t_{skew-pair}$	Skew between positive and negative inputs of the differential receiver of the same differential pair (intra-pair skew)	-0.05	0	0.05	ns
$t_{skew-diff}$	Peak delay skew between one differential pair and any other differential pair	-0.45 t_{BIT}	0	0.45 t_{BIT}	ns
$t_{Rise-Fall}$	Rise/Fall time(20%-80% of swing)	200	-	Note(1)	ps

Note : The maximum rise and fall time is either 35% of the interval to transmit one bit on one differential pair or 100 nsec, hichever is smaller.

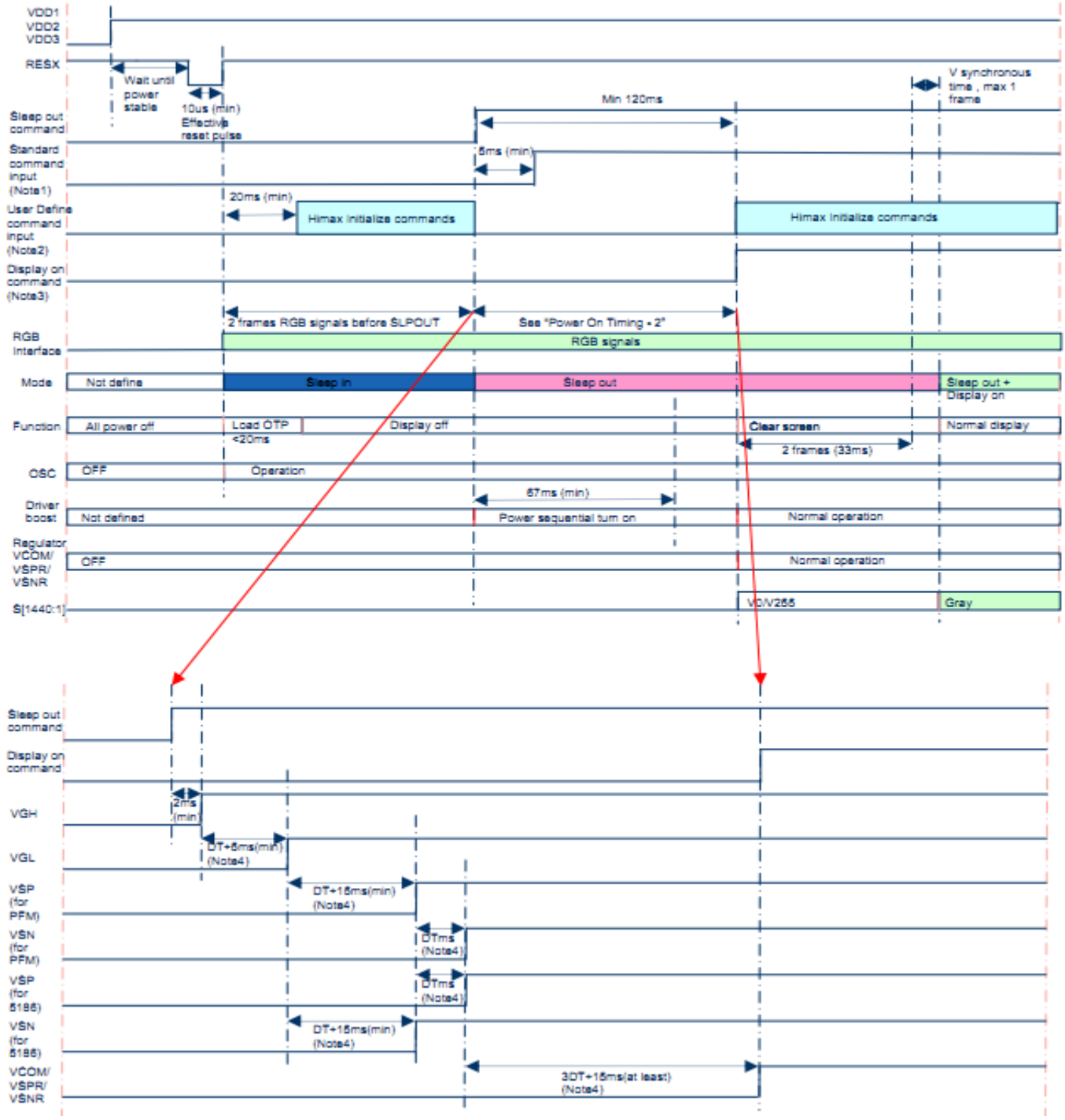
Host-Initiated Wake-up



Parameter	Description	Min.	Typ.	Max.	Unit
$t_{restart\text{-}high}$	Duration of host link restart high pulse	140	150	250	Stb clock
$t_{restart\text{-}low}$	Duration of host link restart low pulse	50	50	50	Stb clock
$t_{stb\text{-}data\text{-}enbl}$	MDDI_Stb completely enabled to MDDI_Data0 enabled	0	-	-	μsec
$t_{client\text{-}startup}$	Time for host to hold MDDI_Stb at logic-zero level after MDDI_Data0 reaches logic-high level	200	-	-	nsec

7.6 DPI Interface Power On/Off Timing

Power On Timing



Note1:
"Standard" command except "01h" & "10h" command must wait 5ms after "Sleep out" command then can be sent. "01h" & "10h" command must wait 100ms after "Sleep out" command then can be sent.

Note2:
"User Define" command must be sent "B9h" first then other commands can be available.

Note3:
"Display on" command must send after "User Define" command or at the same time.

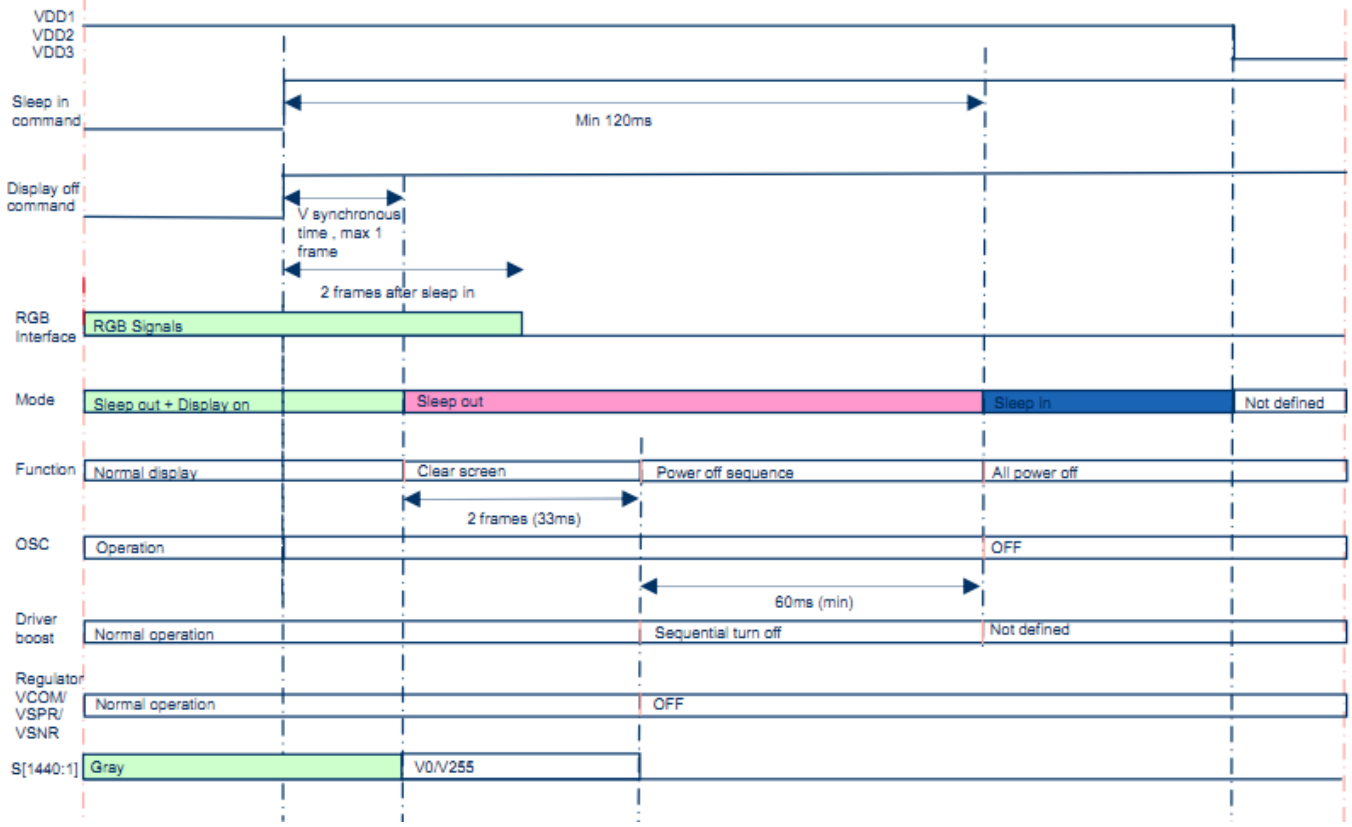
Note4:

DT[1:0]:Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

Default DT=5ms

Power Off Timing



8. Backlight Characteristics

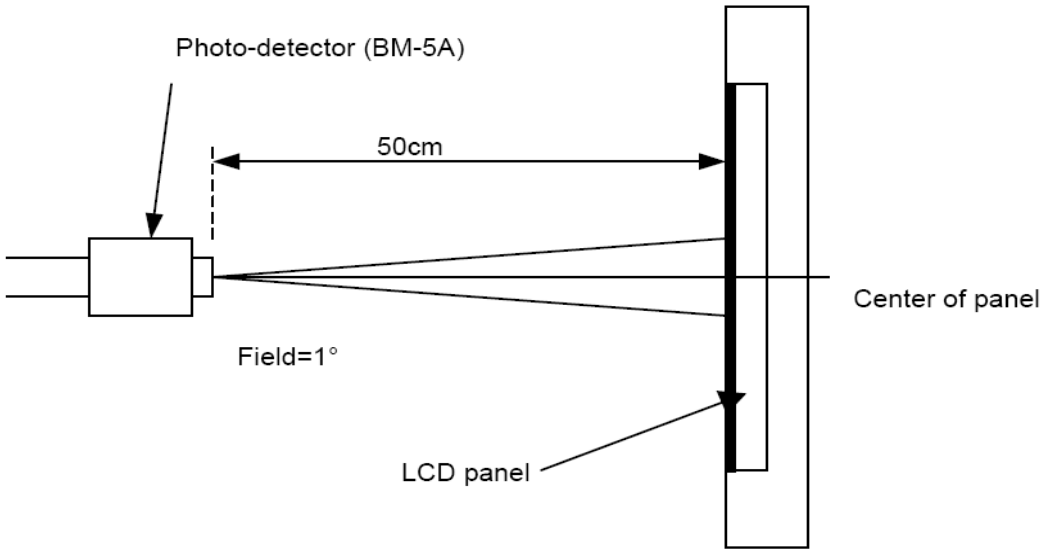
LED CIRCUIT:

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	23.2	25.6	28	V	If=20mA
Supply Current	If	-	20	-	mA	-
Luminous Intensity for LCM	-	300	350	-	cd/m^2	If=20mA
Uniformity for LCM	-	80	-	-	%	If=20mA
Life Time	-	-	50000	-	Hr	If=20mA
Backlight Color	White					

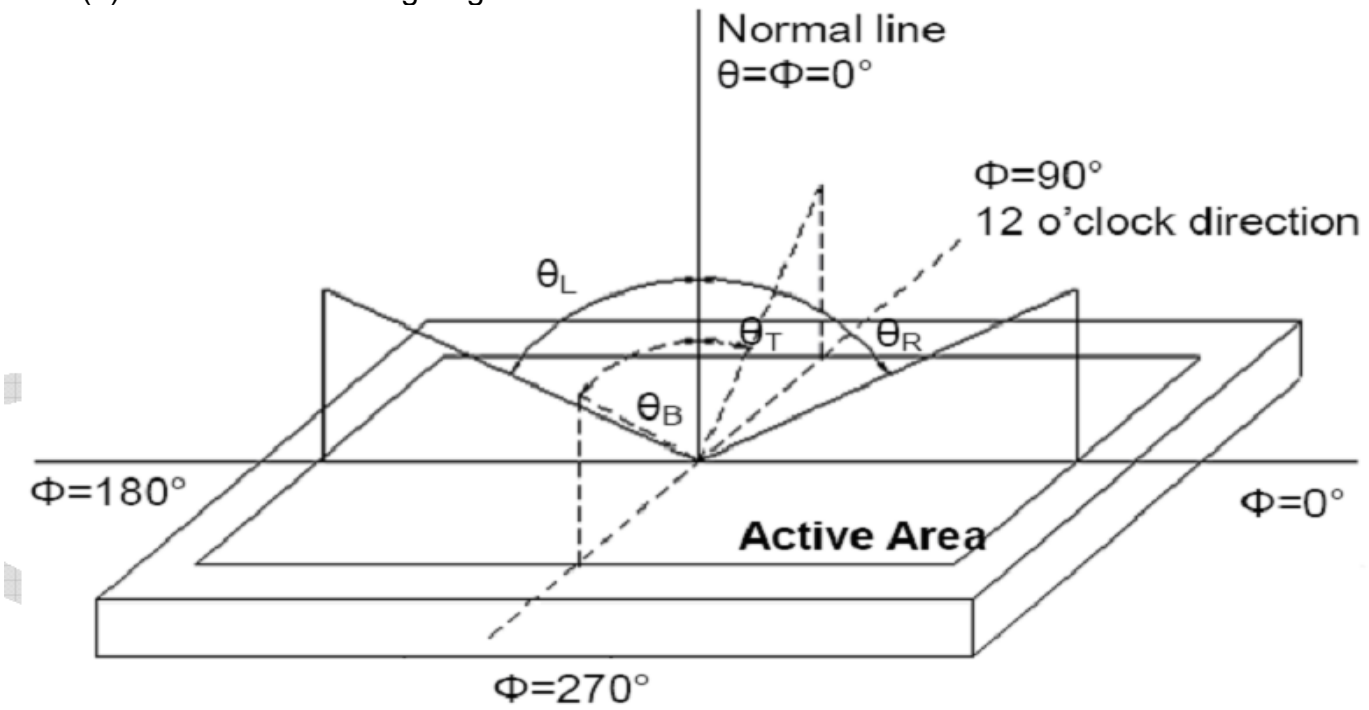
9. Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	θ_L	70	80	-	degree	(1),(2),(6)
		θ_R	70	80	-		
	Vertical	θ_T	70	80	-		
		θ_B	70	80	-		
Contrast Ratio	Center		-	800	-	-	(1),(3),(6)
Response Time	Rising + Falling		-	33	40	ms	(1),(4),(6)
CF Color Chromaticity (CIE1931)	Red x		Typ. -0.05	0.61	Typ. +0.05	-	(1), (6)
	Red y			0.35		-	
	Green x			0.29		-	
	Green y			0.56		-	
	Blue x			0.14		-	
	Blue y			0.06		-	
	White x			0.27		-	
	White y			0.29		-	

Note (1) Measurement Setup: The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



Note (2) Definition of Viewing Angle



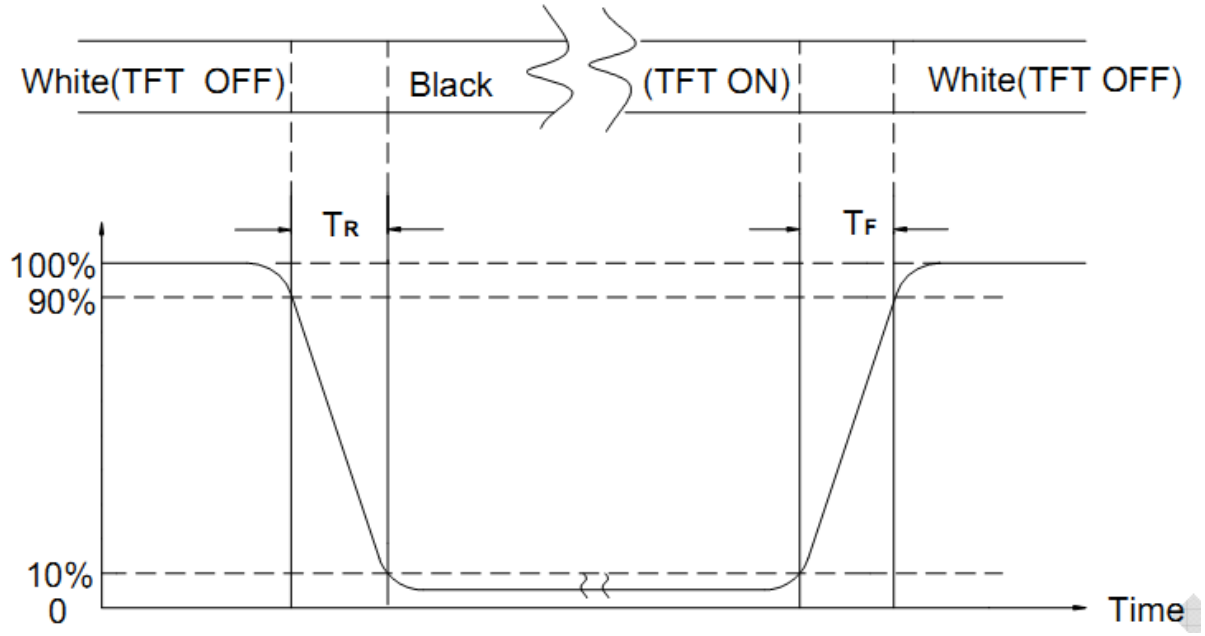
Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition of response time



Note (5) Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

Note (6) Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD

10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
□	High Temperature Storage	80°C±2°C×200Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
□	Low Temperature Storage	-30°C±2°C×200Hours	
□	High Temperature Operating	70°C±2°C×120Hours	
□	Low Temperature Operating	-20°C±2°C×120Hours	
□	Temperature Cycle(Storage)	-20°C ⟺ 25°C ⟺ 70°C (30min) (5min) (30min) 1cycle Total 10cycle	
□	Damp Proof Test (Storage)	50°C±5°C×90%RH×120Hours	
□	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (Packing Condition)	
□	Drooping Test	Drop to the ground from 1M height one time every side of carton. (Packing Condition)	
□	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:
1, The Test samples should be applied to only one test item.
2, Sample side for each test item is 5~10pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Inspection Standard

11.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

11.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM AMSON TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10℃ TO 40℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

11.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

11.1.3. WARRANTY POLICY

AMSON WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. AMSON WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF AMSON.

11.2. CHECKING CONDITION

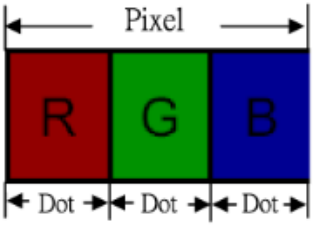
11.2.1.CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

11.2.2.CHECKER SHALL SEE OVER 300±25 mm. WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

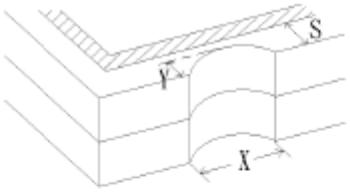
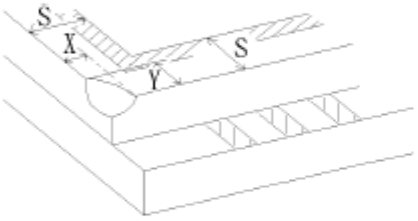
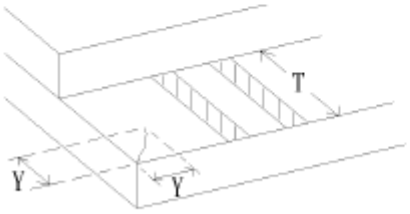
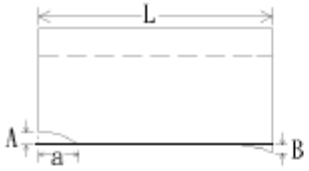
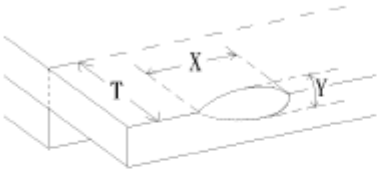
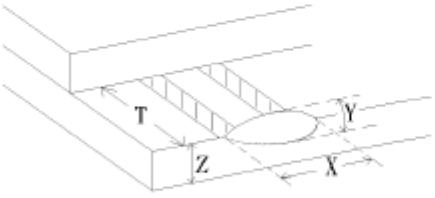
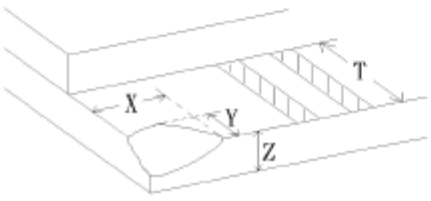
11.3. INSPECTION PLAN :

CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA .....REJECTED	Minor
	6. BLEMISH、BLACK SPOT、 WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	7. BLEMISH、BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST、VOP、 CHROMATICITY ... ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
	11.MISSING LINE	MISSING DOT、LINE、CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT、 WRONG PATTERN DISPLAY	NO DISPLAY、WRONG PATTERN DISPLAY、CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

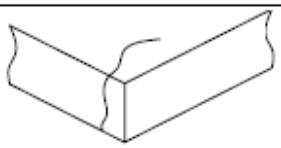
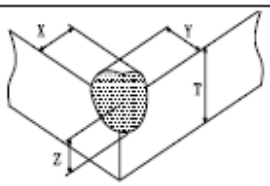
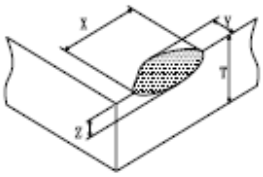
11.4. STANDARD OF VISUAL INSPECTION

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGEMENT</th></tr>
<tr><td>11.4.1</td><td>MINOR</td><td>BLACK AND WHITE SPOT
FOREIGN MATERIEL
DUST IN THE CELL
BLEMISH
SCRATCH</td><td>(A) ROUND TYPE: unit : mm.
<table>
<tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3 (Distance>5mm)</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
NOTE: Φ=(LENGTH+WIDTH)/2
(B) LINEAR TYPE: unit : mm.
<table>
<tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>------</td><td>W ≦0.03</td><td>DISREGARD</td></tr>
<tr><td>L ≦ 5.0</td><td>0.03 < W ≦0.07</td><td>3 (Distance>5mm)</td></tr>
<tr><td>------</td><td>0.07 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>11.4.2</td><td>MINOR</td><td>BUBBLE IN POLARIZER
DENT ON POLARIZER</td><td>unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.2</td><td>DISREGARD</td></tr>
<tr><td>0.2 < Φ ≦ 0.5</td><td>2 (Distance>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>11.4.3</td><td>MINOR</td><td>Dot Defect</td><td>
<table>
<tr><th>Items</th><th>ACC. Q'TY</th></tr>
<tr><td>Bright dot</td><td>N≦ 4</td></tr>
<tr><td>Dark dot</td><td>N≦ 4</td></tr>
</table>
Pixel Define :
 

Note 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
Note 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
Note 3: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green ,blue pattern.</td></tr>
</table>

NO.	CLASS	ITEM	JUDGEMENT
11.4.4	MINOR	LCD GLASS CHIPPING	 Y > S Reject
11.4.5	MINOR	LCD GLASS CHIPPING	 X or Y > S Reject
11.4.6	MAJOR	LCD GLASS GLASS CRACK	 Y > (1/2) T Reject
11.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	 1. a> L/3 , A>1.5mm. Reject 2. B : ACCORDING TO DIMENSION
11.4.8	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm Reject
11.4.9	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL SURFACE)	 Y > (1/3) T Reject
11.4.10	MINOR	LCD GLASS CHIPPING	 Y > T Reject

11.5 INSPECTION STANDARD OF TOUCH PANEL

NO.	CLASS	ITEMS		JUDGEMENT	
11.5.1	MAJOR	Touch Panel Crack			Reject
11.5.2	MINOR	Touch Panel Chipping	Corner	 X≦2mm, Y≦2mm, Z＜1/2T	Accept
			Edge	 X≦3mm, Y≦3mm, Z＜1/2T	Accept
11.5.3	MINOR	Scratch Dust and Foreign materiel (Linear Type)		W≦0.05, L≦20mm	Accept
				0.05mm<W≦0.07mm; L≦10.0mm Distance between seratch＞5.0mm	Accept 3 ea Max.
				W>0.07mm	Reject
11.5.4	MINOR	Scratch Dust and Foreign materiel (Round Type: Φ=(Length+Width)/2)		Φ≦0.25mm	Accept
				0.25mm＜Φ≦0.35mm Distance between spots＞5.0mm	Accept 5 ea Max.
				Φ＞0.35mm	Reject
11.5.5	MINOR	Touch Panel Dent / Fish Eyes		Φ≦0.35mm	Accept
				0.35mm＜Φ≦1.0mm Distance＞5.0mm	Accept 3 ea Max.
				Φ＞1.0mm	Reject
11.5.6	MINOR	Touch Panel Air Bubble		Φ≦0.2mm	Accept
				0.2mm＜Φ≦0.5mm Distance between bubbles＞5.0mm	Accept 3 ea Max.
				Φ＞0.5mm	Reject
11.5.7	MINOR	Touch Panel Printing area Scratch		W≦0.05mm, L≦5mm Distance between scratch＞5.0mm	Accept 3 ea Max.
				W＞0.05mm or L＞5mm (W>0.05 Follow 11.5.4 Round type)	Reject
11.5.8	MINOR	Touch Panel White Haze Mark / Dust		Can not be removed	Reject

12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  [It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen this is not specified in this specification.
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD