



SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-800480STMQW-TW0H
APPROVED BY	
DATE	

Approved For Specifications

Approved For Specifications & Sample

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2009/10/19	--	New Release	JOHN

1. INTRODUCTION

Ampire Display Module is a color active matrix TFT-LCD that uses amorphous silicon TFT as a switching device . This model is composed of a TFT-LCD panel ,driving circuit ,LCD Controller and touch panel. This TFT-LCD has a high resolution (800(R.G.B) X 480) and can display up to 262,144 colors .

1-1. Features

- 7" WVGA (16:9 diagonal) configuration
- Input interface voltage : 3.3V
- Interface: 40 pin pitch 0.5 FFC
- Backlight supply voltage : 5.0V

1-2. LCD Controller Feature:

- (1) MCU interface: i80/M68 series MCU interface (default: i80 series).
- (2) Pixel data format: 8, 9, 16 and 18 bit.
- (3) Display RAM size: Built-in 1215K bytes frame buffer. Support up to 864 x 480 at 24bpp display.
- (4) Arbitrary display memory starts position selection.
- (5) 16 bit interface support 65K (R5 G6 B5) Color.

2. PHYSICAL SPECIFICATIONS

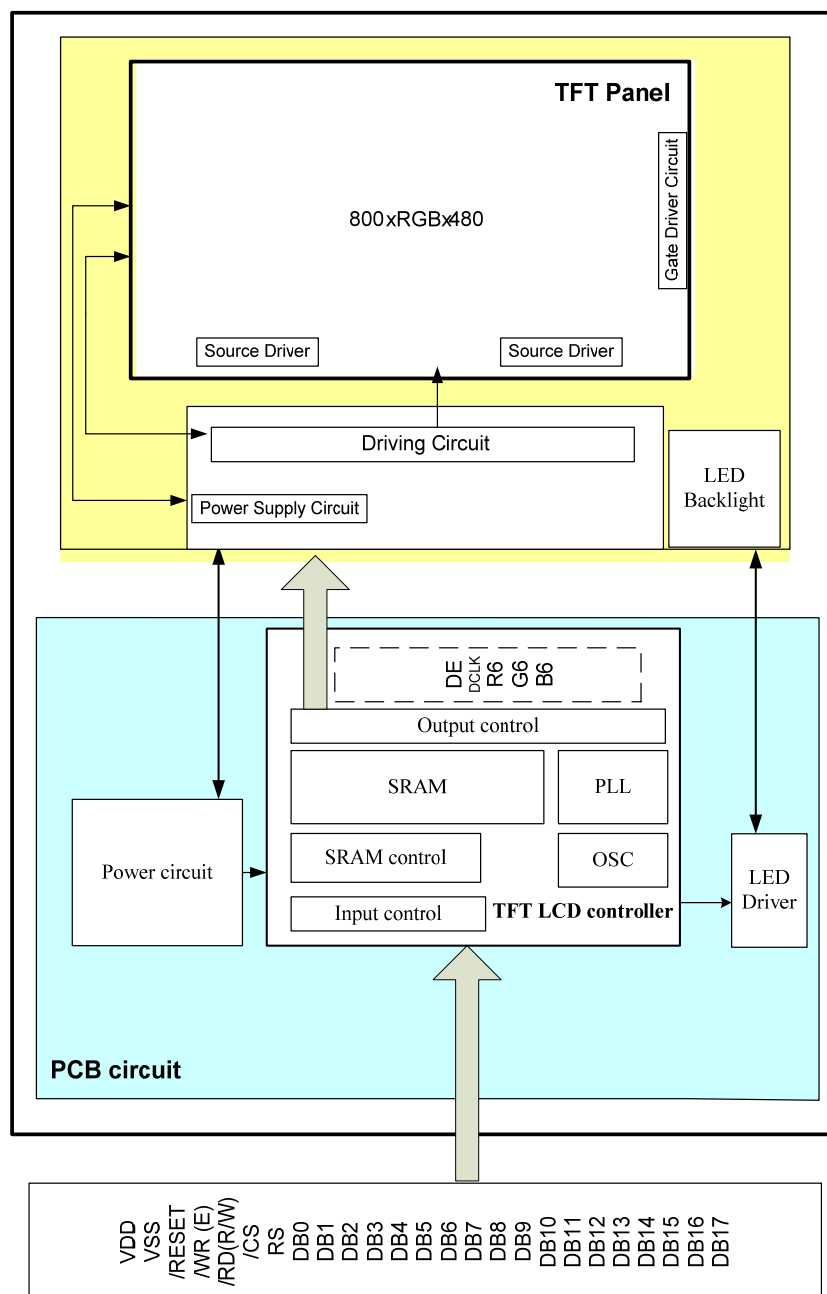
Item	Specifications	unit
Display resolution(dot)	800RGB (W) x 480(H)	dots
Active area	152.4 (W) x 91.44 (H)	mm
Pixel pitch	0.1905 (W) x 0.1905 (H)	mm
Color configuration	R.G.B Vertical stripe	
Overall dimension	165.0(W)x104.44(H)x10.72 (T)	mm
Brightness	280 nit(typ)	cd/m ²
Contrast ratio	400 : 1	
Backlight unit	LED	
Display color	262,144	colors

3. ABSOLUTE MAX. RATINGS

3.1 Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	VSS=0	-0.3	4.6	V	
Input voltage	V _{in}		-0.3	VDD+0.3	V	Note 1

Note1: /CS,/WR,/RD,RS,DB0~DB17



4. ELECTRICAL CHARACTERISTICS

4-1 DC Electrical characteristic of the LCD

(VSS=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	VDD	3.0	3.3	4	V	
Input Voltage for logic	H Level	V_{IH}	0.7 VDD	--	VDD	Note 1
	L Level	V_{IL}	VSS	--	0.3 VDD	
Power Supply current (Without B/L)	IDD	-	200	-	mA	Note 2

Note 1: /CS,/WR,/RD,RS,DB0~DB17

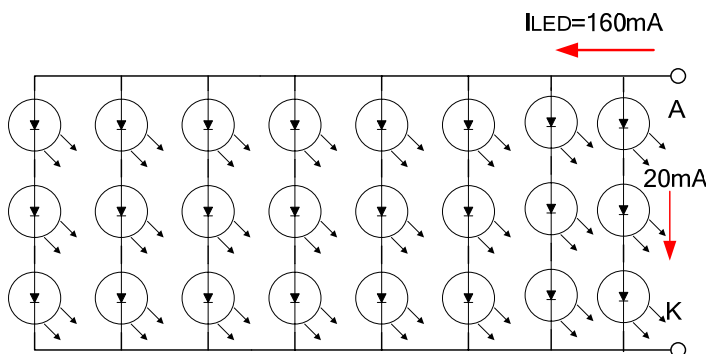
Note 2: fV =60Hz , Ta=25°C , Display pattern : All Black

4-2 Electrical characteristic of LED Back-light

Ta=25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LED voltage	V_{AK}	-	9.9	-	V	$I_{LED} = 160mA$
LED forward current	I_{LED}	--	160	-	mA	Note 1
LED DRIVER current	I_{DLED}	--	360	--	mA	$V_{LED} = 5V$
LED Life time		10000	20000		Hr	Note 2

Note 1 : There are 8 Groups LED shown as below , $V_{LED} = 9.9V$, $I_{LED} = 160mA$.



Note 2 : Brightness to be decreased to 50% of the initial value.

4-3 Touch Panel ELECTRICAL SPECIFICATION

Parameter	Condition	Standard Value
Terminal Resistance	X Axis	200 ~ 900 Ω
	Y Axis	160 ~ 640 Ω
Insulating Resistance	DC 25 V	More than 20M Ω
Linearity	--	$\leq 1.5 \%$
Notes life by Pen	Note a	100,000 times(min)
Input life by finger	Note b	1,000,000 times (min)

Note A .

Notes area for pen notes life test is 10 x 9 mm.

Size of word is 7.5 x 6.75

Shape of pen end : R0.8mm

Load : 250 g

Note B

By Silicon rubber tapping at same point

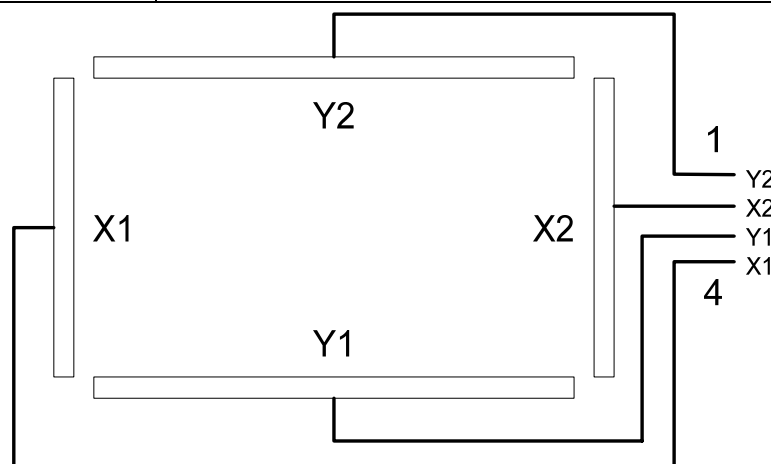
Shape of rubber end : R8mm

Load : 250gf

Frequency : 5 Hz

Interface

No.	Symbol	Function
1	Y2	Touch Panel Top Signal in Y Axis
2	X2	Touch Panel Right Signal in X Axis
3	Y1	Touch Panel Bottom Signal in Y Axis
4	X1	Touch Panel Left Signal in X Axis



5. INTERFACE

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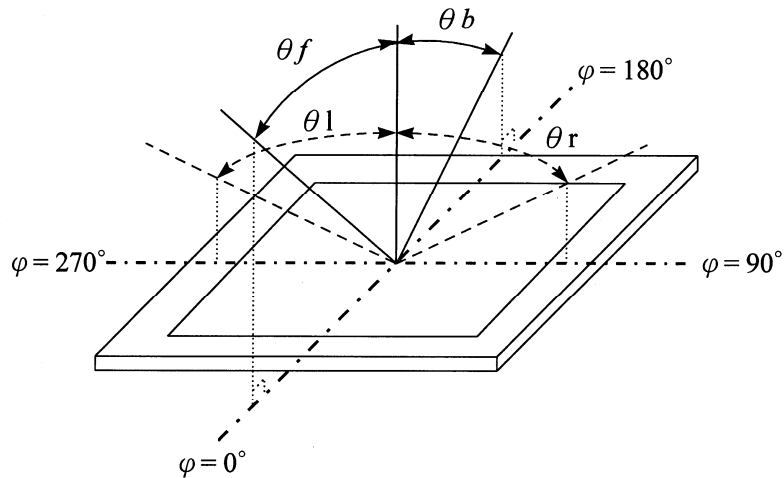
Pin no	Symbol	I/O	Description	Remark
1	DGND	-	GND	
2				
3	VLED	I	LED Power input (5V)	
4	NC	-	No connection	
5	/RESET	I	Reset signal for TFT LCD controller.	
6	RS	I	Register and Data select for TFT LCD controller.	
7	/CS	I	Chip select low active signal for TFT LCD controller.	
8	/WR	I	80mode: /WR low active signal for TFT LCD controller. 68mode: E signal latch on rising edge.	
9	/RD	I	80mode: /RD low active signal for TFT LCD controller. 68mode: R/W signal Hi: read, Lo: write.	
10	DB0	I	Data bus.	
11	DB1	I		
12	DB2	I		
13	DB3	I		
14	DB4	I		
15	DB5	I		
16	DB6	I		
17	DB7	I		
18	DB8	I		
19	DB9	I		
20	DB10	I		
21	DB11	I		
22	DB12	I		
23	DB13	I		
24	DB14	I		
25	DB15	I		
26	DB16	I		
27	DB17	I		
28	NC	-	No connection.	
29	DGND	-	GND	
30	NC	-	No connection.	
31	NC	-	No connection.	
32	NC	-	No connection.	
33	NC	-	No connection.	
34	NC	-	No connection.	
35-37	VDD	-	Power supply for the logic (3.3V).	
38-40	DGND	-	GND.	

6. OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	Front	θf	$CR \geq 10$	50	60	--	deg.	(1)(2)(3)
	Back	θb		60	70	--		
	Left	θl		60	70	--		
	Right	θr		60	70	--		
Contrast ratio		CR	$\Theta = \Phi = 0^\circ$	250	400	--	--	(1)(3)
Response Time		T_r	$\Theta = \Phi = 0^\circ$	--	5	10	ms	(1)(4)
		T_f		--	11	16	ms	(1)(4)
Color chromaticity	White	W_x	$\Theta = \Phi = 0^\circ$	0.249	0.299	0.349	--	(1)
		W_y		0.278	0.328	0.378		
Luminance		L	$\Theta = \Phi = 0^\circ$	240	280	--	cd/m ²	(1)(5)
Luminance Uniformity		ΔL	$\Theta = \Phi = 0^\circ$	70	--	--	%	(1)(5)(6)

Note 1: $T_a = 25^\circ\text{C}$. To be measured on the center area of panel after 10 minutes operation.

Note 2: Definition of Viewing Angle



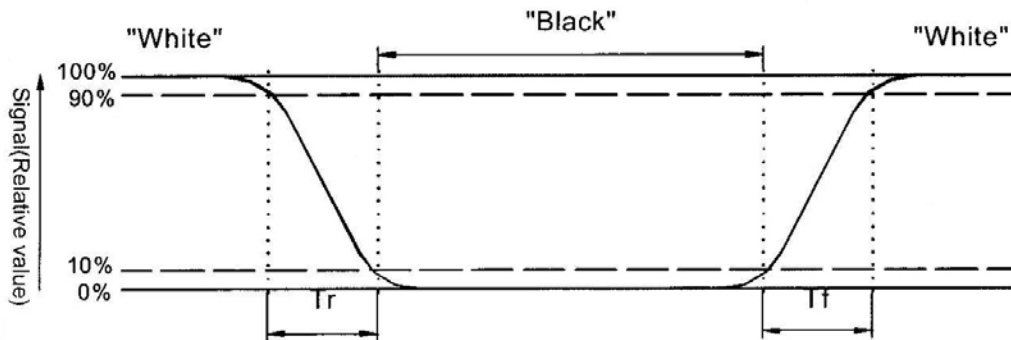
Note 3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

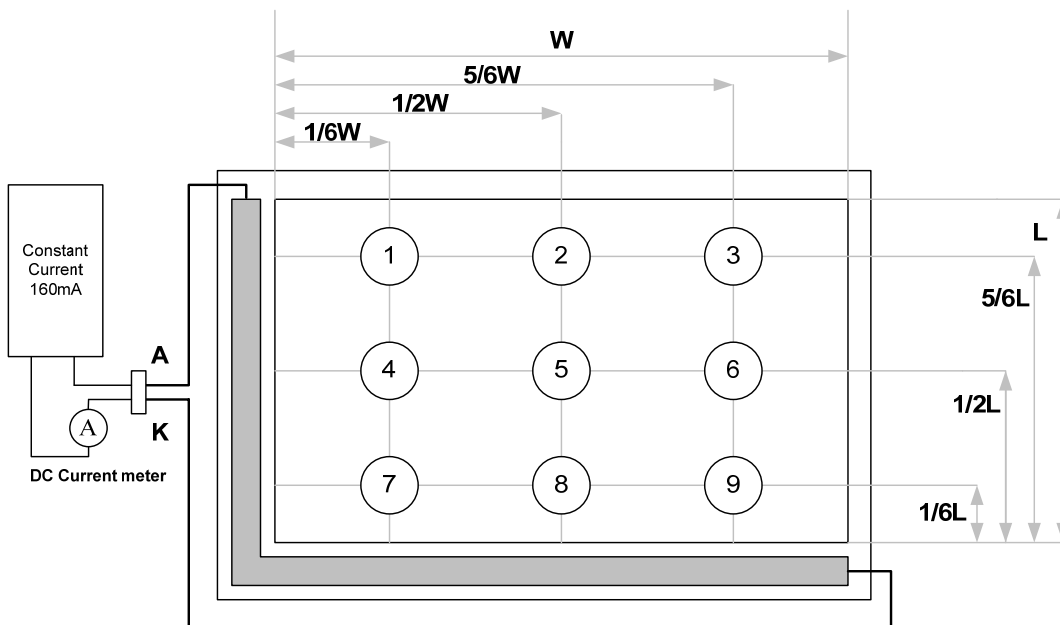
$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time) respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5 : Luminance is measured at point 5 of the display.



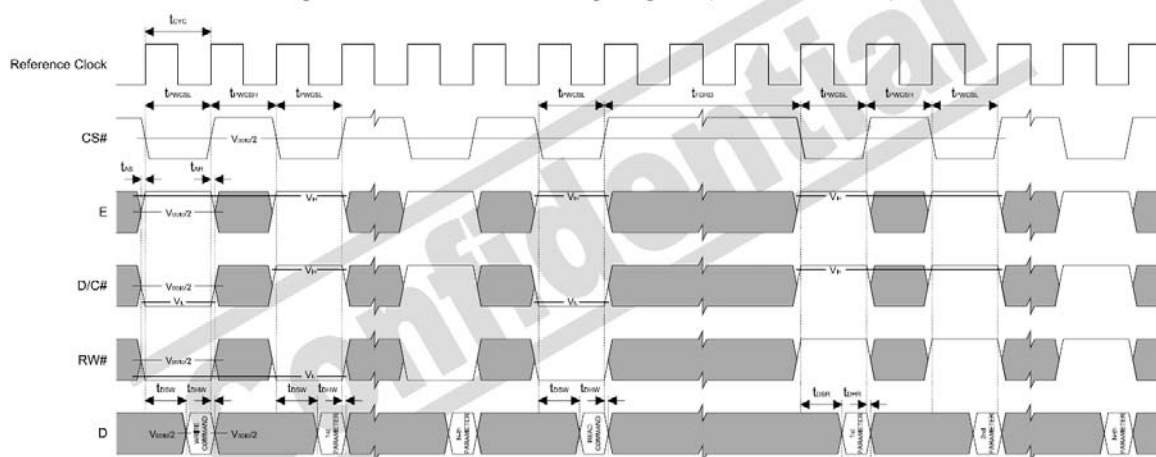
Note 6 : Definition of Luminance Uniformity

$$\Delta L = [L(\text{min.}) \text{ of 9 points} / L(\text{max.}) \text{ of 9 points}] \times 100\%$$

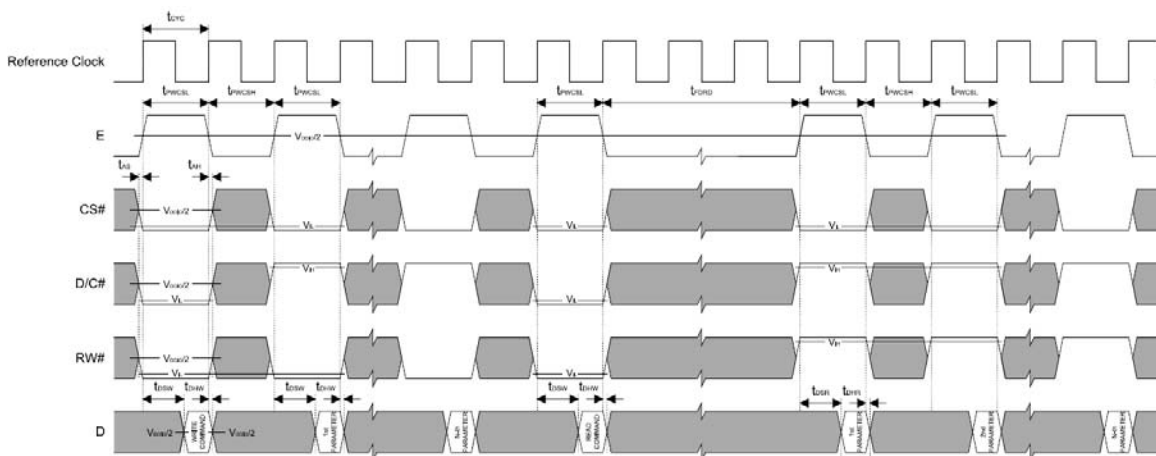
7 Interface Protocol

7.1 M68 Series

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYC}	Reference Clock Cycle Time	9	-	-	ns
t_{PWCSL}	Pulse width CS# or E low	1	-	-	t_{CYC}
t_{PWCSH}	Pulse width CS# or E high	1	-	-	t_{CYC}
t_{FDRD}	First Data Read Delay	5	-	-	t_{CYC}
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	1	-	-	ns
t_{DSW}	Data Setup Time	4	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{DSR}	Data Access Time	-	-	5	ns
t_{DHR}	Output Hold time	1	-	-	ns



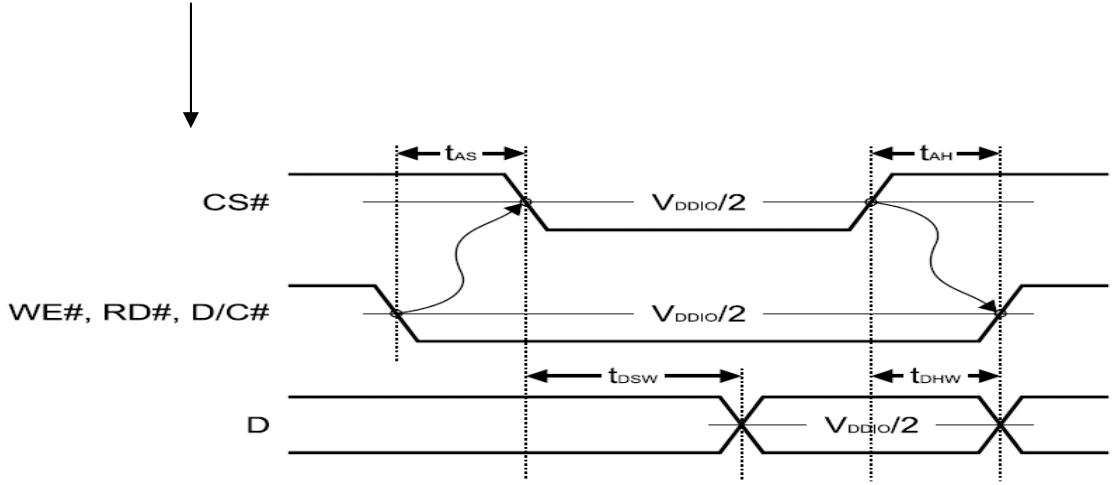
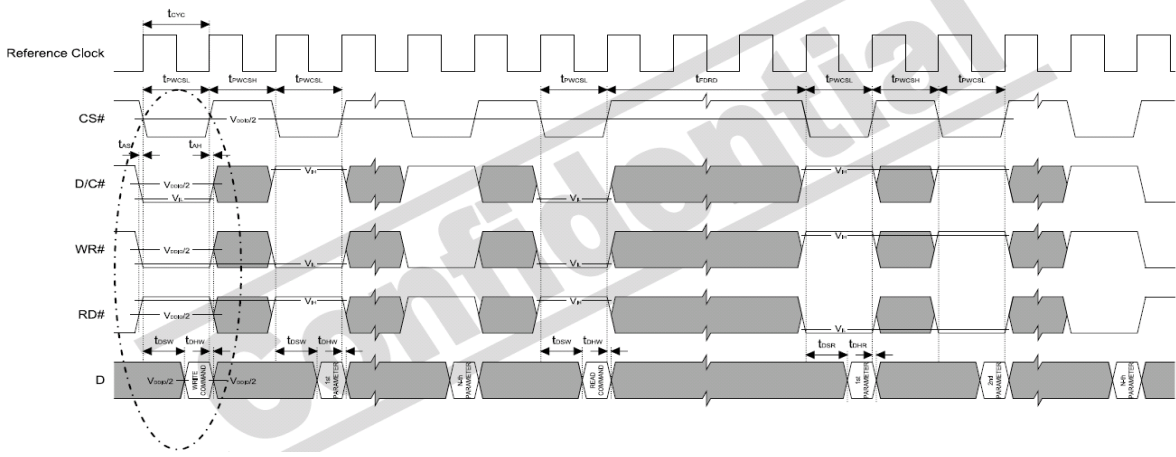
6800 Mode Timing Diagram (Use CS# as Clock)



6800 Mode Timing Diagram (Use E as Clock)

7.2 i80 Series

Symbol	Parameter	Min	Typ	Max	Unit
t_{cyc}	Reference Clock Cycle Time	9	-	-	ns
t_{PWCSL}	Pulse width CS# low	1	-	-	t_{cyc}
t_{PWCSH}	Pulse width CS# high	1	-	-	t_{cyc}
t_{FDRD}	First Read Data Delay	5	-	-	t_{cyc}
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	1	-	-	ns
t_{DSW}	Data Setup Time	4	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{DSR}	Data Access Time	-	-	5	ns
t_{DHR}	Output Hold time	1	-	-	ns



7.3 Data transfer order Setting

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	
24 bits	1 st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
18 bits	1 st								R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1 st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits	1 st									R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X	
	2 nd									B5	B4	B3	B2	B1	B0	X	X	R5	R4	R3	R2	R1	R0	X	X	
	3 rd									G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X	
9 bits	1 st																R5	R4	R3	R2	R1	R0	G5	G4	G3	
	2 nd																G2	G1	G0	B5	B4	B3	B2	B1	B0	
8 bits	1 st																	R5	R4	R3	R2	R1	R0	X	X	
	2 nd																	G5	G4	G3	G2	G1	G0	X	X	
	3 rd																	B5	B4	B3	B2	B1	B0	X	X	

X: Don't Care

8 Command Table

Hex Code	Command	Description
0x 00	nop	No operation
0x 01	soft_reset	Software Reset
0x 0A	get_power_mode	Get the current power mode
0x 0B	get_address_mode	Get the frame memory to the display panel read order
0x 0C	get_pixel_format	Get the current pixel format
0x 0D	get_display_mode	The display module returns the Display Signal Mode.
0x 0E	get_signal_mode	Get the current display mode from the peripheral
0x 10	enter_sleep_mode	Turn off the panel. This command will pull low the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x 11	exit_sleep_mode	Turn on the panel. This command will pull high the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x 12	enter_partial_mode	Part of the display area is used for image display.
0x 13	enter_normal_mode	The whole display area is used for image display.
0x 20	exit_invert_mode	Displayed image colors are not inverted.
0x 21	enter_invert_mode	Displayed image colors are inverted.
0x 26	set_gamma_curve	Selects the gamma curve used by the display device.
0x 28	set_display_off	Blanks the display device.
0x 29	set_display_on	Show the image on the display device.
0x 2A	set_column_address	Set the column extent.
0x 2B	set_page_address	Set the page extent.
0x 2C	write_memory_start	Transfer image information from the host processor interface to the peripheral starting at the location provided by set_column_address and set_page_address.
0x 2E	read_memory_start	Transfer image data from the peripheral to the host processor interface starting at the location provided by set_column_address and set_page_address.
0x 30	set_partial_area	Defines the partial display area on the display device.
0x 33	set_scroll_area	Defines the vertical scrolling and fixed area on display area.
0x 34	set_tear_off	Synchronization information is not sent from the display module to the host processor.
0x 35	set_tear_on	Synchronization information is sent from the display module to the host processor at the start of VFP.
0x 36	set_address_mode	Set the read order from frame buffer to the display panel.
0x 37	set_scroll_start	Defines the vertical scrolling starting point.
0x 38	exit_idle_mode	Full color depth is used for the display panel.
0x 39	enter_idle_mode	Reduce color depth is used on the display panel.
0x 3A	set_pixel_format	Defines how many bits per pixel are used in the interface.
0x 3C	write_memory_continue	Transfer image information from the host processor interface to the peripheral from the last written location.
0x 3E	read_memory_continue	Read image data from the peripheral continuing after the last read_memory_continue or read_memory_start.
0x 44	set_tear_scanline	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the provided scan line.
0x 45	get_scanline	Get the current scan line.
0x A1	read_ddb	Read the DDB from the provided location.
0x B0	set_lcd_mode_pad_size	Set the LCD panel mode (RGB TFT or TTL).
0x B1	get_lcd_mode_pad_size	Get the current LCD panel mode, pad strength and resolution.
0x B4	set_hori_period	Set front porch.
0x B5	get_hori_period	Get current front porch settings.
0x B6	set_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse.
0x B7	get_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse.

0x B8	set_gpio_conf	Set the GPIO configuration. If the GPIO is not used for LCD, set the direction. Otherwise, they are toggled with LCD signals.
0x B9	get_gpio_conf	Get the current GPIO configuration.
0x BA	set_gpio_value	Set GPIO value for GPIO configured as output.
0x BB	get_gpio_status	Read current GPIO status. If the individual GPIO was configured as input, the value is the status of the corresponding pin. Otherwise, it is the programmed value.
0x BC	set_post_proc	Set the image post processor.
0x BD	get_post_proc	Set the image post processor.
0x BE	set_pwm_conf	Set the image post processor.
0x BF	get_pwm_conf	Set the image post processor.
0x C0	set_lcd_gen0	Set the rise, fall, period and toggling properties of LCD signal generator 0
0x C1	get_lcd_gen0	Get the current settings of LCD signal generator 0
0x C2	set_lcd_gen1	Set the rise, fall, period and toggling properties of LCD signal generator 1.
0x C3	get_lcd_gen1	Get the current settings of LCD signal generator 1.
0x C4	set_lcd_gen2	Set the rise, fall, period and toggling properties of LCD signal generator 2.
0x C5	get_lcd_gen2	Get the current settings of LCD signal generator 2.
0x C6	set_lcd_gen3	Set the rise, fall, period and toggling properties of LCD signal generator 3.
0x C7	get_lcd_gen3	Get the current settings of LCD signal generator 3.
0x C8	set_gpio0_rop	Set the GPIO0 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO0 is configured as general GPIO.
0x C9.	get_gpio0_rop	Get the GPIO0 properties with respect to the LCD signal generators.
0x CA	set_gpio1_rop	Set the GPIO1 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO1 is configured as general GPIO.
0x CB	get_gpio1_rop	Get the GPIO1 properties with respect to the LCD signal generators.
0x CC	set_gpio2_rop	Set the GPIO2 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO2 is configured as general GPIO.
0x CD	get_gpio2_rop	Get the GPIO2 properties with respect to the LCD signal generators.
0x CE	set_gpio3_rop	Set the GPIO3 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO3 is configured as general GPIO.
0x CF	get_gpio3_rop	Get the GPIO3 properties with respect to the LCD signal generators.
0x D0	set_abc_dbc_conf	Set the ambient back light and dynamic back light configuration.
0x D1	get_abc_dbc_conf	Get the ambient back light and current dynamic back light configuration.
0x D4	set_dbc_th	Set the threshold for each level of power saving.
0x D5	get_dbc_th	Get the threshold for each level of power saving.
0x E0	set_pll_start	Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input.
0x E2	set_pll_mnk	Set the PLL.
0x E3	get_pll_mnk	Get the PLL settings.
0x E4	get_pll_status	Get the current PLL status.
0x E5	set_deep_sleep	Set deep sleep mode.
0x E6	set_lshift_freq	Set the LSHIFT (pixel clock) frequency.
0x E7	get_lshift_freq	Get current LSHIFT (pixel clock) frequency setting.
0x F0	set_pixel_data_interface	Set the pixel data format of the parallel host processor interface.
0x F1	get_pixel_data_interface	Get the current pixel data format settings.

About the further detail, please refer the datasheet of SSD1963.

9 DISPLAYED COLOR AND INPUT DATA

	Color & Gray Scale	DATA SIGNAL																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

10. QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $60 \pm 25\% \text{ RH}$.

10.2 SAMPLING PLAN

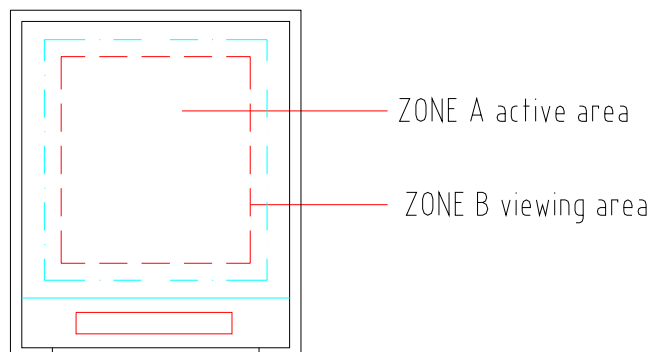
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.

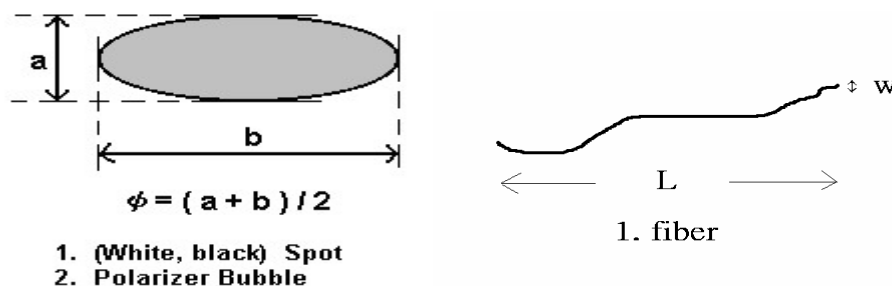


10.5 Incoming Inspection Standard

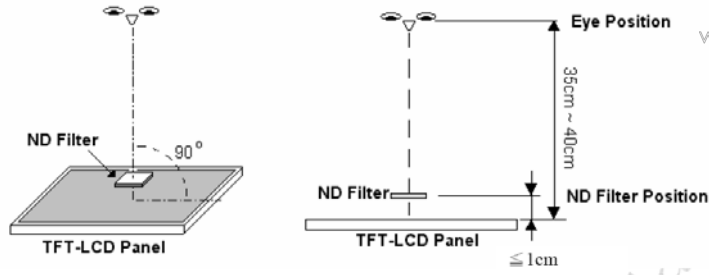
Defect Type			Limit			Note		
Visual Defect	Internal	Spot	$\phi < 0.15\text{mm}$		Ignore	(1)		
			$0.15\text{mm} \leq \phi \leq 0.5\text{mm}$		$N \leq 4$			
			$0.5\text{mm} < \phi$		$N=0$			
		Fiber	$0.1\text{mm} < W \leq 0.5\text{mm},$ $L \leq 1.5\text{mm}$		$N \leq 4$	(1)		
			$1.0\text{mm} < W, 1.5\text{mm} < L$		$N=0$			
		Polarizer Bubble	$\phi < 0.15\text{mm}$		Ignore	(1)		
			$0.15\text{mm} \leq \phi \leq 0.5\text{mm}$		$N \leq 4$			
			$0.5\text{mm} < \phi$		$N=0$			
		Mura	It' OK if mura is slight visible through 6%ND filter					
Electrical Defect	Bright Dot	A Grade			B Grade			
		C Area	O Area	Total	C Area	O Area	Total	(3)
		$N \leq 0$	$N \leq 2$	$N \leq 2$	$N \leq 2$	$N \leq 3$	$N \leq 5$	(2)
	Dark Dot	$N \leq 2$	$N \leq 4$	$N \leq 4$	$N \leq 3$	$N \leq 5$	$N \leq 8$	
	Total Dot	$N \leq 4$			$N \leq 5$	$N \leq 6$	$N \leq 8$	(2)
	Two Adjacent Dot	$N \leq 0$	$N \leq 1$ pair	$N \leq 1$ pair	$N \leq 1$ pair	$N \leq 1$ pair	$N \leq 1$ pair	(4)
	Three or More Adjacent Dot	Not Allowed						
	Line Defect	Not Allowed						

- (1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)
 (2) LITTLE BRIGHT DOT acceptable under 6% ND-Filter

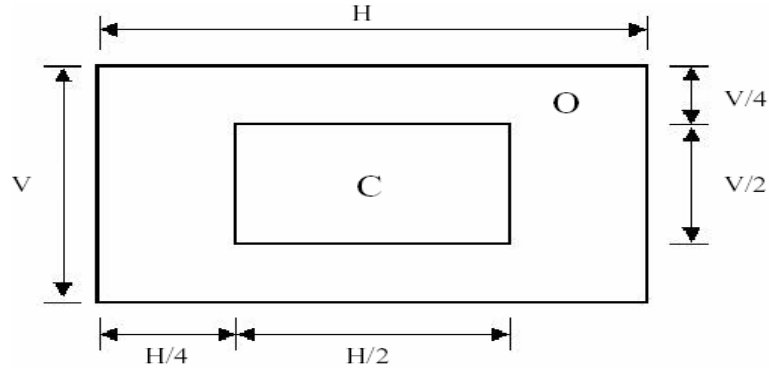
[Note1] W : Width[mm], L : Length[mm], N : Number, ϕ : Average Diameter



[Note2] Bright dot is defined through 6% transmission ND Filter as following.



[Note3]

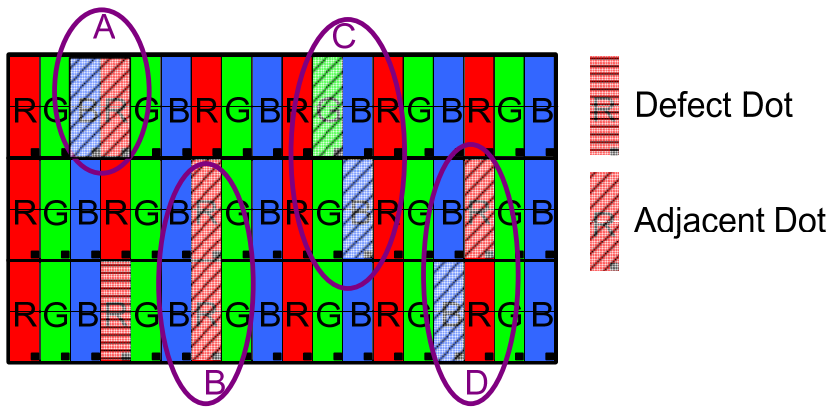


C Area: Center of display area

O Area: Outer of display area

[Note4]

Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dark adjacent dot. And they will be counted 2 defect dots in total quantity.



- (1) The defects that are not defined above and considered to be problem shall be reviewed and discussed by both parties.
- (2) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

10. RELIABILITY TEST CONDITIONS

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Humidity Test	40 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12. USE PRECAUTIONS

12-1 Handling precautions

- (1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- (2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzene and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- (3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- (1) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12-2 Installing precautions

- (1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1M\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- (2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- (3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- (4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off

12-3 Storage precautions

- (1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- (2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- (3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12-4 Operating precautions

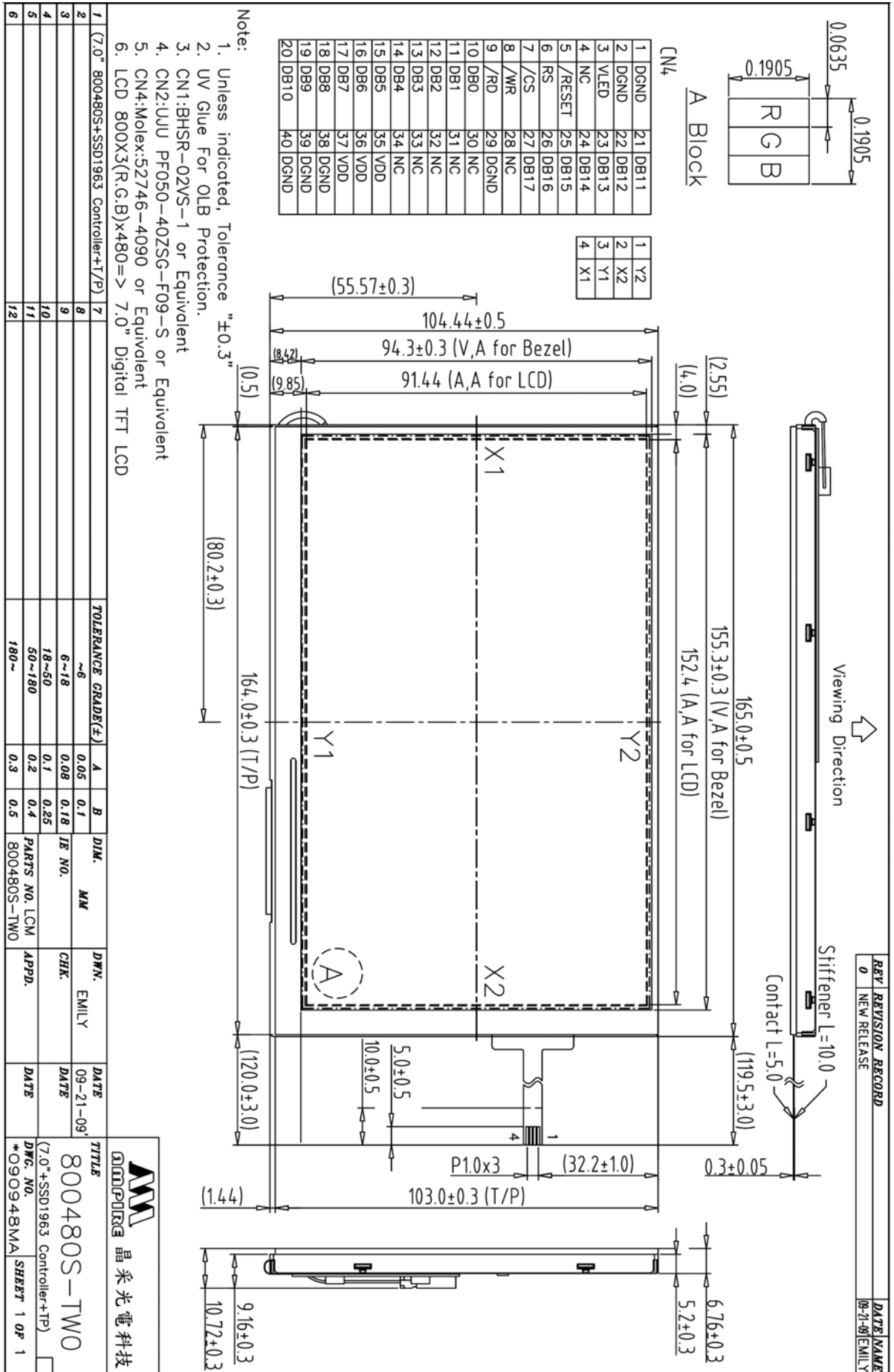
www.DataSheet4U.com

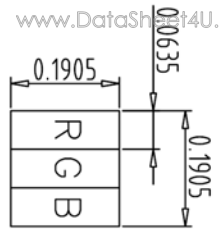
- (1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- (2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- (3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- (4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- (5) Make certain that each signal noise level is within the standard (L level: $0.2V_{dd}$ or less and H level: $0.8V_{dd}$ or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- (6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- (7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
- (8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12-5 Other

- (1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- (2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
- (3) AMIPRE will provide one year warranty for all products and three months warranty for all repairing products..

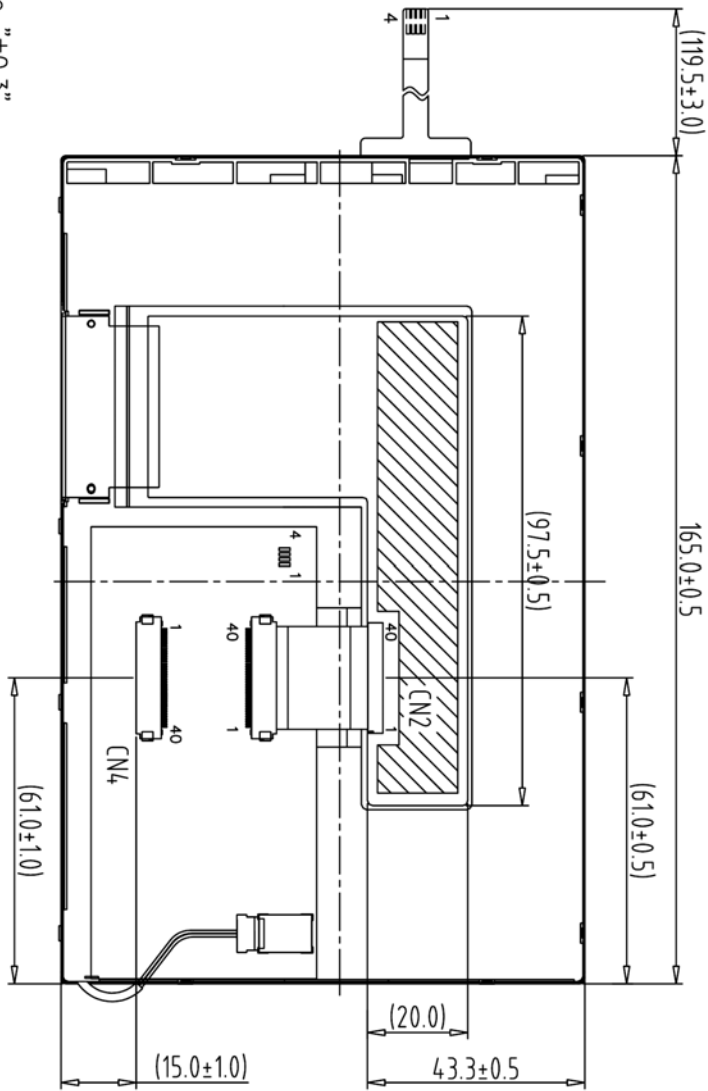
13. OUTLINE DIMENSION





A Block

1	DGND	21	DB11
2	DGND	22	DB12
3	VLED	23	DB13
4	NC	24	DB14
5	/RESET	25	DB15
6	RS	26	DB16
7	/CS	27	DB17
8	/WR	28	NC
9	/RD	29	DGND
10	DB0	30	NC
11	DB1	31	NC
12	DB2	32	NC
13	DB3	33	NC
14	DB4	34	NC
15	DB5	35	VDD
16	DB6	36	VDD
17	DB7	37	VDD
18	DB8	38	DGND
19	DB9	39	DGND
20	DB10	40	DGND



Back View

- Note:
1. Unless indicated, Tolerance "±0.3"
 2. UV Glue For OLB Protection.
 3. CN1:BHSR-02VS-1 or Equivalent
 4. CN2:JUJU PF050-40ZSG-F09-S or Equivalent
 5. CN4:Molex:52746-4090 or Equivalent
 6. LCD 800X3(R,G,B)x480=> 7.0" Digital TFT LCD

1	(7.0" 800480S+SSD1963 Controller+TP)	7																			
2		8																			
3		9																			
4		10																			
5		11																			
6		12																			

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	09-21-09	EMILY

1	Y2
2	X2
3	Y1
4	X1

MM 晶采光电科技
AMPIRE
800480S-TWO
 (7.0"+SSD1963 Controller+TP)
 DWG. NO. *090949MA
 SHEET 1 OF 1