AMP DISPLAY INC.

A Brighter Solution

SPECIFICATIONS

CUSTOMER	
CUSTOMER PART NO.	
AMP PART NO.	**AM-800600M3TNQW-01H-F**
APPROVED BY	
DATE	

☐ Approved For Specifications

☑ **Approved For Specifications & Sample**

AMP DISPLAY INC

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2010/9/13	-	New Release	Kevin
2011/03/23	3,4	Correct the brightness	Kevin

1. INSTRUCTION

Amp 8.4" Display Module is a color active matrix TFT-LCD that uses amorphous silicon TFT as a switching device . This model is composed of a TFT-LCD panel, a driving circuit. This TFT-LCD has a high resolution (800(R.G.B) X 600) and can display up to 262,144 colors.

1.1 Features

(1) Construction : a-Si TFT-LCD with driving system, White LED Backlight.

(2) LCD type : Transmissive , Normally White

(3) Number of the Colors : (a) 262K colors (LVDS 6 bits mode) (default)

(b) 16.2M colors (LVDS 8 bits mode).

(4) LVDS Interface **(Default setting : 6 bit mode)**.

(5) LCD Power Supply Voltage : 3.3V single power input, built-in power supply circuit.

(6) Build-in LED Driver IC (VLED=12V).

(7) ROHS compliant.

(8) **Reflective ratio 0.5% ~ 2%**

2. PHYSICAL SPECIFICATIONS

Item	Specifications	unit
Display resolution(dot)	800RGB (W) x 600(H)	dots
Active area	170.40 (W) x 127.80(H)	mm
Pixel pitch	213 (W) x 213 (H)	um
Color configuration	R.G.B -stripe	
Overall dimension	203.0(W) x 145.5(H) x 8.0(D)	mm
Weight	280	g
Brightness	450	Cd/m^2
Backlight unit	LED	
Display color	262K (default)	colors

If user wants to change the default setting for mass production, please contact with Ampire. We'll apply a new P/N for you.

3. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Supply voltage range	VCC	-0.3	4	V	(1)
Voltage range at any terminal	VI	-0.3	VCC + 0.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tstg	-30	80	℃	

Note : All voltage values are with respect to the GND terminals unless otherwise noted.

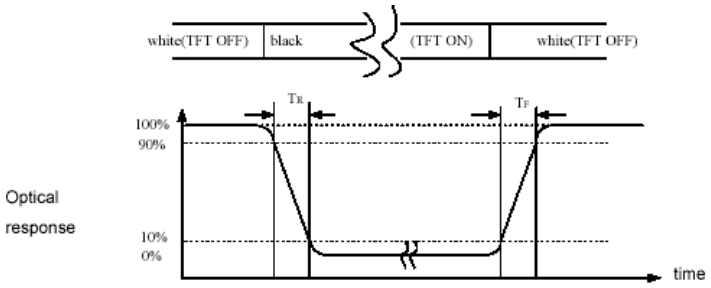
4. OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Response Time		$T_r + T_f$	Θ=Φ=0°	-	8	16	ms	(1)
Contrast ratio		CR		480	600	-	-	(2)(3)
Viewing Angle	Horizontal	ΘL	CR≧10	65	75	-	Deg.	(5)
		ΘR		65	75	-		
	Vertical	ΘU		50	60	-		
		ΘD		60	70	-		
Luminance (Center)		L	Θ=Φ=0°	280	450	--	cd/m^2	(3)(4) IL=52mA Ta=25℃
Luminance Uniformity		ΔL		-	70	-	%	(3)(4)
Color chromaticity	White	Wx		0.26	0.31	0.367		
		Wy		0.28	0.33	0.38		

NOTE :

- These items are measured by BM-5A(TOPCON) or CA-1000(MINOLTA) in the dark room (no ambient light)

(1) Definition of Response Time (White-Black)



(2) Definition of Contrast Ratio

Measure contrast ratio on the below 5 points(refer to figurel,#1~#5point) and take the average value

Contrast ratio is calculated with the following formula :

Contrast Ratio(CR)=(White)Luminance of ON ÷ (Black)Luminance of OFF

(3) Definition of Luminance :

Measure white luminance on the center point (point 5) and take the value.

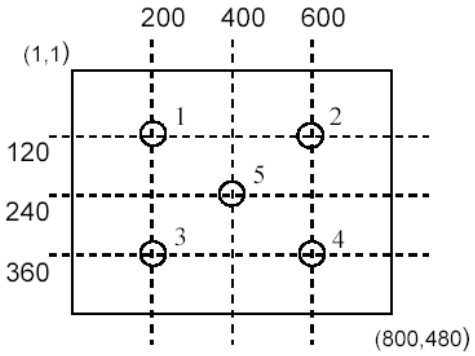


Fig.1 Measuring point

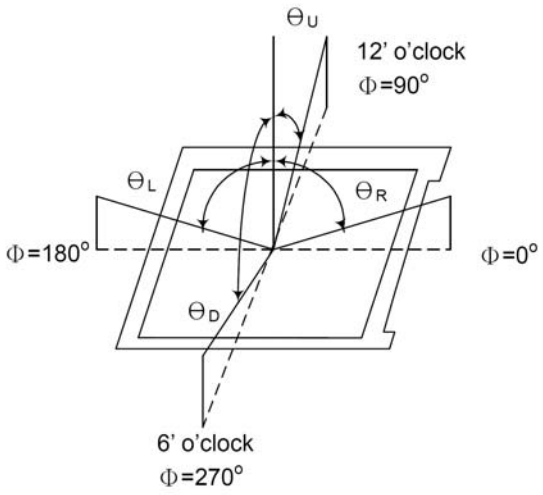
(4)Definition of Luminance Uniformity :

Measured Maximum luminance[L(MAX)] and Minimum luminance[L(MIN)] on the 5 points

Luminance Uniformity is calculated with the following formula :

ΔL =[L(MIN) / L (MAX)] X 100%

(5)Definition of Viewing Angle



5. ELECTRICAL CHARACTERISTICS

5.1 Power Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Logic / LCD Drive Voltage	VCC	3.0	3.3	3.6	V	
VCC Current	ICC		120		mA	(1)

Note1: fv =60Hz , Ta=25℃ , Display pattern : All Black

5.2 LVDS electrical Specification

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level output Voltage	I_{OH}=-4mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}=4mA			0.4	V
I_{IN}	Input Current	0V ≦ V_{IN} ≦ Vcc			±10	μA
I_{PD}	Pull Down Current	R/F pin,V_{IH}=Vcc			100	μA
I_{OS}	Output Short Circuit Current	V_{OUT}=0V			-50	mA

LVDS DRIVER DC SPECIFICATIONS

V_{OD}	Differential Output Voltage	RL=100Ω	250	350	450	mV
ΔV_{OD}	Change in VOD between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in VOC between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=0V,RL=100Ω			-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=0V, V_{OUT}=0V to Vcc			±10	µA

LVDS RECEIVER DC SPECIFICATIONS

V_{TH}	Differential Input High Threshold	V_{OC}=+1.2V			+100	mV
V_{TL}	Differential Input low Threshold		-100			mV
I_{IN}	Input Current	V_{IN}=+2.4V/ 0V Vcc=3.6V			±10	µA

6. BACKLIGHT UNIT

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage	VLED	10.8	12.0	12.6	V	
Input Current	ILED	--	210	--	mA	100% PWM duty
Dimming Frequency	Fpwm	200		30K	Hz	
Dimming Voltage High		2	--	5.0	V	
Dimming Voltage Low		0	--	0.8	V	
LED Forward Current	IF	--	52	60	mA	Ta=25℃
LED Forward Voltage	VF		38.4	43.8	V	IF=52mA, Ta=25℃
LED life time			50,000	-	Hr	IF=52mA, Ta=25℃

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: VLED, ILED are defined for LED B/L. (100% duty of PWM dimming)

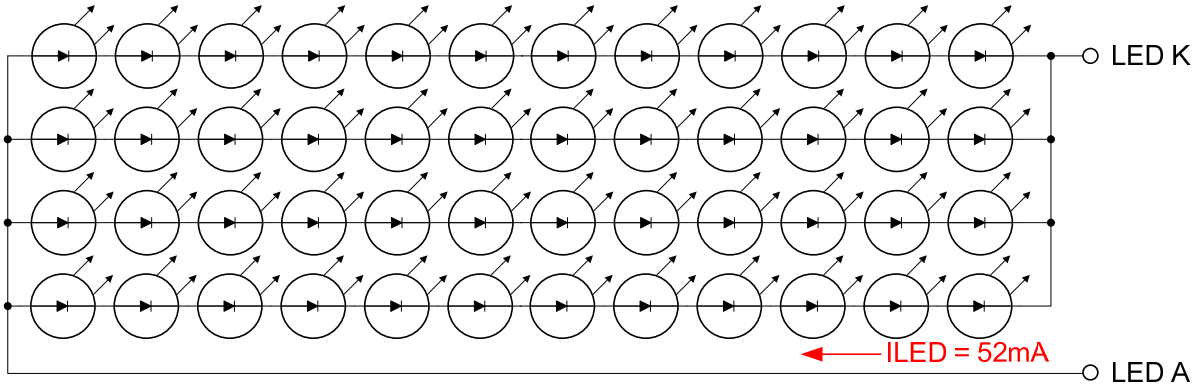
Note 3: IF, VF, Fpwm are defined for LED Driver.

Note 4: If the module is driven by high current or at high ambient temperature &

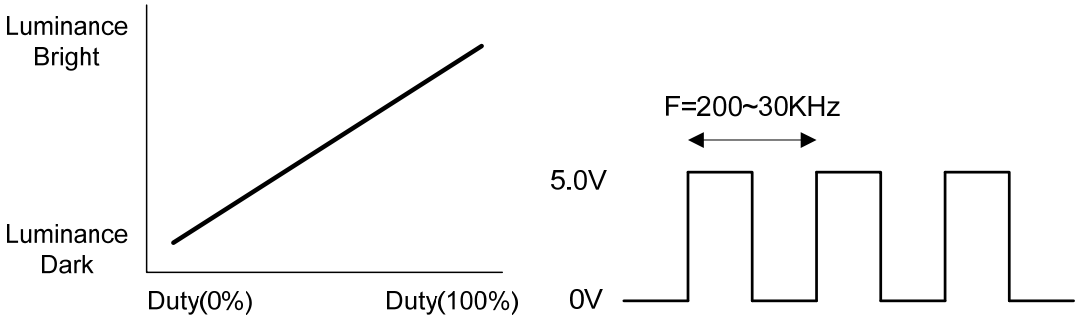
humidity condition. The operating life will be reduced.

Note 5: Operating life means brightness goes down to 50% minimum brightness. LED life time is estimated data.

Note 6: the structure of LED B/L shows as below.



6.1 PWM Dimming Control



7. INTERFACE

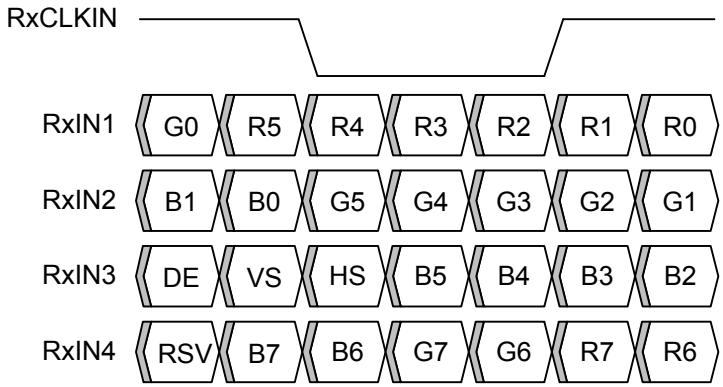
7.1 Interface Definition

CN1 : LVDS Connector

Pin no	Symbol	Function
1	VCC	POWER SUPPLY:3.3V
2	VCC	POWER SUPPLY:3.3V
3	UD	Vertical Reverse Scan Control.
4	LR	Horizontal Reverse Scan Control.
5	RXIN1-	Transmission Data of Pixels 1
6	RXIN1+	Transmission Data of Pixels 1

7	GND	Power Ground
8	RXIN2-	Transmission Data of Pixels 2
9	RXIN2+	Transmission Data of Pixels 2
10	GND	Power Ground
11	RXIN3-	Transmission Data of Pixels 3
12	RXIN3+	Transmission Data of Pixels 3
13	GND	Power Ground
14	RXCKIN-	Sampling Clock
15	RXCKIN+	Sampling Clock
16	GND	Power Ground
17	NC	No connection
18	NC	No connection
19	NC	**LVDS 6 bits mode : No connection (default)** LVDS 8 bit mode : (RXIN4-) Transmission Data of Pixels 4
20	NC	**LVDS 6 bits mode : No connection (default)** LVDS 8 bit mode : (RXIN4+) Transmission Data of Pixels 4

8 bits LVDS input

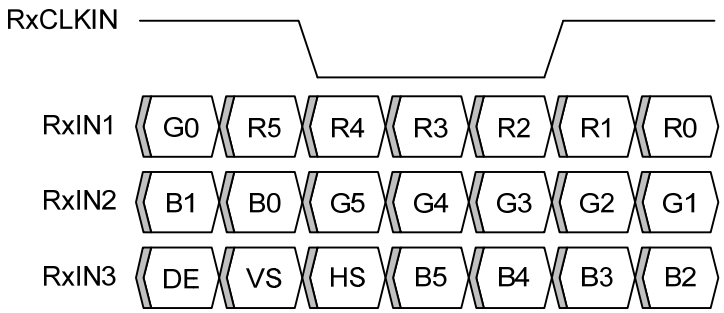


Note : R/G/B data 7 : MSB, R/G/B data 0 : LSB

Signal Name	Description	Remark
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.

G7 G6 G5 G4 G3 G2 G1 G0	Green Date 7 (MSB) Green Date 6 Green Date 5 Green Date 4 Green Date 3 Green Date 2 Green Date 1 Green Date 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2 B1 B0	Blue Data 7 (MSB) Blue Data 6 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.
RxCLKIN+ RxCLKIN-	LVDS Clock Input	
DE	Display Enable	
VS	Vertical Sync	
HS	Horizontal Sync	

6 bits LVDS input



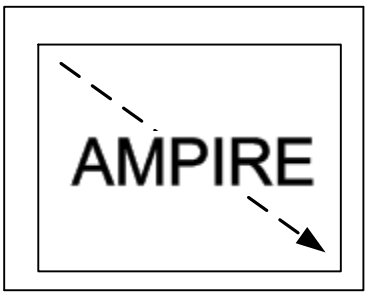
Note : R/G/B data 5 : MSB, R/G/B data 0 : LSB

Signal Name	Description	Remark
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.

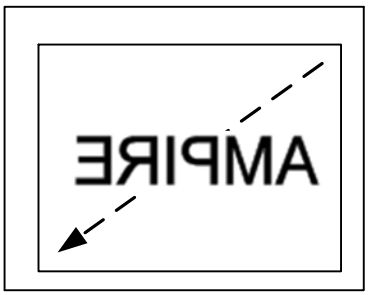
G5 G4 G3 G2 G1 G0	Green Date 5 (MSB) Green Date 4 Green Date 3 Green Date 2 Green Date 1 Green Date 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN+ RxCLKIN-	LVDS Clock Input	
DE	Display Enable	
VS	Vertical Sync	
HS	Horizontal Sync	

Setting of scan control input		**Scanning direction**
UD	**LR**	
GND	GND	Up to Down, Left to Right
VCC	VCC	Down to Up, Right to Left
GND	VCC	Up to Down, Right to Left
VCC	GND	Down to Up, Left to Right

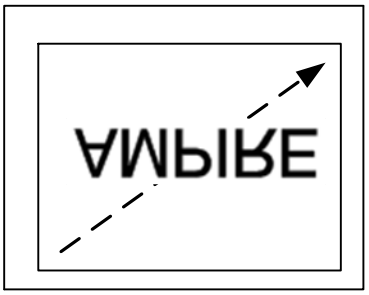
UD : L, LR : L



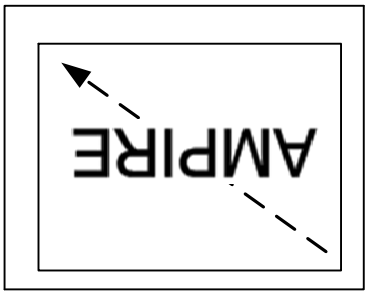
UD : L, LR : H



UD : H, LR : L



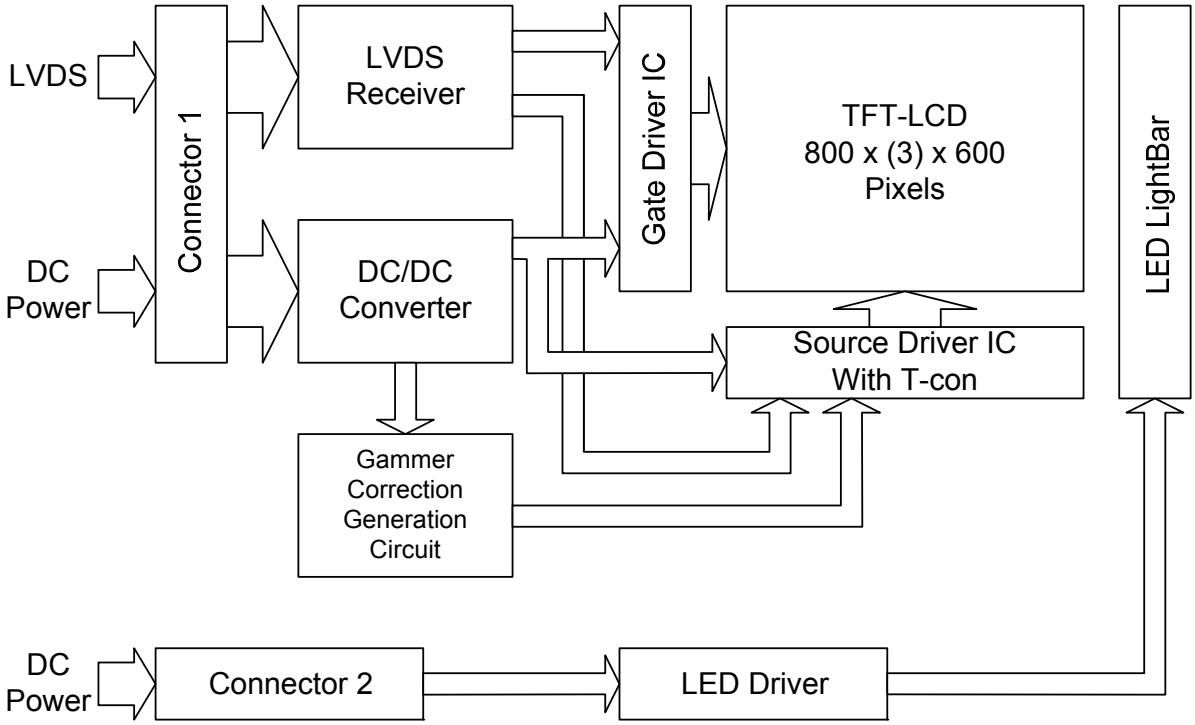
UD : H, LR : H



CN2 : LED Driver Connector

Pin no	Symbol	Function
1	VLED	12V input
2	GND	GND
3	Display_ON/OFF	+3.3V:ON, 0V:OFF
4	Dimming	PWM

7.2 Block Diagram



8. AC Timing characteristic

8.1 AC Timing characteristic of LVDS

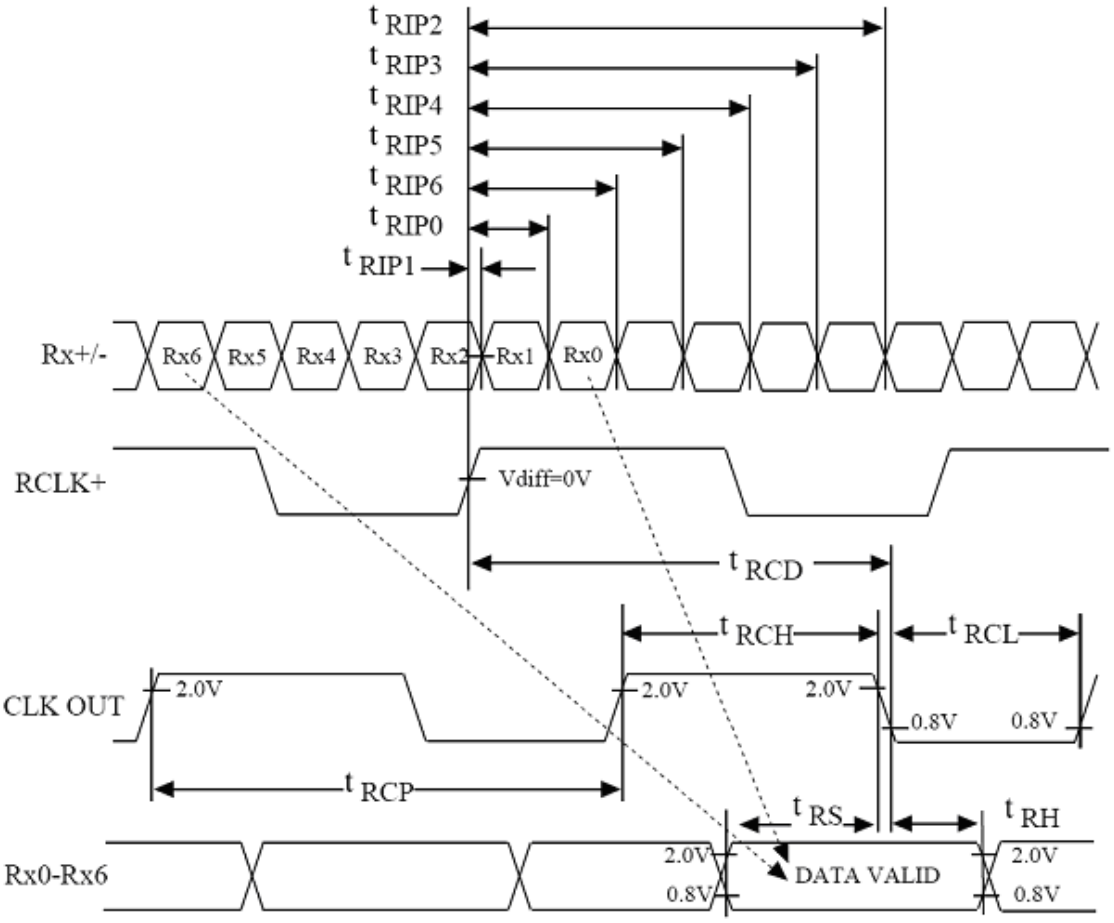
Switching Characteristics

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

RECEIVER

t_{RCP}	CLK OUT Period	11.76	T	50.0	ns
t_{RCH}	CLK OUT High Time		4T/7		ns
t_{RCL}	CLK OUT Low Time		3T/7		ns
t_{RCD}	RCLK+/- to CLK OUT Delay		5T/7		ns
t_{RS}	TTL Data Setup to CLK OUT	3T/7-2.5			ns
t_{RH}	TTL Data Hold from CLK OUT	4T/7-3.5			ns
t_{TLH}	TTL Low to High Transition Time		3.0	5.0	ns
t_{THL}	TTL High to Low Transition Time		3.0	5.0	ns
t_{RIP1}	Input Data Position 0 (T=11.76ns)	-0.4	0.0	0.4	ns
t_{RIP0}	Input Data Position 1 (T=11.76ns)	T/7-0.4	T/7	T/7+0.4	ns
t_{RIP6}	Input Data Position 2 (T=11.76ns)	2T/7-0.4	2T/7	2T/7+0.4	ns
t_{RIP5}	Input Data Position 3 (T=11.76ns)	3T/7-0.4	3T/7	3T/7+0.4	ns
t_{RIP4}	Input Data Position 4 (T=11.76ns)	4T/7-0.4	4T/7	4T/7+0.4	ns
t_{RIP3}	Input Data Position 5 (T=11.76ns)	5T/7-0.4	5T/7	5T/7+0.4	ns
t_{RIP2}	Input Data Position 6 (T=11.76ns)	6T/7-0.4	6T/7	6T/7+0.4	ns
t_{RPLL}	Phase Lock Loop Set			10.0	ms

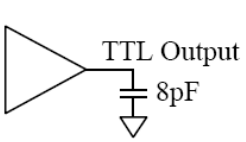
RECEIVER DEVICE



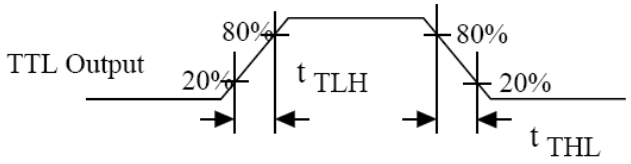
Note:
1) Vdiff = (RA+) - (RA-), ... (RCLK+) - (RCLK-)

RECEIVER DEVICE TRANSITION TIMES

TTL Output

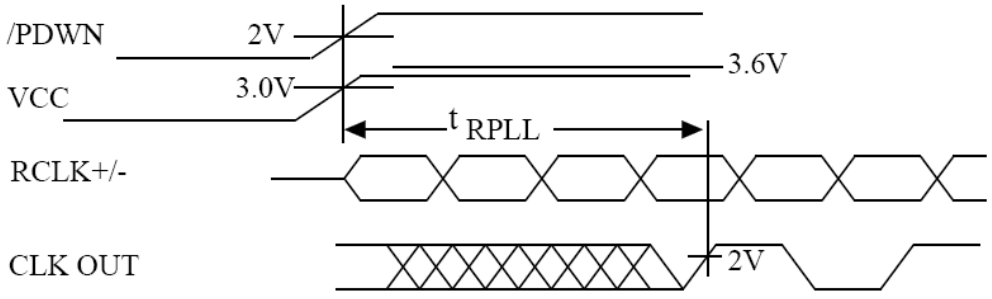


TTL output load



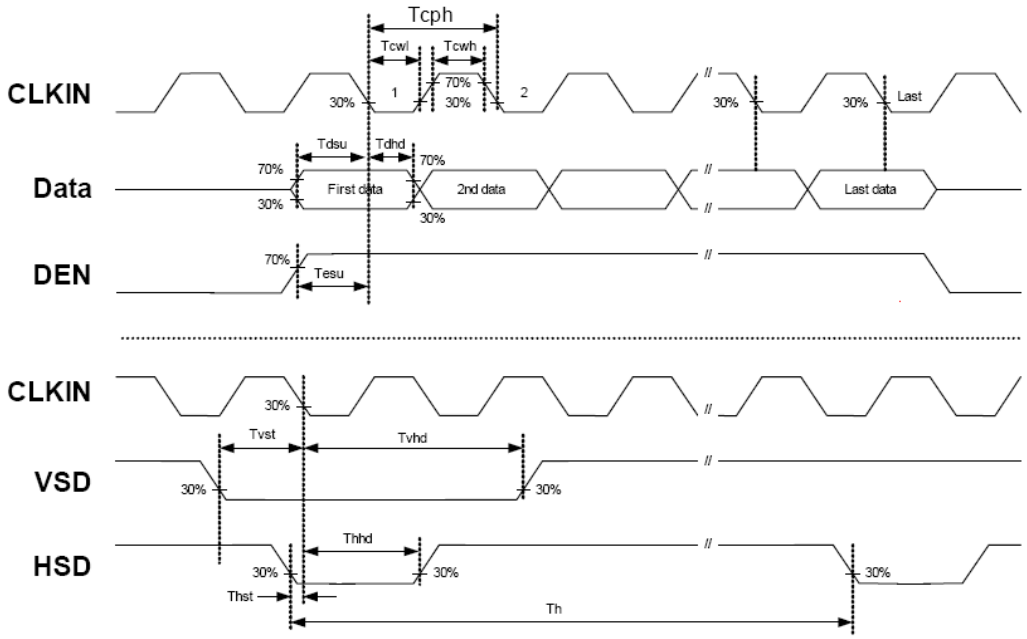
PHASE LOCK LOOP SET TIME

RECEIVER DEVICE

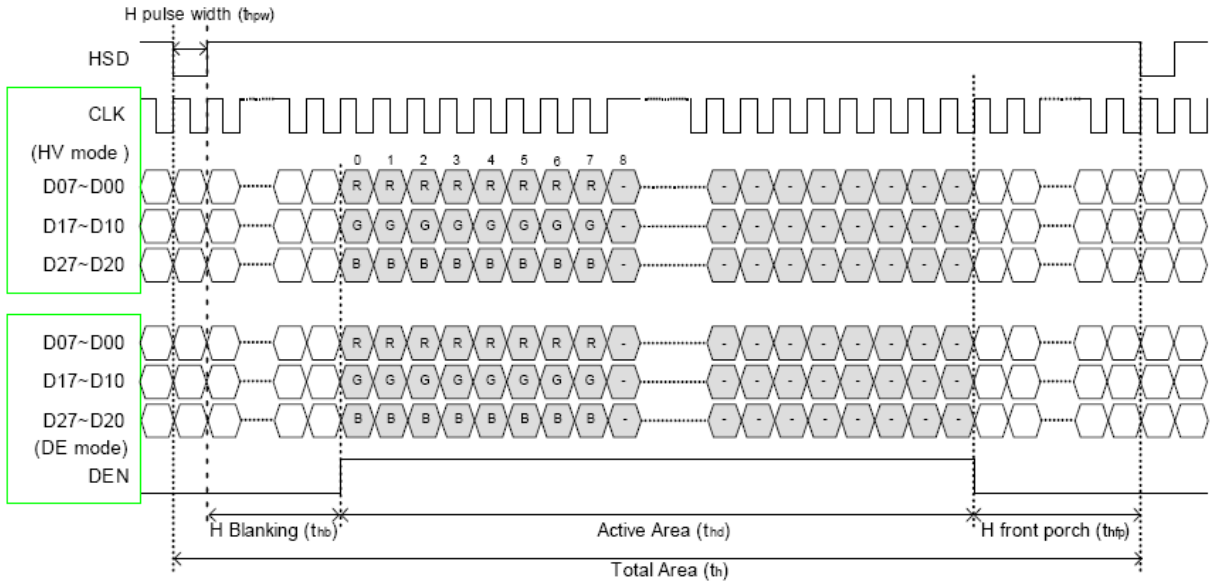


8.2 AC Timing characteristic of Panel

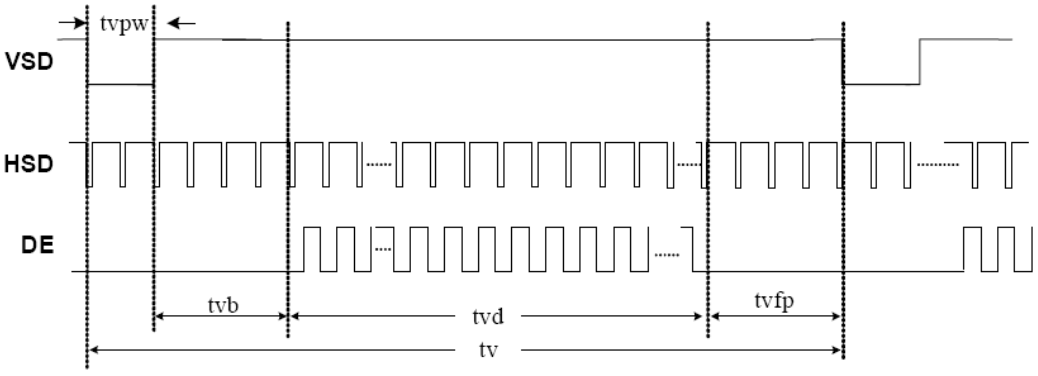
Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK cycle time	Tcph	20			ns	
DCLK frequency	fclk		40	50	MHz	
DCLK pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	8			ns	
VSD hold time	Tvhd	8			ns	
HSD setup time	Thst	8			ns	
HSD hold time	Thhd	8			ns	
Data setup time	Tdsu	8			ns	
Data hold time	Tdhd	8			ns	
DE setup time	Tesu	8			ns	
DE hold time	Tehd	8			ns	
Horizontal display area	thd		800		Tcph	
HSD period time	th		1000		Tcph	
HSD pulse width	thpw	1	48		Tcph	
HSD back porch	thb		40		Tcph	
HSD front porch	thfp		112		Tcph	
Vertical display area	tvd		600		th	
VSD period time	tv		660		th	
VSD pulse width	tvpw		3		th	
VSD back porch	tvb		39		th	
VSD front porch	tvfp		18		th	



Sampling clock timing

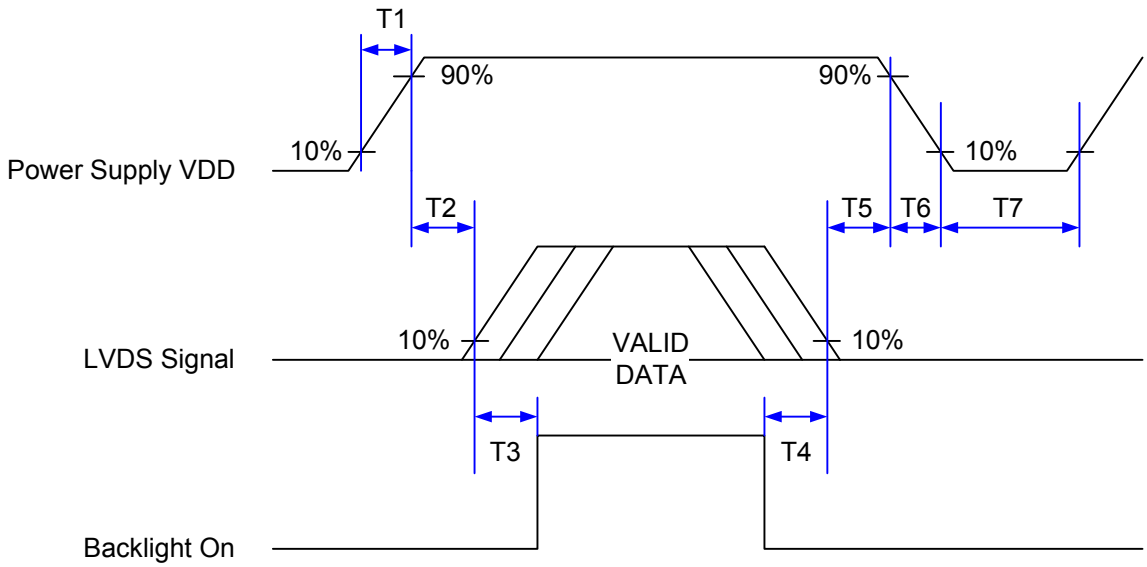


Horizontal display timing range



Vertical timing

8.3 Power ON/OFF Sequence



8.3.1 Power ON/OFF sequence timing

Symbol	Value			Unit
	Min.	Typ.	Max.	
T1	0.5	--	20	ms
T2	0	40	50	ms
T3	200	--	--	ms
T4	200	--	--	ms
T5	0	40	50	ms
T6	0	--	20	ms
T7	1000	--	--	ms

9 . QUALITY AND RELIABILITY

9.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

9.2 SAMPLING PLAN

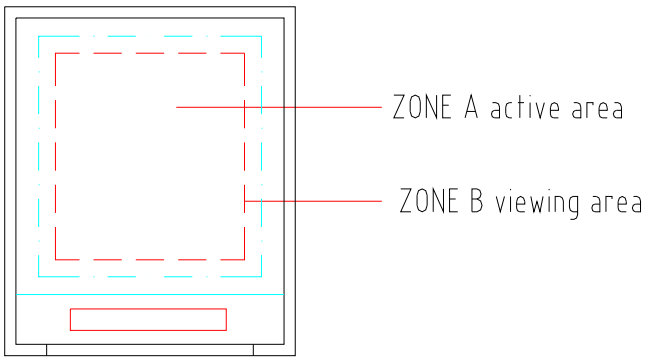
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

9.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

9.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



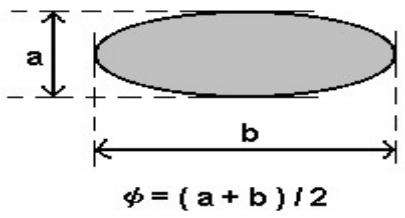
9.5 INCOMING INSPECTION STANDARD FOR TFT-LCD PANEL

<table>
<tr><th colspan="3">DEFECT TYPE</th><th colspan="4">LIMIT</th><th>Note</th></tr>
<tr><td rowspan="8">VISUAL DEFECT</td><td rowspan="8">INTERNAL</td><td rowspan="3">SPOT</td><td colspan="3">φ＜0.15mm</td><td>Ignore</td><td rowspan="3">Note1</td></tr>
<tr><td colspan="3">0.15mm≦φ≦0.5mm</td><td>N≦4</td></tr>
<tr><td colspan="3">0.5mm＜φ</td><td>N=0</td></tr>
<tr><td rowspan="2">FIBER</td><td colspan="3">0.03mm<W≦0.1mm, L≦5mm</td><td>N≦3</td><td rowspan="2">Note1</td></tr>
<tr><td colspan="3">1.0mm＜W, 1.5mm＜L</td><td>N=0</td></tr>
<tr><td rowspan="3">POLARIZER BUBBLE</td><td colspan="3">φ＜0.15mm</td><td>Ignore</td><td rowspan="3">Note1</td></tr>
<tr><td colspan="3">0.15mm≦φ≦0.5mm</td><td>N≦2</td></tr>
<tr><td colspan="3">0.5mm＜φ</td><td>N=0</td></tr>
<tr><td>Mura</td><td colspan="4">It' OK if mura is slight visible through 6%ND filter</td><td></td></tr>
<tr><td rowspan="7">ELECTRICAL DEFECT</td><td colspan="2" rowspan="2">BRIGHT DOT</td><td>C Area</td><td>O Area</td><td>Total</td><td>Note3</td></tr>
<tr><td>N≦0</td><td>N≦2</td><td>N≦2</td><td>Note2</td></tr>
<tr><td colspan="2">DARK DOT</td><td>N≦2</td><td>N≦4</td><td>N≦4</td><td></td></tr>
<tr><td colspan="2">TOTAL DOT</td><td colspan="3">N≦4</td><td>Note2</td></tr>
<tr><td colspan="2">TWO ADJACENT DOT</td><td>N≦0</td><td>N≦0</td><td>N≦0</td><td>Note4</td></tr>
<tr><td colspan="2">THREE OR MORE ADJACENT DOT</td><td colspan="3">NOT ALLOWED</td><td></td></tr>
<tr><td colspan="2">LINE DEFECT</td><td colspan="3">NOT ALLOWED</td><td></td></tr>
</table>

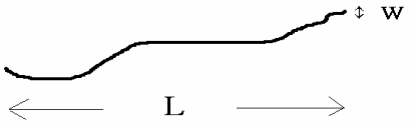
(1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)

(2) LITTLE BRIGHT DOT ACCEPTABLE UNDER 6 % ND-Filter

[Note1] W : Width[mm], L : Length[mm], N : Number, φ: Average Diameter

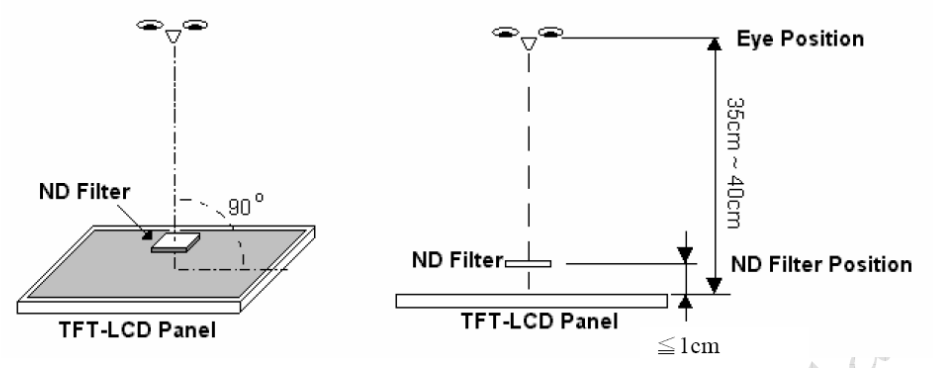


1. (White, black) Spot
2. Polarizer Bubble

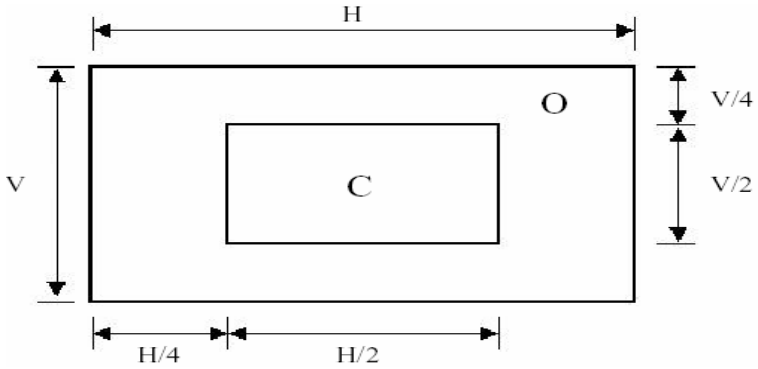


1. fiber

[Note2] Bright dot is defined through 6% transmission ND Filter as following.



[Note3]

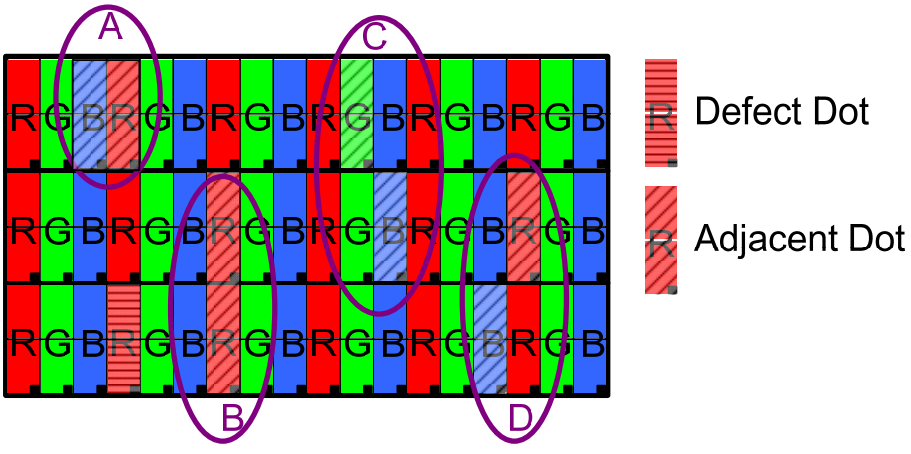


C Area: Center of display area

O Area: Outer of display area

[Note4]

Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity.



(1) The defects that are not defined above and considered to be problem shall be reviewed and discussed by both parties.

(2) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

9.6 Reliability Test

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Humidity Test	60 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

10. USE PRECAUTIONS

10.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

10.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

10.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

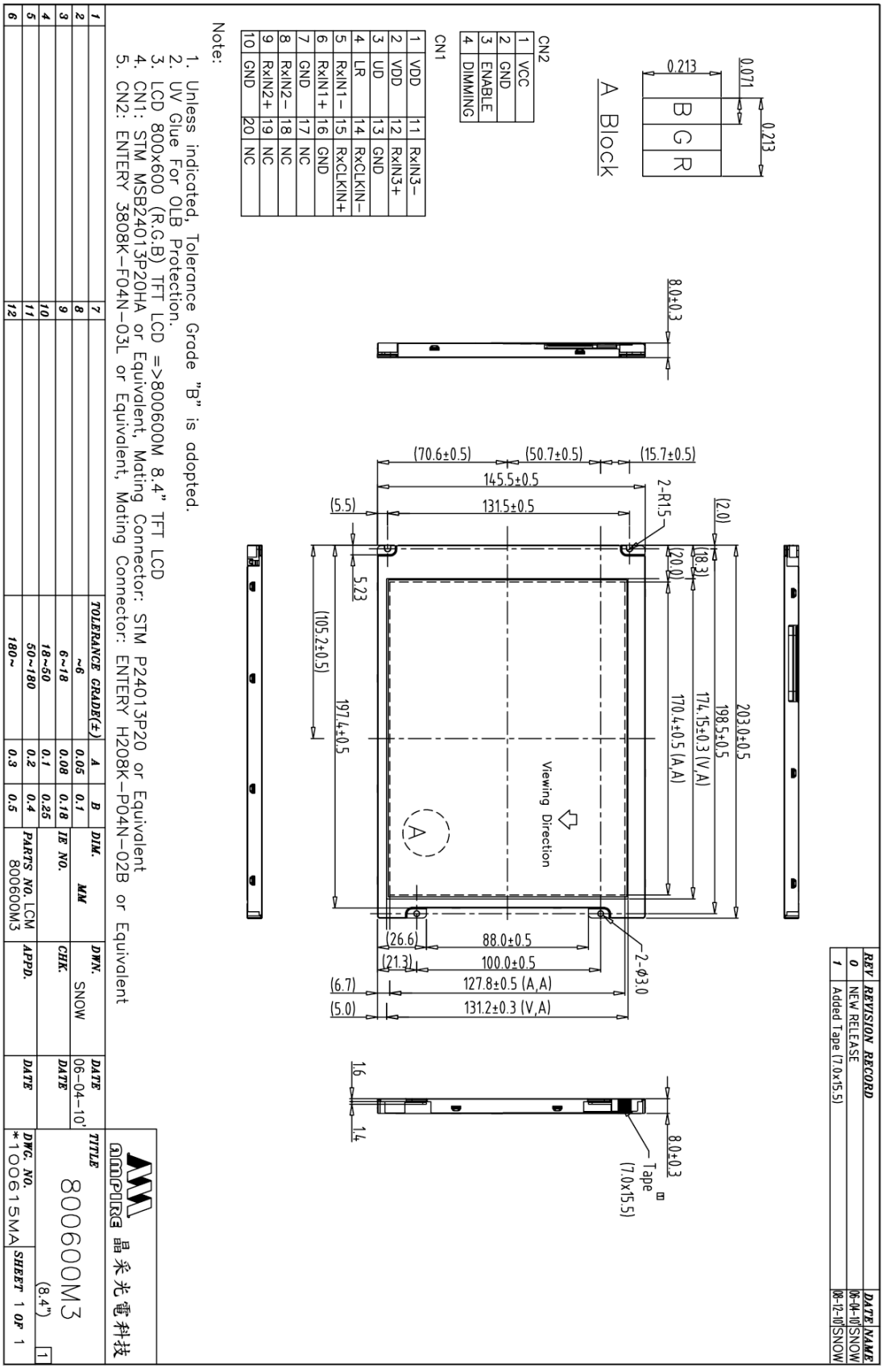
10.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

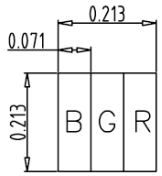
10.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warranty for all products and three months warrantee for all repairing products.

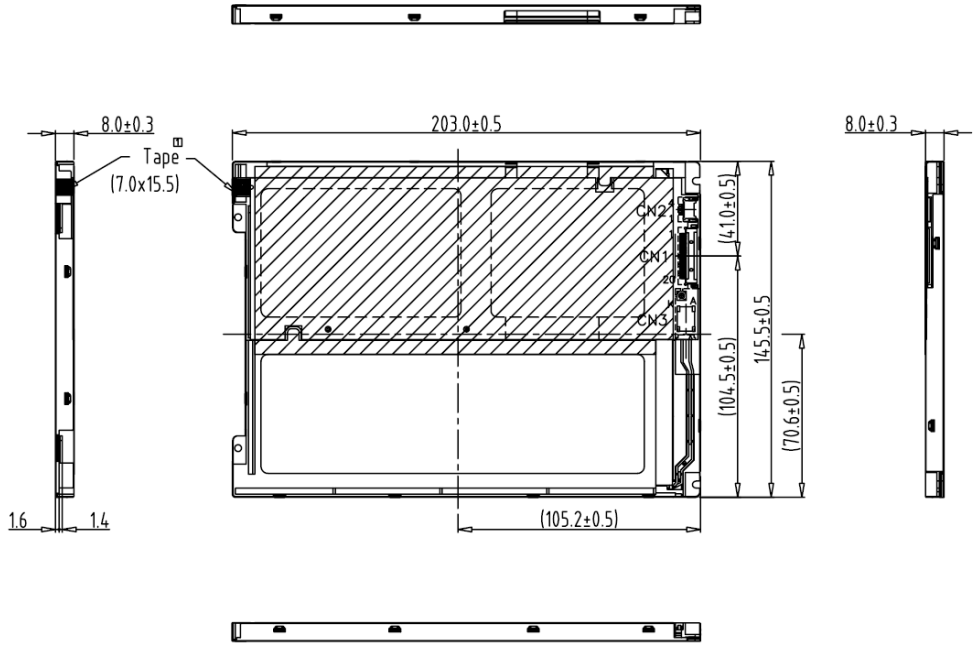
11. OUTLINE DIMENSION



REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	06-04-10'	SNOW
1	Added Tape (7.0x15.5)	08-12-10'	SNOW



A Block



Back View

CN2

1	VCC
2	GND
3	ENABLE
4	DIMMING

CN1

1	VDD	11	RxIN3−
2	VDD	12	RxIN3+
3	UD	13	GND
4	LR	14	RxCLKIN−
5	RxIN1−	15	RxCLKIN+
6	RxIN1+	16	GND
7	GND	17	NC
8	RxIN2−	18	NC
9	RxIN2+	19	NC
10	GND	20	NC

Note:

1. Unless indicated, Tolerance Grade "B" is adopted.
2. UV Glue For OLB Protection.
3. LCD 800x600 (R.G.B) TFT LCD =>800600M 8.4" TFT LCD
4. CN1: STM MSB24013P20HA or Equivalent, Mating Connector: STM P24013P20 or Equivalent
5. CN2: ENTERY 3808K−F04N−03L or Equivalent, Mating Connector: ENTERY H208K−P04N−02B or Equivalent

AMPIRE 晶采光電科技

				TOLERANCE GRADE(±)	A	B	DIM.	DWN.	DATE	TITLE
1		7					MM	SNOW	06-04-10'	800600M3
2		8		~6	0.05	0.1				(8.4") 1
3		9		6~18	0.08	0.18	IE NO.	CHK.	DATE	
4		10		18~50	0.1	0.25				
5		11		50~180	0.2	0.4	PARTS NO. LCM-1 800600M3	APPD.	DATE	DWG. NO. *100616MA SHEET 1 OF 1
6		12		180~	0.3	0.5				

Date : 2011/03/23