Am0056•Am0056C

5MHz Two-Phase MOS Clock Driver

Distinctive Characteristics

- 20ns rise and fall times with 1000pF load
- 20V output voltage swing
- ±1.5 amps output current drive
- High speed 5 to 10MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883
- Improved V_{OH} compared with Am0026

FUNCTIONAL DESCRIPTION

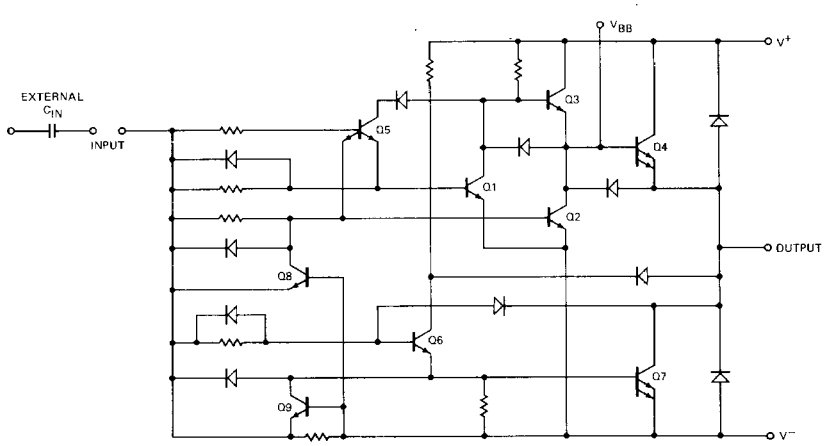
The Am0056 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0056 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in a TO-99, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a ceramic DIP.

The V_{BB} terminal is intended to be connected through a series resistor to a supply higher than V^+. This connection will enable the output to pull-up to V^+–0.1V. Under no conditions should the V_{BB} terminal be connected directly to a positive supply as the device will be damaged when the driver switches LOW.

SCHEMATIC DIAGRAM (One Driver Shown)



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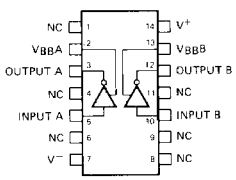
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
TO-99	0°C to 70°C	DS0056CH
Mini-DIP	0°C to 70°C	DS0056CN
Ceramic DIP	0°C to 70°C	DS0056CJ
Dice	0°C to 70°C	AM0056XC
TO-99	–55°C to +125°C	DS0056H
Ceramic DIP	–55°C to +125°C	DS0056J
Dice	–55°C to +125°C	AM0056XM

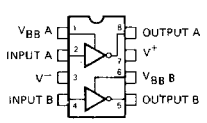
CONNECTION DIAGRAMS

Top Views

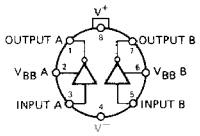
Ceramic DIP



Mini DIP



TO-99



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22V
Input Current	100mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Power Dissipation	See curves
V_{BB} Voltage	V^+ +5.0V
Current Into V_{BB}	50mA
Operating Temperature—Am0056	−55°C to +125°C
Am0056C	0°C to 70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Logical "0" Output Voltage)	$V_{IN} - V^- = 0.4V$, V_{BB} Open Circuit ($R_{BB} = \infty$)		$V^+ - 2.5$	$V^+ - 1.4$		Volts
		$V_{IN} - V^- = 0.4V$, $R_{BB} = 1k\Omega$; V_{BB} $V_B \geq V^+ + 1.0V$		$V^+ - 0.3$	$V^+ - 0.1$		
V_{OL}	Output LOW Voltage (Logical "1" Output Voltage)	$V_{IN} - V^- = 2.4V$			$V^- + 0.7$	$V^- + 1.0$	Volts
V_{IH}	Input HIGH Level	$V_{OUT} = V^- + 1.0V$		2.0	1.5		Volts
V_{IL}	Input LOW Level	$V_{OUT} = V^+ - 1.0V$			0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$			−0.005	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} - V^- = 2.4V$, $V_{OUT} = V^- + 1.0V$			10	15	mA
$I_{CC\,ON}$	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$			15	30	mA
$I_{CC\,OFF}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$	COM'L		10	100	μA
			MIL		50	500	
I_{BB}	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$, $V_{BB} = V^+ + 3.0V$, $R_{BB} = 1k\Omega$			22		mA

Notes: 1. These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000pF$, over the temperature range −55°C to +125°C for the Am0056 and 0°C to +70°C for the Am0056C.
2. All typical values for $T_A = 25°C$.

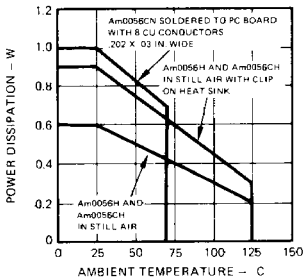
SWITCHING CHARACTERISTICS (Notes 1 and 2 Above)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
t_{PHL}	Turn ON Delay			5.0	8.0	12	ns
t_{PLH}	Turn OFF Delay			5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^- = 17V$,	$C_L = 500pF$		15	18	ns
			$C_L = 1000pF$		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^- = 17V$,	$C_L = 500pF$		12	16	ns
			$C_L = 1000pF$		17	25	

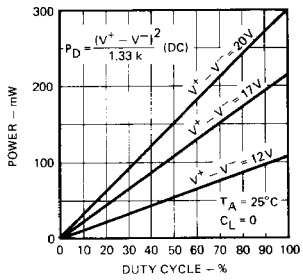
Note: 3. Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See switching time waveforms.

TYPICAL PERFORMANCE CURVES

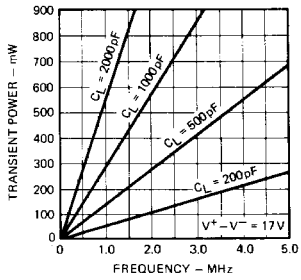
Power Ratings TO-5 & 8-Pin DIP



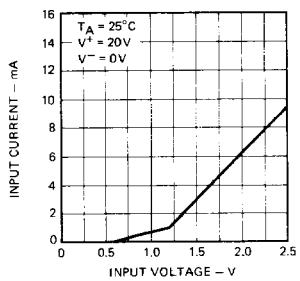
DC Power (P_{DC}) Versus Duty Cycle (DC)



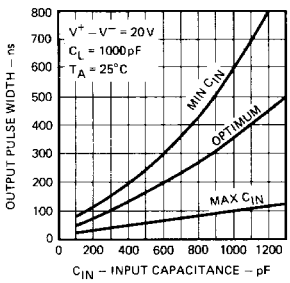
Transient Power (P_{AC}) Versus Frequency



Input Current Versus Input Voltage



Optimum Input Capacitance Versus Output Pulse Width



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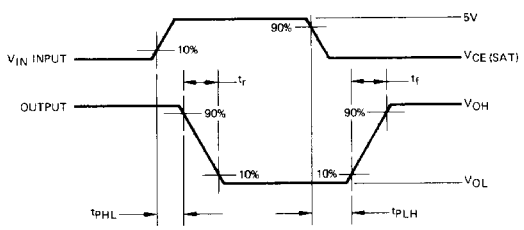
SWITCHING TIME WAVEFORMS



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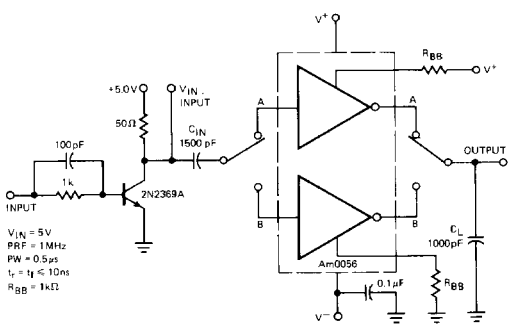
AC TEST CIRCUIT



LIC-614

APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0056 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}.$$

With the device dissipating only 10 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per Driver

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S\,(LOW)} \times \text{Duty Cycle}$$

where $I_{S\,(LOW)}$ is $I_{SUPPLY\,(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY\,(ON)} \text{ is } 30\text{mA} \times \frac{(V^+ - V^-)}{20\text{ V}} \text{ worst case}$$

$$\text{or } 15\text{mA} \times \frac{(V^+ - V^-)}{20\text{ V}} \text{ typically}$$

AC Transient Power per Driver

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \times f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-99 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent – derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

MAXIMUM LOAD CONSIDERATIONS

The maximum capacitive load that the Am0056 can drive is determined by:

The AC power consumed = $nVs^2\ C_L f \times 10^{-3}$ mW

The DC power consumed = $\frac{nVs^2}{Req}\ \rho \times 10^3$ mW

The package power rating for a given package, heatsink, and maximum ambient temperature = Pmax mW

Combining these expressions:

$$Pmax = \frac{nVs^2\ \rho \times 10^3}{Req} + nVs^2\ C_L f \times 10^{-3}$$

from which the maximum capacitive load:

$$C_{L(max)} = \frac{10^3}{n} \cdot \frac{(Pmax\ Req - nVs^2 \rho \times 10^3)}{Vs^2 f\ Req}$$

Where n = number of drivers employed in the package

Vs = total supply voltage $(V^+ - V^-)$ across device

ρ = duty cycle = time in output LOW state/time in output LOW + time in output HIGH

Req = $(V^+ - V^-)/I_{CC}$ ON = 1000 Ω worst case or 1300 Ω TYP

C_L = load capacitance per driver in pF

f = input signal frequency in MHz

When used as a non-overlapping, two-phase driver with each side operating at the same frequency and duty cycle and with V_s = 17 V, the above equation reduces to:

$$C_{L(max)} = \frac{10^3}{f}\left(\frac{Pmax}{578} - \rho\right)$$

Table 1 gives maximum drive capability using above equation.

PULSE WIDTH CONTROL

The Am0056 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_f = PW_{IN} + 17\text{ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0056 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN}\ (3 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (3 \times 10^{-3})\ (500 \times 10^{-9}) = 1500\text{pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0056's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leq 1.5\text{ A}$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)\ (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20\,V$, $C_L = 1000\,pF$, t_r is:

$$t_r \cong (20\,V)\ (250 \times 10^{-12} + 1000 \times 10^{-12})$$

$$= 25\,ns$$

For small values of C_L, the equation above predicts optimistic values for t_r.

The output fall time may be predicted by:

$$t_f \cong 2.2\,R\left(C_S + \frac{C_L}{h_{FE}+1}\right)$$

CLOCK OVERSHOOT

The output waveform of the Am0056 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0056. The critical value for $R_S = 2\sqrt{L/C_L}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2 R_S\,C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0056 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output will drop until Q_4 becomes active. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0056 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ and V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each Am0056 is strongly recommended. This decoupling is necessary because of the 1.5 ampere currents which flow during logic transition when charging clock lines.

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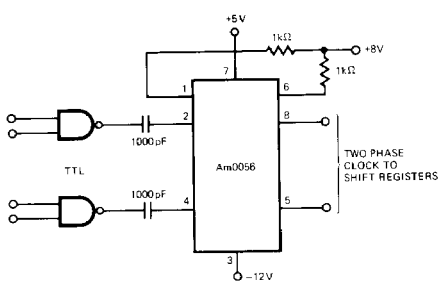
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0056*

Package Type			TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
		P_{Max} mW	1775	1400	1150	900	769	604	460	360	665
Max. Operating Frequency	Duty Cycle	Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100kHz	5%		30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500kHz	10%		6.0k	4.6k	3.8k	2.9k	2.5k	1.9k	1.4k	1.0k	2k
1MHz	20%		2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2MHz	25%		1.4k	1.1k	870	650	540	400	270	190	390
5MHz	25%		560	440	350	260	220	160	110	75	165
10MHz	25%		280	220	170	130	110	80	55	37	90

*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17\,V$.

TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver



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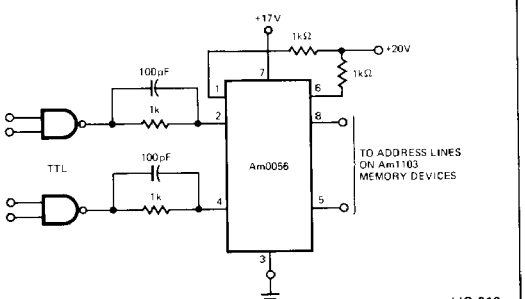
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



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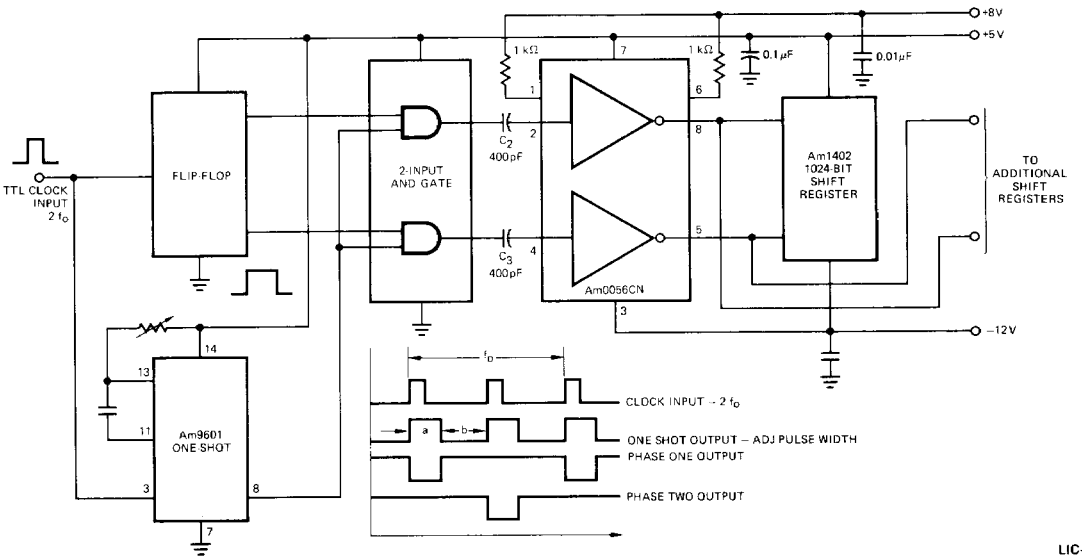
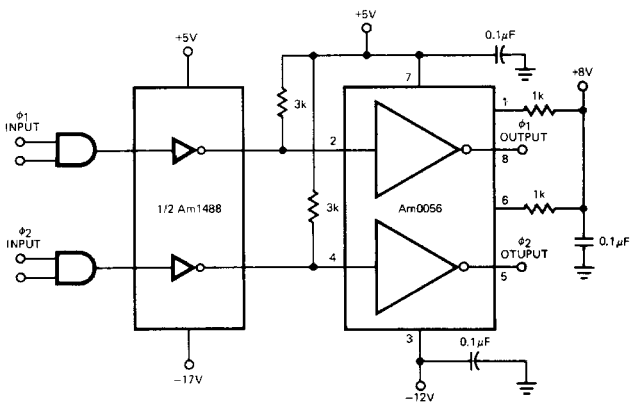
TYPICAL APPLICATIONS (Cont.)

Logically Controlled AC Coupled Clock Driver



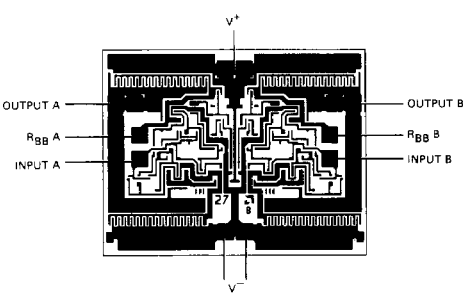
LIC-617

DC Coupled MOS Clock Driver



LIC-618

Metallization and Pad Layout



DIE SIZE 0.056" X 0.074"